Amplifier Analysis Example

Amplifier circuit spec:

Vin = 0.01V and Vout = 1V

Vin = 1V and Vout = 4.5V

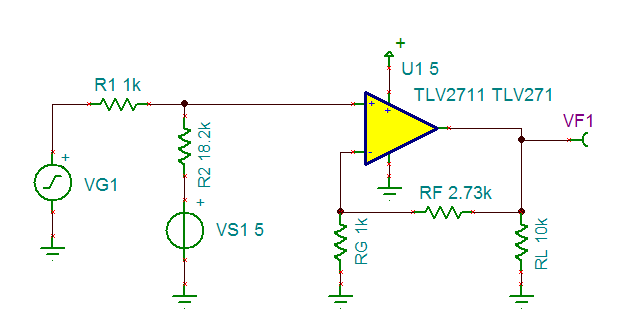
The circuit and component values were done in CH 4. The MATHCAD example is [here](../chap04/plus_m_plus_b.xmcd).

This implementation uses the TLV271 op amp from TI.

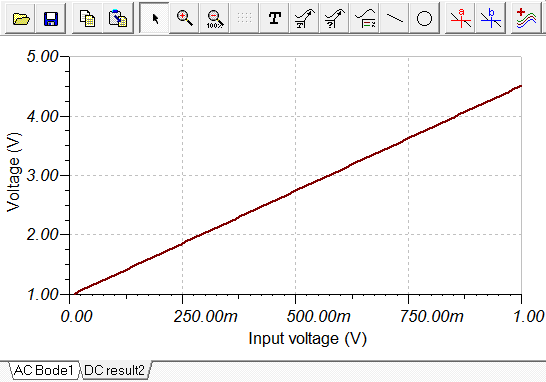
* [Datasheet](tlv271.pdf)
* [Simulation models](sboc221.zip)

Closed Loop Analysis without Load Capacitor

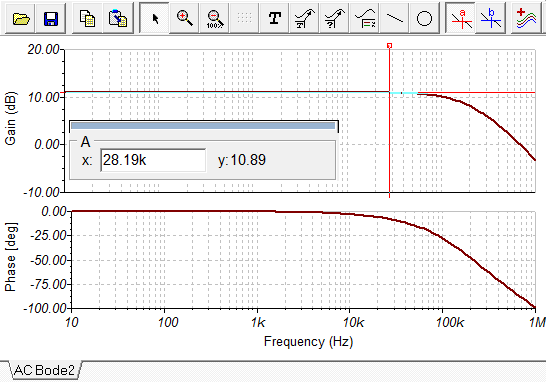
Tina close loop simulation is [here](amplifier_close_loop.TSC).



The DC transfer function is verified to be correct:



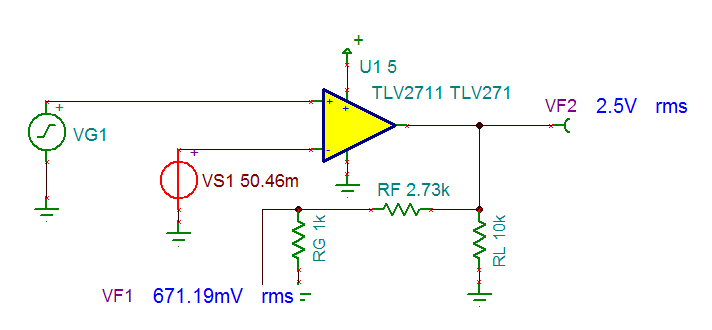
AC close loop gain graphs shows that it’s good for up to about 28 kHz.



Open Loop Analysis with Load Capacitor and Lead Compensation

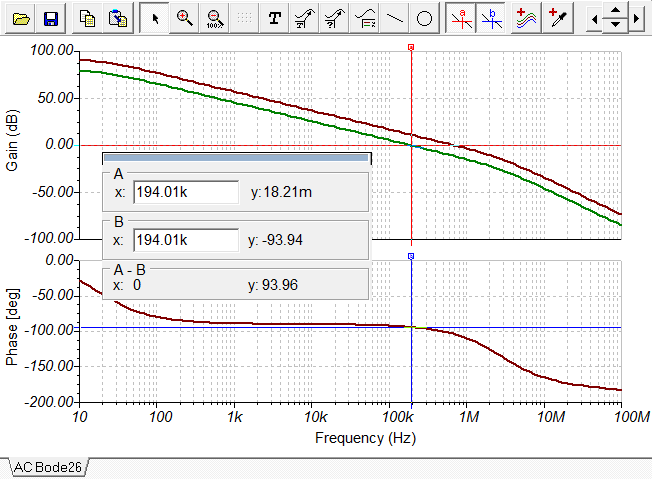
The Tina open loop simulation is [here](amplifier_open_loop.TSC).

For the open loop analysis, you have to tune the input so to take out the effect of offset voltage. In the following screen capture, VG is sine wave with 100uV amplitude. VGDC = 50 mV, but note that VS1 is not 50mV. Go into AC interactive mode and adjust VS1 until the output has an RMS of 2.5V.



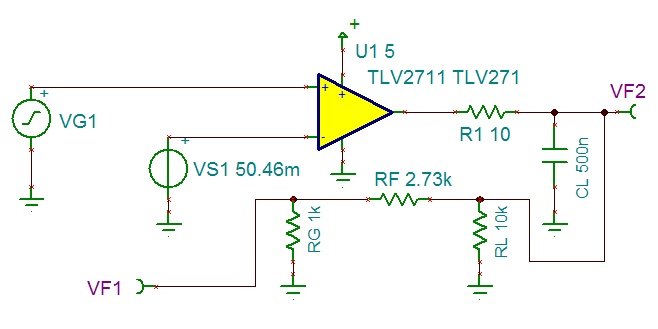
The sine wave being used by Tina to do the AC analysis is not the same as VG1 --- so the result will not be perfect.

The bode plot:

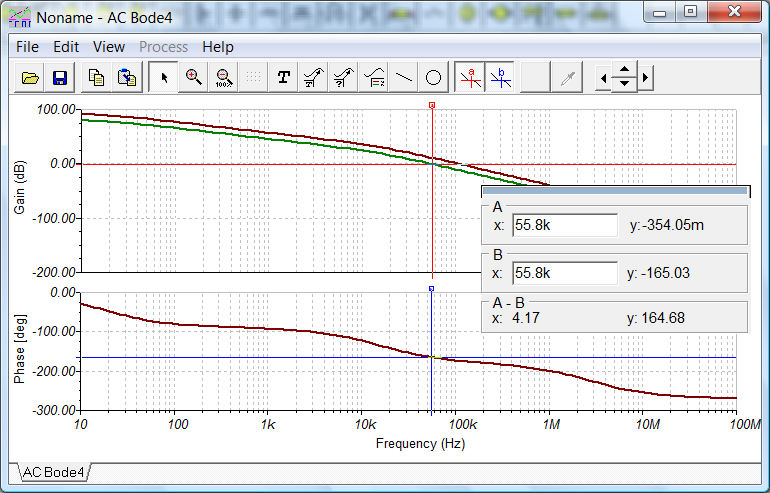


The phase margin is about 90 degrees. You can see the two poles from the op-amp in this bode plot. Those are the only two poles because the feedback is purely resistive, and output has no capacitor.

Adding output resistor and capacitor changes the bode plot by adding a pole:



Phase margin is now just 15 degrees:



Also notice that the phase will eventually go to -270 degrees.

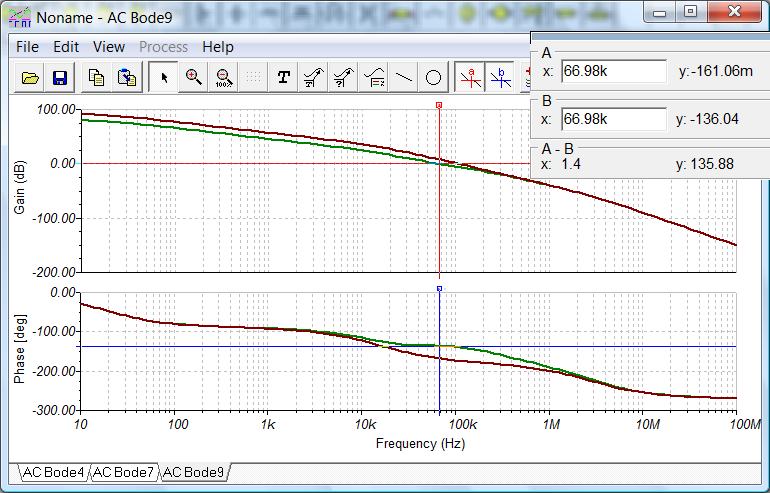
Increasing CL will move the pole to a lower location.

We can use the lead compensation to put a zero at 55.8 KHz, so to boost the phase there by 45 degrees. The magnitude graph will cross unity a little later due to the zero though, so the phase improvement won’t be quite 45 degrees.

The second pole in this case seems to be at 10 kHz.

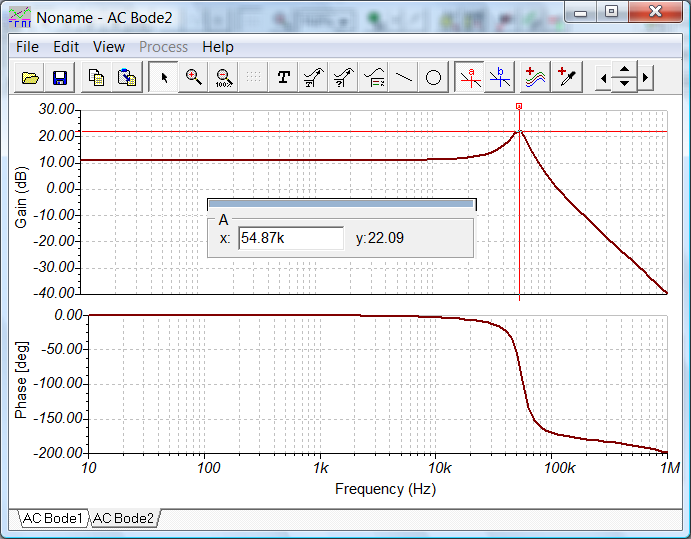
CF comes out to be 1 nF.

Bode plot shows the phase margin increased to 44 degrees.

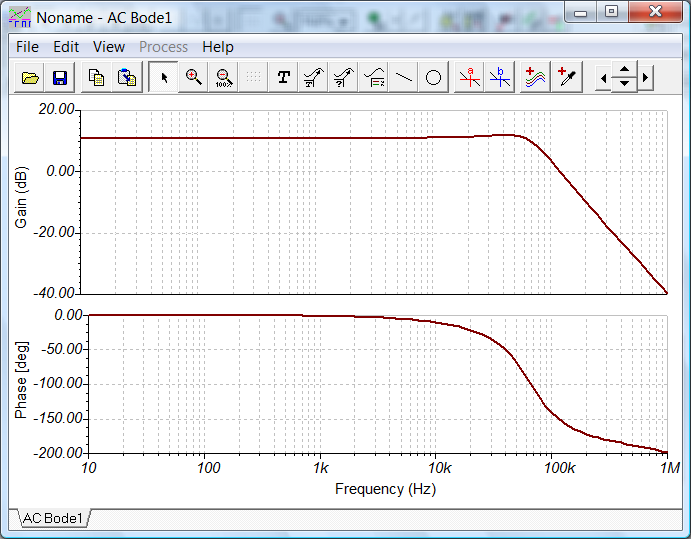


Closed Loop Analysis with Load Capacitor and Lead Compensation

Close loop Bode plot without the CF added --- bandwidth is 55 kHz with a peak toward the end.

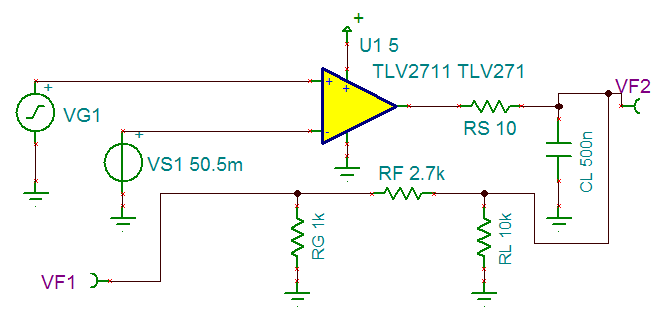


Close loop Bode plot with the CF added --- bandwidth is 48 kHz, with the high frequency peak mostly fixed.



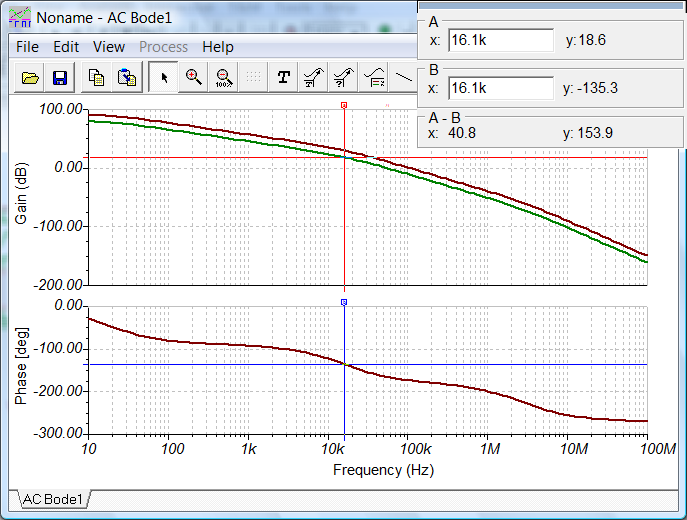
Lead-Lag Compensation Solution to the Load Capacitor Problem

The circuit:



The phase margin, as previously mentioned, is only 15 degrees.

This is the open loop Bode plot without any compensation:



Note that if we can make the unity gain frequency 16.1 kHz, without any modification to the phase, then the phase margin will be 45 degrees.

Right now, at this 16.1kHz, the open loop gain is 18.6 dB.

18.6 = 20 \* log10 G

G = 8.51 @ 16.1kHz

We want to make this gain 1, or in other words, we need to reduce the loop gain by 8.51 times.

The resistor divider in the feedback is 1 / (1 + 2.7) = 0.27 @ all frequencies.

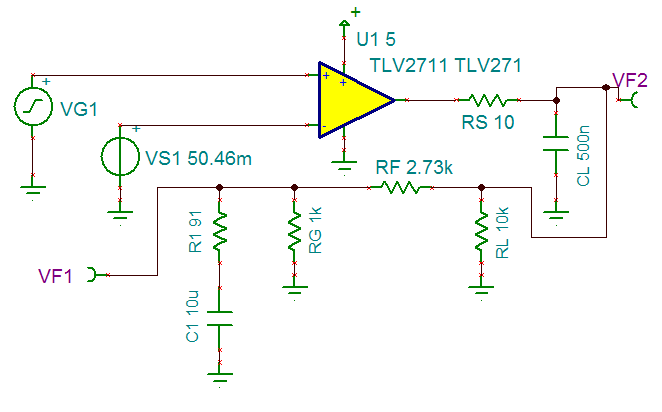
We want 0.27 / 8.51 = 0.0317 @ 16.1kHz

RG-new / (RG-new + 2.7) = 0.0317 @ 16.1kHz

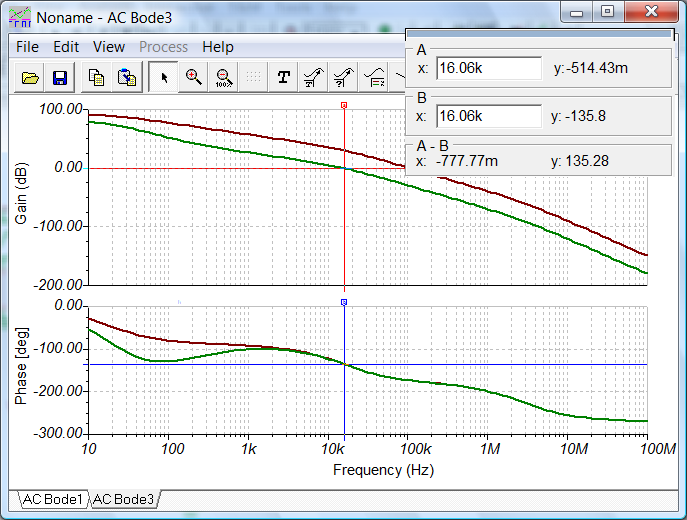
RG-new = 0.0884 kOhm @ 16.1kHz

The calculations to achieve this particular impedance at 16.1kHz is done in a MathCad worksheet [here](impedance_calc.xmcd).

New circuit (note the RG-new network):

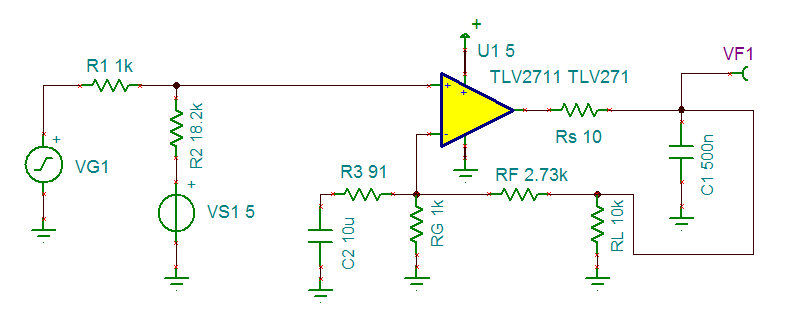


New open loop Bode plot:



Note that phase margin is now 44 degrees.

Close loop gain circuit with the compensation:



Close loop gain Bode plot:

