

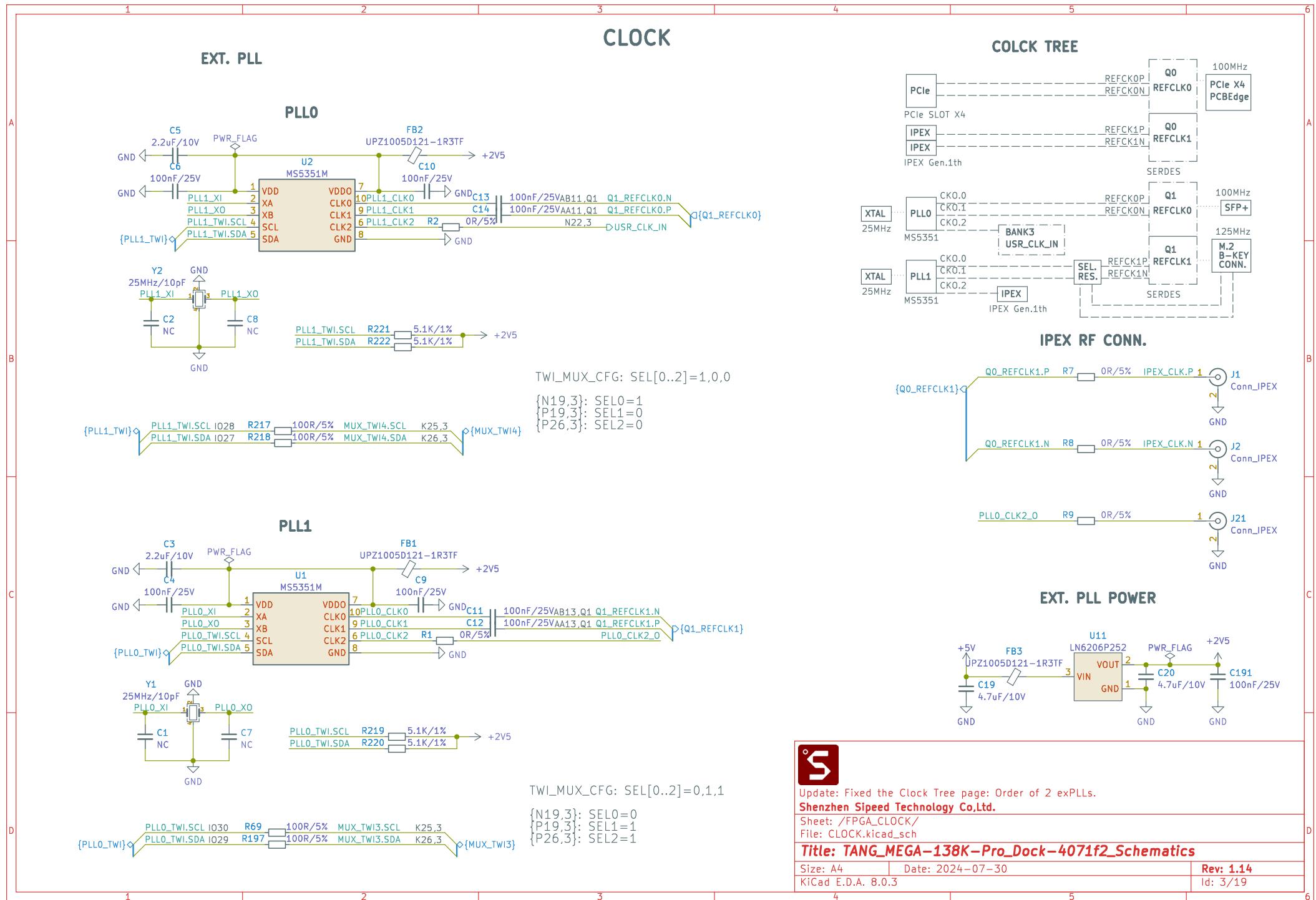
Update: Fixed the Clock Tree page: Order of 2 exPLLs.
Shenzhen Sipeed Technology Co.,Ltd.

Sheet: /POWER/
File: POWER.kicad_sch

Title: TANG_MEGA-138K-Pro_Dock-4071f2_Schematics

Size: A4 Date: 2024-07-30
KiCad E.D.A. 8.0.3

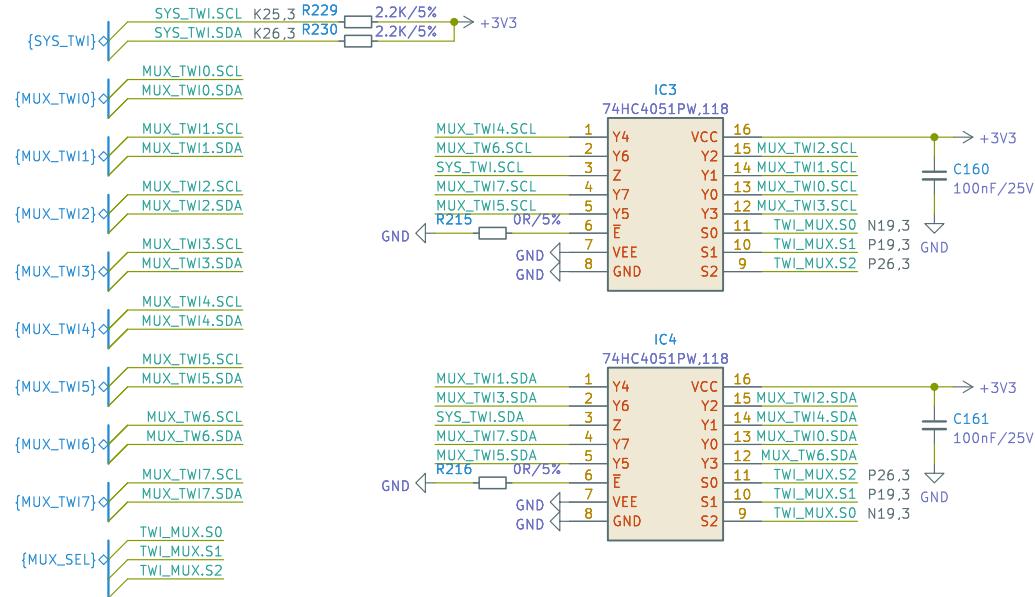
Rev: 1.14
Id: 2/19



A

A

8-WAY TWI MUX



| NO. | CONFIG | SEL0 | SEL1 | SEL2 |
|-----|------------------------|------|------|------|
| 0 | SFPO | 0 | 0 | 0 |
| 1 | SFP1 | 0 | 0 | 1 |
| 2 | EEPROM | 0 | 1 | 0 |
| 3 | DVL_TX_DDC MS5331-0 | 0 | 1 | 1 |
| 4 | DVL_RX_DDC MS5331-1 | 1 | 0 | 0 |
| 5 | DVP_CAM | 1 | 0 | 1 |
| 6 | MIPI_RX0 | 1 | 1 | 0 |
| 7 | MIPI_RX1 | 1 | 1 | 1 |

B

B

C

C

D

D



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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Sheet: /TWI_MUX/
File: TWI_MUX.kicad_sch

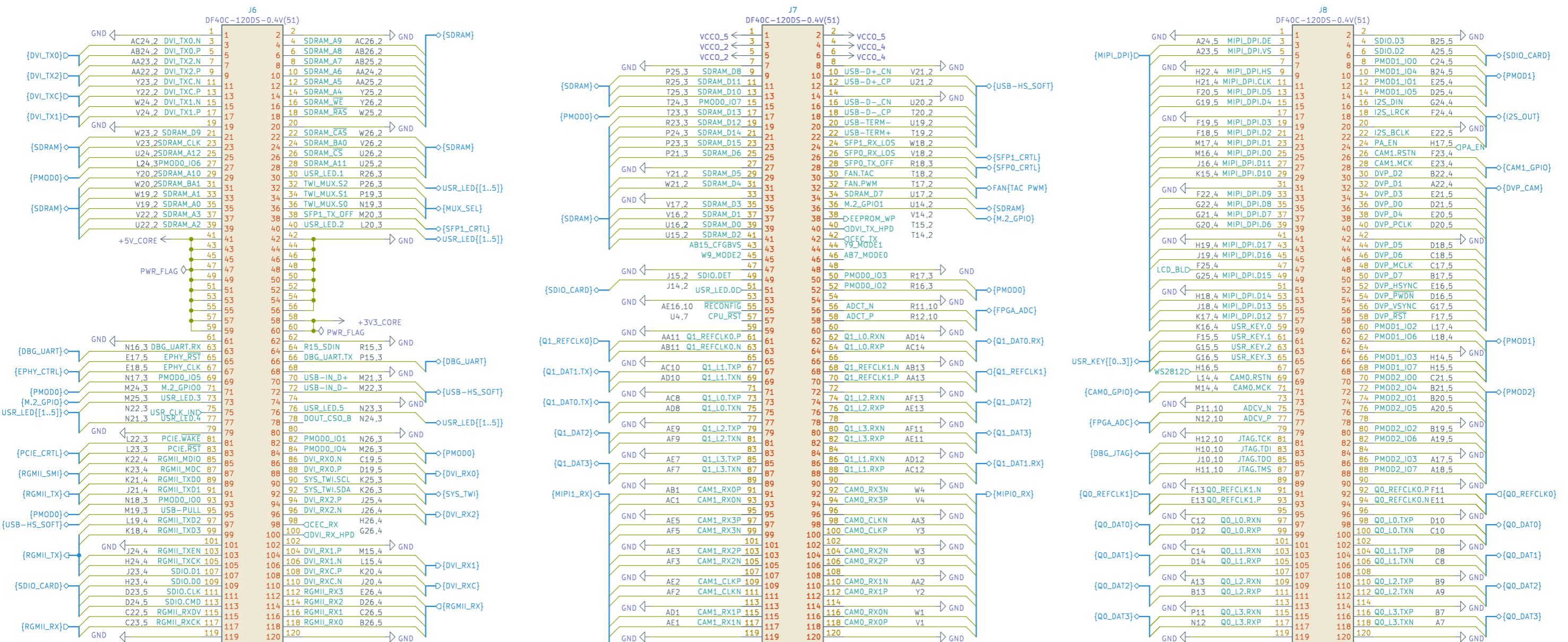
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Size: A4 Date: 2024-07-30
KiCad E.D.A. 8.0.3

Rev: 1.14
Id: 4/19

FPGA CORE MODULE

Note: that the pinout (numbers) of these conn. here is mirrored compared to the SOM.



TEST POINT

TP24 R15_SDIN
R15_SDIN

TP25 DOUT_CS0_B
DOUT_CS0_B

TP12 +3V3_CORE
DOUT_CS0_B

MODE SET



NOTE: MODE[0..2] is set to 001 by default on CM Board
Set CFGBVS to 1 to enable maximum driving of the pin during FPGA configuration

| CONFIG | MODE0 | MODE1 | MODE2 |
|----------|-------|-------|-------|
| JTAG | X | X | X |
| MSPI | 0 | 0 | 1 |
| SSPI | 0 | 1 | 0 |
| M SERIAL | 0 | 0 | 0 |
| S SERIAL | 1 | 1 | 1 |
| M CPU | 1 | 0 | 0 |
| S CPU | 1 | 1 | 0 |



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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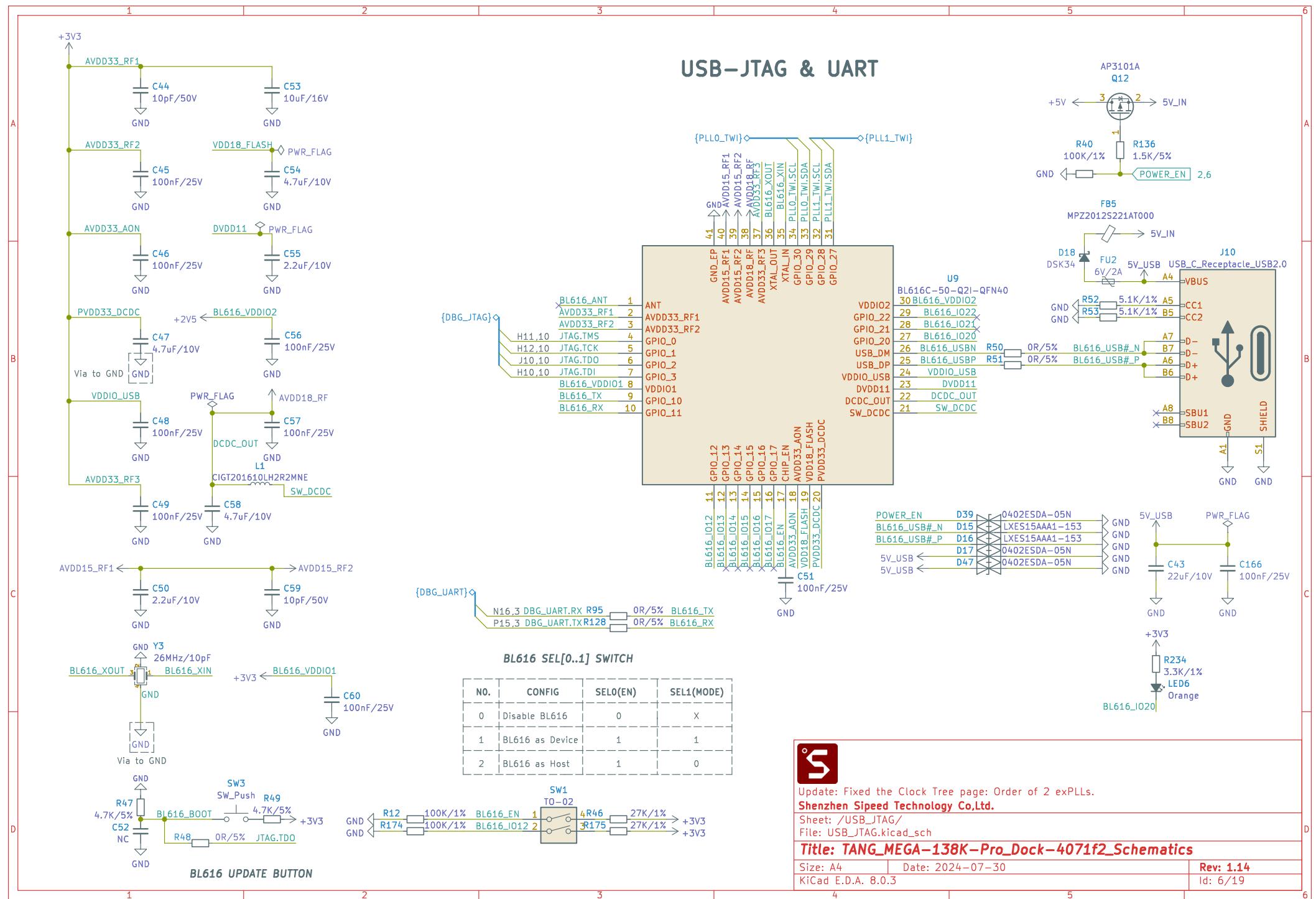
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Title: TANG_MEGA-138K-Pro_Dock-4071f2_Schematics

Size: A3 Date: 2024-07-30
KiCad E.D.A. 8.0.3

Rev: 1.14
Id: 5/19

USB-JTAG & UART



PCI-Express X4

A

B

C

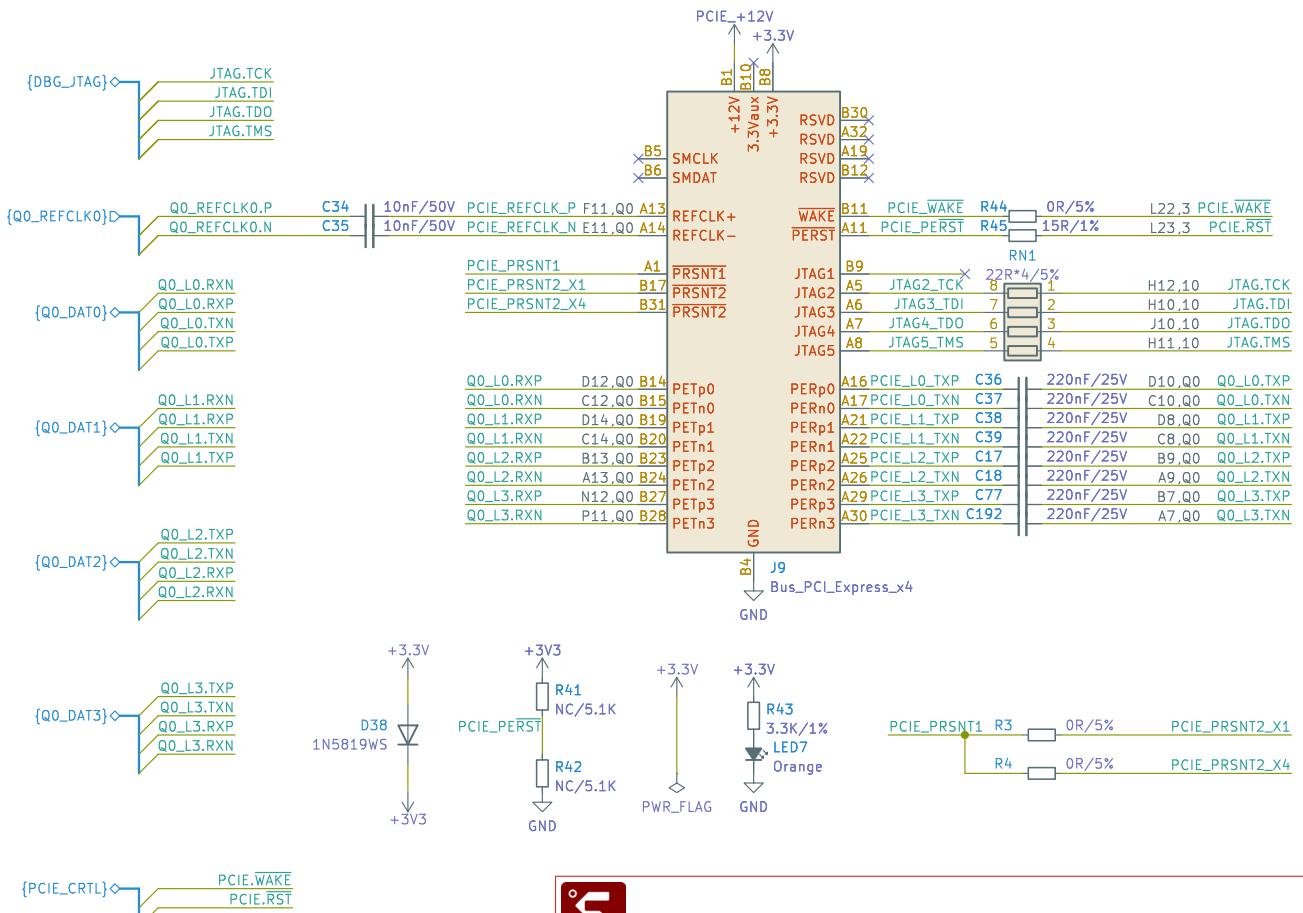
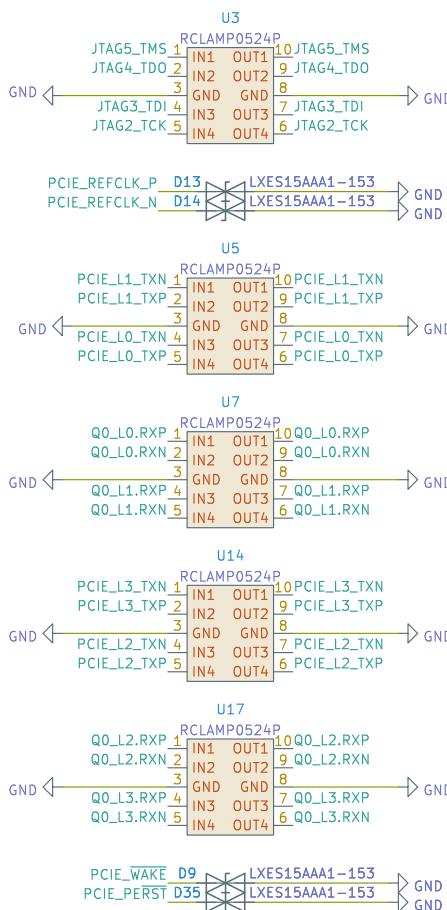
D

A

B

C

D



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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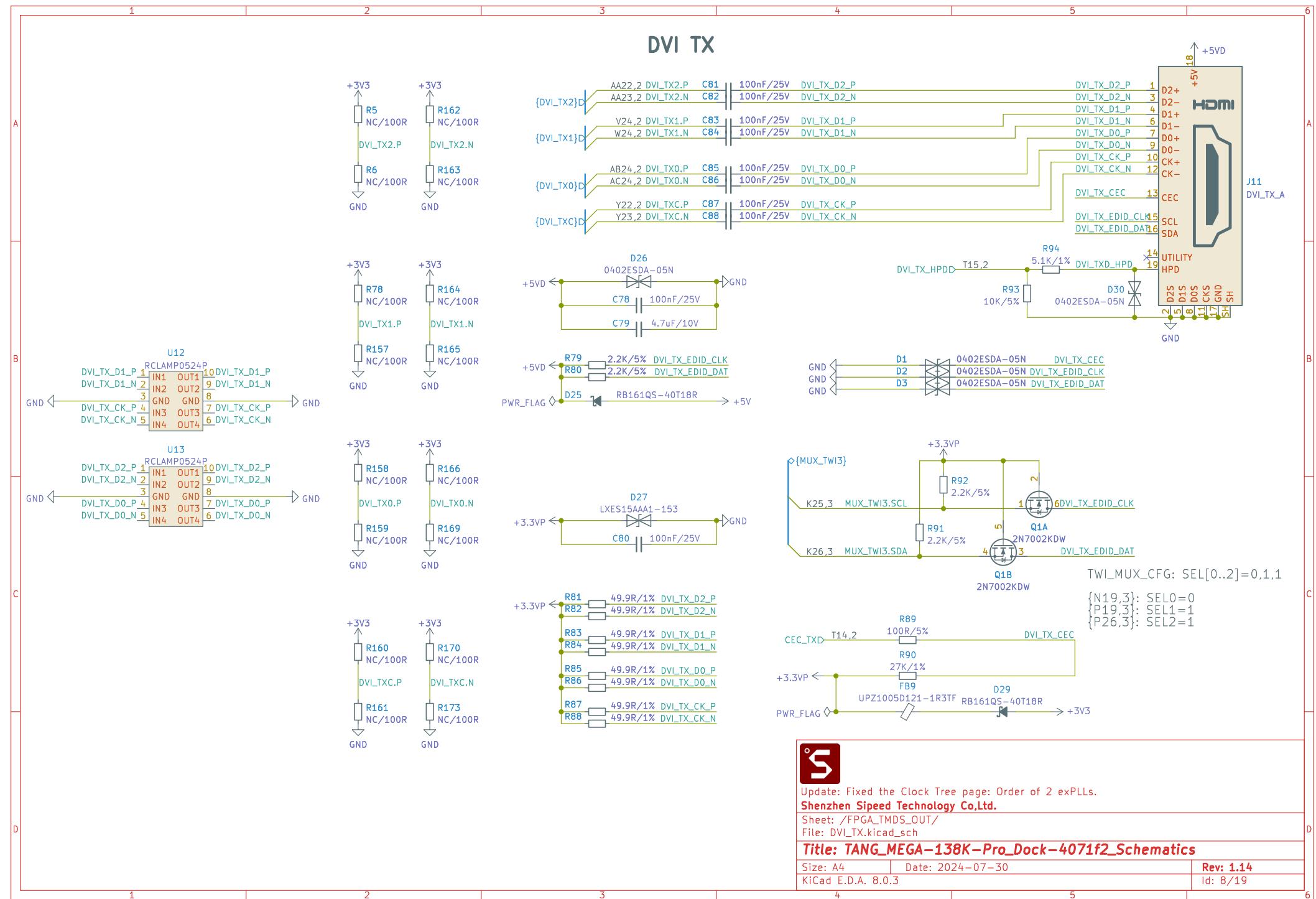
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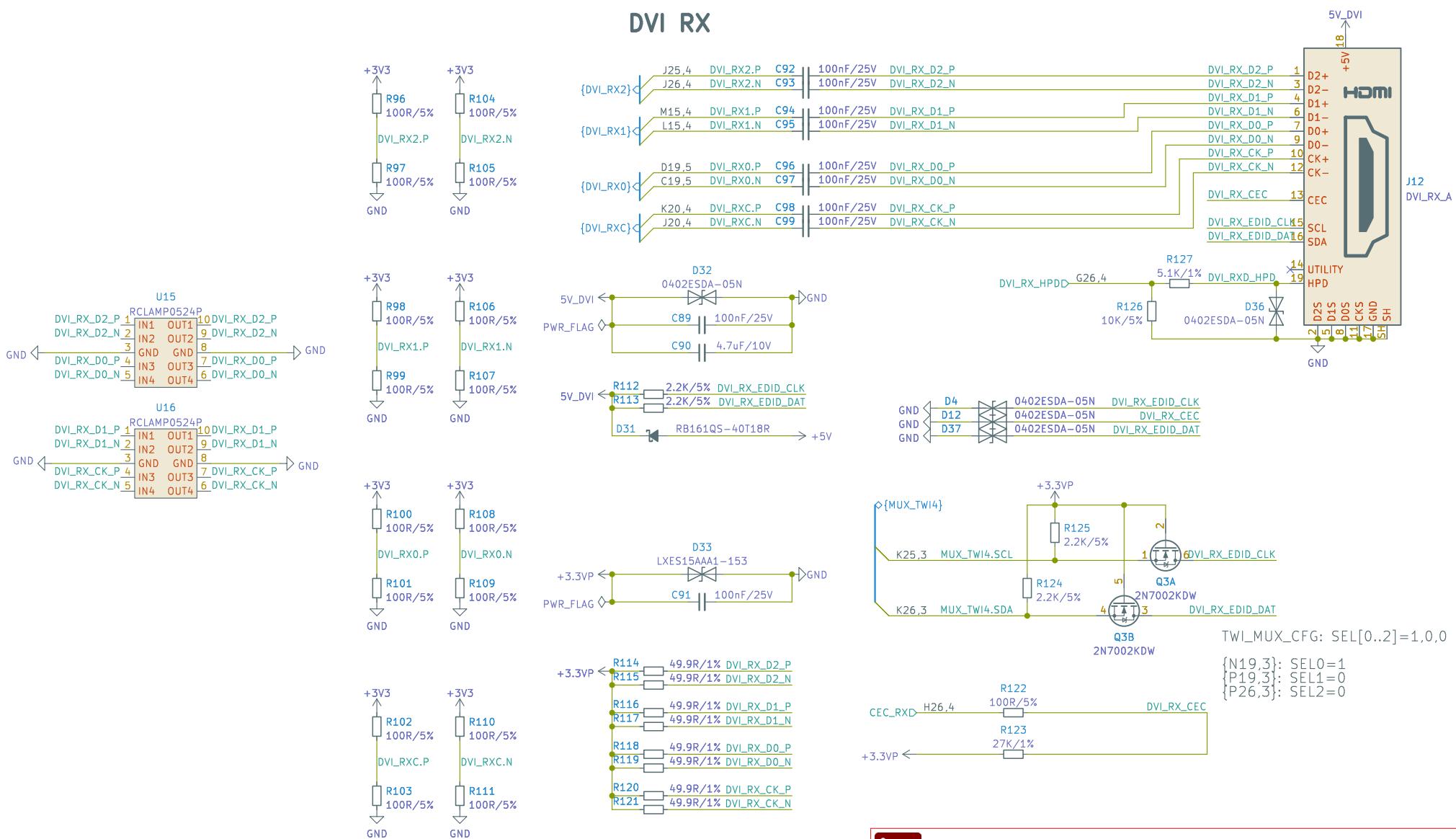
Size: A4 Date: 2024-07-30
 KiCad E.D.A. 8.0.3

Rev: 1.14
 Id: 7/19

DVI TX



DVI RX



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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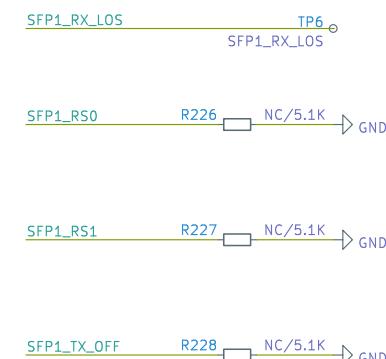
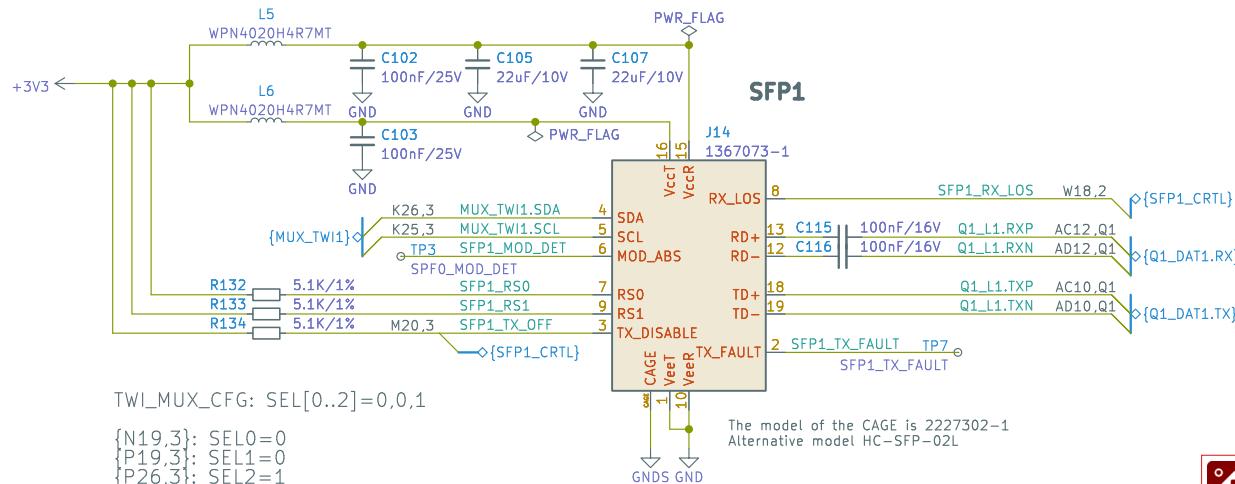
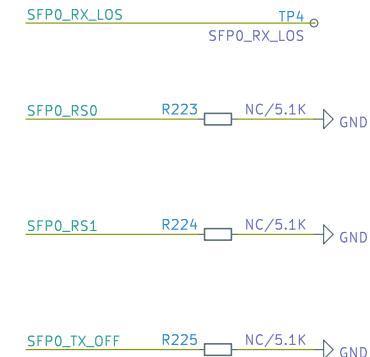
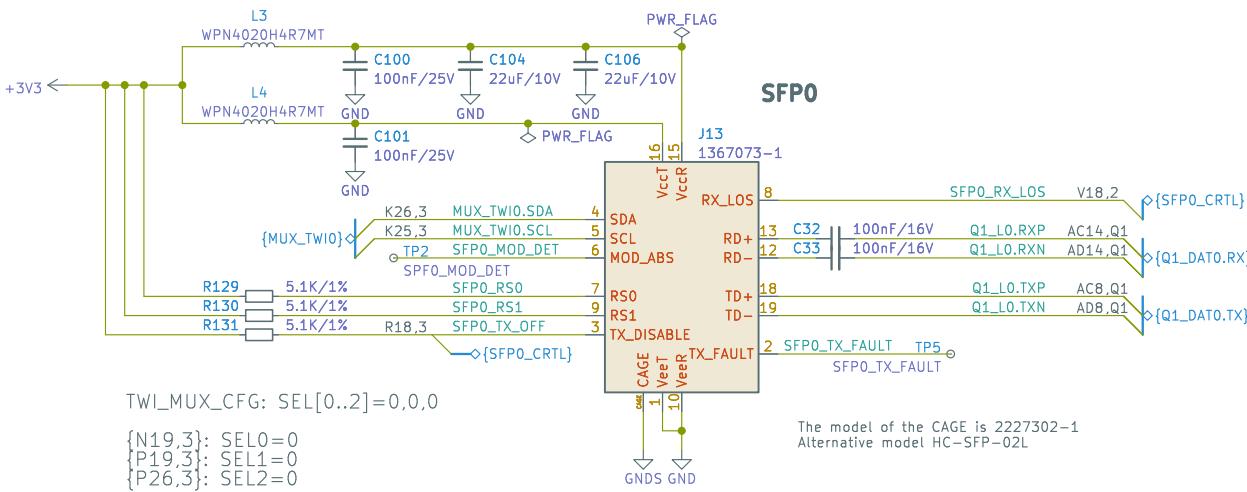
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Title: TANG_MEGA-138K-Pro_Dock-4071f2_Schematics

Size: A4 Date: 2024-07-30
KiCad E.D.A. 8.0.3

Rev: 1.14
Id: 9/19

SFP+



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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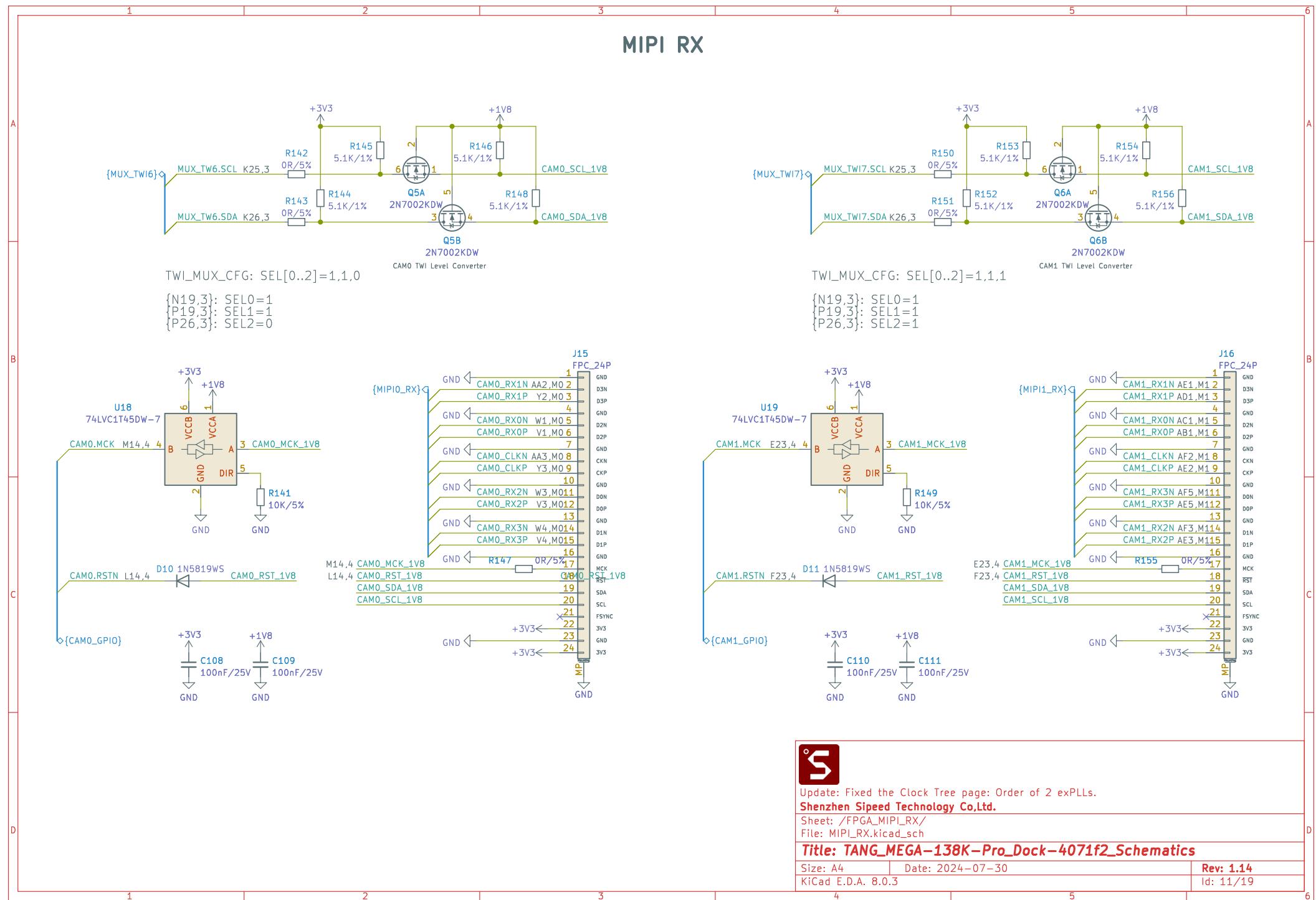
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Size: A4 Date: 2024-07-30
KiCad E.D.A. 8.0.3

Rev: 1.14
Id: 10/19

MIPI RX



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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Sheet: /FPGA_MIPI_RX/
File: MIPI_RX.kicad_sch

Title: TANG_MEGA-138K-Pro_Dock-4071f2_Schematics

Size: A4 Date: 2024-07-30
KiCad E.D.A. 8.0.3

Rev: 1.14
Id: 11/19

DVP-CAMERA

A

B

C

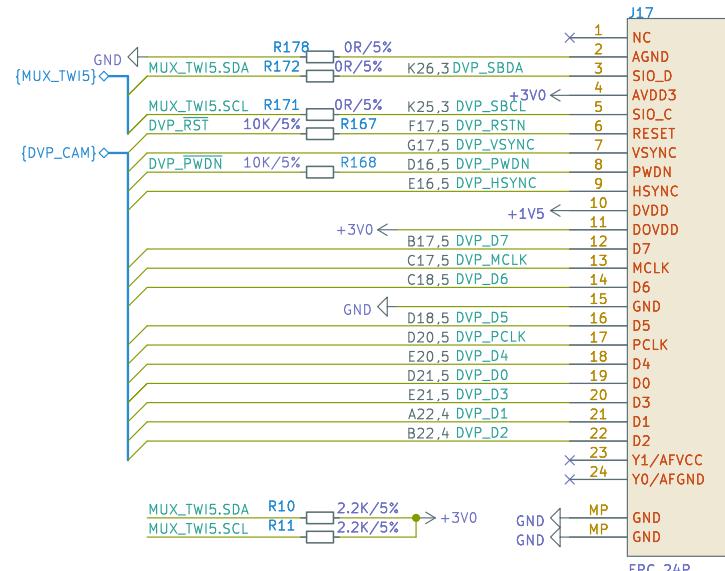
D

A

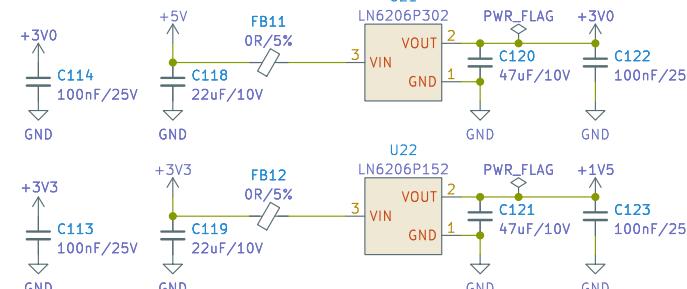
B

C

D



TWI_MUX_CFG: SEL[0..2]=1,0,1

{N19,3}: SEL0=1
{P19,3}: SEL1=0
{P26,3}: SEL2=1

Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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Sheet: /DVP_CAMERA/
File: DVP.kicad_sch

Title: TANG_MEGA-138K-Pro_Dock-4071f2_Schematics

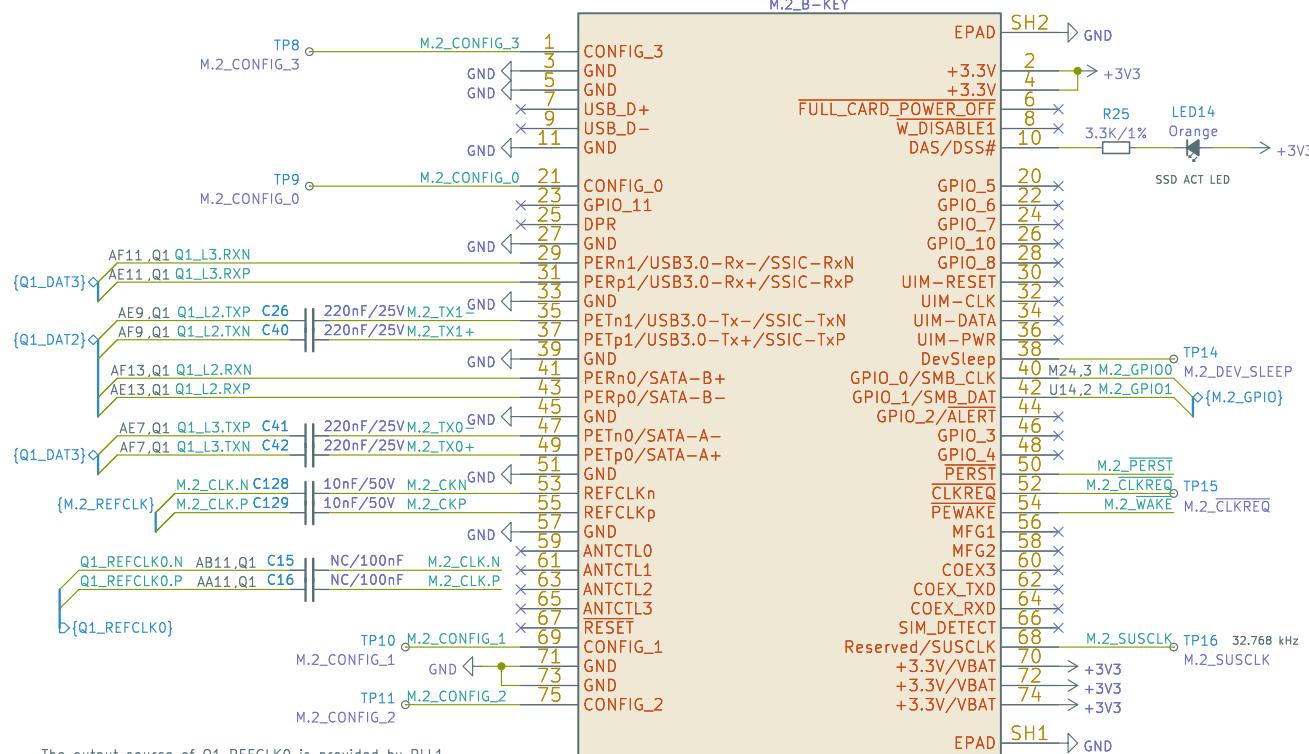
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KiCad E.D.A. 8.0.3

Rev: 1.14
Id: 12/19

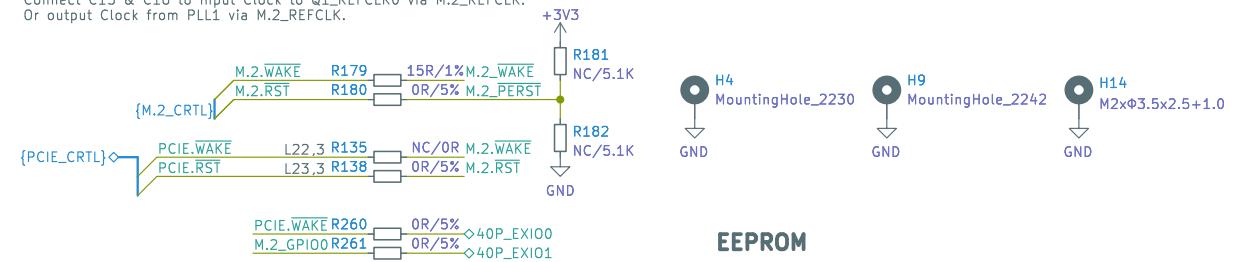
STORAGE

M.2 SOCKET KEY-B

J18
M.2_B-KEY



Connect C15 & C16 to input Clock to Q1_REFCLK0 via M.2_REFCLK.
Or output Clock from PLL1 via M.2_REFCLK.

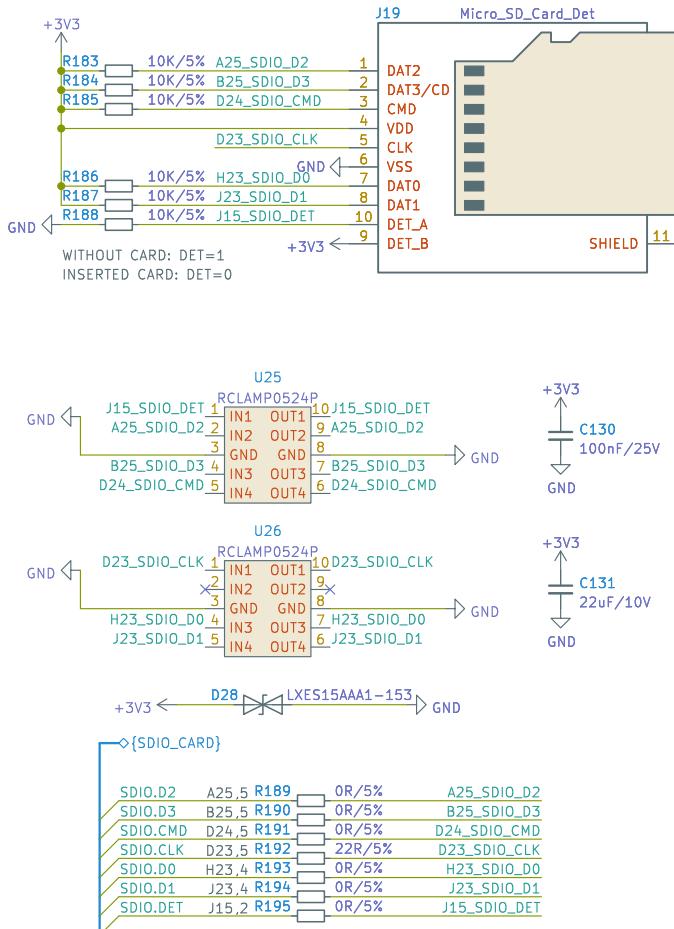
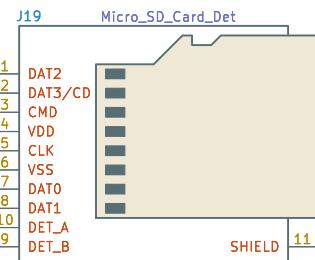


EEPROM



TWI_MUX_CFG: SEL[0..2]=0,1,0
{N19.3}: SEL0=0
{P19.3}: SEL1=1
{P26.3}: SEL2=0

MICRO SD CARD



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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Sheet: /FPGA_STORAGE/
File: SDIO&M.2.kicad_sch

Title: TANG_MEGA-138K-Pro_Dock-4071f2_Schematics

Size: A4 Date: 2024-07-30

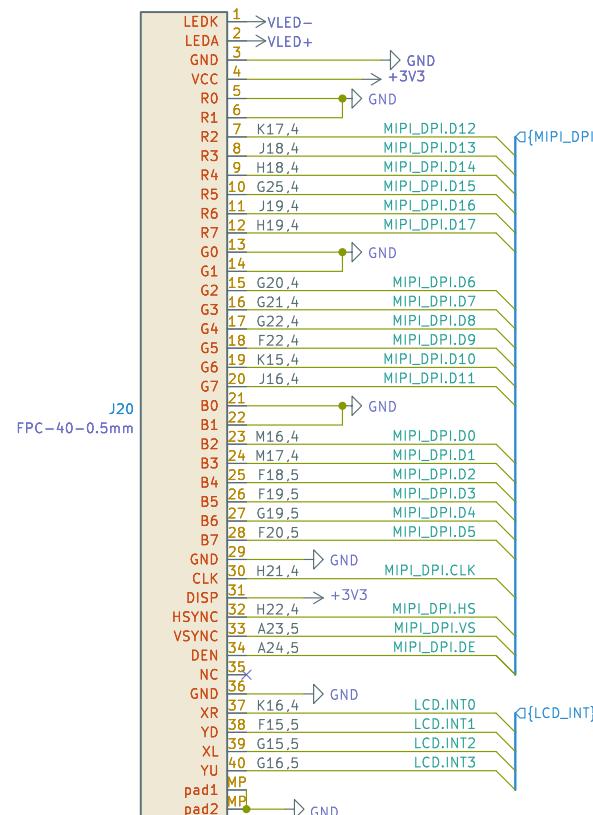
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Rev: 1.14

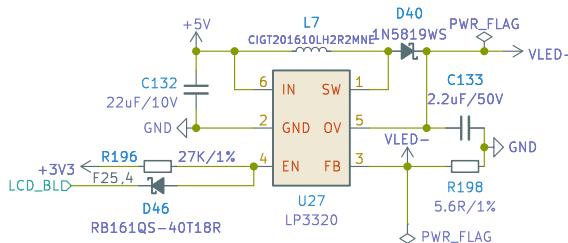
Id: 13/19

FPGA-LCD

MIPI DPI CONN.



LCD BACKLIGHT



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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Sheet: /FPGA_LCD/
File: LCD_DPI.kicad_sch

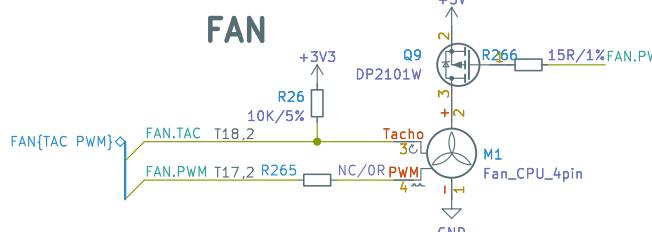
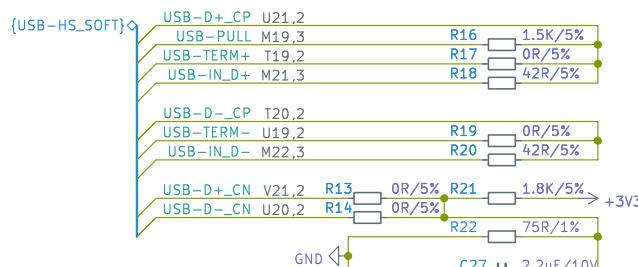
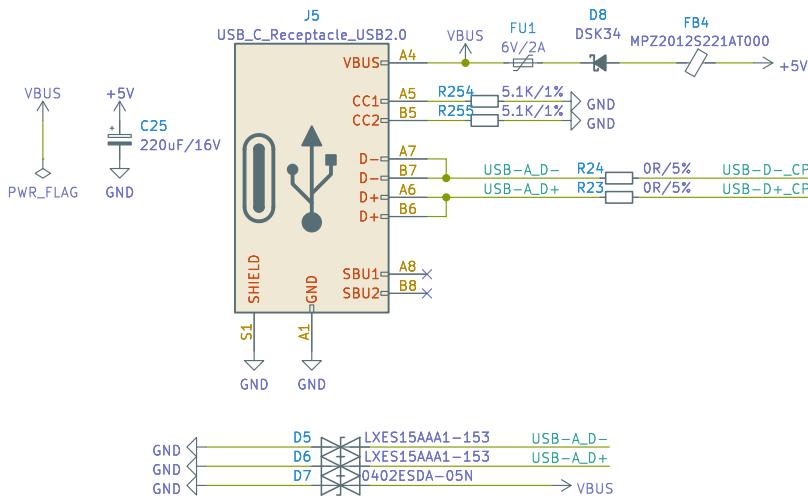
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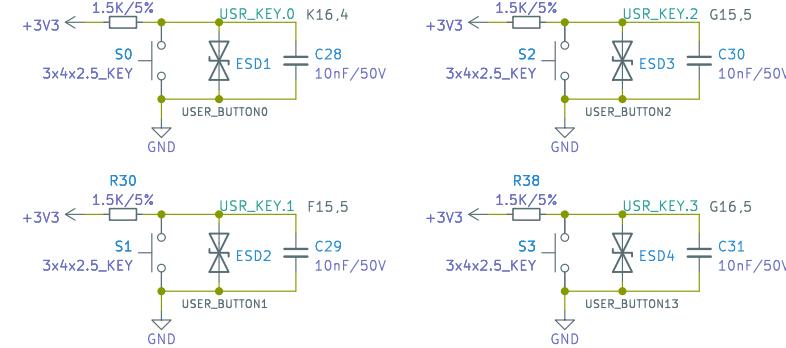
Rev: 1.14
Id: 14/19

PERIPHERALS

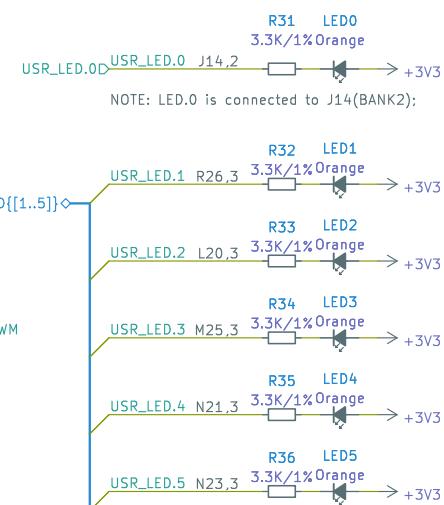
USB2.0-DEV.



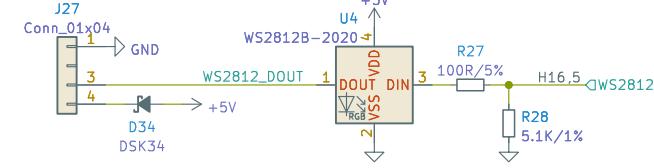
BUTTON



LED



WS2812



Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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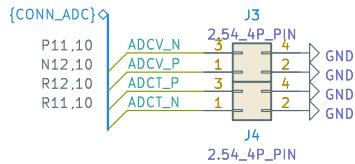
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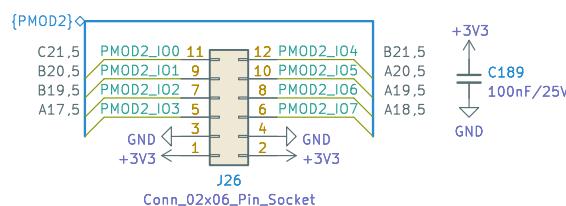
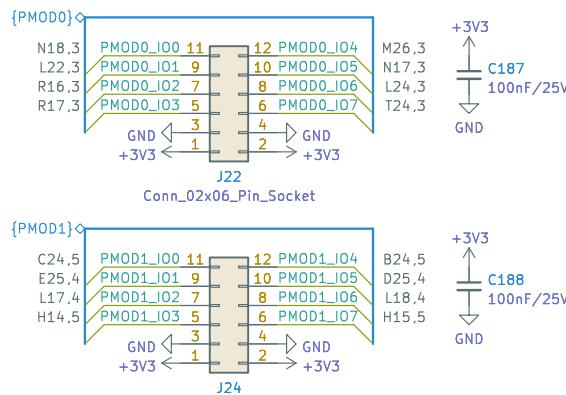
Rev: 1.14
Id: 15/19

EX CONN.

ADC CONN.



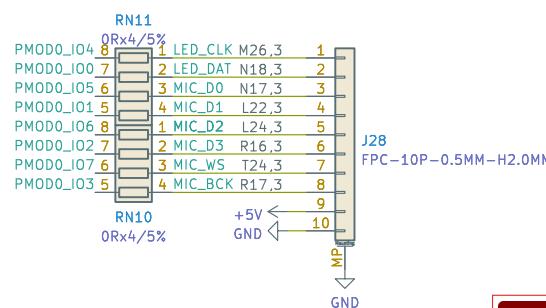
PMOD



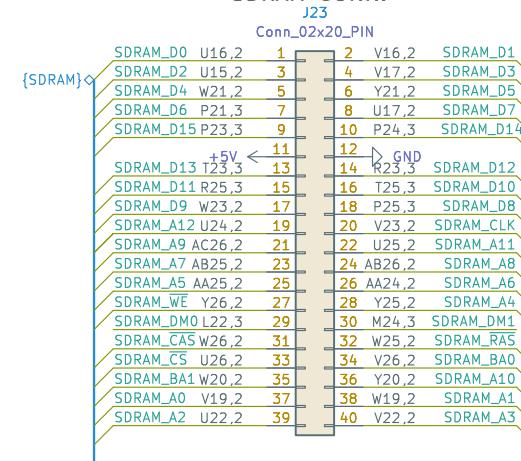
SSPI

| PIN | FUCTION | PMODO |
|-----|-----------|-------|
| N18 | SSPI_SO | I00 |
| R16 | SSPI_CLK | I02 |
| R17 | SSPI_WP | I03 |
| N17 | SSPI_SI | I05 |
| L24 | SSPI_CS | I06 |
| T24 | SSPI_HOLD | I07 |

MIC-ARRAY CONN.



SDRAM CONN.



SDRAM_DM0 SDRAM_DM1
SDRAM_DM1 SDRAM_DM0



Update: Fixed the Clock Tree page: Order of 2 exPLLs.

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Sheet: /FPGA_EXT_CONN./

File: EX_CONN..kicad_sch

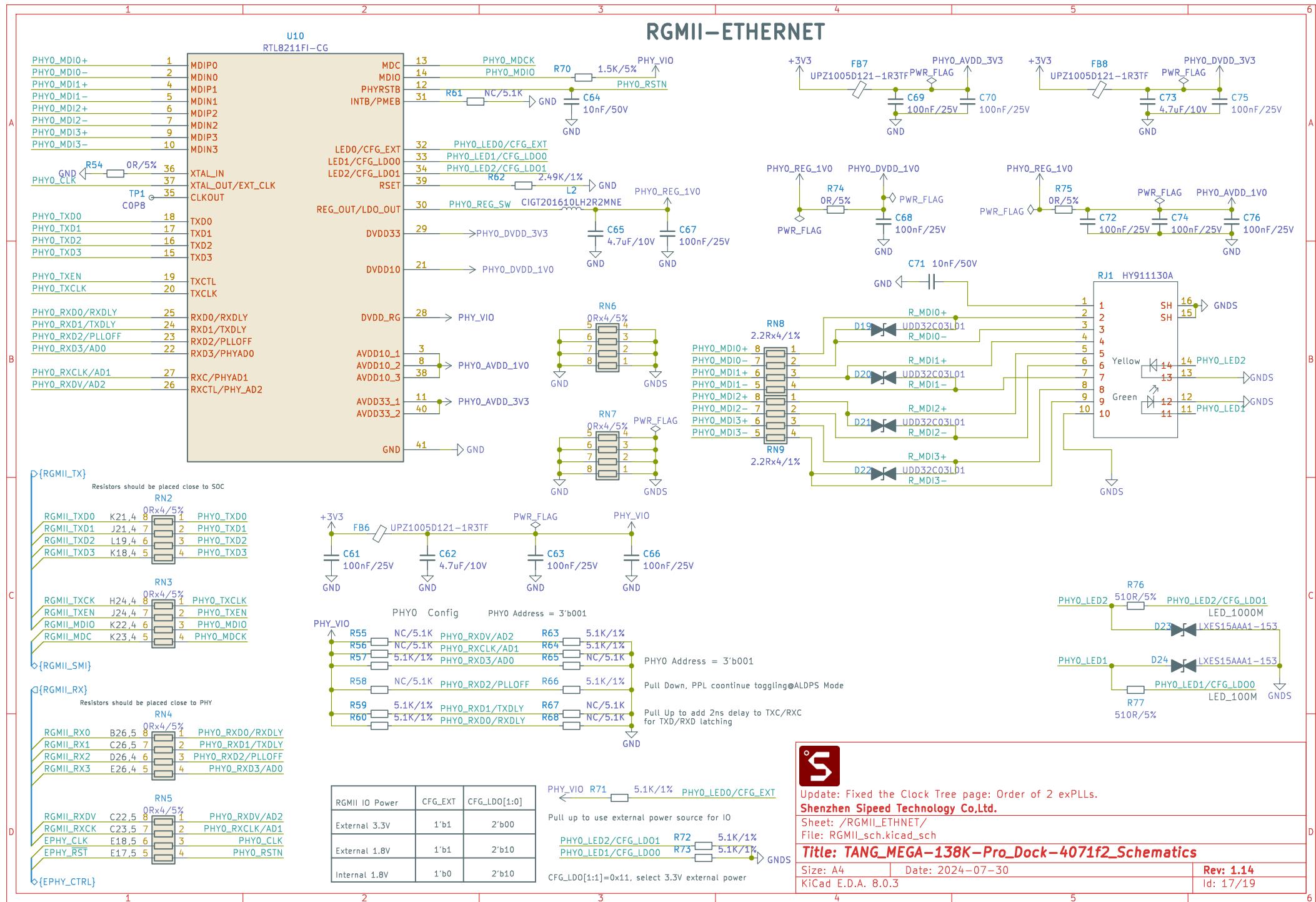
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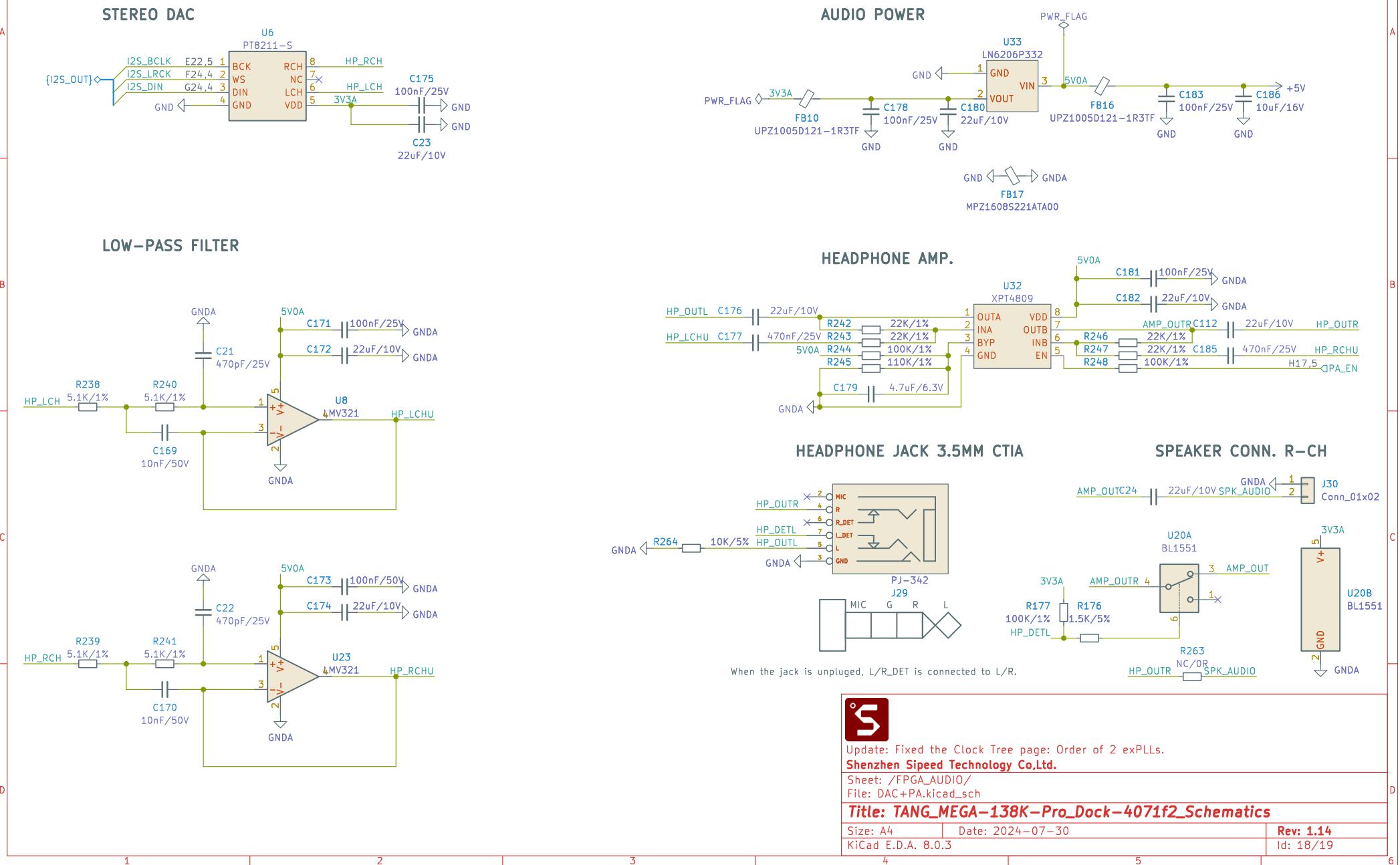
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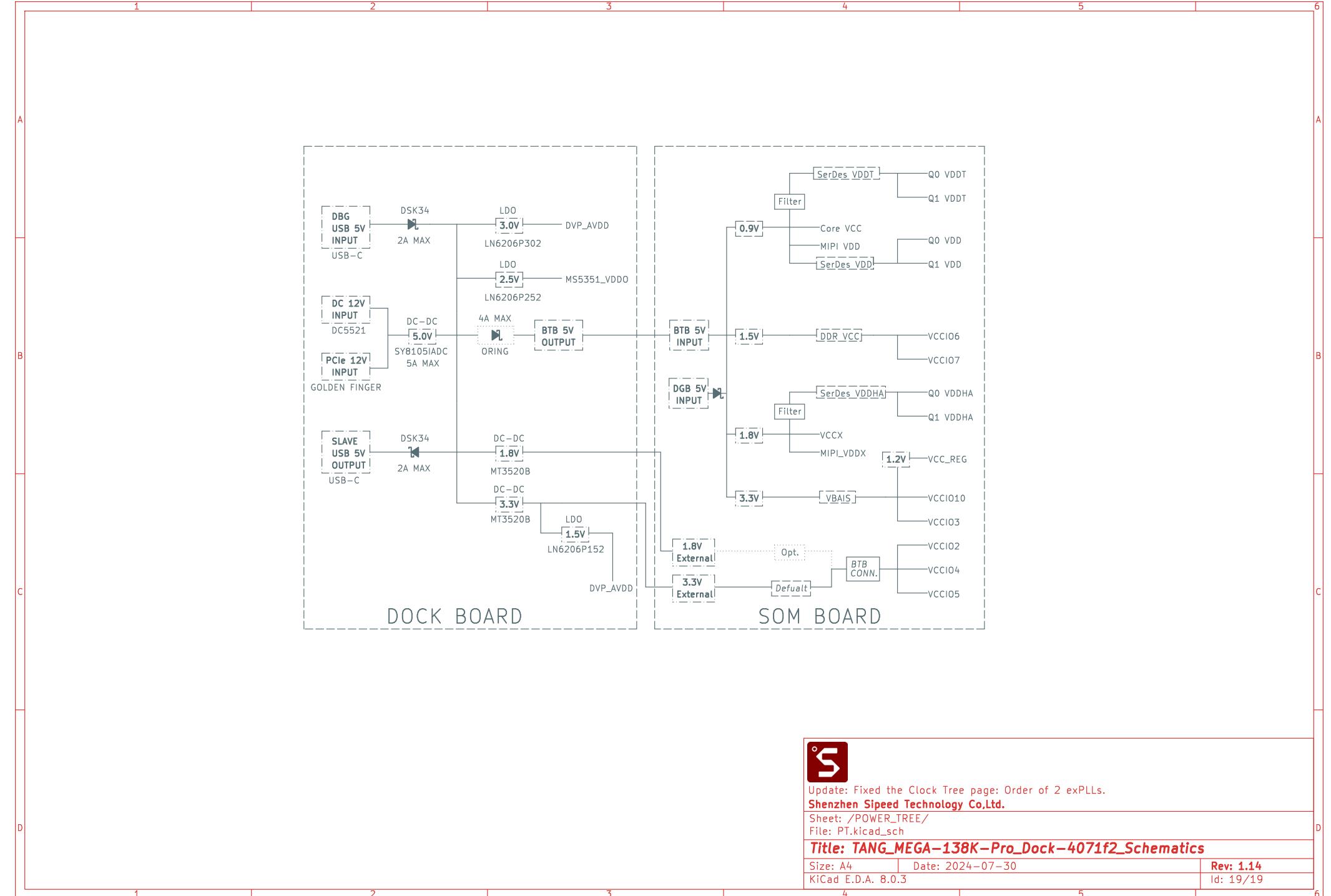
Rev: 1.14

Id: 16/19



FPGA-Audio





Update: Fixed the Clock Tree page: Order of 2 exPLLs.
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Sheet: /POWER_TREE/
File: PT.kicad_sch

Title: TANG_MEGA-138K-Pro_Dock-4071f2_Schematics

Size: A4 Date: 2024-07-30
KiCad E.D.A. 8.0.3

Rev: 1.14
Id: 19/19