Design Guide: TIDA-010086

Digital Control Reference Design for Cost-Optimized Battery Test Systems

Description

This reference design provides a cost-effective solution for battery formation and test applications. The design uses the C2000™ real-time control MCU for high-resolution pulse-width modulation (PWM) generation, and constant-current (CC) and constant-voltage (CV) control loops. It efficiently utilizes the MCU, and does not require a precision digital-to-analog converter, which saves more than 30% in the bill of materials. The flexibility of current and voltage loops in software allows users to achieve multiple current and voltage levels output with one design.

Features

- Bidirectional current control up to 10 A with less than ±0.01% accuracy
- C2000 on-chip 12-bit ADC achieves control accuracy better than ±0.05%
- Parallel up to 8 channels for wide output current range
- Flexible digital constant-current and constant-voltage control loops
- Channel-to-channel crosstalk error below 0.01%
- Multilevel protection in hardware and software for reliable power supply design

Resources

TIDA-010086	Design Folder
TMS320F280049	Product Folder
ADS131M08	Product Folder
INA821	Product Folder
TLV07	Product Folder

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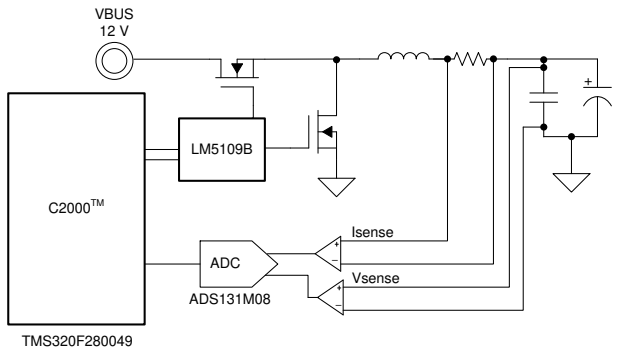
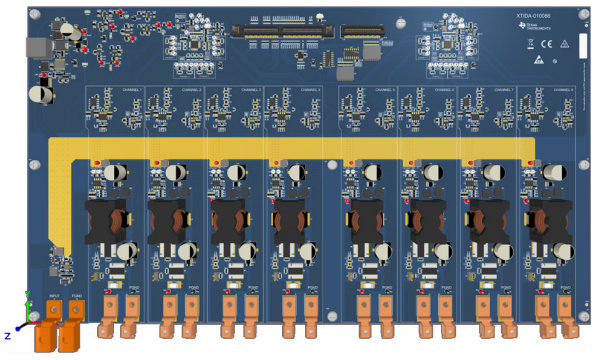
Applications

- Battery test





1 System Description

The battery tester equipment includes a wide variety of battery formation and test equipment for single cells, battery modules, and high-voltage battery packs. The test equipment contains precision control circuits, data acquisition systems, and various manufacturing tools that are important quality control and battery research activities.

1.1 Li-ion Battery Formation

Figure 1-1 shows a simplified Li-Ion battery manufacturing process. Battery testing comes at final stages of the production, in which formation is the most critical process. After the cell assembly process, each Li-ion battery goes through gradual charging, during which it forms a solid electrolyte interphase (SEI) layer that can consume significant portions of total battery capacity. Therefore, the test equipment must be able to precisely control the thickness of the SEI layer, which can bring down the capacity loss during formation to below 5%.

Tests such as self-discharge measurement and life span estimation are performed to remove defective cells during production. The battery test equipment must possess accurate voltage and current control, often better than ±0.05%, over the specified temperature range.

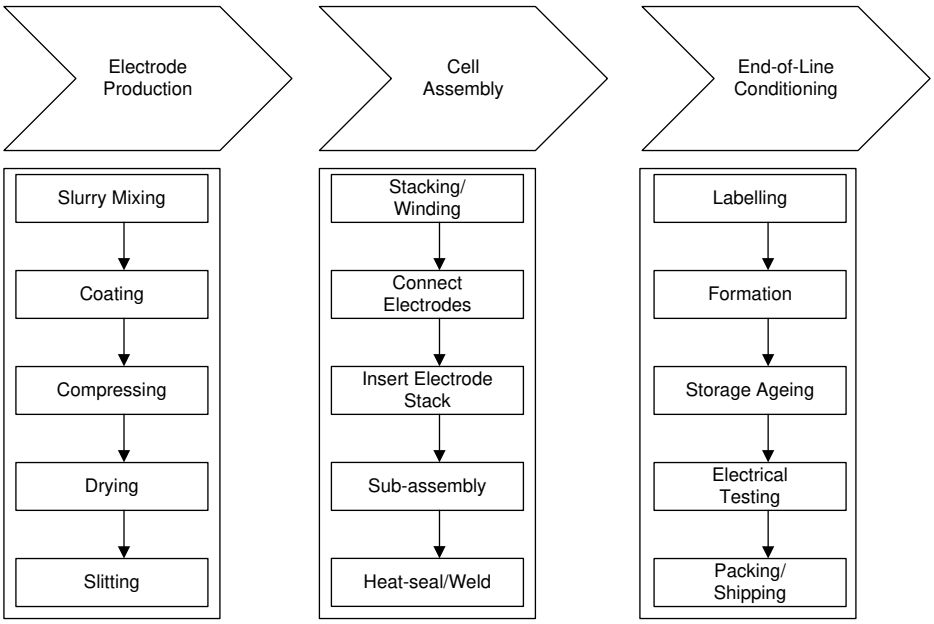


Figure 1-1. Simplified Li-Ion Battery Manufacturing Process

1.2 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS
LV port – Battery port	50 mV to 4.7 V
HV port–Bus voltage	9 V to 14 V
Switching frequency	100 kHz
Maximum DC current per channel, bidirectional	10 A
Current control accuracy	±0.01% FSR
Voltage control accuracy	±0.01% FSR
Current transient time	< 1 ms
Power stage and mode of operation	Synchronous buck converter, CCM Mode
Overcurrent protection PWM trip time	Protection in hardware < 1 PWM cycle using C2000 Comparators Protection in software < 50 µs to 100 µs (depends control loop frequency)

2 System Overview

2.1 Block Diagram

Figure 2-1 is a block diagram of the reference design. The TMS320F280049 MCU can control up to 8 independent channels. It generates a high-resolution 16-bit PWM for a synchronous buck power stage and performs subroutines for current and voltage control loops. The INA821 instrumentation amplifier senses the current and the TLV07 operational amplifier senses the voltage. Current and voltage signals are converted to digital data by both the external ADS131M08 ADC and the C2000 on-chip ADC. Having the 16-bit ADC in the feedback achieves a control accuracy better than ±0.01%. For cost-optimized systems, you can eliminate the ADS131M08 from the feedback and use the on-chip 12-bit ADC instead to achieve a control accuracy less than ±0.05%. See the *Test Results* section for more details.

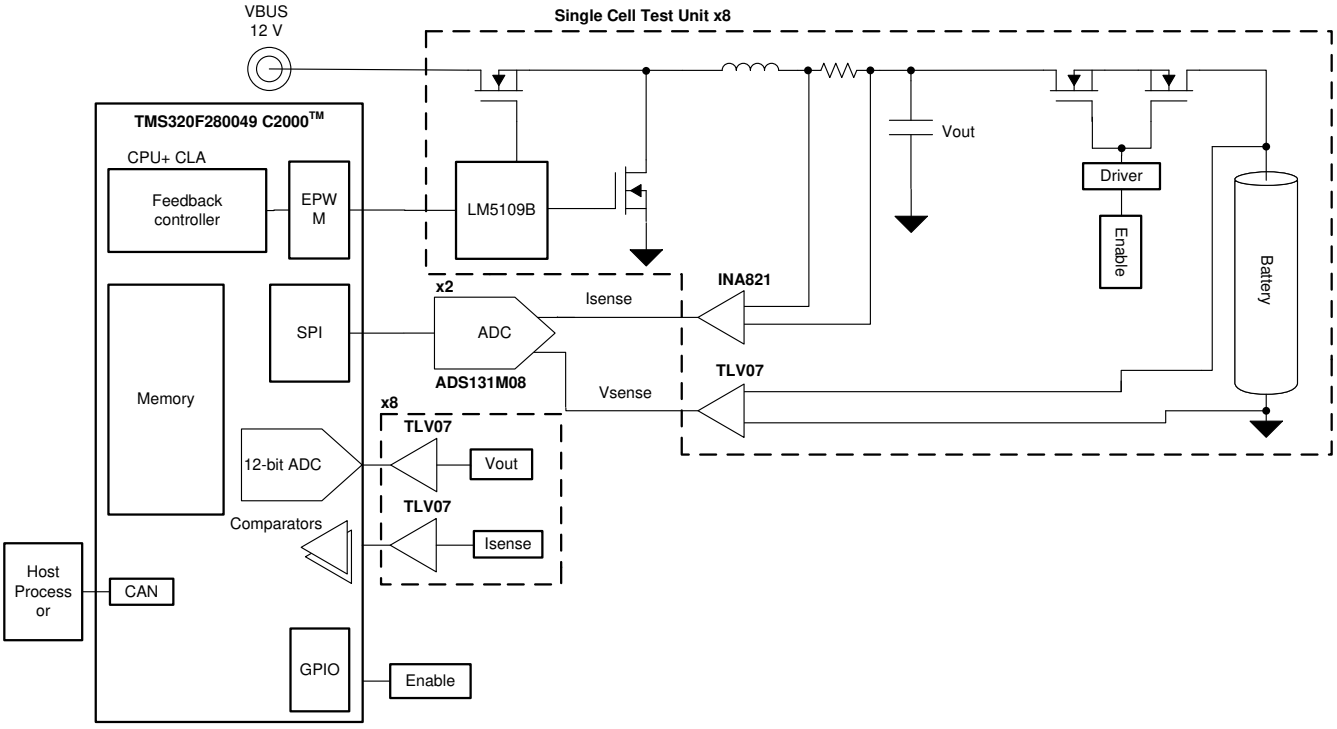


Figure 2-1. Digital Control Battery Tester

2.2 Design Considerations

2.2.1 High-Resolution PWM Generation

To generate high resolution, a C2000 with high-resolution PWM output capability is used. The high-resolution counter is capable of 150-ps time step, which is equivalent to 16-bit resolution at 100-kHz PWM frequency for a 100-MHz CPU clock. Table 2-1 shows PWM resolution at different switching frequencies.

Table 2-1. C2000™ MCU Resolution for PWM and HRPWM

PWM Freq	Regular Resolution (PWM)		High Resolution PWM	
	100-MHz EPWMCLK			
(kHz)	Bits	%	Bits	%
20	12.3	0.02	18.1	0
50	11	0.05	16.8	0.001
100	10	0.1	15.8	0.002
150	9.5	0.15	15.2	0.003
200	9	0.2	14.8	0.004
250	8.6	0.25	14.4	0.005

2.2.2 Feedback Controller

A C2000 must perform three actions in closed loop systems, which are sensing, control effort calculation, and output generation. For a digitally-controlled buck converter it will be reading and normalizing ADC current and voltage data, calculating error and compensation, and finally generating the duty cycle. CPU utilization for these tasks should not exceed 50%.

Figure 2-2 shows the feedback controller for a test channel. A multi-feedback controller is used to achieve smooth constant-current to constant-voltage transition where inner loop is always in constant-current mode. Upon detection of constant-voltage mode, the constant-voltage loop output is connected to the constant-current loop. Each test channel takes less than 500 CPU cycles. For a buck converter running at 100-kHz switching frequency and controller running at 10 kHz, it will only utilize 40% of total CPU to simultaneously control 8 test channels. The CPU utilization can be further reduced by half if the controller is implemented on the control-law accelerator (CLA), C2000 co-processor.

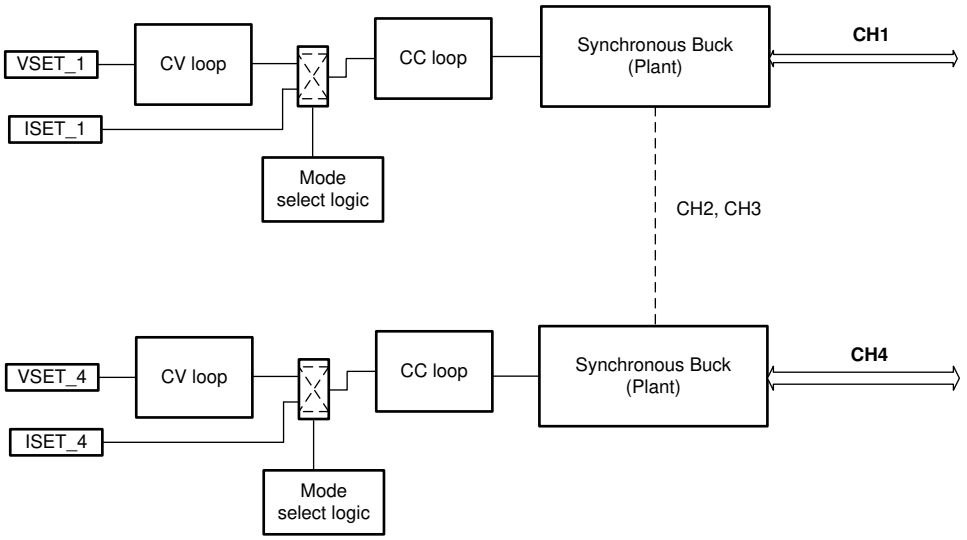


Figure 2-2. CCCV Feedback Controller

2.2.3 Multiphase Configuration

Since the feedback controller is in software, it gives the flexibility to operate multiple channels in parallel without any hardware changes. The design is configured in multiphase mode with a simple software change shown in Figure 2-3. In multiphase configuration, each phase uses separate CC loops and are connected in parallel. A single constant-voltage loop is nested to all constant current loops, which ensures current balancing in CV mode.

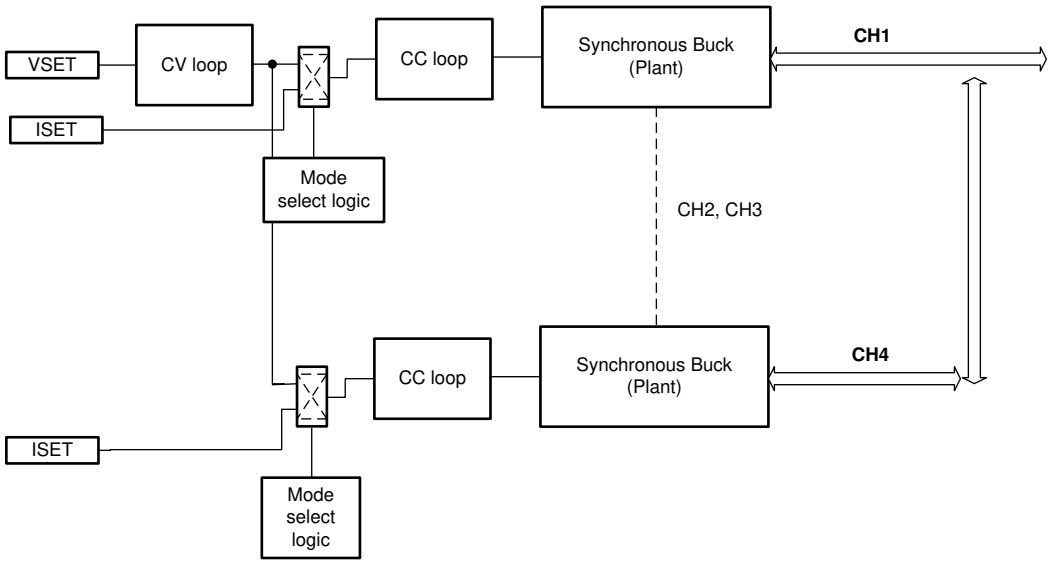


Figure 2-3. Multiphase Software Configuration

2.2.4 Current and Voltage Feedback

Current feedback uses a sense resistor to accurately measure the current of the battery. An instrumentation amplifier is used to measure the voltage across the sense resistor and scale it to ADC input level. Offset and gain errors are not a major concern because all test equipment gets calibrated. But gain and temperature drift parameters of the circuit are important to achieve current control accuracy below ±0.01% or ± 100 ppm over ±5°C temperature variation. For an example, selecting a 10 ppm/°C current-sense resistor gives only about 50 PPM margin. The INA821 device has 0.1-µV/°C input offset drift and 5-ppm/°C gain drift. For a 3-mΩ sense resistor and 10-A maximum current, the total drift will be 8 ppm/°C. ADC drift comes from its reference and with a reference of 3 ppm/°C device, the error is just slightly over 100 ppm.

Flicker or 1/f noise of the instrumentation amplifier might be concerning if the current sense resistor is too small. For an example, with a 3-mΩ sense resistor and 10-A output current, 1 fine current step corresponds to 3 µV change at the input of the instrumentation amplifier. Therefore, the 1/f noise of the amplifier should be smaller than 3 µV.

Voltage feedback path gives better error margin over temperature change. A 1-µV/C drift operation amplifier is less than 0.2 ppm/C error. Including error due to ADC, it gives a margin of more than 80 ppm.

2.2.5 Delta-Sigma ADC Clock Frequency Tuning

The digital filter of the delta-sigma ADC can be used effectively when its modulation frequency is 2^N times the switching frequency of the buck converter. Figure 2-4 shows ADS131M08 delta-sigma sinc filter frequency response. ADC frequency tuning will make sure of maximum attenuation of switching noise without decreasing the system bandwidth.

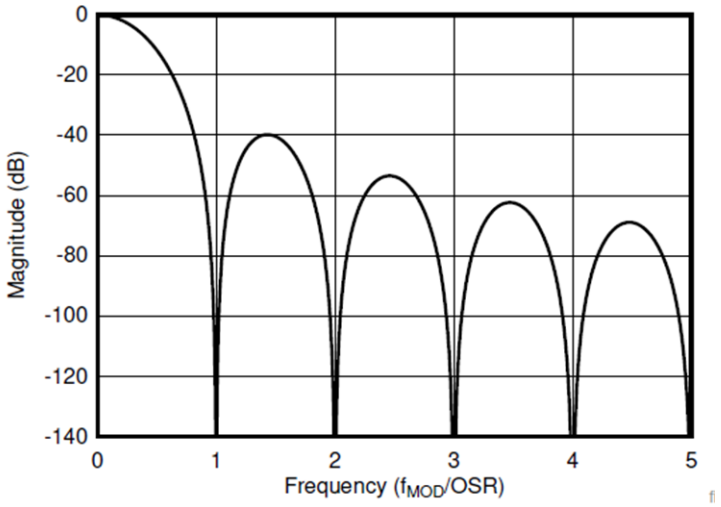


Figure 2-4. Sinc Digital Filter Response

2.2.6 Minimize Crosstalk Error With a Differential ADC

In a very dense PCB layout, error at the output is seen when the settings of adjacent channels are changed. This happens due to variations in the analog ground. Even a few µVs change in ground can produce few mA error in the current. To reduce this error, a differential ADC is used to sense ground of each instrumentation amplifiers.

2.2.7 Overcurrent Protection

The TMS320F280049 C2000 device includes 14 comparators with DAC or 7 window comparators. These comparators are utilized for overcurrent protection. In case of a fault, the comparators shut both high- and low-side PWM within 1 switching cycle. The second-level protection is implemented in control loop, where current controller is being reset during fault.

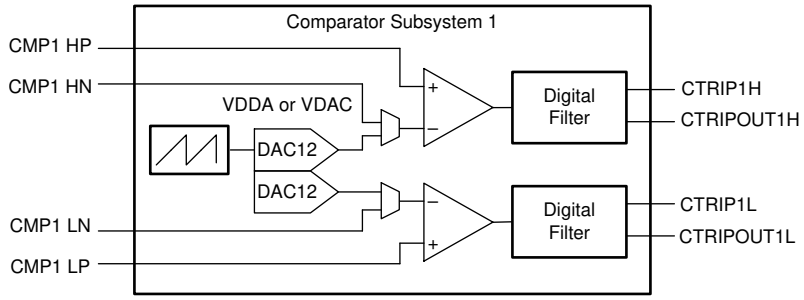


Figure 2-5. TMS320F280049 Comparator Subsystem

2.3 Highlighted Products

2.3.1 TMS320F280049

The TMS320F280049 C2000 device has 16 PWM outputs with high-resolution PWM control, 2 SPI ports, 21 analog input pins, and 40 digital pins that are sufficient to control 8 independent synchronous buck converter. The device runs at a 100-MHz clock and features a control law accelerator (CLA) that executes code independently of the main CPU. The CLA helps to reduce main CPU utilization to free up bandwidth for background tasks.

2.3.2 ADS131M08

The ADS131M08 is an eight-channel, simultaneously sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) that allows max sample rate up to 32 ksps and is sufficient for ± 0.01% accuracy and 1-kHz loop bandwidth.

2.3.3 INA821

The INA821 is a high-precision, low-noise instrumentation amplifier with low input offset (0.1 µV/C) and gain drift (5 ppm/C), which is capable to achieve ± 0.01% current control accuracy over ±5°C temperature change.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

Figure 3-1 shows various portions of TIDA-010086 hardware. The board requires a F280049C controlCARD Evaluation Module to test the hardware and software performance.

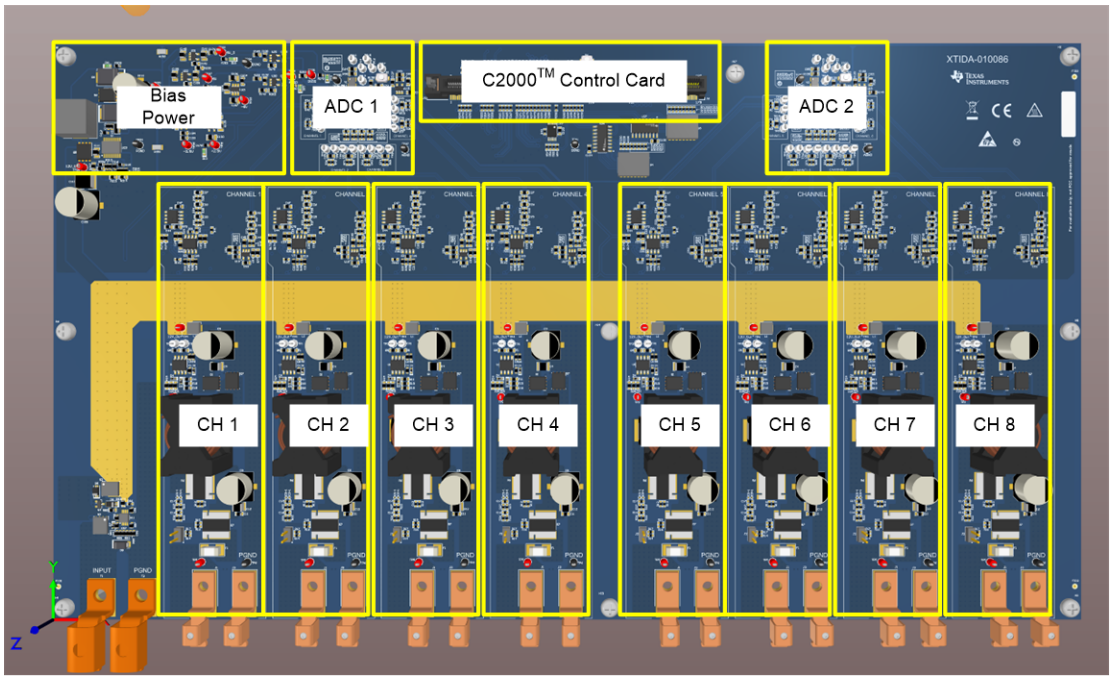


Figure 3-1. TIDA-010086 Hardware

3.2 Software

The software uses the Code Composer Studio (CCS) Integrated Development Environment (IDE) and C2000WARE-DIGITALPOWER-SDK library. Both C-Background and C-ISR framework is implemented in C-code. Figure 3-2 shows the software flow of this design. The background loop of the main application manages all system tasks, decision making, intelligence, and host interaction. The real-time critical actions such as ADC read, control updates, and PWM updates are executed inside the Interrupt Service Routine (ISR).

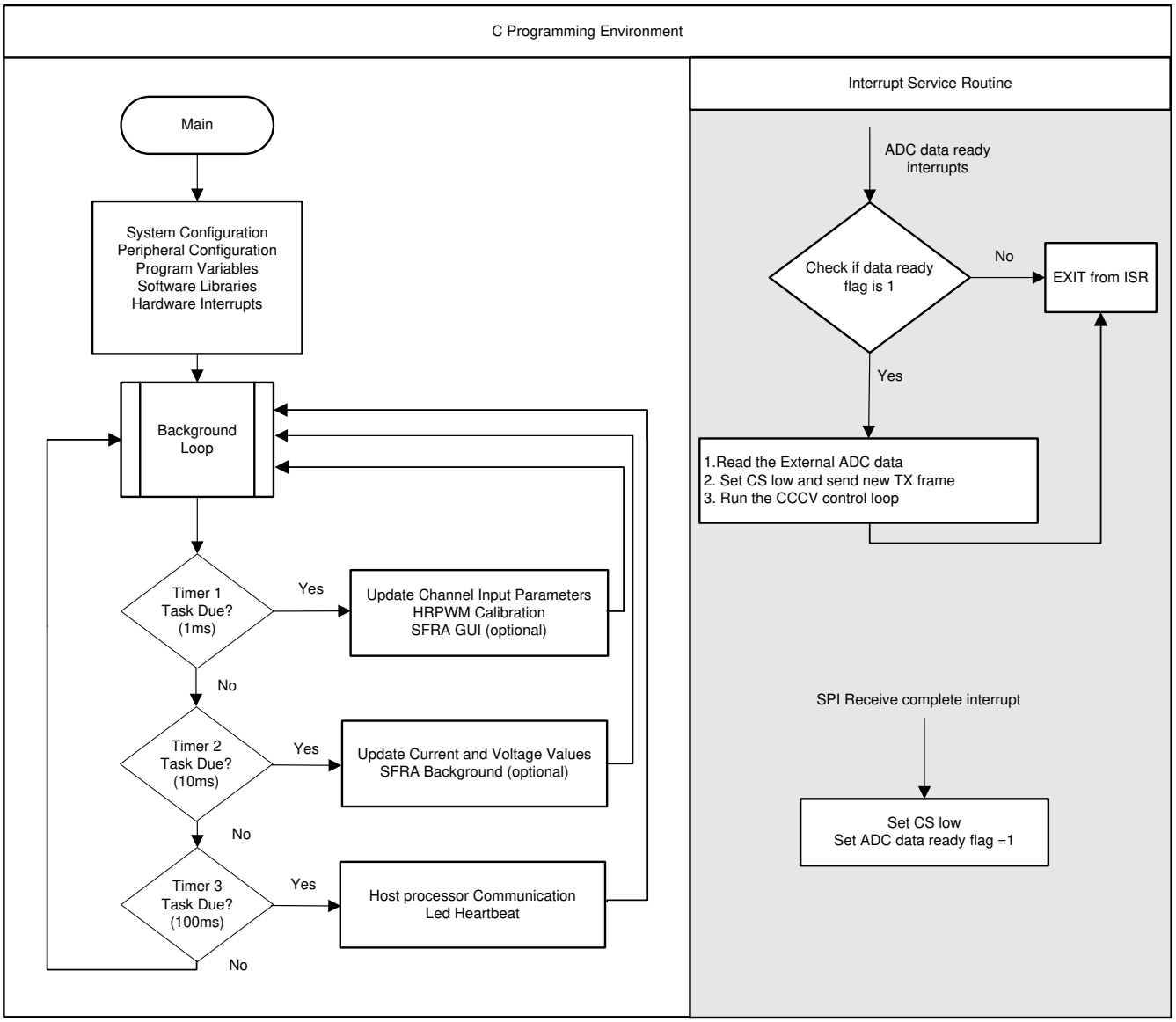


Figure 3-2. Software Flow Chart

3.3 Test Setup

The following steps are used to setup the hardware and software

1. Setup the hardware as shown in the test setup image in Figure 3-3

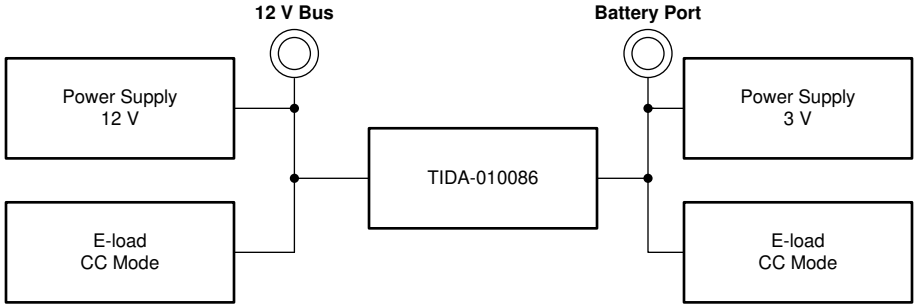


Figure 3-3. Test Setup

2. Insert F280049 Control Card in the control card slot on TIDA-010086 board
3. Turn on 12-V power supply and check bias power supplies (+10 V, +5 V, –5 V, +3.3 VA and +3.3 VD) on the TIDA-010086 board
4. Open CCS software and install C2000WARE-DIGITALPOWER-SDK if not installed. C2000WARE-DIGITALPOWER-SDK can be installed from CCS Resource Explorer Window.
5. Import TIDA-010086 code and re-build the project. Once the build is finished, click the debug button to load the code into C2000™ MCU.
6. Run the setupdebugenv.js file in the project to automatically load the user variables in the expression window
7. Set Enable = 1 to turn on the channel. The new current and voltage can be updated to Iref_A and Vref_V variables.

If it is desired to re-tune the whole control loop, it can be done in following steps using SFRA and compensation designer. See *C2000 Software Frequency Response Analyzer (SFRA) Library and Compensation Designer in SDK Framework User's Guide* for more information.

- Enable the SFRA and set it up as shown in Figure 3-4 to extract constant-current open-loop plant model.

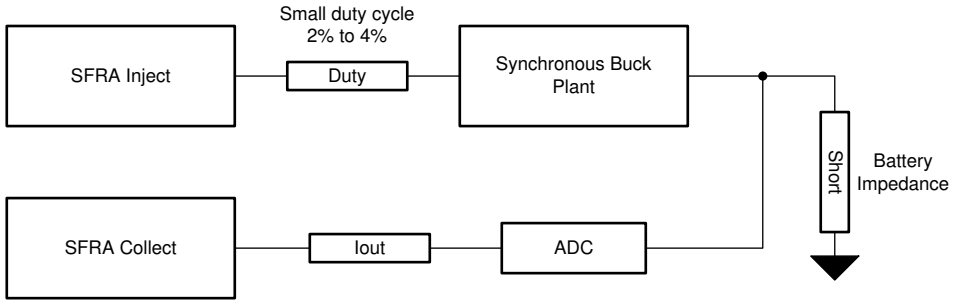


Figure 3-4. SFRA Setup for Plant Model Extraction

- Set the mode of operation to constant-current open loop and duty to about 2 to 5% such that output current is half of the rated current. Run SFRA to record plant data. Figure 3-5 shows plant frequency response for 10-mΩ output load.

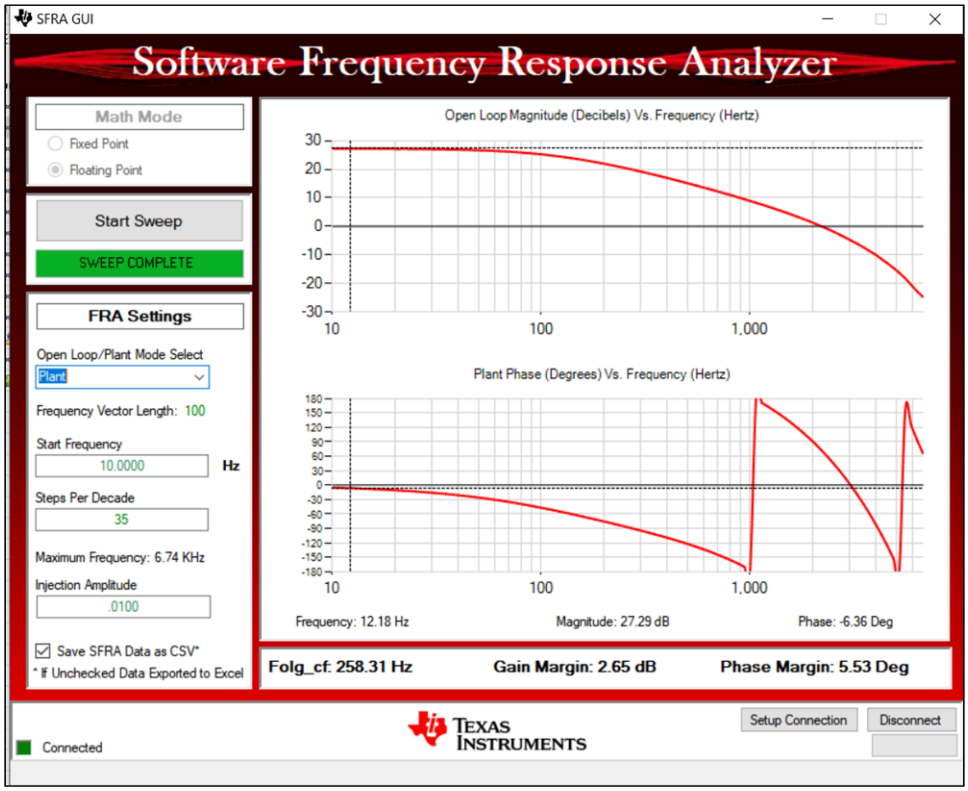


Figure 3-5. Plant Frequency Response

- Open compensation designer and load the plant data. Tune the compensation and update in the code

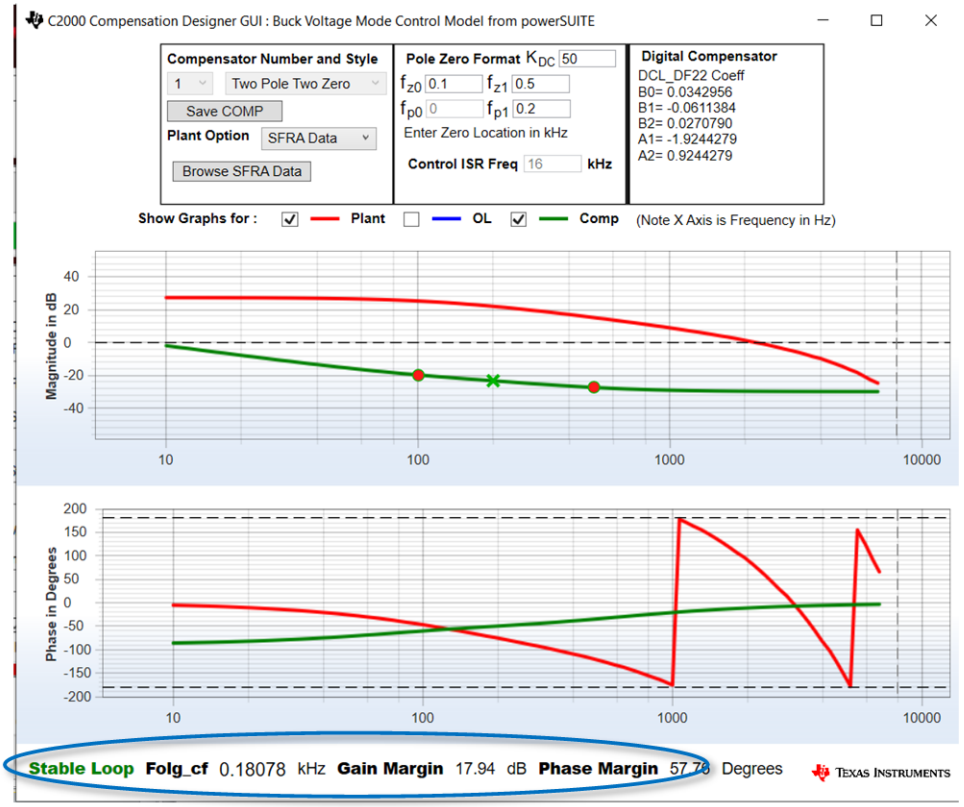


Figure 3-6. Tuning CC Loop Using Compensation Designer

- Setup SFRA as shown in Figure 3-7 to verify closed loop stability

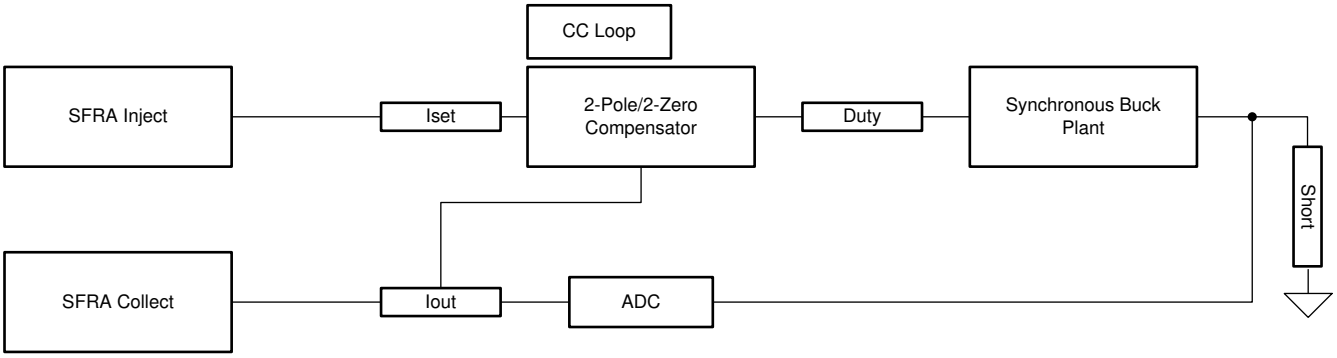


Figure 3-7. SFRA Setup Closed-Loop CC Mode

- Run SFRA to capture the data. Figure 3-8 shows CC mode frequency response. The closed-loop bandwidth matches to compensation designer value.

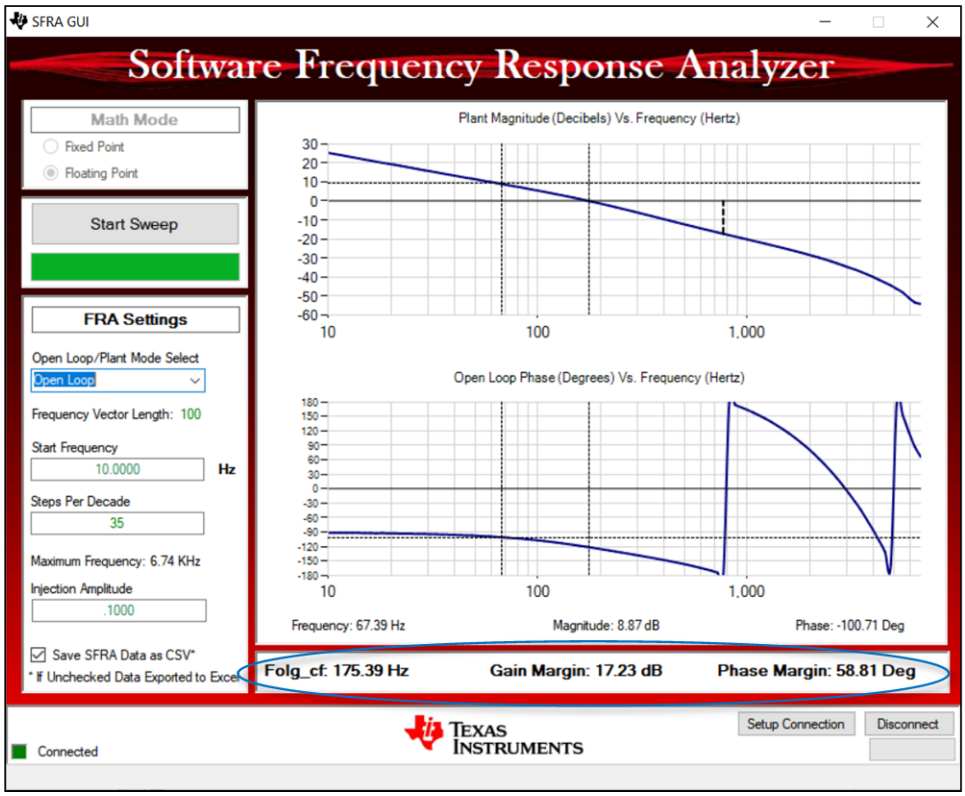


Figure 3-8. CC Mode Frequency Response

- Similar steps are followed to tune CV loop. Figure 3-9 and Figure 3-10 show CV mode SFRA setup in open and closed operation, respectively.

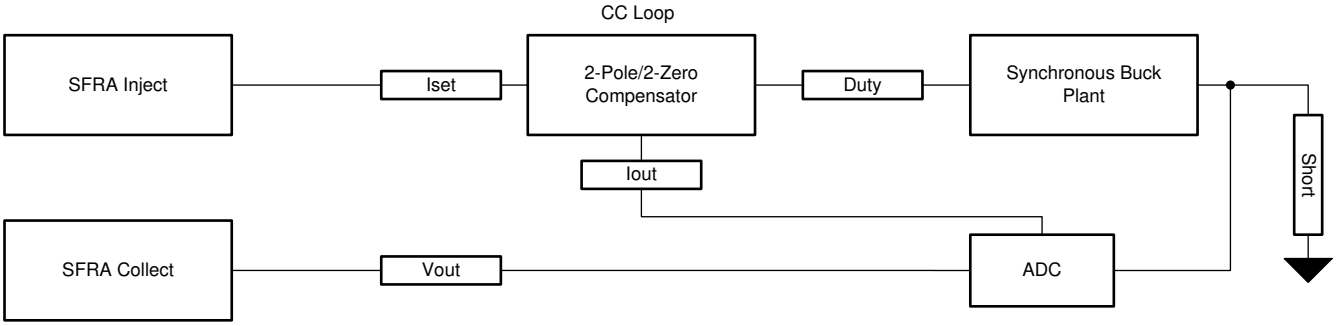


Figure 3-9. SFRA Setup Open-Loop CV Mode

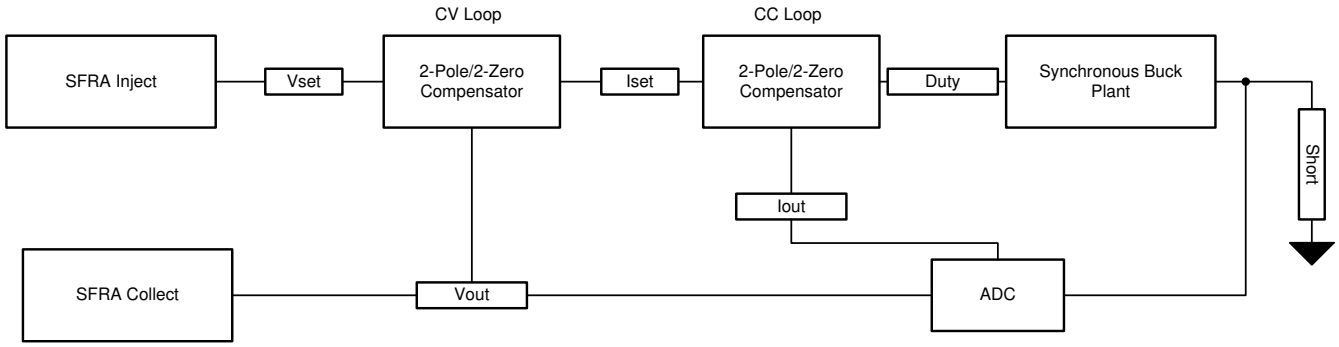


Figure 3-10. SFRA Setup Closed-Loop CV Mode

3.4 Test Results

3.4.1 Constant Control Accuracy ADS131M08 Feedback

The current accuracy depends on the current-sensing resistor, the gain, offset, and drift of the current amplifier, INA821, and TLV07 devices. These parameters vary from device to device. To achieve good current-control accuracy, the total gain and the offset of the designed circuit must be calibrated. Figure 3-11 shows current error after calibration at room temperature with ADS131M08 in the feedback. It can be seen that error increases at high output current > 8 A. This is due to heating of the current-sense resistor at higher output current. This error can be reduced by using smaller current-sense resistors such as 2 to 3 mΩ for 10-A output current.

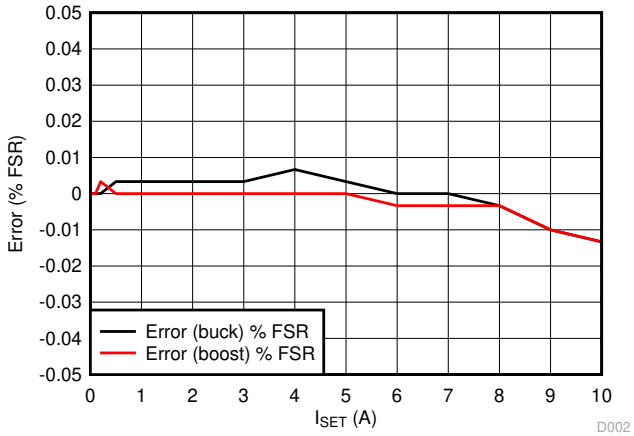


Figure 3-11. Constant-Current Control Accuracy ADS131M08 Feedback

Current feedback noise may change the average output current with variation in battery voltage. Table 3-1 shows output current under different battery voltage and current settings. The test data shows that variation in battery voltage has very little effect on the current.

Table 3-1. Output Current Under Different Battery Voltage and Current Settings

Vbat	Iset									
	0.01 A	0.1 A	1 A	6 A	10 A	0.01 A	0.1 A	1 A	6 A	10 A
	Charge Mode					Discharge Mode				
0.5	0.0103	0.1003	1.0007	6.001	10.001	0.01	0.1	1.0003	6.0003	-
1	0.0103	0.1003	1.0007	6.001	10.0007	0.01	0.1003	1.0003	6.0003	9.9993
2	0.0103	0.1003	1.0007	6.0007	10.0003	0.01	0.1003	1	6	9.9993
3	0.0103	0.1003	1.0007	6.0007	10	0.01	0.1	1	6	9.999
4	0.0103	0.1	1.0007	6.0007	9.9997	0.01	0.1	1	6	9.999
5	0.0103	0.1	1.0007	6.001	9.9997	0.01	0.1	1	6	9.999
Variation (% FSR)	0	0.003%	0	0.003%	0.013%	0	0	0.003%	0.003%	0.003%

3.4.2 Constant Control Accuracy 12-bit ADC Feedback

For cost-optimized systems, instead of the ADS131M08, use the 12-bit on-chip ADC in the feedback. In each PWM cycle 4 current measurements are taken, which is then averaged over 6 PWM cycles. Figure 3-12, Table 3-2, and Table 3-3 show output current error at different output current and voltage levels. It is observed that with a 12-bit ADC feedback, it is possible to achieve ±0.05% current control accuracy.

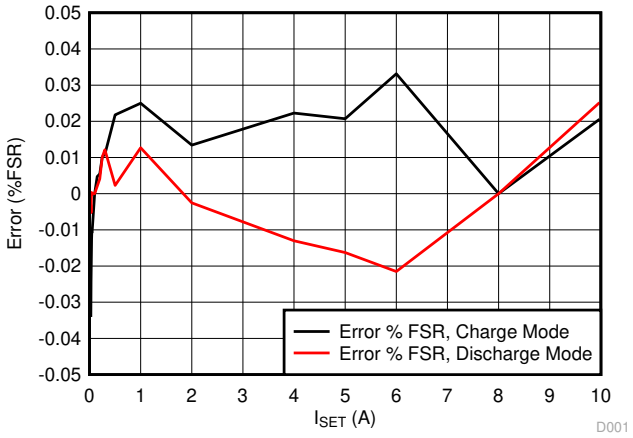


Figure 3-12. Constant-Current Control Accuracy 12-bit ADC Feedback

Table 3-2. Charge Current Under Different Output Voltage, 12-bit ADC Feedback

Vbattery	Iset - Charge Mode			
	0.1 A	1 A	5 A	10 A
0.5	1.0016	0.0984	5.01	10.025
1	1.0016	0.0984	5.01	10.023
1.5	1.0016	0.0984	5.0089	10.023
2	1.004	0.0984	5.0078	10.023
3	1.0004	0.0984	5.0078	10.023
4	1.0004	0.0984	5.0078	10.021
4.5	***1.0004***	0.0972	5.0066	10.023
Variation (% FSR)	***0.012%***	***0.036%***	**0.034%**	**0.04%**

Table 3-3. Discharge Current Control With Different Battery Voltage, 12-bit ADC Feedback

Vbattery	Iset – Discharge Mode			
	0.1 A	1 A	5 A	10 A
1	**0.0986**	**1.0034**	**5.0226**	**10.05**
2	0.0984	1.0032	5.0224	10.0484
3.1	0.0982	1.0028	5.0234	10.0448
3.7	0.098	1.003	5.0218	10.0458
4	0.0982	1.0036	5.023	10.0466
4.5	0.0982	1.0032	5.0222	10.0468
Variation (% FSR)	***0.006%***	***0.008%***	***0.016%***	***0.052%***

3.4.3 Constant-Voltage Control Accuracy

The voltage control accuracy of this system depends on the gain offset, offset of the resistor division, and the TLV07 device. This also requires calibration to achieve good voltage control accuracy. Figure 3-13 shows room temperature constant voltage control accuracy. The constant-voltage loop is calibrated under no load condition, and with same calibration coefficient the data is taken at 10-A load current. It is observed that control-voltage loop error is less than ±0.01% under both voltage setting and output current variation.

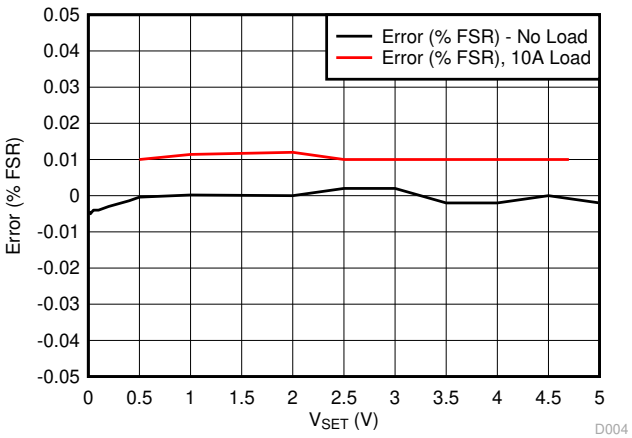


Figure 3-13. Constant-Voltage Control Accuracy

3.4.4 CC, CV Transformation

The complete battery formation profile should include both the CC control and the CV control. The transition from CC to CV mode should be smooth. Figure 3-14 and Figure 3-15 show CV mode the transition from CC mode under different current settings and charging-discharging modes.

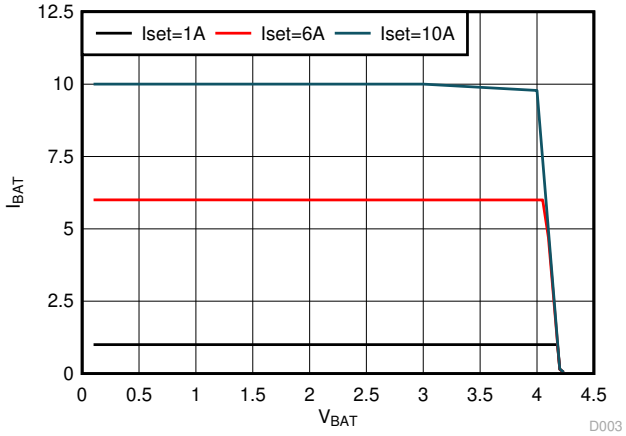


Figure 3-14. Charge Mode CC to CV Transition

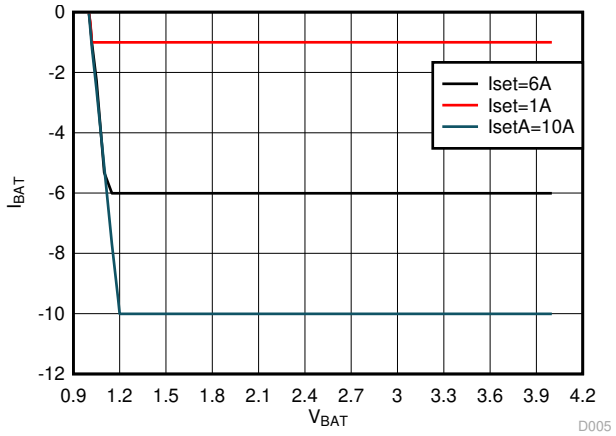


Figure 3-15. Discharge Mode CC to CV Transition

3.4.5 Constant-Current Transient Response

The current rise time of synchronous buck is a function of L/R time. Larger power inductor and smaller path impedance limits the current speed. Figure 3-16 shows current transient response in charge mode tested at 10 mΩ. If the control loop is optimized at 10-mΩ output load, the current transient will be slower by 10 times when the circuit is tested at 100-mΩ load. It is important to optimize the loop with the battery load to achieve the desired result.

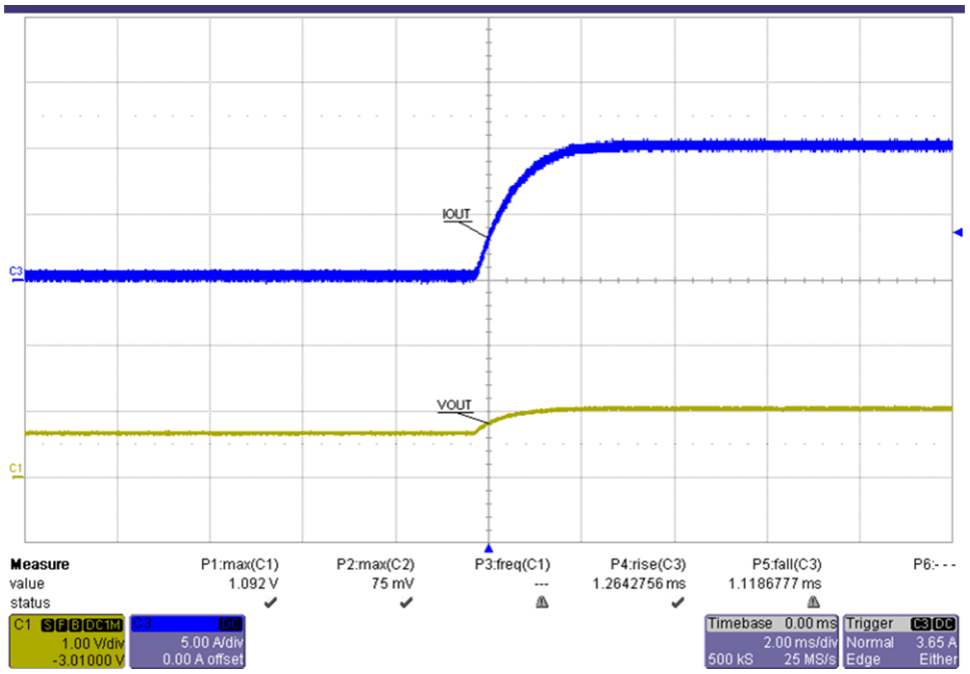


Figure 3-16. Output Current Transient Response

3.4.6 Charge to Discharge Mode Transition

Automotive batteries are tested for fast current source and sink capability. The battery tester should be able to quickly switch between charge and discharge modes. Figure 3-17 shows smooth current transition when the mode is changed from discharging to charging at 10-A output current.

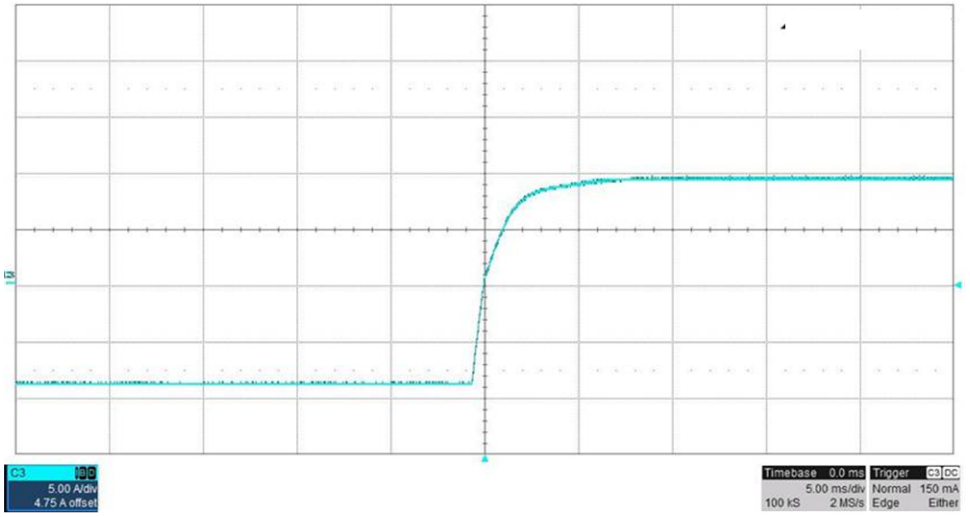


Figure 3-17. Current Transition When Switching From Discharge to Charge Mode

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010086.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010086.

4.2 Tools and Software

Tools

TMDSCNCD280049C	F280049C controlCARD Evaluation Module

Software

CCSTUDIO	Code Composer Studio (CCS) Integrated Development Environment (IDE)
C2000WARE-DIGITALPOWER-SDK	DigitalPower software development kit (SDK) for C2000™ MCUs

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

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