

# Lab 1 Report

Ben Lowman | brl2xx | Sec. 105

February 16, 2014

## 1 Problem Statement

This lab activity required the development and testing of a simple logic circuit. The circuit was intended to help the workers of a smoothie shop decide when to open a second smoothie prep station. As the owners already kept good records of the number of smoothies being prepped at any given time (a four bit binary number with terms  $n_3, n_2, n_1, n_0$ ), all that was needed was a circuit to return true when the number of smoothies in the queue was more than ten or less than six – when to open and close the second prep station, respectively. In addition, the logic circuit had to be implemented using a limited number of gate packages:

- Four two-input AND gates
- Four two-input OR gates
- Six inverters

## 2 Solution

Before attempting to construct any logic functions, a truth table was created for  $f_1$  and  $f_2$ .

$f_1$  is true when the 4-bit positive binary number  $N = n_3 n_2 n_1 n_0$  is greater than ten.  $f_2$  is true when  $N$  is less than six. The equivalent decimal value is listed in the leftmost column of the table. In this circuit, these decimal values represent the number of smoothies currently being processed.


$N$	$n_3$	$n_2$	$n_1$	$n_0$	$f_1$	$f_2$
0	0	0	0	0	0	1
1	0	0	0	1	0	1
2	0	0	1	0	0	1
3	0	0	1	1	0	1
4	0	1	0	0	0	1
5	0	1	0	1	0	1
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	0	0
10	1	0	1	0	0	0
11	1	0	1	1	1	0
12	1	1	0	0	1	0
13	1	1	0	1	1	0
14	1	1	1	0	1	0
15	1	1	1	1	1	0

From this table, functions  $f_1$  and  $f_2$  were expressed as a sum of products. The functions were then algebraically reduced to a form that was more conducive to implementation on the provided hardware. This process is enumerated below for both functions:

$$\begin{aligned}
f_1 &= n_3 n'_2 n_1 n_0 + n_3 n_2 n'_1 n'_0 + n_3 n_2 n'_1 n_0 + n_3 n_2 n_1 n'_0 + n_3 n_2 n_1 n_0 \\
&= n_3 (n_1 n_0 (n_2 + n'_2) + n_2 (n'_1 n'_0 + n'_1 n_0 + n_1 n'_0)) \\
&= n_3 n_1 n_0 + n_3 n_2 (n_1 n_0)' \\
&= (n'_3 + (n_1 n_0)')' + n_3 n_2 (n_1 n_0)'
\end{aligned}$$

$$\begin{aligned}
f_2 &= n'_3 n'_2 n'_1 n'_0 + n'_3 n'_2 n'_1 n_0 + n'_3 n'_2 n_1 n'_0 + n'_3 n'_2 n_1 n_0 + n'_3 n_2 n'_1 n'_0 + n'_3 n_2 n'_1 n_0 \\
&= n'_3 (n'_2 n'_1 (n_0 + n'_0) + n'_2 n_1 (n_0 + n'_0) + n_2 n'_1 (n_0 + n'_0)) \\
&= n'_3 (n'_2 n'_1 + n'_2 n_1 + n_2 n'_1) \\
&= n'_3 (n_2 n_1)' \\
&= (n_3 + n_2 n_1)' \quad \dots
\end{aligned}$$

The functions were then implemented in Logisim. Note that the pins were labeled in the form  $a.b.c$ , where  $a$  and  $b$  are inputs and  $c$  is the output. For inverters, the form was  $a.b$  where  $a$  and  $b$  represent the input and output, respectively.



logisim.png

In addition to digital implementation, the circuit was also implemented on real hardware. As little documentation was required for this process, comments are minimal. Using a breadboard, appropriate IC chips, and

switches for the four binary variables, the circuit was implemented successfully; behaviour was as predicted.

### 3 Problems Encountered

I did encounter some difficulties during the lab. Most principally, the Prelab was completed far earlier than it needed to be (my personal calendar was marked incorrectly). As such, I was not aware of Karnaugh Maps and lacked a more general “algebraic intuition.” In other words, simplifying the logic expressions was far more difficult than it needed to be. In addition, my implementation of the circuit is not the most minimal. It *does* fall within the specified parameters, however, upon further simplification  $n_0$  is not even needed.

Consequently, implementing my circuit design in the lab section was a bit more tedious. It might also be worth mentioning that I did initially have a bad inverter package. It was an easy fix, although it took a significant amount of time to diagnose.

### 4 Conclusion

I have learned – more than anything – that minimal logic expressions are absolutely crucial when implementing circuits in the real world. While this lab was fairly simple, I imagine the difficulty will ramp up quickly.

In addition, I was never really aware of the power that lies behind simple logic gates. Watching your bunch of wires react expectedly is actually quite exciting.