Homework 1

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1.3 Insructions in a high level language (Such as C) are first translated into assembly language by a compiler. An assembler then coverts from assembly language into machine langauge. This is the language that executes on the processor.

1.4 (a) The buffer size B in bytes is given by the equation

$$B = (\text{bytes per subpixel}) \times (\text{number of subpixels per pixel}) \times (\text{number of pixels})$$

Substituting the given qunatities:

$$B = \frac{8\,\text{bits}}{8}\,\text{MB} \times 3 \times 1280 \times 1024 = 3.93\,\text{MB}$$

(b) The time t required for the transfer is given by dividing the total data transfered by the transfer rate

$$t = \frac{3.93\,\text{MB}}{\frac{100\,\text{bits}}{8}\,\text{MB/s}} = 0.31\,\text{s}$$

1.5 (a) Performance P in instructions per second is given by dividing clock rate by the CPI

$$P_1 = \frac{3\,\text{GHz}}{1.5\,\text{CPI}} = 2 \times 10^9\,\text{instructions/s}$$
$$P_2 = \frac{2.5\,\text{GHz}}{1.0\,\text{CPI}} = 2.5 \times 10^9\,\text{instructions/s}$$
$$P_3 = \frac{4\,\text{GHz}}{2.2\,\text{CPI}} = 1.82 \times 10^9\,\text{instructions/s}$$

(b) Multiplying the performance by time gives the total number of instructions I

$$
\begin{aligned}
I_1 &= 2 \times 10^9 \,\text{instructions/s} \times 10\,\text{s} = 2 \times 10^{10} \,\text{instructions} \\
I_2 &= 2.5 \times 10^9 \,\text{instructions/s} \times 10\,\text{s} = 2.5 \times 10^{10} \,\text{instructions} \\
I_3 &= 1.82 \times 10^9 \,\text{instructions/s} \times 10\,\text{s} = 1.82 \times 10^{10} \,\text{instructions}
\end{aligned}
$$

Multiplying the total number instructions by the CPI gives the total cycles C

$$
\begin{aligned}
C_1 &= 2 \times 10^{10} \,\text{instructions} \times 1.5\,\text{CPI} = 3 \times 10^{10} \,\text{cycles} \\
C_2 &= 2.5 \times 10^{10} \,\text{instructions} \times 1\,\text{CPI} = 2.5 \times 10^{10} \,\text{cycles} \\
C_3 &= 1.82 \times 10^{10} \,\text{instructions} \times 2.2\,\text{CPI} = 4.0 \times 10^{10} \,\text{cycles}
\end{aligned}
$$

(c) The clock rate must increase proportionally (20 percent) with the increase in CPI to acheive the target time reduction.

1.6 (a) The global CPI G is the weighted average of the CPI per each individual instruction set

$$
\begin{aligned}
G_1 &= .1 \times 1\,\text{CPI} + .2 \times 2\,\text{CPI} + .5 \times 3\,\text{CPI} + .2 \times 3\,\text{CPI} = 2.6\,\text{CPI} \\
G_2 &= .1 \times 2\,\text{CPI} + .2 \times 2\,\text{CPI} + .5 \times 2\,\text{CPI} + .2 \times 2\,\text{CPI} = 2\,\text{CPI}
\end{aligned}
$$

(b) Multiplying the total instructions by the CPI gives the total clock cycles needed C

$$
\begin{aligned}
C_1 &= 1 \times 10^6 \,\text{instructions} \times 2.6\,\text{CPI} = 2.6 \times 10^6 \,\text{cycles} \\
C_2 &= 1 \times 10^6 \,\text{instructions} \times 2\,\text{CPI} = 2 \times 10^6 \,\text{cycles}
\end{aligned}
$$

The question in the book does also ask which processor is faster. The time t needed to execute the cycles is given by dividing the total number of cycles by the clock rate

$$
\begin{aligned}
t_1 &= \frac{2.6 \times 10^6 \,\text{cycles}}{2.5\,\text{GHz}} = 1.04 \times 10^{-3}\,\text{s} \\
t_2 &= \frac{2 \times 10^6 \,\text{cycles}}{3\,\text{GHz}} = 0.67 \times 10^{-3}\,\text{s}
\end{aligned}
$$

P_2 is faster.