Sumedha IT
Where Success Begins

Feb & March Batches

For MAR PD

1. What are the inputs and outputs of Synthesis?
2. What is synthesis? Explain synthesis flow?
3. What is the difference between Logical synthesis and physical synthesis?
4. Explain goals of Synthesis?
5. What is the information present in .lib file?

For March & Feb DV

1. Serial Adder
2. Counters
   a) 4-bit Synchronous Counters
   b) 4-bit Asynchronous Counters
   c) 8-bit Single Up Counter
   d) 8-bit Up Counter with Load
   e) 8-bit Up-Down Counter
   f) Random LFSR
   g) LFSR Up/Down
   h) Gray Counter
   i) One-hot Counter
   j) Divide by 2 Counter

March PD & CL - CF

1. Explain short channel device. What are the short channel effects?
2. What is channel length modulation and velocity saturation how does it impact short channel devices?

March CL - CL

1. Draw the AND gate(tranststor level) Schematic,Stick digram & generate Netlist.
2. What is meant by p-cell & advantages ?