Science & Technology Facilities Council
Rutherford Appleton Laboratory

SDC Timing Constraints Quick Reference Card

Revision 1.4

Synopsys Design Constraints

The Synopsys Design Constraints (SDC) format is widely used for specifying timing constraints for a design. SDC is based on the tool command language (TCL) and is used by all Synopsys EDA tools. This quick reference card aims to illustrate the most important SDC commands.

Useful SDC switches

Most of the commands will accept the following switches, to specify which type of edge or timing path the constraint is being applied:

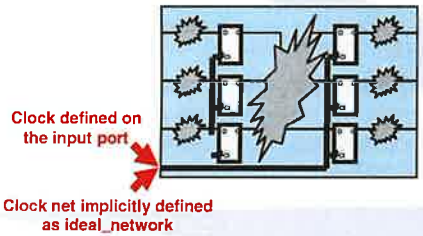
`-min` = used for hold timing analysis
`-max` = used setup timing analysis
`-rise` = delay associated with rising edge input
`-fall` = delay associated with falling edge input

Clocks

Defining Clocks

The most important constraint is the clock constraints, since this will constrain the vast majority of timing paths:

```
create_clock -period 15 -name my_clock \
                              [get_ports clk]
```



Modelling Clocks

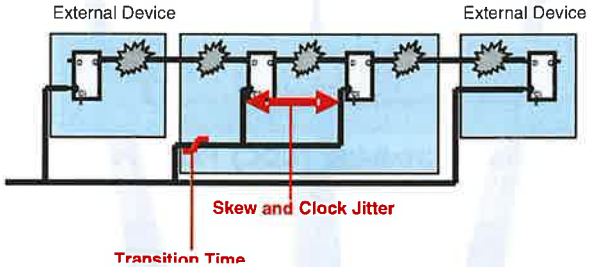
You need to model the clock during synthesis and during the initial stages of place and route to ensure that the tools leave enough slack for the insertion of the clock tree. Note: After CTS the tools need to ignore all of these clock modelling values/commands except for the jitter value.

Clock Skew and Jitter (added together)

```
set_clock_uncertainty 0.2 [get_clocks my_clock]
```

Clock Transition Time

```
set_clock_transition 0.1  [get_clocks my_clock]
```



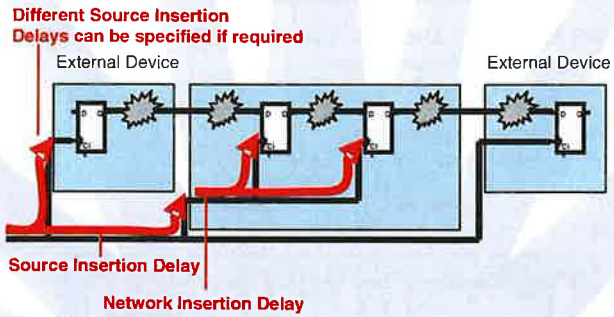
Clock Source Insertion Delay

```
set_clock_latency -source 0.5 \
                              [get_clocks my_clock]
```

Clock Network Insertion Delay

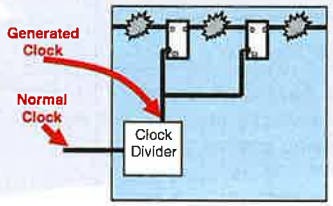
Also called the clock insertion delay

```
set_clock_latency 0.5 [get_clocks my_clock]
```



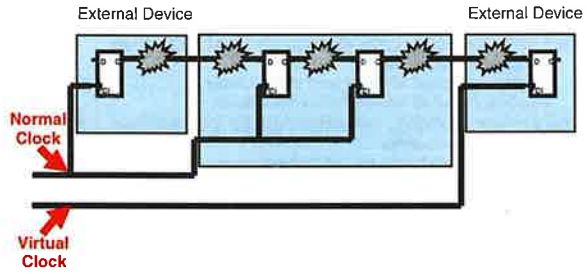
Generated Clocks

```
create_generated_clock -name my_gclock \
  -source clk -divide_by 2 INFF1/Q
```



Virtual Clocks

```
create_clock -period 10 -name off_chip_clk
set_output_delay 2.5 -clock off_chip_clk OUT2
```

Input/Output Constraints

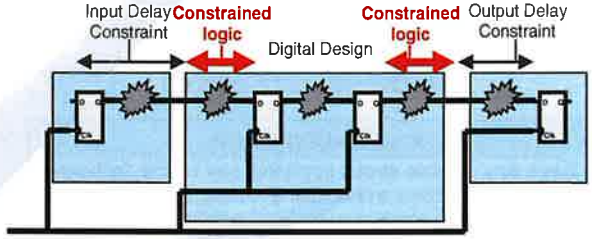
Warning: The default IO constraints are zero and must be overridden, otherwise your timing analysis/optimisation will be optimistic.

Input Delay

```
set_input_delay 1 -max -min -clock my_clock \
  [remove_from_collection [all_inputs] clk]
```

Output Delay

```
set_output_delay 1 -max -min -clock my_clock \
  [all_outputs]
```



Input Drive Resistance

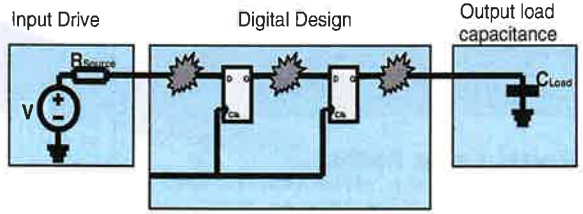
```
set_drive -max 1 [all_inputs]
set_drive -min 0.01 [all_inputs]
```

Input Drive Resistance from a Library Cell

```
set_driving_cell -cell lib_cell -pin pin_name \
[remove_from_collection [all_inputs] clock]
```

Output Load Capacitance

```
set_load -max 3 [all_outputs]
set_load -min 1 [all_outputs]
```



Understanding values for IO Constraints

For hold (-min switch), considering the optimal case

- Smallest external delay
- Smallest expected external load capacitances
- Smallest expected external drive resistances

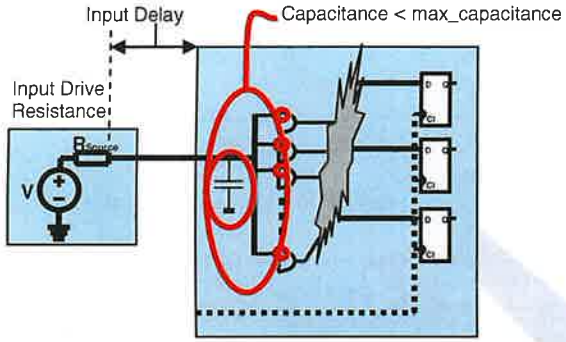
For setup (-max switch), considering the pessimistic case

- Largest external delay
- Largest expected external load capacitances
- Largest expected external drive resistances

It is typical to set the rising (-rise) and falling (-fall) edge constraints to be the same unless you know otherwise.

Internal Input Capacitance

```
set_max_capacitance 4 [remove_from_collection \
                      [all_inputs] [get_ports clk]]
```

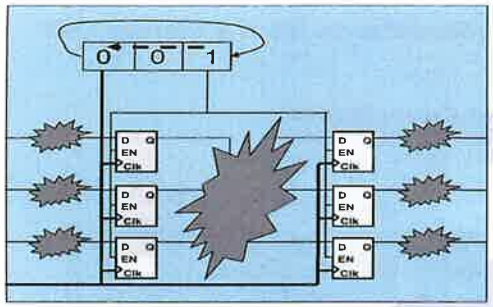


Timing Exceptions

If you have any doubts about applying any of the following timing exceptions, then avoid using them, since they will give incorrect timing analysis results if applied incorrectly!

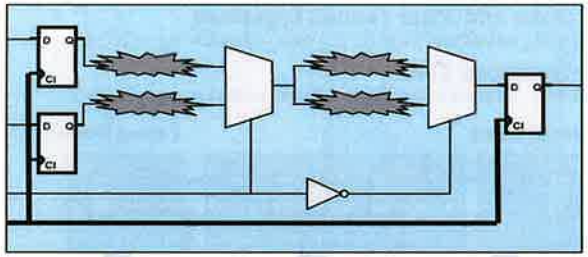
Multicycle Paths

```
set_multicycle_path -setup 3 -to FF2
set_multicycle_path -hold 2 -to FF2
```



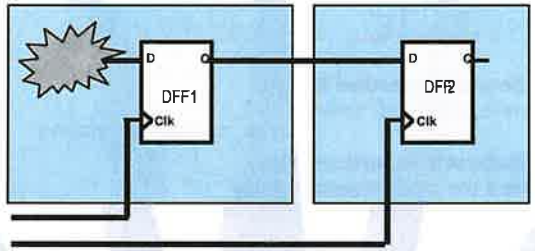
Functional False Paths

```
set_false_path -setup -from IN2 -to FF12
reset_path -setup -from IN2 -to FF12
```

Clock Domain Crossing (CDC) False Paths

```
set_false_path -from [get_clock clk1] \
               -to   [get_clock clk2]
```



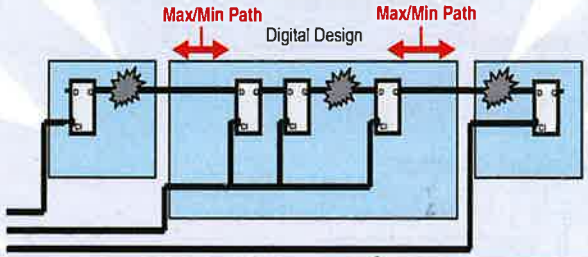
Point to Point Delays Constraints

For setup analysis/optimisation:

```
set_max_delay 10 -from [get_pins ff1/q] \
                 -to [get_ports output1]
```

For Hold analysis/optimisation:

```
set_min_delay 8 -from [get_pins ff1/q] \
                -to [get_ports output1]
```



Other Constraints

Defining Resets / High fan-out nets

Note: It is generally best to ignore all high fan-out nets during synthesis using the following command:

```
set_ideal_network [get_ports rst_n]
```

Preventing Modification/Timing Analysis

`set_dont_touch`	Don't modify an object
`set_dont_touch_network`	Don't modify a network

Note: Timing analysis is still performed if either of these "don't_touch" commands are used.

`set_ideal_net`	Don't modify a net, or perform timing analysis on the net
`set_ideal_network`	Don't modify a network (or objects in the network), or perform timing analysis on the network

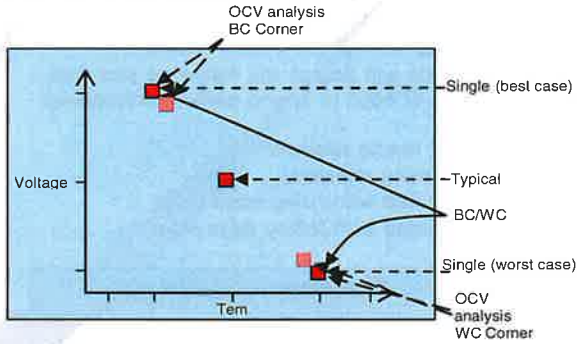
Setting constant inputs / outputs

These settings enable the optimization of unnecessary logic. Do not set if you do not want this to occur!

`set_logic_one in1`	Specify a constant logic 1 on an input
`set_logic_zero in1`	Specify a constant logic 0 on an input
`set_logic_dc in1`	Specify a don't care on an input
`set_equal in1 in2`	Specify two inputs as being the same
`set_opposite in1 in2`	Specify two inputs as being opposites
`set_unconnected out1`	Specify an output port as unused

Timing setup

Operating Conditions



Single (Best case OR worst case) analysis

```
set_operating_conditions WC_corner
```

Best Case Worst Case (bc_wc) analysis

```
set_operating_conditions -analysis_type bc_wc \
  -min_library BC_lib -min BC_corner \
  -max library WC_lib -max WC_corner
```

On-Chip Variation (OCV) analysis

With OCV analysis two analyses runs are required:

One Analysis at the best case corner:

```
set_operating_conditions -analysis_type \
   on_chip_variation \
  -min_library BC_lib -min BC_corner \
  -max library BC_lib -max Worst_BC_corner
```

One at the worst case corner:

```
set_operating_conditions -analysis_type \
   on_chip_variation \
  -min_library WC_lib -min Best_WC_corner \
  -max library WC_lib -max WC_corner
```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