Digital Electronics

- Part I: Digital Principle -

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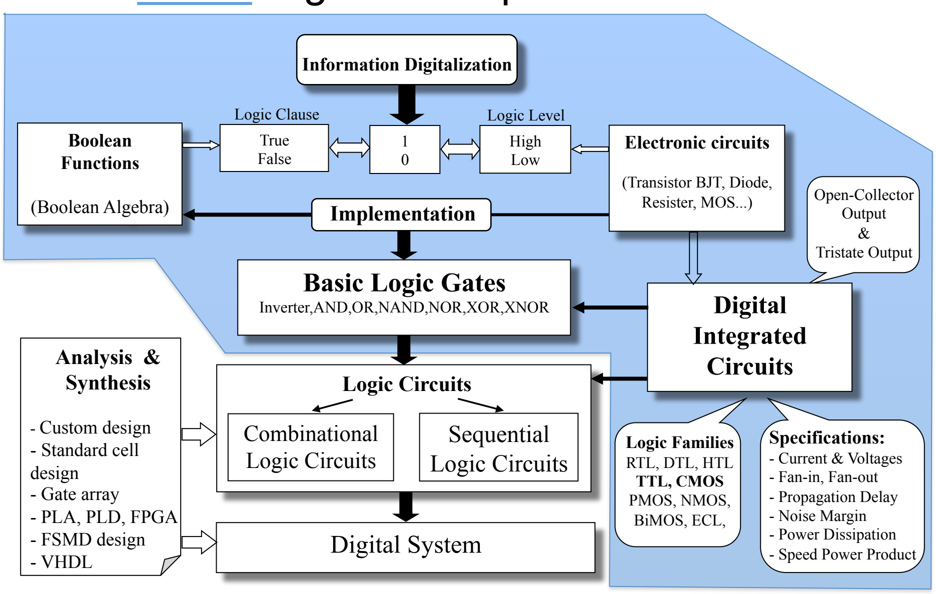
Part I: Digital Principles - Overview



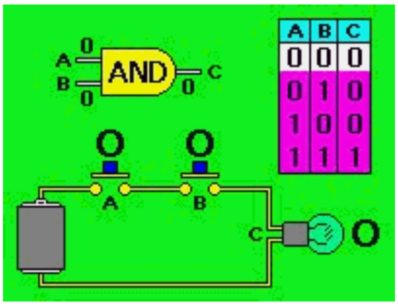
Part I: Digital Principles - Contents

Chapter 3

Logic Gates, Logic Circuits and Digital Integrated Circuits

3.1 LOGIC GATES

✓ Digital circuits work with 0 and 1 and use "switches"

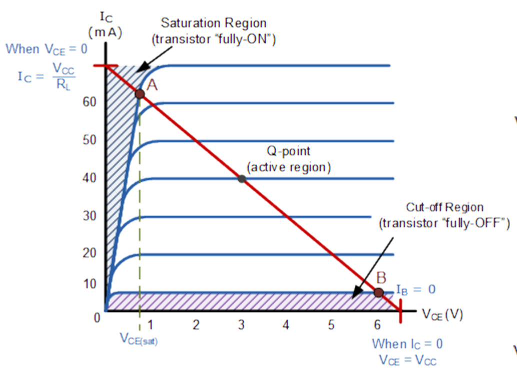


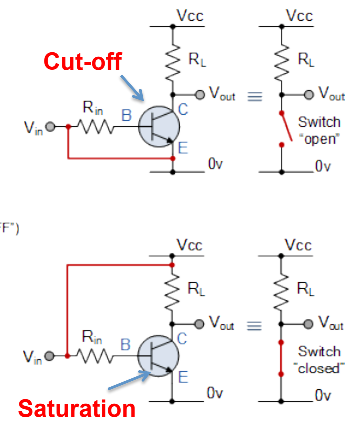
Ref.: http://www.wordbench.com/video/ucan.html

How to make an electronic "**switch**" in digital circuit ?.

3.1 LOGIC GATES

✓ BJT works as a switch in a digital circuits



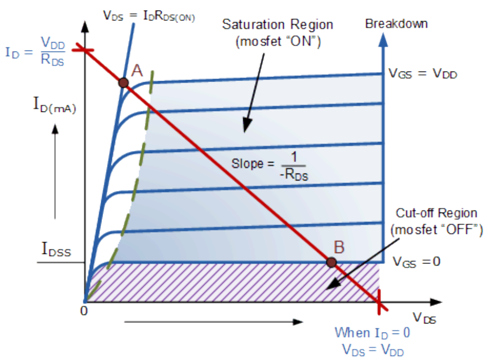


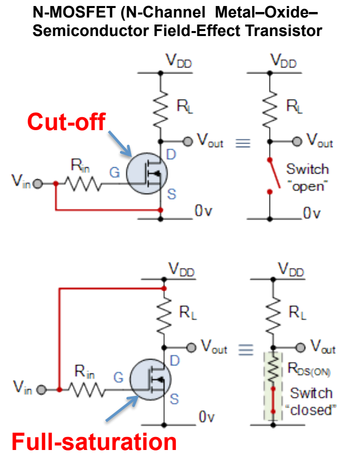
BJT switches → TTL families

Ref.: http://www.electronics-tutorials.ws/transistor/tran_4.html

3.1 LOGIC GATES

✓ MOSFET works as a switch in a digital circuits



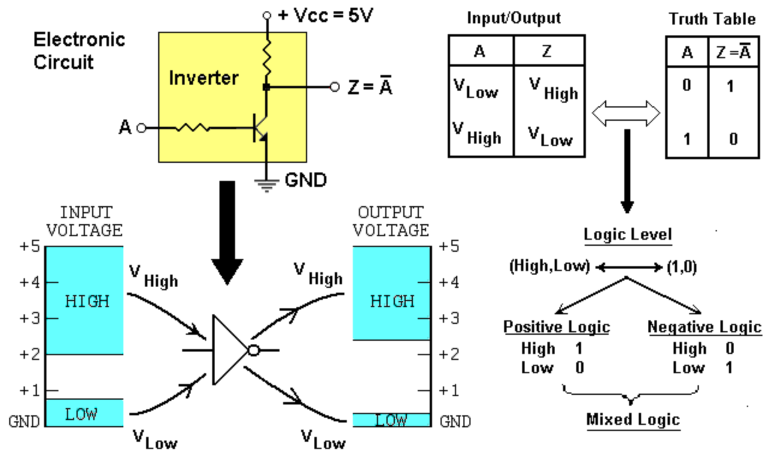


MOSFET switches → CMOS Families

Ref.: http://www.electronics-tutorials.ws/transistor/tran_4.html

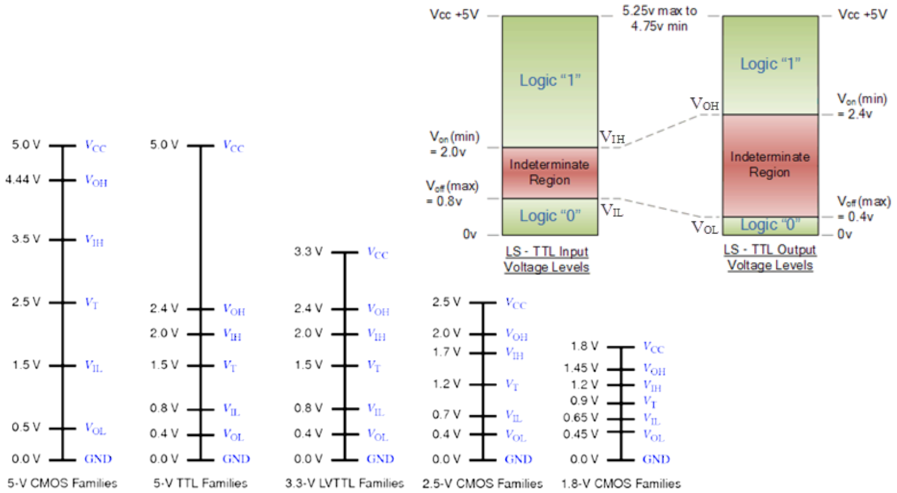
3.1 LOGIC GATES

✓ Logic Levels: are usually represented by the voltage ranges.



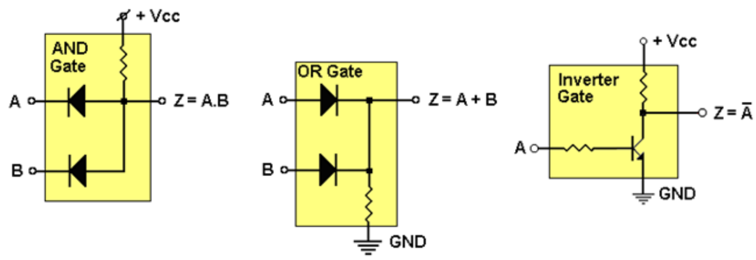
3.1 LOGIC GATES

✓ Logic Levels: V_{CC}, V_{IH}, V_{IL}, V_{OH}, V_{OL}

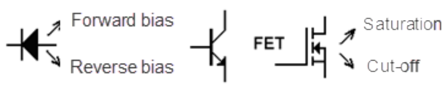


3.1 LOGIC GATES

✓ A Logic Gate is physical device implementing a basic Boolean function and working on logic levels.



Logic gates are primarily implemented using diodes or transistors acting as electronic switches



3.1 LOGIC GATES

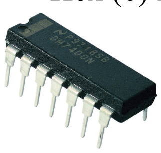
✓ 7 Logic Gates

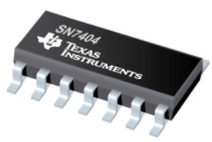
LOGIC GATE	TRADITIONAL LOGIC SYMBOL	IEEE/ANSI LOGIC SYMBOL	FUNCTION	TRUTH TABLE		
				INPUT		OUTPUT
				B	A	Z
INVERTER (NOT)	A — Z	A — 1 — Z	Z = $\overline{A}$		0	1
					1	0
AND	A, B — Z	A, B — & — Z	Z = A.B	0	0	0
				0	1	0
				1	0	0
				1	1	1
OR	A, B — Z	A, B — ≥ 1 — Z	Z = A + B	0	0	0
				0	1	1
				1	0	1
				1	1	1
NAND	A, B — Z	A, B — & — Z	Z = $\overline{A.B}$	0	0	1
				0	1	1
				1	0	1
				1	1	0
NOR	A, B — Z	A, B — ≥ 1 — Z	Z = $\overline{A+B}$	0	0	1
				0	1	0
				1	0	0
				1	1	0
XOR	A, B — Z	A, B — = 1 — Z	Z = A ⊕ B	0	0	0
				0	1	1
				1	0	1
				1	1	0
XNOR	A, B — Z	A, B — = 1 — Z	Z = A ~ B = $\overline{A \oplus B}$	0	0	1
				0	1	0
				1	0	0
				1	1	1

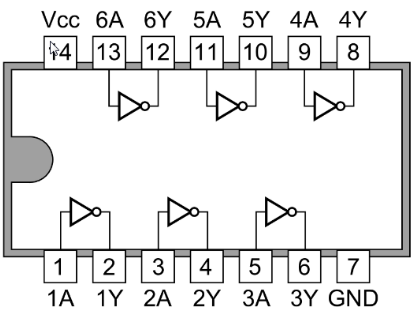
3.1 LOGIC GATES

✓ Logic Gates in Small Scale Integrated IC

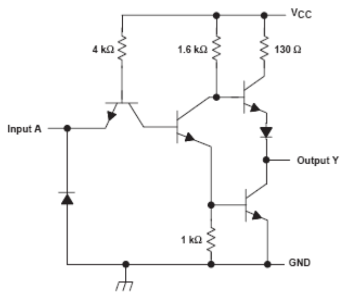
Hex (6) Inverters IC 7404







INVETER gate

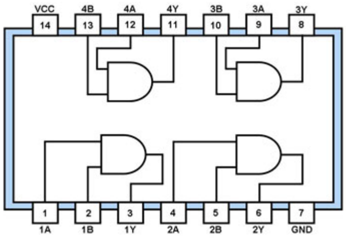


TTL inverter gate circuit

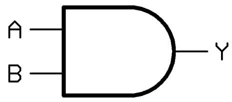
3.1 LOGIC GATES

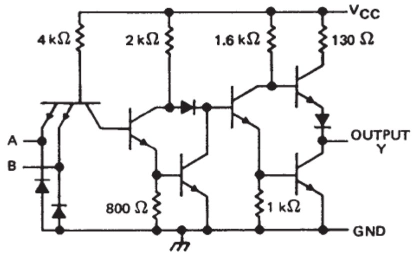
✓ Logic Gates in Small Scale Integrated IC

Quadruple 2-Input And-gates IC 7408



AND gate



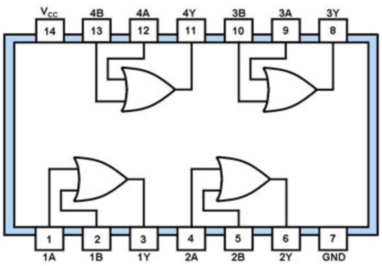


TTL AND gate circuit

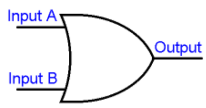
3.1 LOGIC GATES

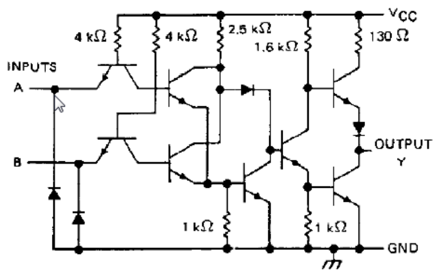
✓ Logic Gates in Small Scale Integrated IC

Quadruple 2-Input OR-gates IC 7432



OR gate



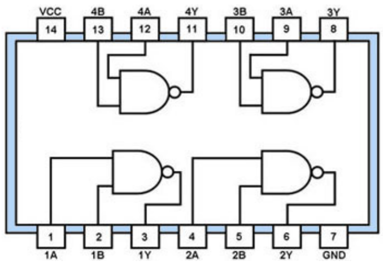


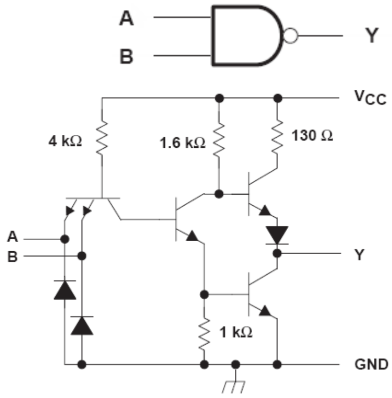
TTL OR gate circuit

3.1 LOGIC GATES

✓ Logic Gates in Small Scale Integrated IC

Quadruple 2-Input NAND-gates IC 7400 NAND gate



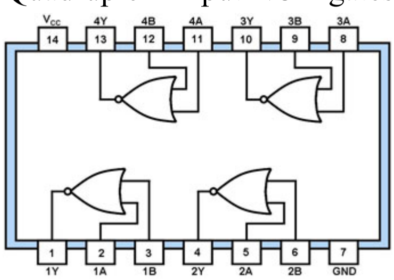


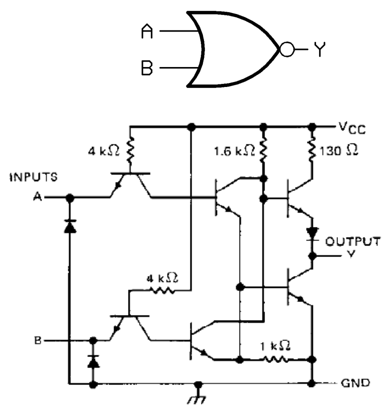
TTL NAND gate circuit

3.1 LOGIC GATES

✓ Logic Gates in Small Scale Integrated IC

Quadruple 2-Input NOR-gates IC 7402 NOR gate



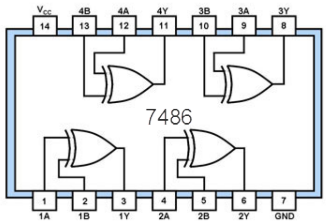


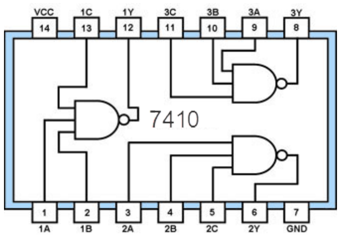
TTL NOR gate circuit

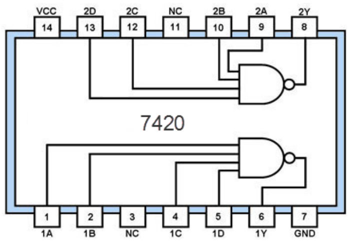
3.1 LOGIC GATES

✓ Logic Gates in Small Scale Integrated IC

Quad 2-Input Exclusive-Or Gates: 7486, 74136

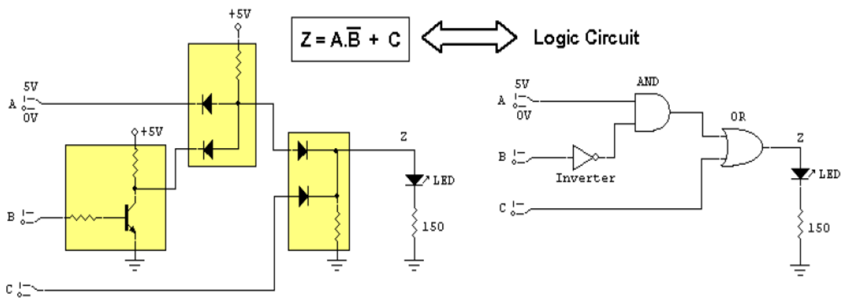






3.2 LOGIC CIRCUITS

✓ Principles of Logic Gate Connection

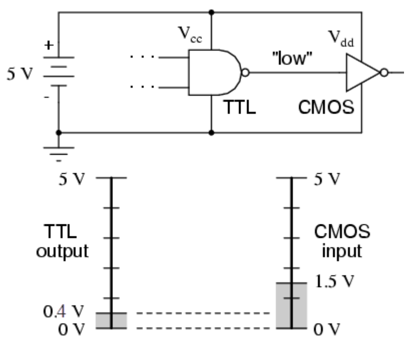


The rules of connection ?.

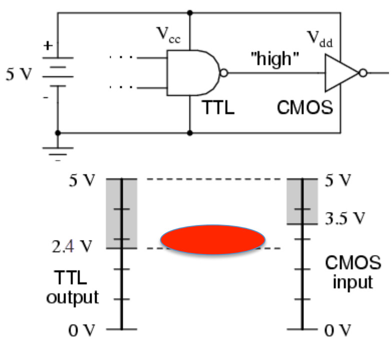
3.2 LOGIC CIRCUITS

✓ Principles of Logic Gate Connection

e.g. TTL output connects to CMOS input



TTL output falls within acceptable limits for CMOS input



TTL output falls outside of acceptable limits for CMOS input

3.2 LOGIC CIRCUITS

✓ Principles of Logic Gate Connection → **the rules**

+ Must be compatible in logic level

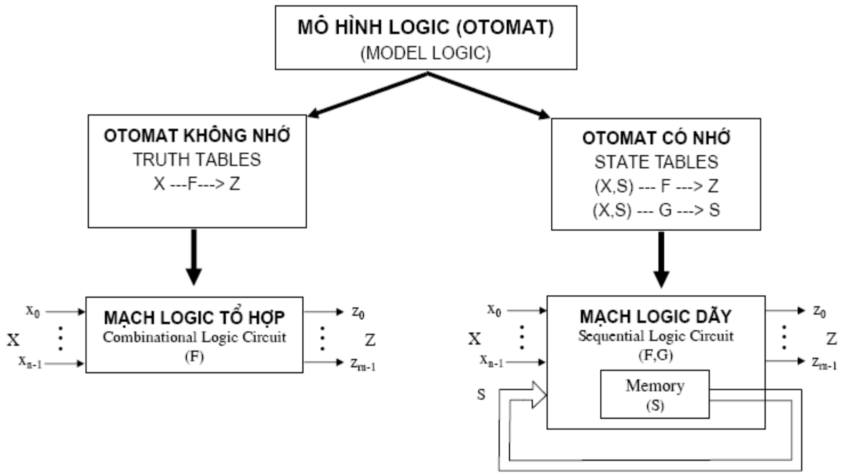
+ One output can control more than one input

+ Two or more outputs usually should not be connected together.

+ Don't let an input as a floating input.

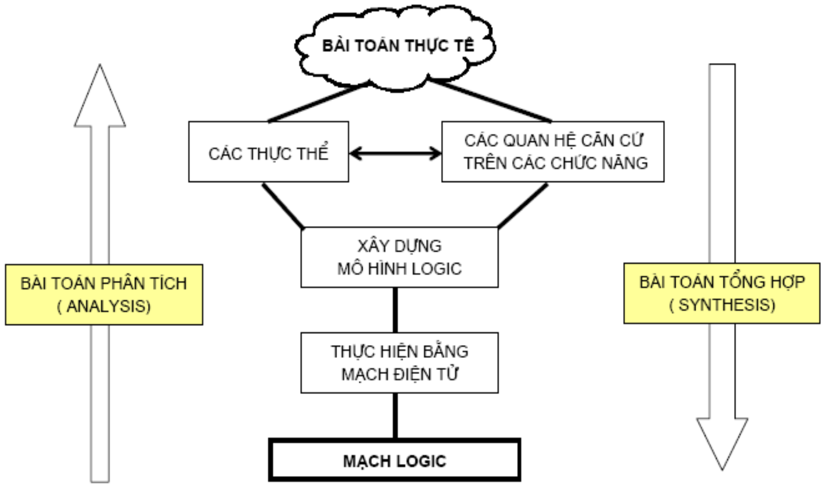
3.2 LOGIC CIRCUITS

✓ Two models of Logic Circuits



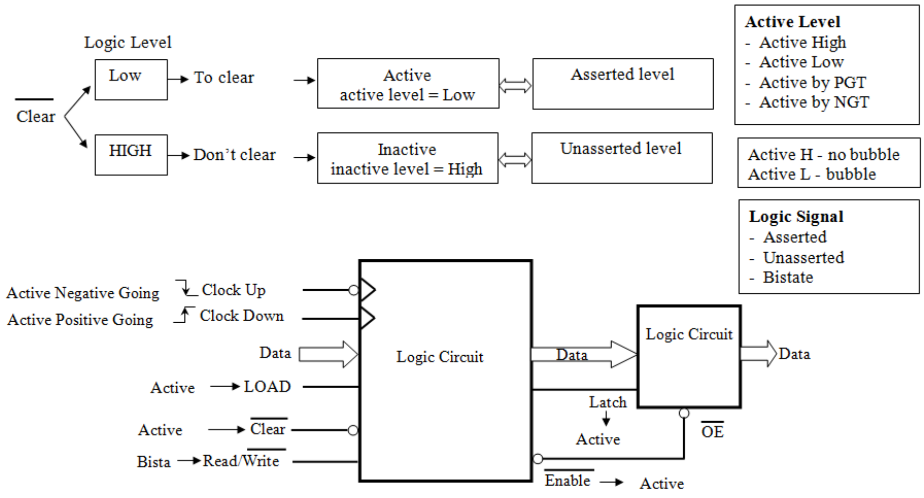
3.2 LOGIC CIRCUITS

✓ Synthesis and Analysis Logic Circuits



3.2 LOGIC CIRCUITS

✓ Active Level (Asserted level)



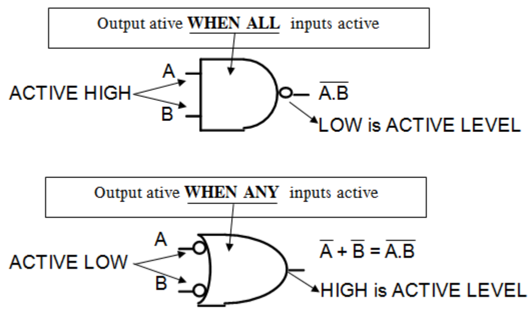
3.2 LOGIC CIRCUITS

✓ Active Level Conversion

DE MORGAN

$\overline{A.B} = \overline{A} + \overline{B}$

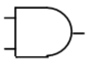
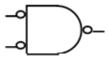
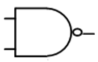
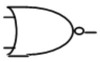
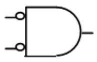
$\overline{A+B} = \overline{A}.\overline{B}$



ALTERNATED LOGIC GATES or
DE MORGAN LOGIC GATES

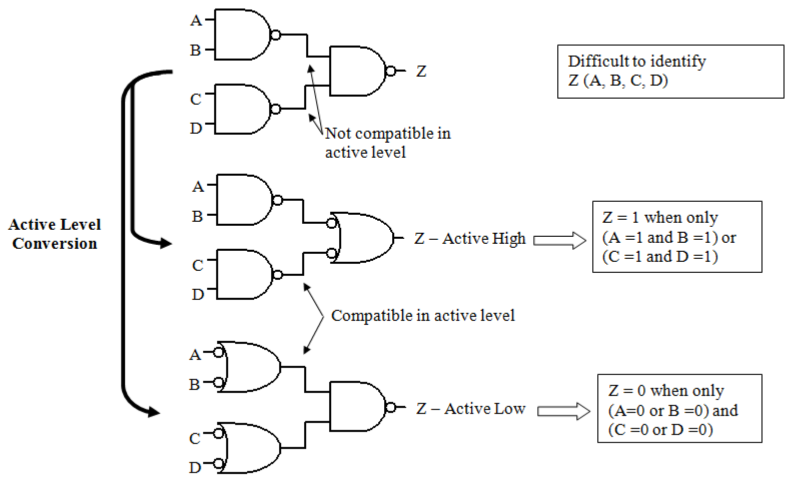
3.2 LOGIC CIRCUITS

✓ Alternated Logic Gates (active level conversion)

GATE	STANDARD LOGIC GATES	ALTERNATED LOGIC GATES
INV		
AND		
OR		
NAND		
NOR		

3.2 LOGIC CIRCUITS

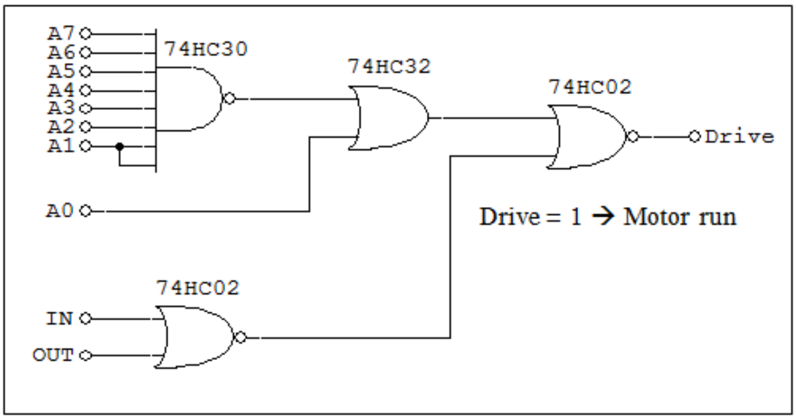
✓ Active level conversion to make a compatible in logic circuits



3.2 LOGIC CIRCUITS

- ✓ Exercise 1: active level conversion

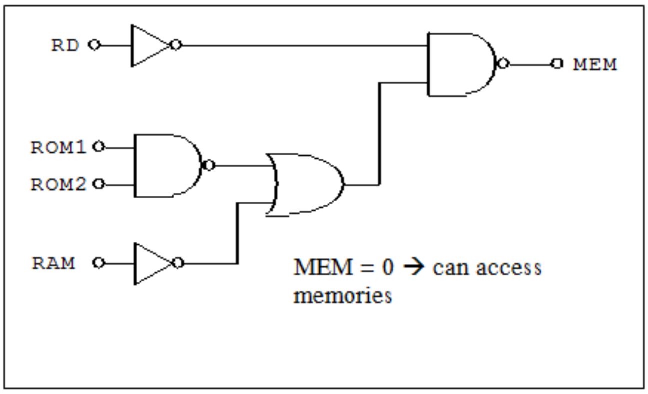
Floppy Driver Controller



3.2 LOGIC CIRCUITS

- ✓ Exercise 2: active level conversion

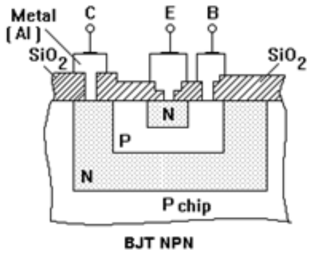
Memory Access Controller

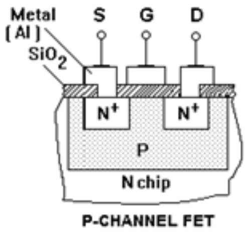


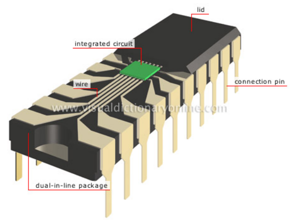
3.3 DIGITAL INTEGRATED CITCUITS

✓ Integrated Circuit ?.

An integrated circuit (also referred to as IC, chip, or microchip) is an electronic circuit manufactured by lithography



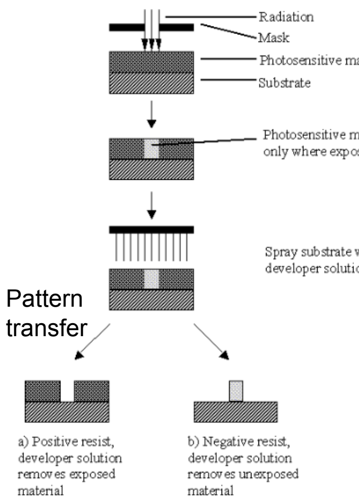


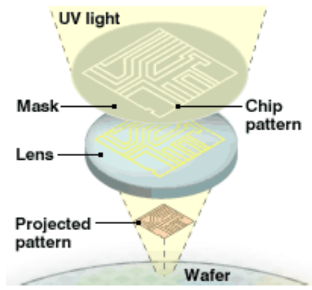


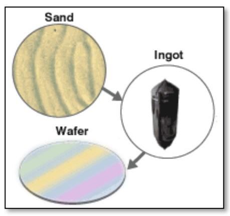
All logic gates, logic circuits → implemented on a single chip → Digital ICs

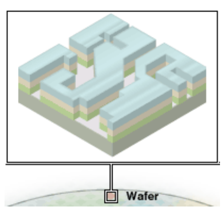
3.3 DIGITAL INTEGRATED CITCUITS

✓ Lithography for integrated circuit fabrication









3.3 DIGITAL INTEGRATED CITCUITS

✓ Scale of Integration

SCALE OF INTEGRATION	NUMBER OF GATES	APPLICATION
SSI *Small-Scale Integrated*	< 12	"Off-the-shelf" IC for basic logic gate and Flip-flop
MSI *Medium-Scale Integrated*	12 ~ 99	"Off-the-shelf" IC Decoder, Encoder, Mux, Counter, Shift registers
LSI *Large-Scale Integrated*	100 ~ 9999	A digital system, such as digital clock, calculator, memory RAM ROM, PROM, EPROM, Flash, Microcontroller, Microprocessors, System on Chip …
VLSI *Very-Large-Scale Integrated*	10.000 ~ 99.999	
ULSI *Ultra-Large-Scale Integrated*	> 100.000	

* Giga-scale integration(GSI)1,000,000 or more(10^9 - 10^{11})
* Tera-scale integration(TSI) (10^{12} or more)

1.2 Billion individual transistor gates onto the Quad-core i7-2700k "Sandy Bridge" 64-bit microprocessor chip

Moore's Law: The number of components that can be packed on a computer chip doubles every 18 months while price stays the same.

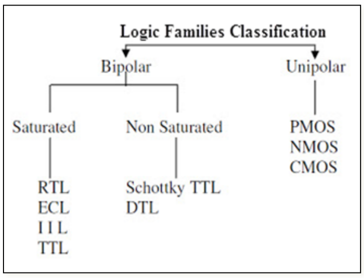
3.3 DIGITAL INTEGRATED CITCUITS

✓ Most of the reasons that modern digital systems use integrated circuits

- ❖IC pack a lot more circuitry in a small package → the overall size of any digital system is reduced.
- ❖IC have made digital systems more reliable by reducing the number of external interconnections.
- ❖IC typically requires less power than their discrete counterparts→ saving in power and a system does not require as much cooling

3.3 DIGITAL INTEGRATED CITCUITS

✓ Logic Families



DL : **Diode Logic.**

RTL : **Resistor Transistor Logic.**

DTL : **Diode Transistor Logic.**

HTL : **High Threshold Logic.**

TTL : **Transistor Transistor Logic.**

I2L : **Integrated Injection Logic.**

ECL : **Emitter Coupled Logic.**

MOS : **Metal Oxide Semiconductor Logic (PMOS and NMOS).**

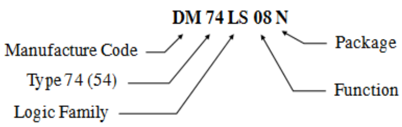
CMOS : **Complementary Metal Oxide Semiconductor Logic.**

BiCMOS : Combines bipolar and CMOS devices into single integrated circuit.

3.3 DIGITAL INTEGRATED CITCUITS

✓ Digital IC notation

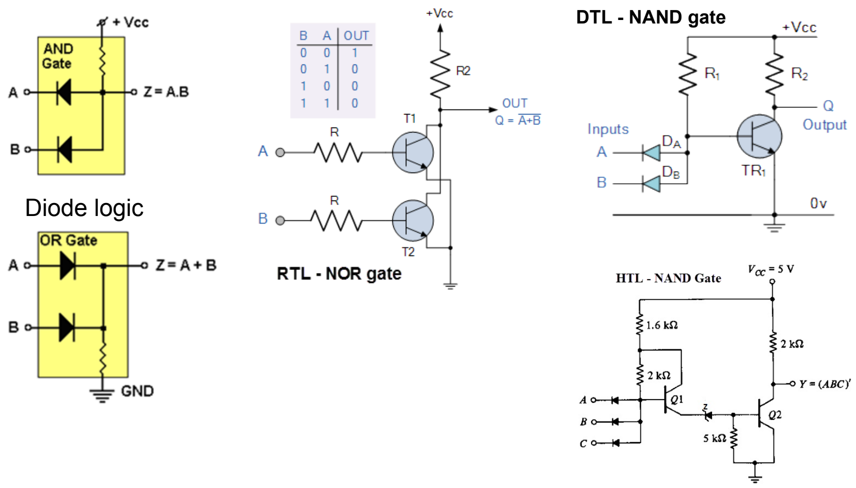
FAIRCHILD SEMICONDUCTOR®



TTL	Hä CMOS
None = Standard TTL **ALS** = Advanced Low-power Schottky TTL logic. **AS** = Advanced Schottky TTL logic. **F** = FACT Fairchild Advanced Schottky TTL logic. **H** = High-speed TTL logic. **L** = Low-power TTL logic. **LS** = Low-power Schottky TTL logic. **S** = Schottky TTL logic.	**C** = compatible with 74 TTL. **HC** = High-speed CMOS with Vcc = from +2V to 6V. **FACT**- Fairchild Advanced CMOS Technology ***Includes:*** **74AC,74ACQ,74ACT,74ACTQ, 74FCT, 74FCTA, 74HCT**

3.3 DIGITAL INTEGRATED CITCUITS

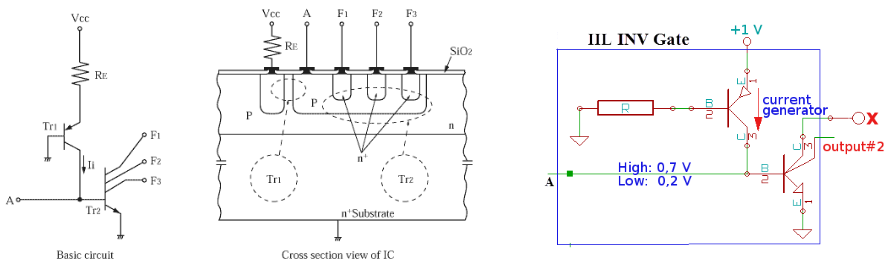
✓ DL, RTL, DTL, HTL structures



3.3 DIGITAL INTEGRATED CITCUITS

✓ IIL structures

- Integrated injection logic (IIL, I2L, or I2L) is a class of digital circuits built with multiple collector bipolar junction transistors (BJT)
- When introduced it had speed comparable to TTL yet was almost as low power as CMOS, making it ideal for use in VLSI (and larger) integrated circuits.
- Although the logic voltage levels are very close (High: 0.7V, Low: 0.2V),

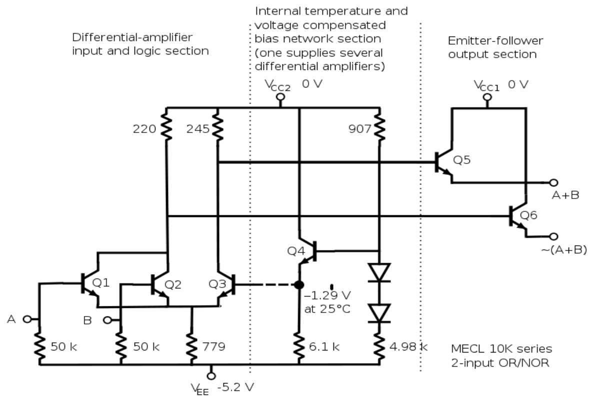


Integrated injection logic

3.3 DIGITAL INTEGRATED CITCUITS

✓ ECL structures

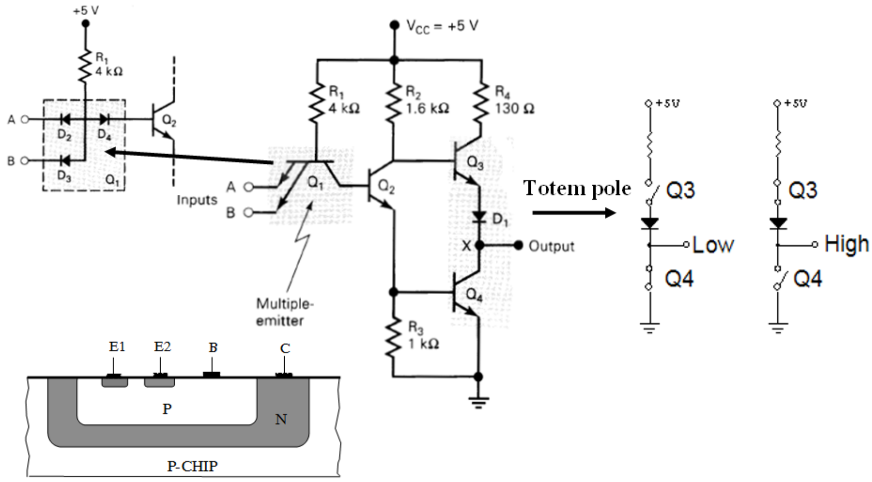
- A high-speed integrated circuit bipolar transistor logic family.
- ECL uses an overdriven BJT differential amplifier with single-ended input and limited emitter current to avoid the saturated (fully on) region of operation and its slow turn-off behavior



3.3 DIGITAL INTEGRATED CITCUITS

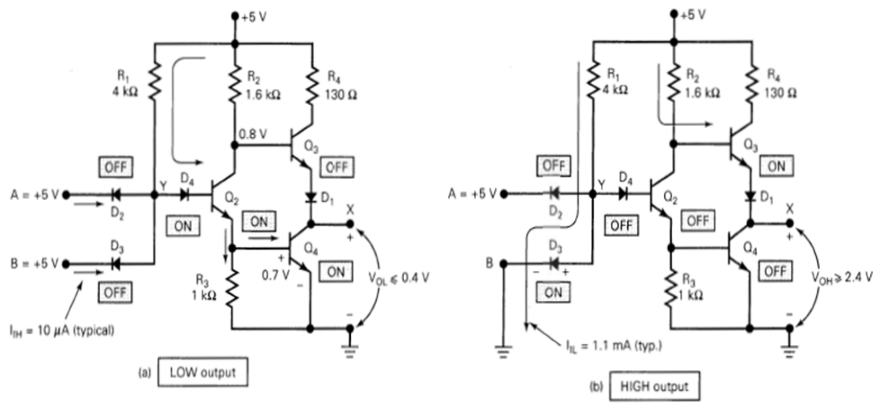
✓ The structure of standard TTL NAND Gate:

Multiple emitter and Totem pole



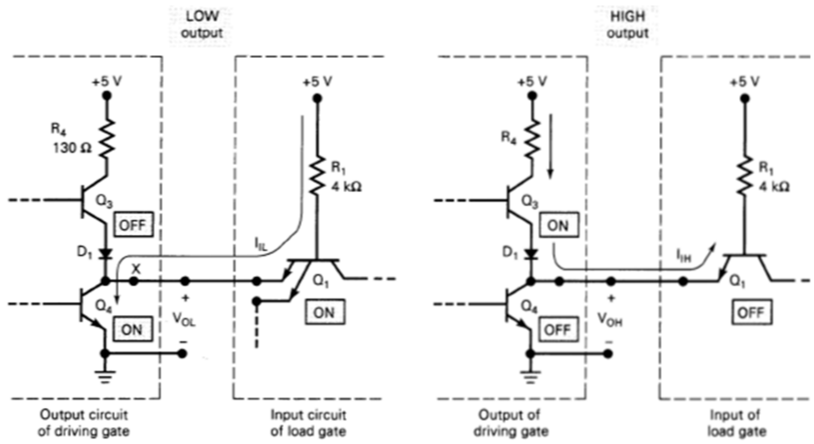
3.3 DIGITAL INTEGRATED CITCUITS

✓ The operation of standard TTL NAND gate



3.3 DIGITAL INTEGRATED CITCUITS

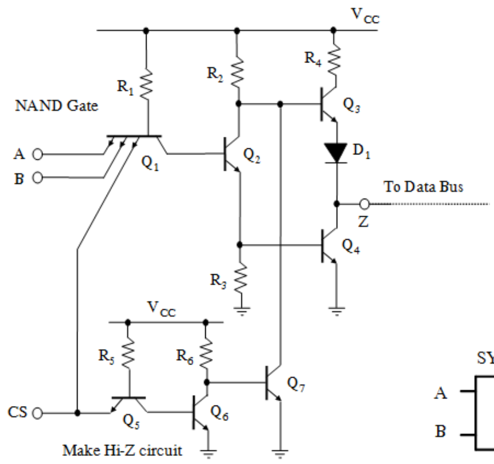
✓ The operation of standard TTL NAND gate

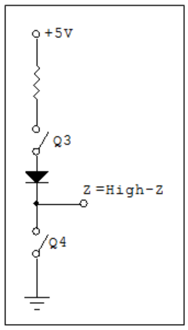


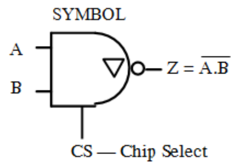
Current-sinking → I_{IL} **Current-providing → I_{IH}**

3.3 DIGITAL INTEGRATED CITCUITS

✓ Tri-state or Hi-Z output of TTL gate

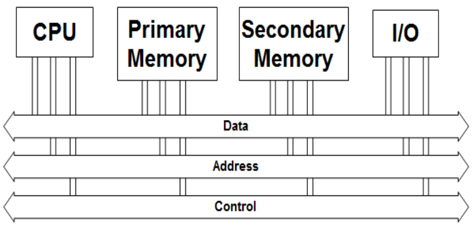


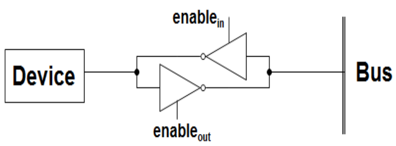


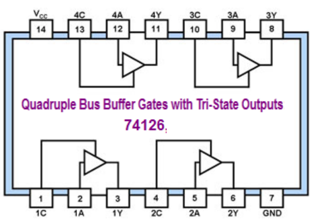


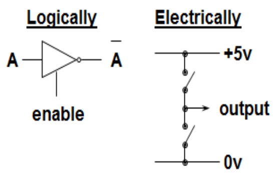
3.3 DIGITAL INTEGRATED CITCUITS

✓ Tri-states output application







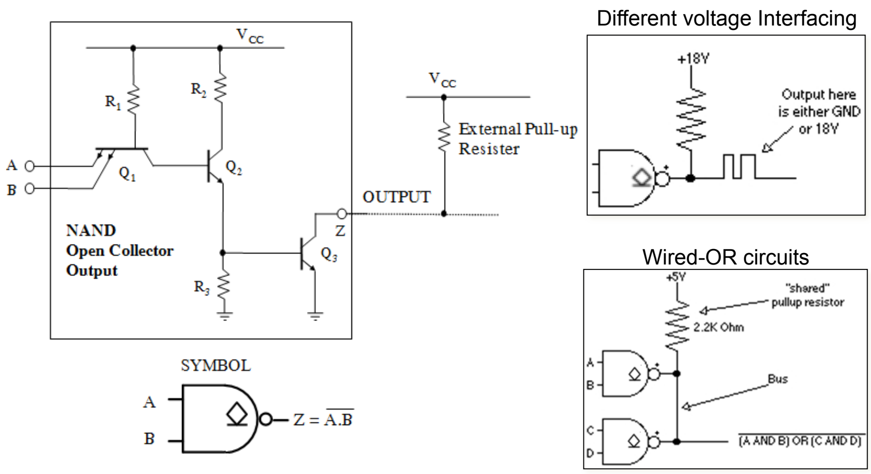


Truth Table

enable	A	Output
0	0	(Z)
0	1	(Z)
1	0	1
1	1	0

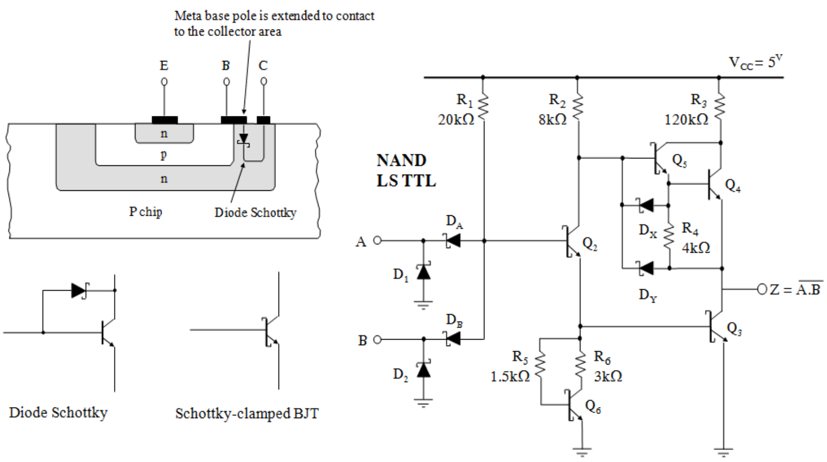
3.3 DIGITAL INTEGRATED CITCUITS

✓ Open collector output of TTL gate



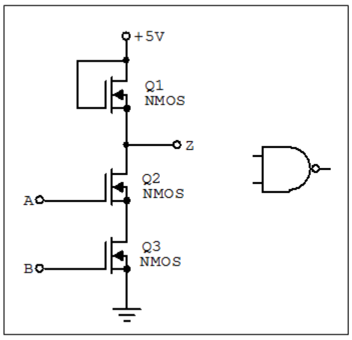
3.3 DIGITAL INTEGRATED CITCUITS

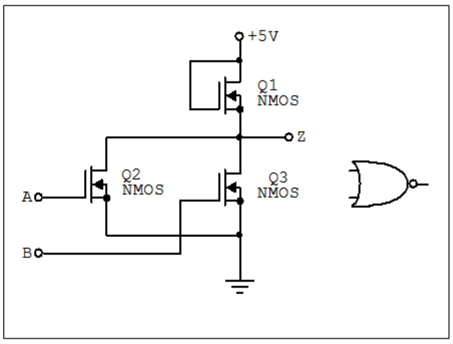
✓ Structure of Low-power Schottky TTL



3.3 DIGITAL INTEGRATED CITCUITS

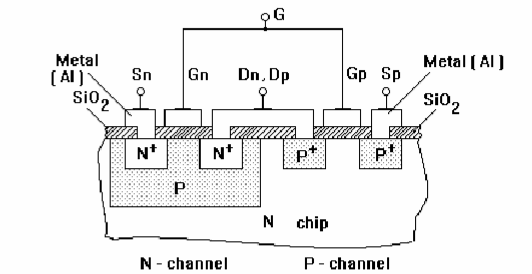
✓ Structure of NMOS gate



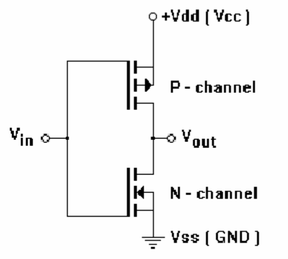


3.3 DIGITAL INTEGRATED CITCUITS

✓ Structure of CMOS gate



Complememtary symmetry Metal Oxide Semiconductor (CMOS)

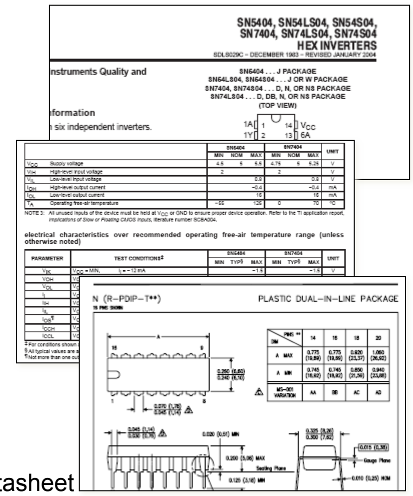


NOT (CMOS)

3.3 DIGITAL INTEGRATED CITCUITS

✓ Specifications of Digital IC

- Currents & Voltages
- Fan-out, Fan-in
- Propagation Delay
- Noise Margin
- Power Dissipation
- Speed Power Product



From Datasheet

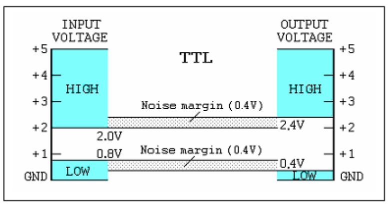
3.3 DIGITAL INTEGRATED CITCUITS

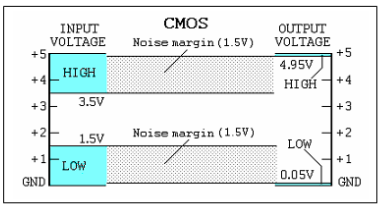
✓ Specifications of Digital IC

- Voltages and Noise Margin

- $V_{IH(min)}$ The minimum voltage level at the input to be recognised as H.
- $V_{IL(max)}$ The maximum voltage level at the input to be recognised as L.
- $V_{OH(min)}$ The minimum voltage at the output when in state H.
- $V_{OL(max)}$ The maximum voltage at the output when in state L.

Condition $\begin{cases} V_{OH(min)} \geq V_{IH(min)} \\ V_{OL(max)} \leq V_{IL(max)} \end{cases}$



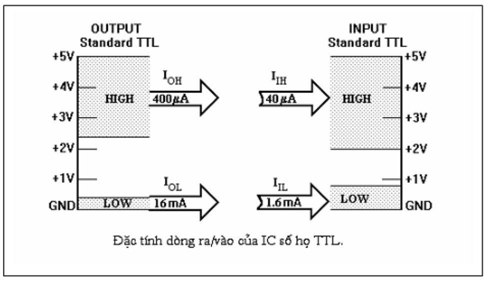


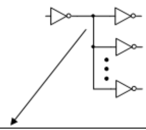
3.3 DIGITAL INTEGRATED CITCUITS

✓ Specifications of Digital IC

➢ Currents & Fan-out, Fan-in

- I_{IH} The current flowing into the input when a specified H voltage is applied.
- I_{IL} The current flowing into the input when a specified L voltage is applied.
- I_{OH} The current flowing out of the output when in state H.
- I_{OL} The current flowing out of the output when in state L.





$$\text{FANOUT} = \min\left(\frac{|I_{OH}|}{|I_{IH}|}, \frac{|I_{OL}|}{|I_{IL}|}\right).$$

e.g.: Standard TTL
FANOUT = 10

3.3 DIGITAL INTEGRATED CITCUITS

✓ Specifications of Digital IC

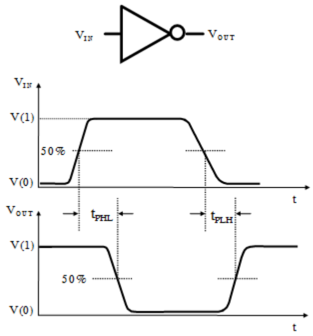
➢ Currents of the logic families

LOGIC FAMILY		OUTPUT	INPUT
TTL	Standard TTL	I_{OH} = 400 µA I_{OL} = 16 mA	I_{IH} = 40 µA I_{IL} = 1.6 mA
	Low Power Schottky (LS)	I_{OH} = 400 µA I_{OL} = 8 mA	I_{IH} = 20 µA I_{IL} = 400 µA
	Advanced Low Power Schottky (ALS)	I_{OH} = 400 µA I_{OL} = 8 mA	I_{IH} = 20 µA I_{IL} = 100 µA
	FAST Fairchild Advanced Schottky TTL (F)	I_{OH} = 1 mA I_{OL} = 20 mA	I_{IH} = 20 µA I_{IL} = 0.6 mA
CMOS	4000 Series	I_{OH} = 400 µA I_{OL} = 400 µA	I_{in} = 1 µA
	74HC00 Series	I_{OH} = 4 mA I_{OL} = 4 mA	I_{in} = 1 µA
	FAST Fairchild Advanced CMOS Technology Series (AC/ACT/ACQ/ACTQ)	I_{OH} = 24 mA I_{OL} = 24 mA	I_{in} = 1 µA
	FAST Fairchild Advanced CMOS Technology Series (FCT/FCTA)	I_{OH} = 15 mA I_{OL} = 64 mA	I_{in} = 1 µA

3.3 DIGITAL INTEGRATED CITCUITS

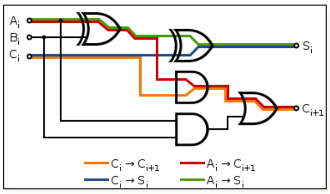
✓ Specifications of Digital IC

➢ Propagation Delay



- t_{PLH} Time taken to go from L to H.
- t_{PHL} Time taken to go from H to L.
- The average propagation delay is

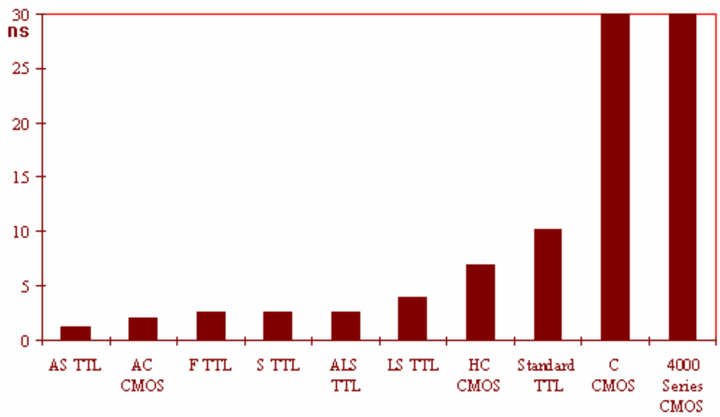
$$t_{P(ave)} = \frac{t_{PLH} + t_{PHL}}{2}.$$



3.3 DIGITAL INTEGRATED CITCUITS

✓ Specifications of Digital IC

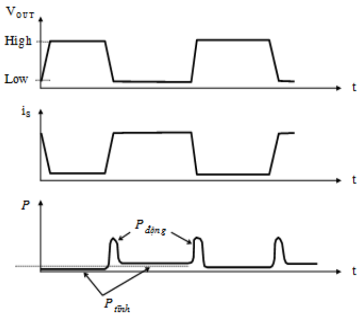
➢ Propagation delay of the TTL and CMOS families



3.3 DIGITAL INTEGRATED CITCUITS

✓ Specifications of Digital IC

➢ Power Dissipation and Speed-Power Product



I_{CCH} The current when all gate outputs in the High.

I_{CCL} The current when all gate outputs in the Low.

The average current drawn is

$$I_{CC(ave)} = \frac{I_{CCH} + I_{CCL}}{2}$$

Therefore the ***average power*** consumed is

$$P_{D(ave)} = I_{CC(ave)} \times V_{CC}$$

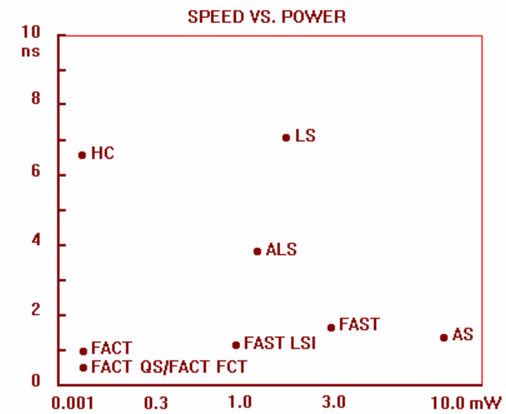
SPEED-POWER PRODUCT

DP = $t_D\, p_D$ *(watt-second) ---> picojoules (pJ)*

3.3 DIGITAL INTEGRATED CITCUITS

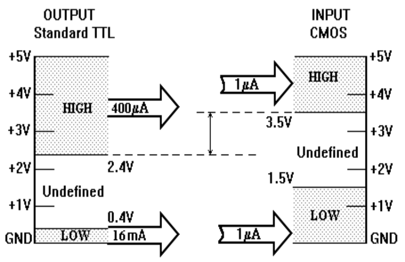
✓ Specifications of Digital IC

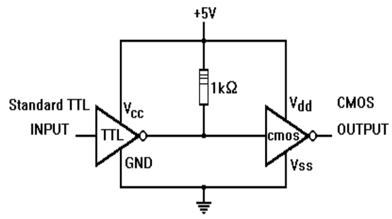
➢ Speed and power dissipation of TTL and CMOS families

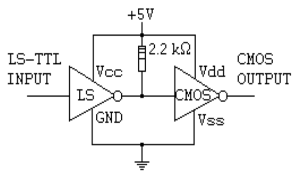


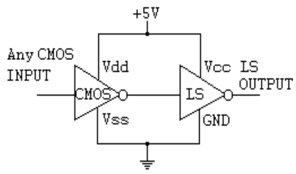
3.3 DIGITAL INTEGRATED CITCUITS

✓ TTL and CMOS connections



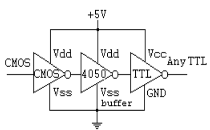


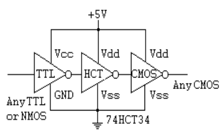


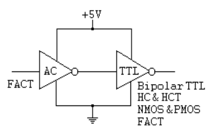


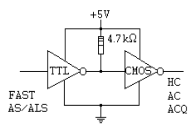
3.3 DIGITAL INTEGRATED CITCUITS

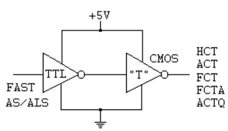
✓ TTL and CMOS connections (cont.)

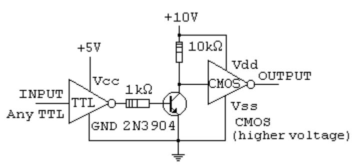


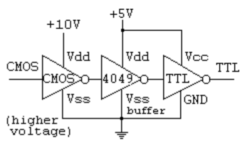


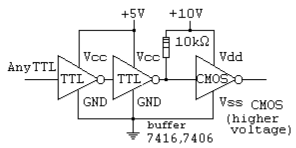






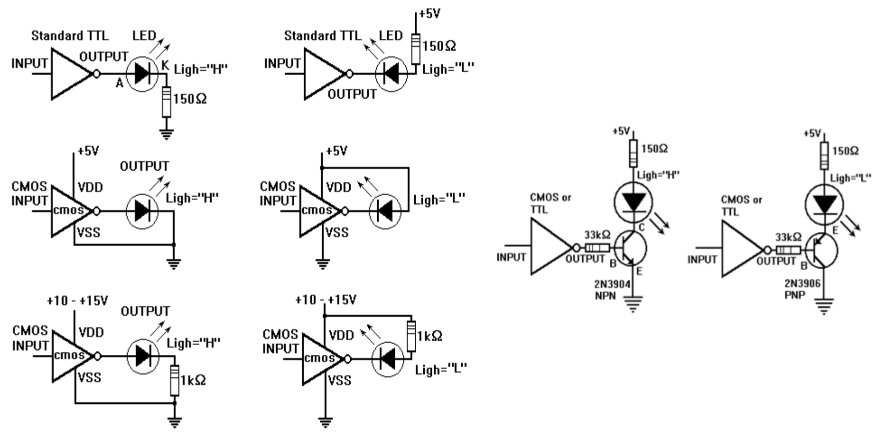






3.3 DIGITAL INTEGRATED CITCUITS

✓ TTL and CMOS connect to LED



3.3 DIGITAL INTEGRATED CITCUITS

✓ TTL and CMOS connect to a push button or a relay