

Các mạch logic tổ hợp cơ bản

(Modular Combinational Logic Circuits)

Dr. Le Dung

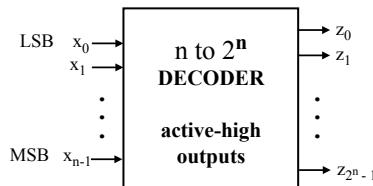
School of Electronics and Telecommunications
Hanoi University of Science and Technology

Hanoi 5/2011

NỘI DUNG

- I. Bộ giải mã (Decoder)
 - 1. Binary Decoder
 - 2. BCD to Decimal Decoder
 - 3. BCD to 7-segment Decoder
- II. Bộ lập mã (Encoder)
 - 1. Binary Encoder
 - 2. Binary Priority Encoder
 - 3. Decimal to BCD Priority Encoder
- III. Bộ dòn kênh – Bộ phân kênh (Multiplexer & Demultiplexer)
 - 1. MUX và DEMUX
 - 2. 1 of 8 MUX và 1 to 16 MUX
 - 3. Dual four-input MUX và Quad two-input MUX
 - 4. Ứng dụng của MUX
 - 5. DEMUX được thực hiện từ Decoder
- IV. Bộ cộng – Bộ trừ - Bộ so sánh – Đơn vị số học và logic
 - 1. Binary Adder
 - 2. BCD Adder
 - 3. Subtractor
 - 4. Comparator
 - 5. Arithmetic Logic Unit (ALU)

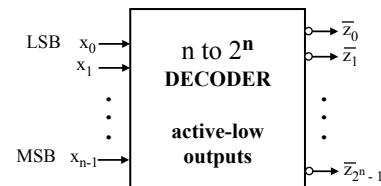
BỘ GIẢI MÃ NHỊ PHÂN - BINARY DECODER



Chi có 1 đầu ra ở mức **HIGH** khi đặt 1 mã nhị phân tại đầu vào

Mô hình toán học

$$\begin{aligned}z_0 &= \overline{x_{n-1}} \dots \overline{x_1} \cdot \overline{x_0} = \text{Minterm}_0 \\z_1 &= \overline{x_{n-1}} \dots \overline{x_1} \cdot x_0 = \text{Minterm}_1 \\z_{2^n-1} &= x_{n-1} \dots x_1 \cdot x_0 = \text{Minterm}_{2^n-1}\end{aligned}$$

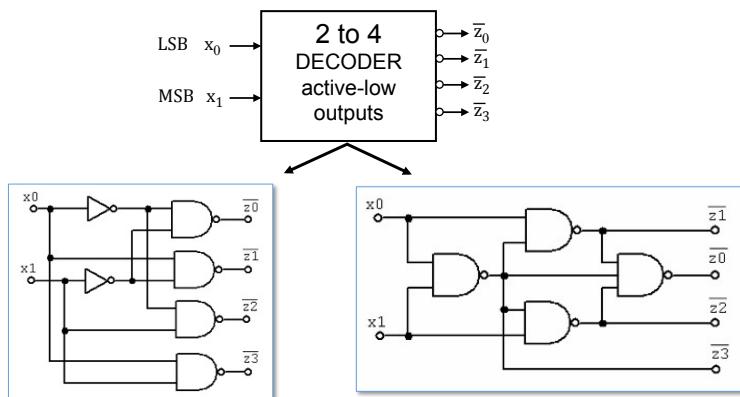


Chi có 1 đầu ra ở mức **LOW** khi đặt 1 mã nhị phân tại đầu vào

Mô hình toán học

$$\begin{aligned}\overline{z}_0 &= \overline{x_{n-1}} \dots \overline{x_1} \cdot \overline{x_0} = \overline{\text{Minterm}}_0 \\z_1 &= \overline{x_{n-1}} \dots \overline{x_1} \cdot x_0 = \overline{\text{Minterm}}_1 \\\overline{z}_{2^n-1} &= x_{n-1} \dots x_1 \cdot x_0 = \overline{\text{Minterm}}_{2^n-1}\end{aligned}$$

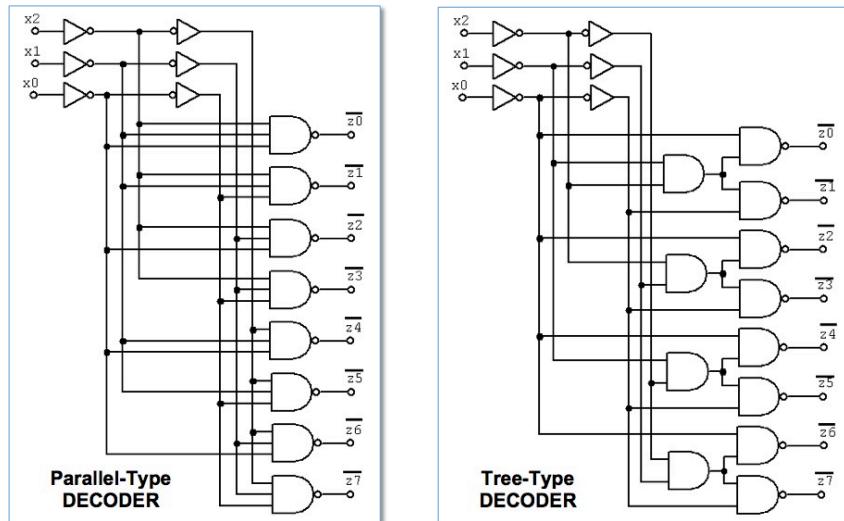
TỔNG HỢP BỘ GIẢI MÃ NHỊ PHÂN 2 TO 4



Vì sao lại hay thực hiện bộ giải mã với đầu ra tích cực ở mức thấp ?

- Fanout
- Power dissipation
- NAND gates

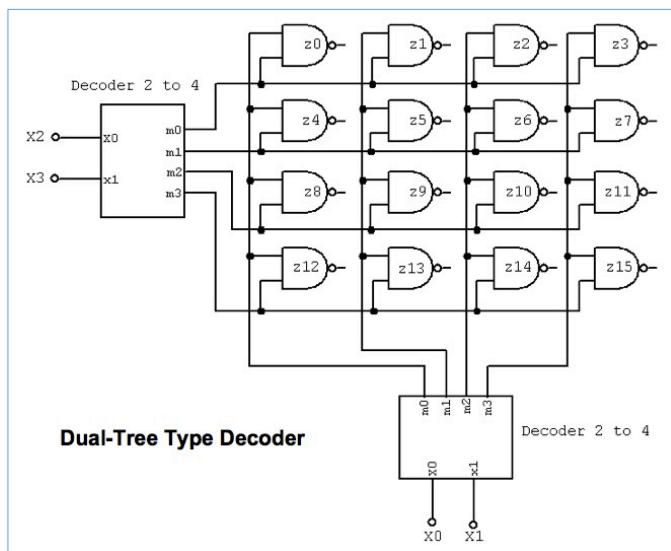
TỔNG HỢP BỘ GIẢI MÃ NHỊ PHÂN 3 TO 8



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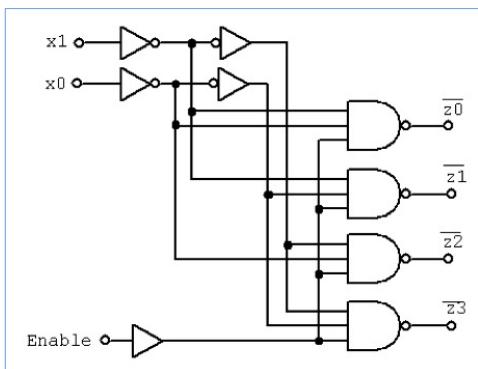
TỔNG HỢP BỘ GIẢI MÃ NHỊ PHÂN 4 TO 16



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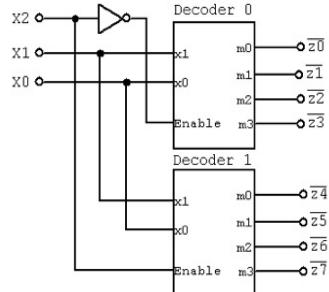
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BỘ GIẢI MÃ VỚI ĐẦU VÀO ENABLE



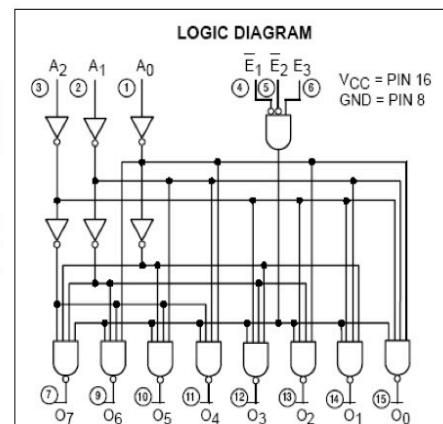
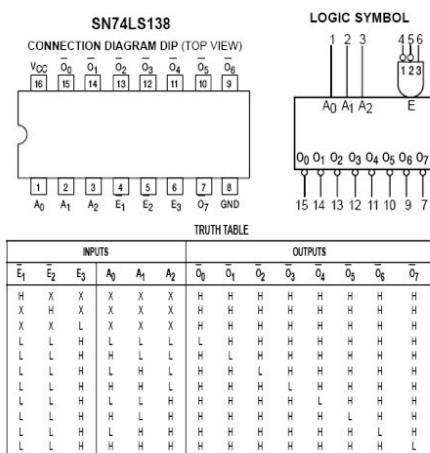
Ý nghĩa của đầu vào Enable ?

X2 = 0 → Decoder₀ active, Decoder₁ inactive
 X2 = 1 → Decoder₀ inactive, Decoder₁ active

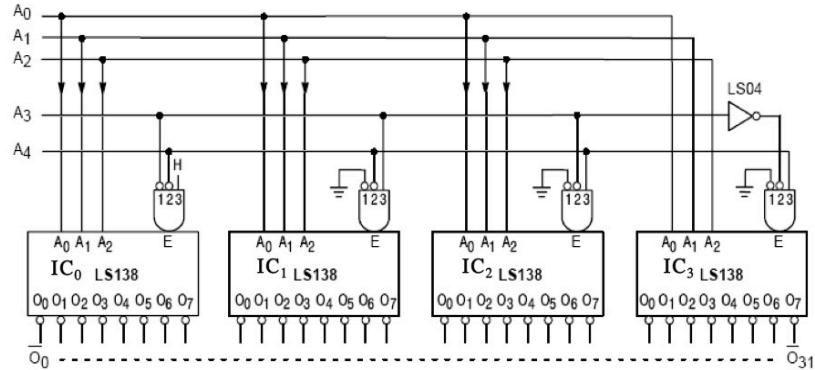


Enable = High → such as normal 2 to 4 Decoder
 Enable = Low → all outputs = High (inactive)

IC 3 TO 8 Decoder – 74LS138



TỔNG HỢP BỘ GIẢI MÃ NHỊ PHÂN 5 TO 32 TỪ IC 74LS138



Tín hiệu A₄ và A₃ dùng để chọn IC hoạt động (only one 74LS138 active)

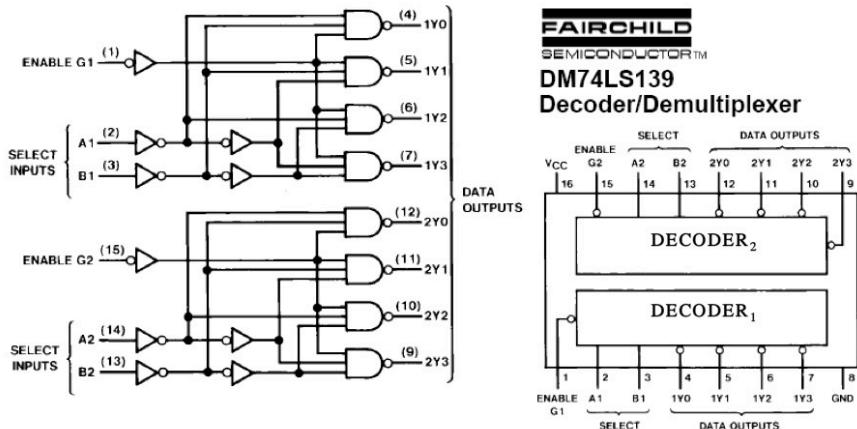
A₄A₃ = 00 ---> IC₀ active

A₄A₃ = 01 ---> IC₁ active

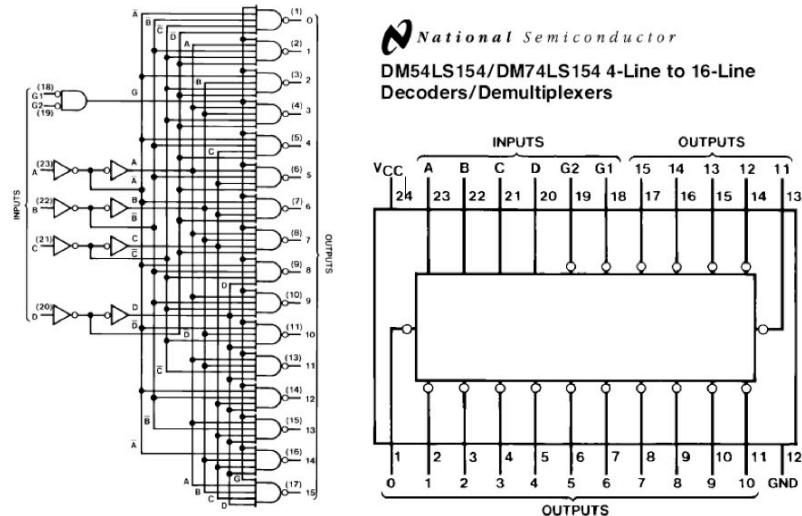
A₄A₃ = 10 ---> IC₂ active

A₄A₃ = 11 ---> IC₃ active

IC 74LS139



IC 74LS154

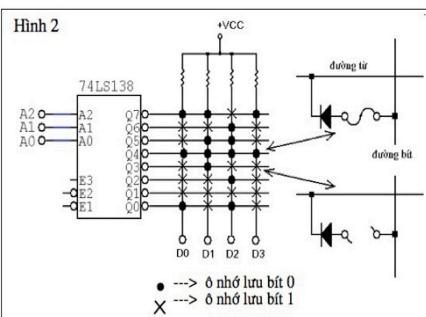
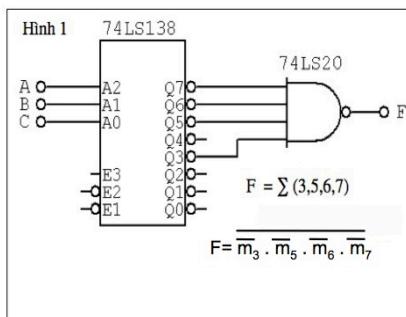


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ỨNG DỤNG CỦA BỘ GIẢI MÃ

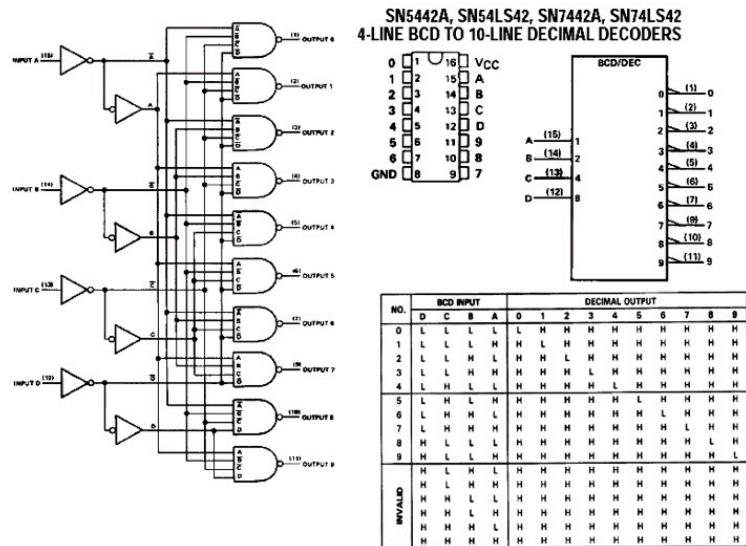
1. Tổng hợp mạch logic tổ hợp (**Hình 1**)
2. Giải mã địa chỉ ô nhớ trong các bộ nhớ RAM, ROM (**Hình 2**)
3. Giải mã lệnh trong các bộ vi xử lý
4. Thực hiện các mạch DEMUX (Phần sau)



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BCD to DECIMAL DECODER – IC 74LS42

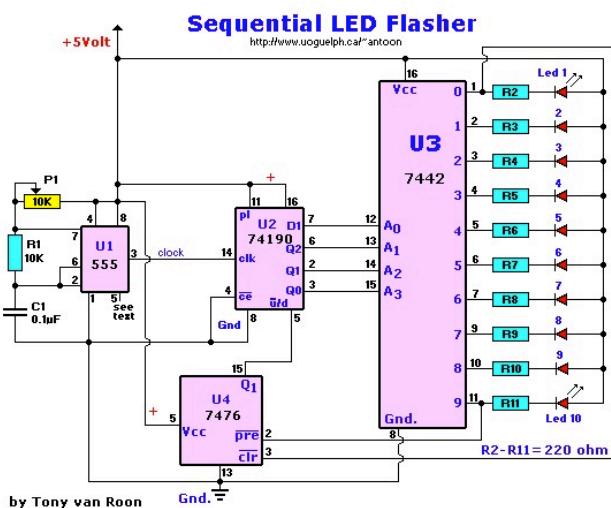


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MỘT ỨNG DỤNG VỚI IC 74LS42

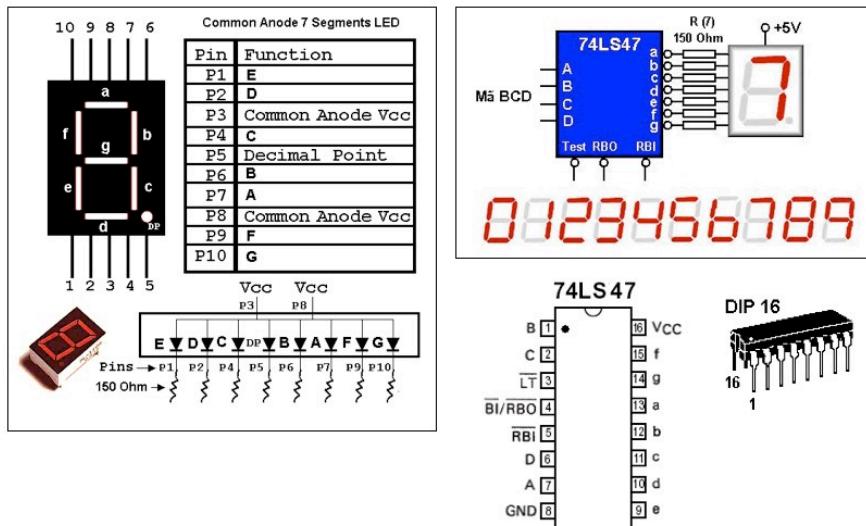
(http://www.matni.com/Arabic/Elec-Info/LED SEQ/bfflash2.htm)



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BCD to 7-segment DECODER – IC 74LS47

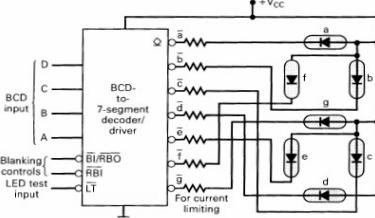


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BẢNG CHỨC NĂNG CỦA IC 74LS47

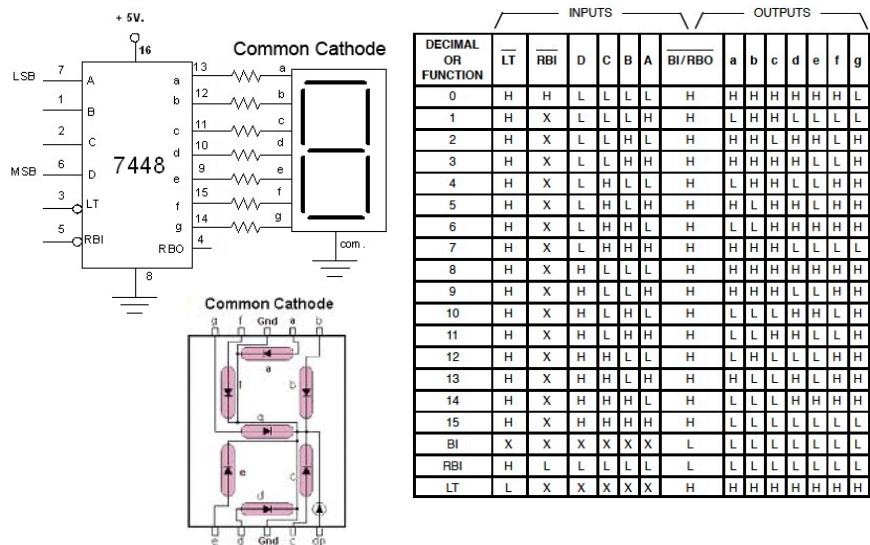
DECIMAL OR FUNCTION	INPUTS				B/RBO ¹	OUTPUTS								
	L _T	RBI	D	C	B	A	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	ON	ON	OFF	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	OFF	OFF	ON	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON						
6	H	X	L	H	H	L	H	OFF	ON	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON						
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	ON	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	ON	ON	OFF	ON	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	OFF	ON	ON	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	ON	ON	ON
13	H	X	H	H	L	H	H	OFF	OFF	ON	OFF	ON	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF						
BI	X	X	X	X	X	X	L	OFF						
RBI	H	L	L	L	L	L	ON	ON	ON	ON	ON	ON	ON	ON
LT	L	X	X	X	X	X	+							



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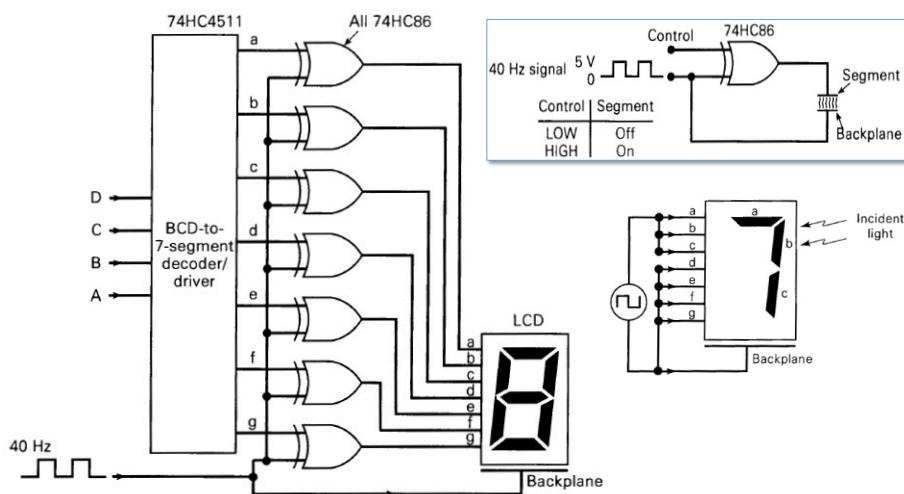
IC 74LS48 dùng cho 7-segment LED CC



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IC 74HC4511 dùng cho 7-segment LCD

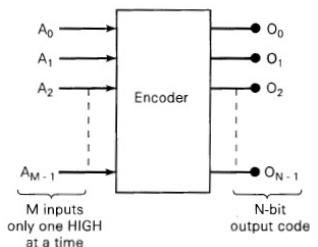


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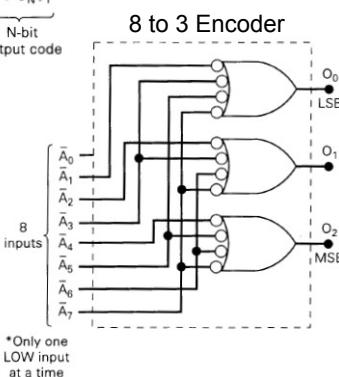
BỘ LẬP MÃ - ENCODER

Bộ lập mã
nhi phân
tổng quát



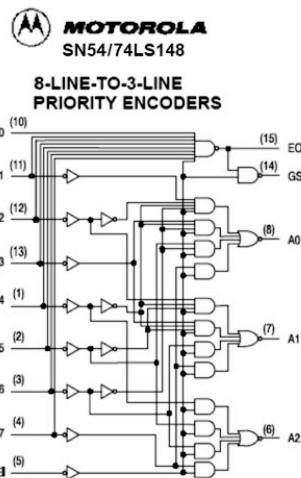
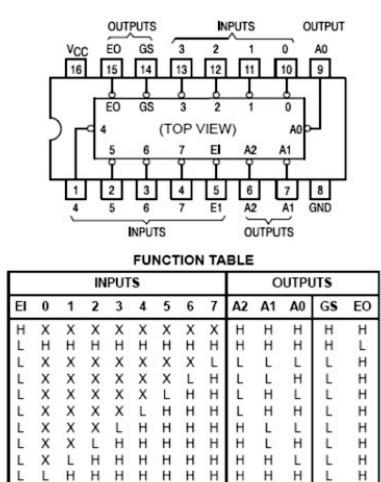
Ví dụ : Bộ lập mã 8 to 3 Encoder

Inputs								Outputs		
\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	O_2	O_1	O_0
X	1	1	1	1	1	1	1	0	0	0
X	0	1	1	1	1	1	1	0	0	1
X	1	0	1	1	1	1	1	0	1	0
X	1	1	0	1	1	1	1	0	1	1
X	1	1	1	0	1	1	1	1	0	0
X	1	1	1	1	0	1	1	1	1	0
X	1	1	1	1	1	0	1	1	1	0
X	1	1	1	1	1	1	0	1	1	1

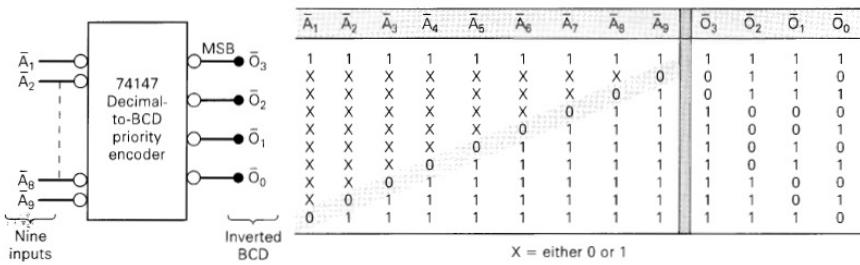


BINARY PRIORITY ENCODER – IC 74LS148

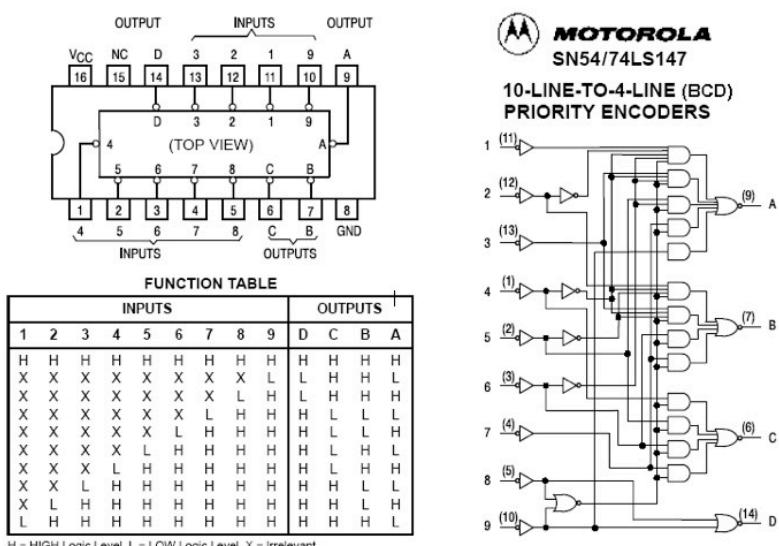
MỨC ƯU TIÊN CHO CÁC ĐẦU VÀO $7 > 6 > 5 > 4 > 3 > 2 > 1 > 0$



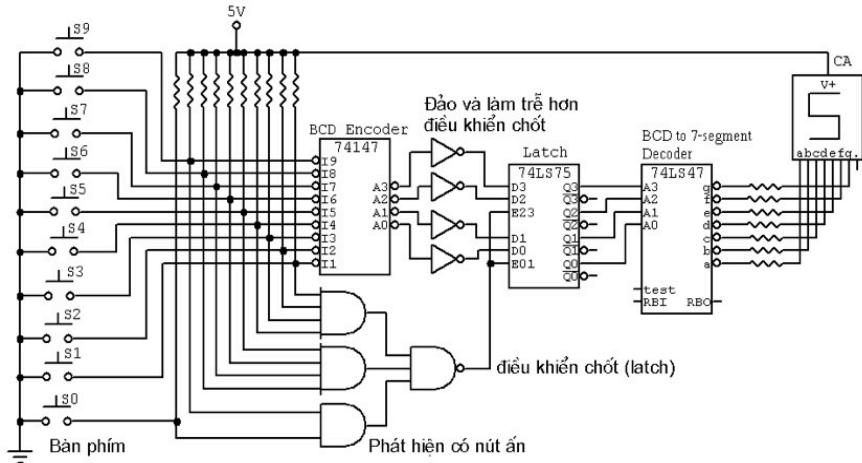
DECIMAL to BCD PRIORITY ENCODER



IC 74LS147

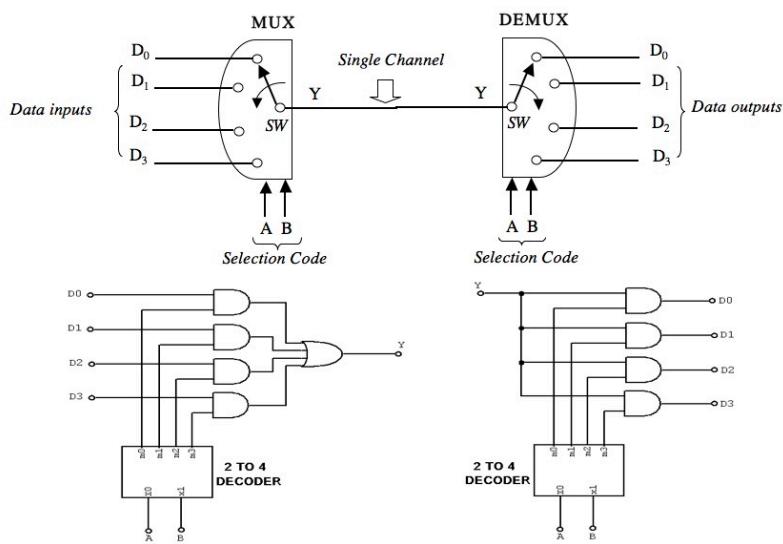


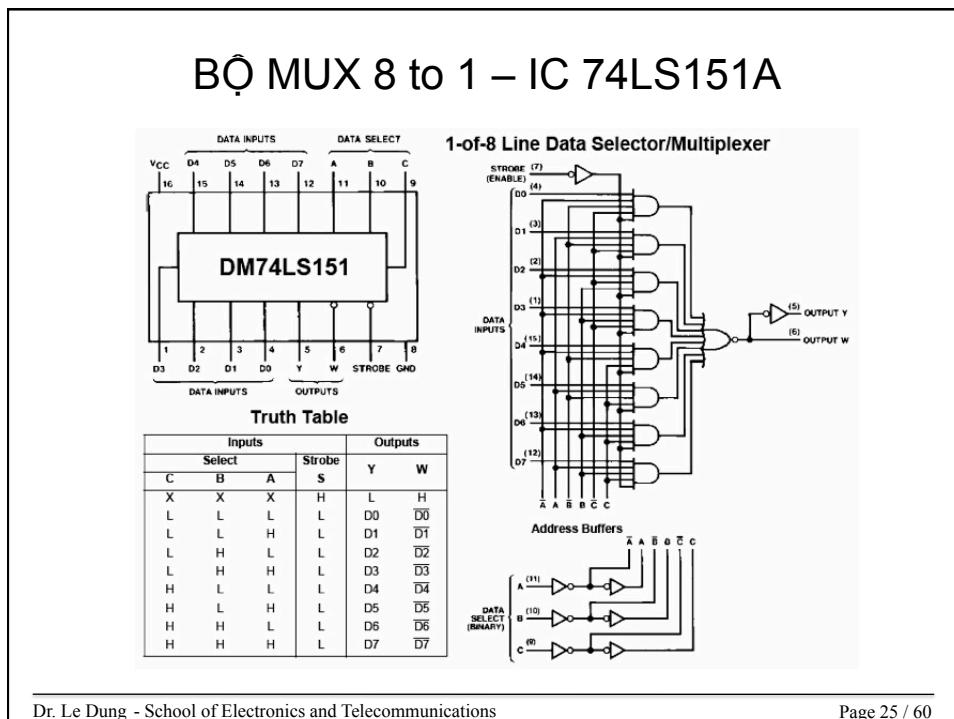
LẬP MÃ BÀN PHÍM VỚI IC 74LS147



(Chạy mô phỏng được trên Circuit Maker 2000)

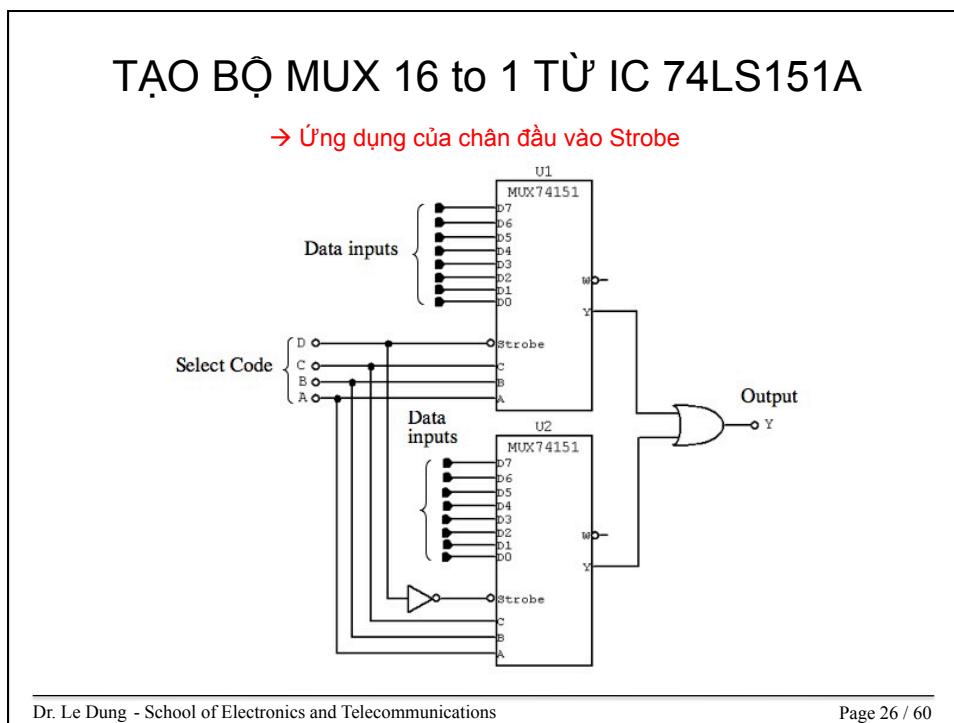
BỘ ĐÔN KÊNH (MUX) – BỘ PHÂN KÊNH (DEMUX)





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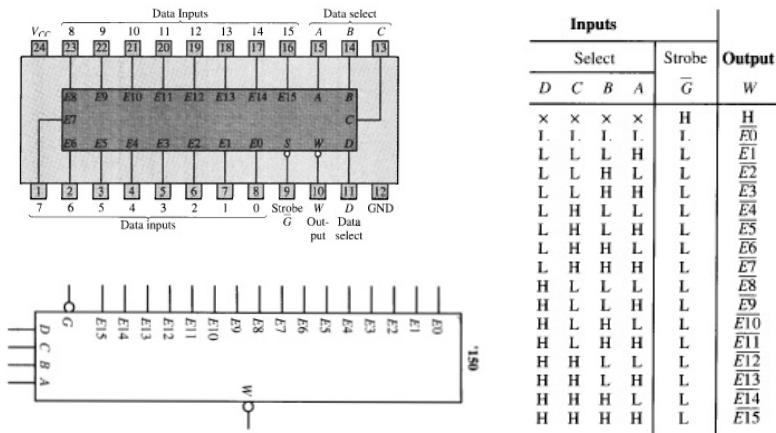
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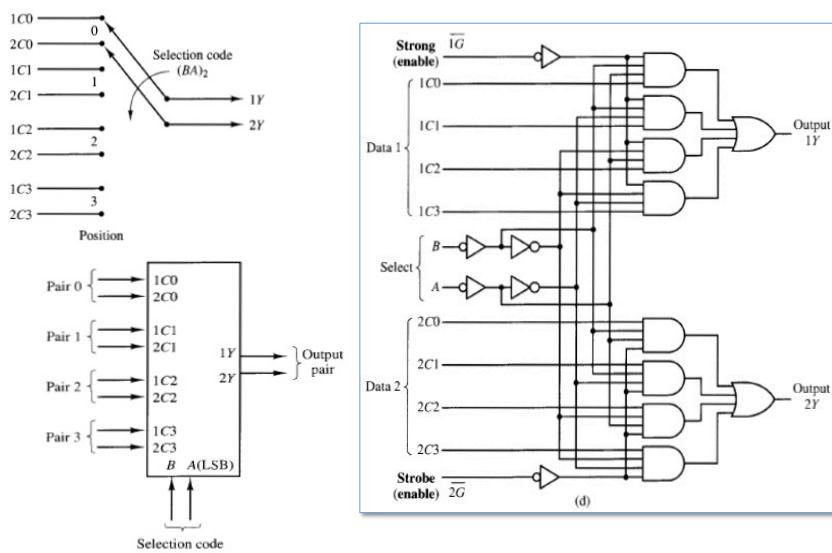
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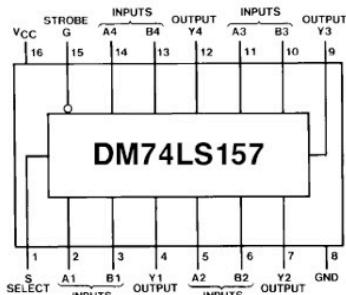
BƠ MUX 16 to 1 - IC 74LS150



DUAL(2 bits) FOUR-INPUT MUX - IC 74LS153



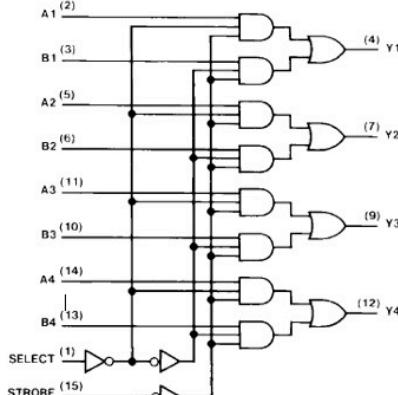
QUAD TWO-INPUT MUX - IC 74LS157



Function Table

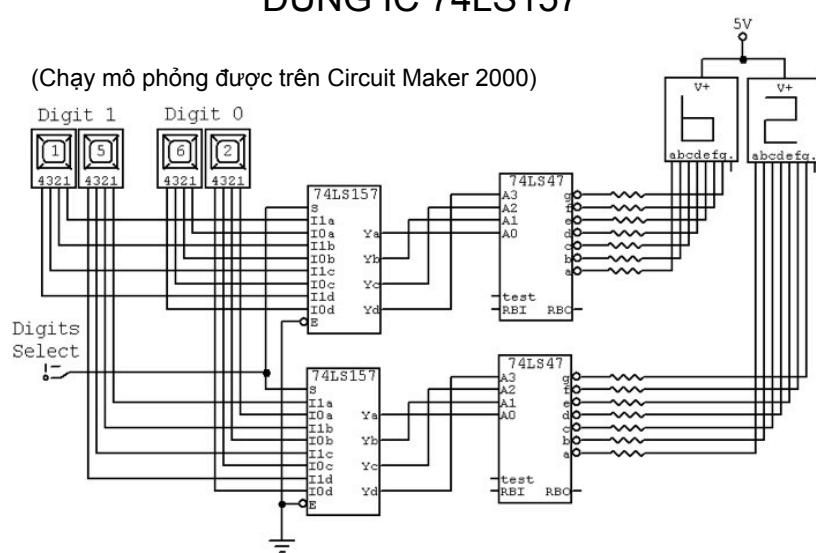
Inputs			Output Y
Strobe	Select	A B	
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

Quad 2-Line to 1-Line
Data Selectors/Multiplexers

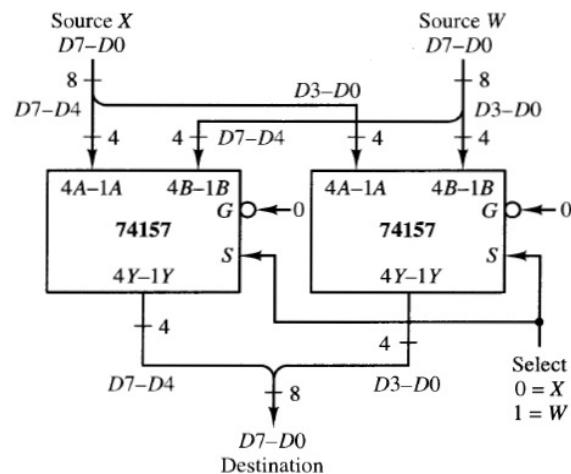


MẠCH CHỌN 1 TRONG 2 SỐ BCD ĐỂ HIỂN THỊ DÙNG IC 74LS157

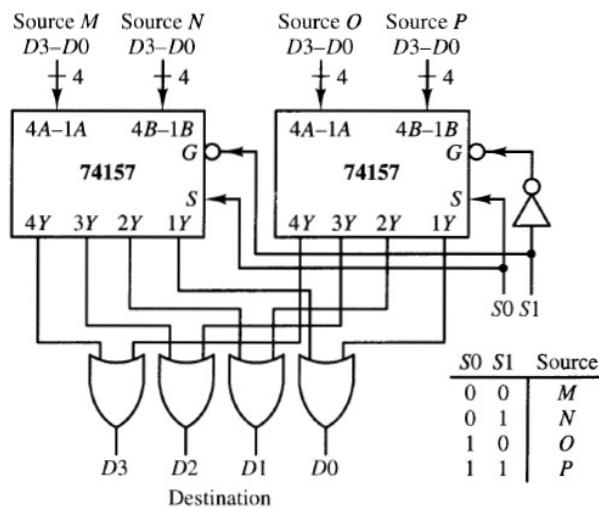
(Chạy mô phỏng được trên Circuit Maker 2000)



THỰC HIỆN 8-bit two-input MUX dùng 74LS157

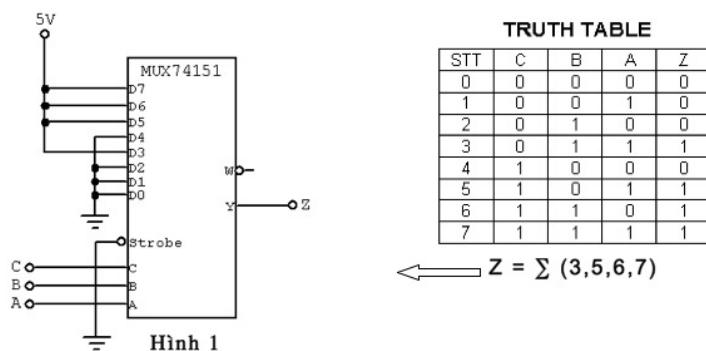


THỰC HIỆN 4-bit four-input MUX dùng 74LS157



ỨNG DỤNG CỦA BỘ ĐӨN KÊNH

1. TỔNG HỢP MẠCH LOGIC TỔ HỢP (Hình 1)
2. ĐỊNH TUYẾN DỮ LIỆU
3. CHUYỂN ĐỔI DỮ LIỆU TỪ SONG SONG SANG NỐI TIẾP
4. TẠO CHUỖI TÍN HIỆU TUẦN HOÀN



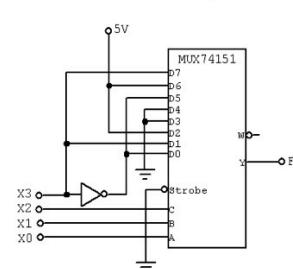
TỔNG HỢP MẠCH LOGIC TỔ HỢP BẰNG MUX

VD: Thực hiện hàm $F = \sum (0, 2, 5, 6, 9, 10, 14, 15)$ dùng 74LS151

Bước 1 : Lập bảng sự thật và tìm điều kiện để $F = Y - \text{đầu ra } 74LS151$)

Minterm	X3	X2	X1	X0	F	Y Select	Đ/c Y=F thi
m0	0	0	0	0	1	D0	$D0 = \overline{X3}$
m8	1	0	0	0	0	D1	$D1 = X3$
m1	0	0	0	1	0	D2	$D2 = 1$
m9	1	0	0	1	1	D3	$D3 = 0$
m2	0	0	1	0	1	D4	$D4 = 0$
m10	1	0	1	0	1	D5	$D5 = \overline{X3}$
m3	0	0	1	1	0	D6	$D6 = 1$
m11	1	0	1	1	0	D7	$D7 = X3$
m4	0	1	0	0	0		
m12	1	1	0	0	0		
m5	0	1	0	1	1		
m13	1	1	0	1	0		
m6	0	1	1	0	1		
m14	1	1	1	0	1		
m7	0	1	1	1	0		
m15	1	1	1	1	1		

Bước 2 : Vẽ mạch

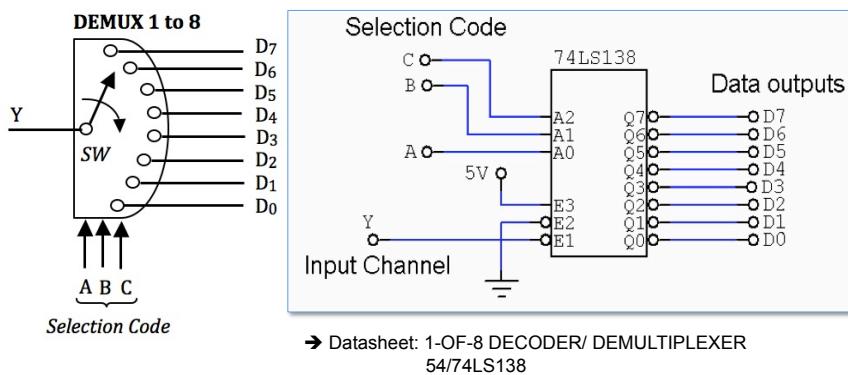


Bài tập: 1. Thực hiện $f = ab' + bc$ bằng MUX 4 to 1.
2. Thực hiện $f = \sum (3, 6, 7, 8, 10, 12, 13, 14)$ bằng MUX 4 to 1.

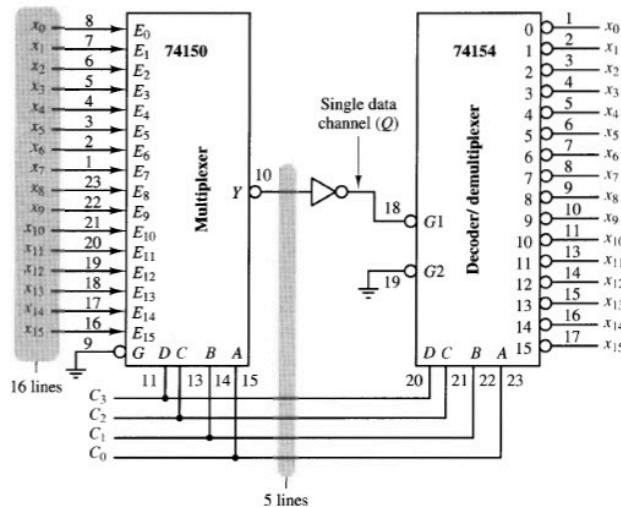
THỰC HIỆN BỘ PHÂN KÊNH DEMUX

→ Dùng DECODER để thực hiện DEMUX

VD: Decoder 74LS138 thực hiện DEMUX 1-line to 8-line



CHUYỂN ĐỔI SONG SONG-NỐI TIẾP DÙNG MUX và DEMUX



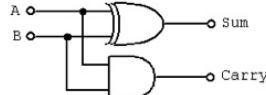
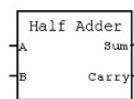
BỘ CỘNG NHỊ PHÂN 1 BIT-ADDER

Bộ cộng Half-Adder

B	A	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = A \cdot B$$

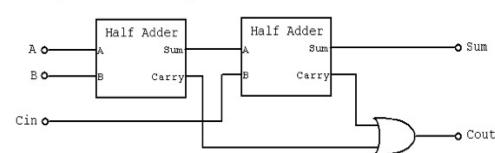
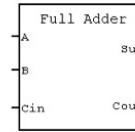


Bộ cộng Full-Adder

Cin	B	A	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{Sum} = A \oplus B \oplus \text{Cin}$$

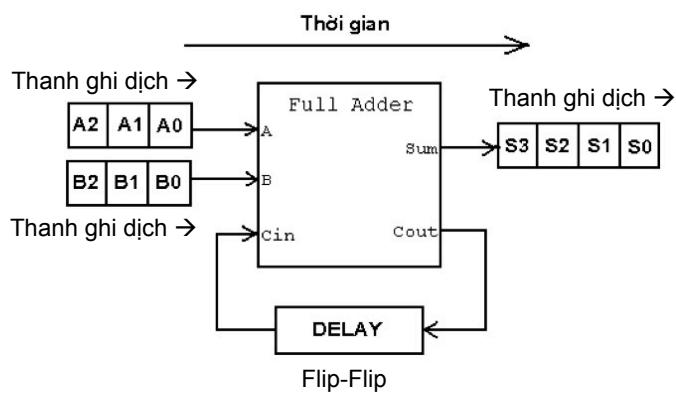
$$\text{Carry} = A \cdot B + (A \oplus B) \cdot \text{Cin}$$



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BỘ CỘNG NHỊ PHÂN n BIT NỐI TIẾP



Các thanh ghi dịch và Flip-Flop làm việc theo xung nhịp → **Tốc độ cộng chậm**

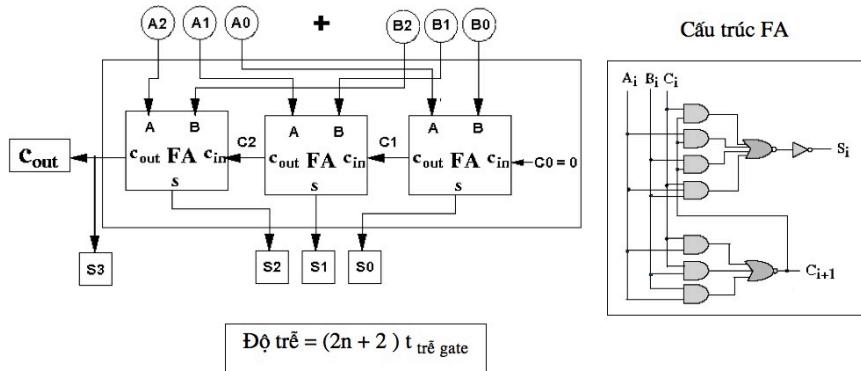
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BỘ CỘNG NHỊ PHÂN KIỀU NỐI TẦNG

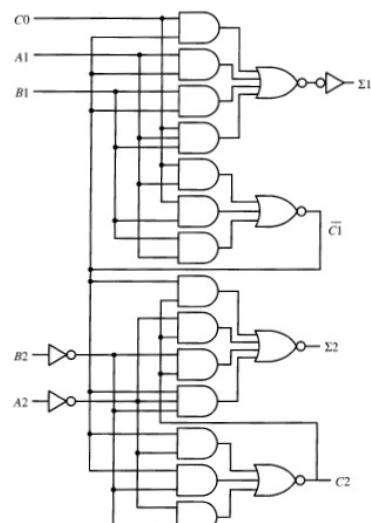
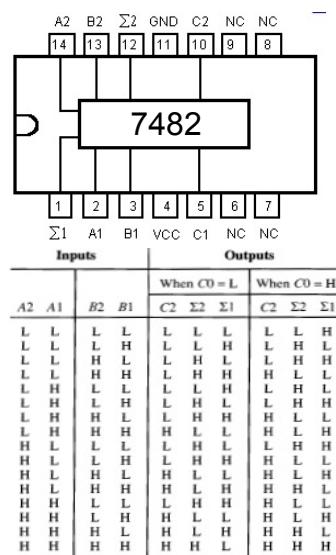
Pseudo-parallel binary Adder or Cascaded Full-Adder

VD: Thực hiện bộ cộng nhị phân giả song song (kiểu nối tầng) 3 bits



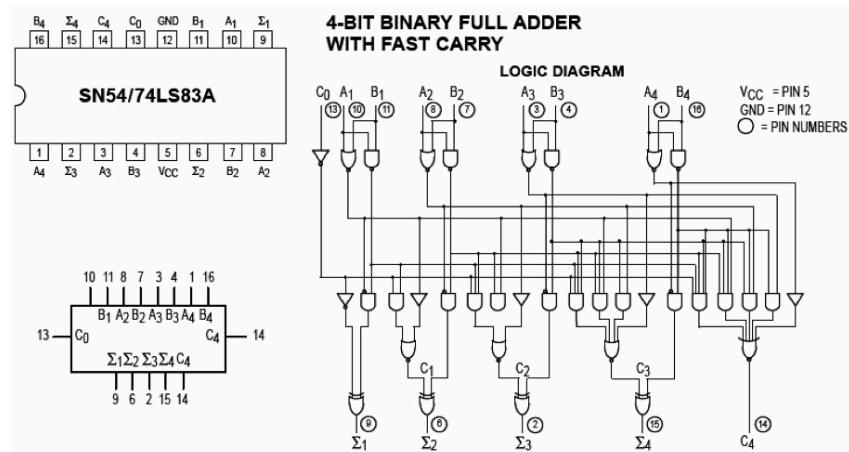
Kiểu nối tầng này còn có tên là Ripple-Carry Adder

IC 7482 TWO-BIT PSEUDO-PARALLEL ADDER

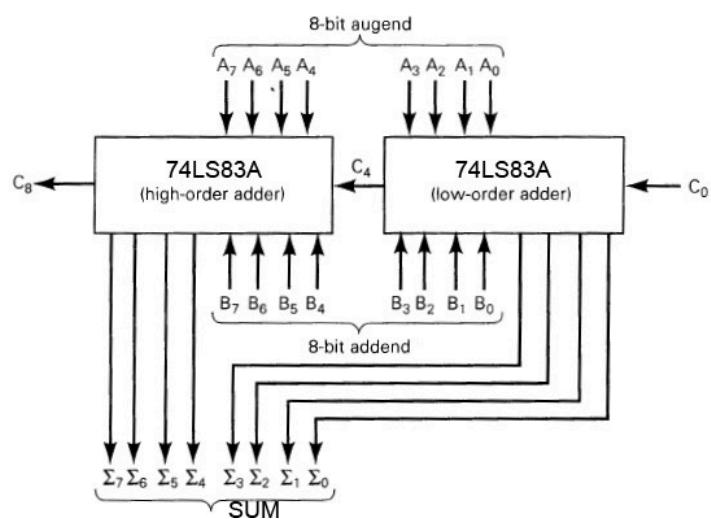


IC 74LS83A FOUR-BIT ADDER

Được thiết kế để tính nhớ nhanh → tăng tốc bộ cộng

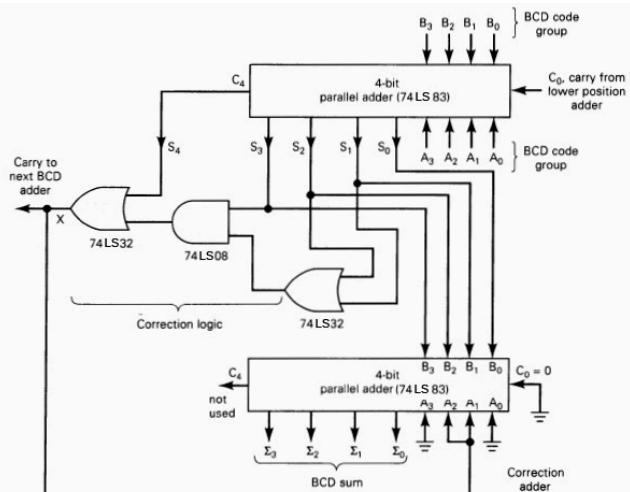


THIẾT KẾ BỘ CỘNG 8-BIT DÙNG 74LS83A



BCD ADDER

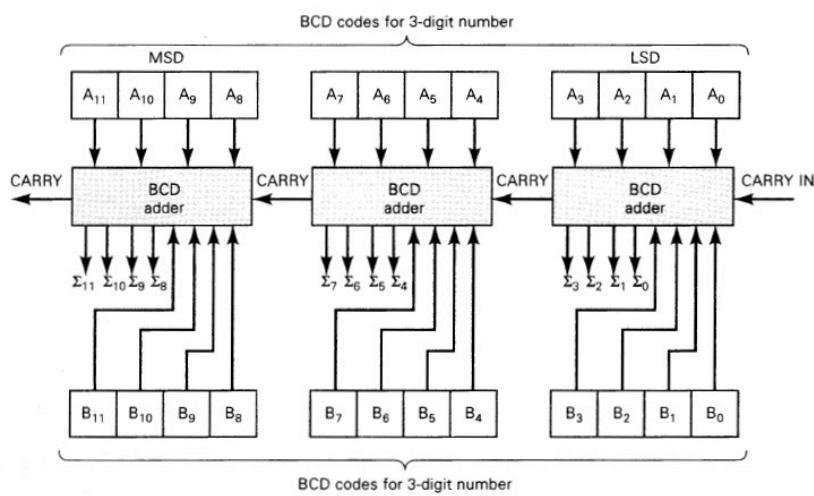
BÀI TẬP: THIẾT KẾ BỘ CỘNG BCD DÙNG 74LS83A



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CASCADING BCD ADDER



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HIGH-SPEED ADDER DESIGN

1. Carry Look-ahead Adder
2. Carry-Save Adder (Đọc thêm)
3. Carry-Bypass Adder (Đọc thêm)
4. Kogge-Stone Adder (Đọc thêm)
5. Fully Parallel Adder (Look-up Table Adder)

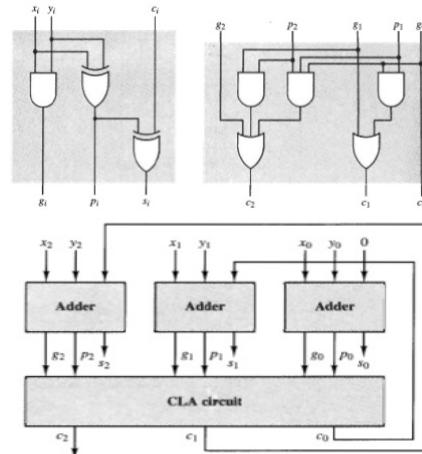
CARRY LOOK-AHEAD ADDER DESIGN

Xuất phát từ công thức $C_{OUT} = C_i = A_i \cdot B_i + (A_i \oplus B_i) \cdot C_{i-1}$

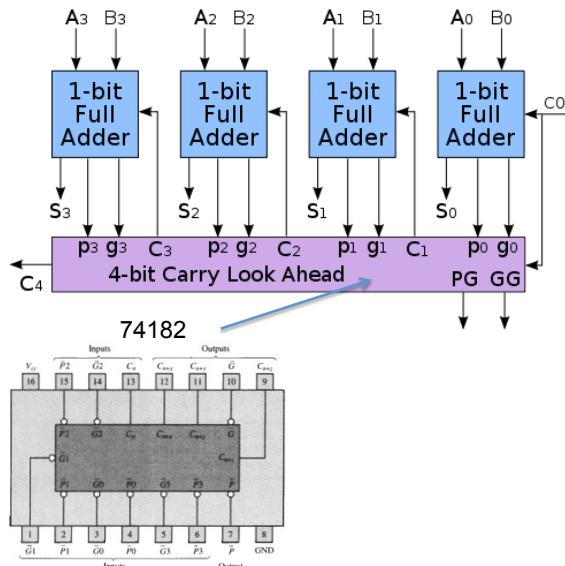
Đặt $G_i = A_i \cdot B_i$ → gọi là Generate term
 $P_i = (A_i \oplus B_i)$ → gọi là Propagate term

$$\rightarrow C_i = G_i + P_i \cdot C_{i-1}$$

$$\begin{aligned} c_0 &= g_0 \\ c_1 &= g_1 + p_1 c_0 \\ &= g_1 + p_1 g_0 \\ c_2 &= g_2 + p_2 c_1 \\ &= g_2 + p_2 g_1 + p_2 p_1 g_0 \\ s_i &= x_i \oplus y_i \oplus c_{i-1} \\ &= p_i \oplus c_{i-1} \end{aligned}$$



IC 74182 LOOK-AHEAD CARRY GENERATOR

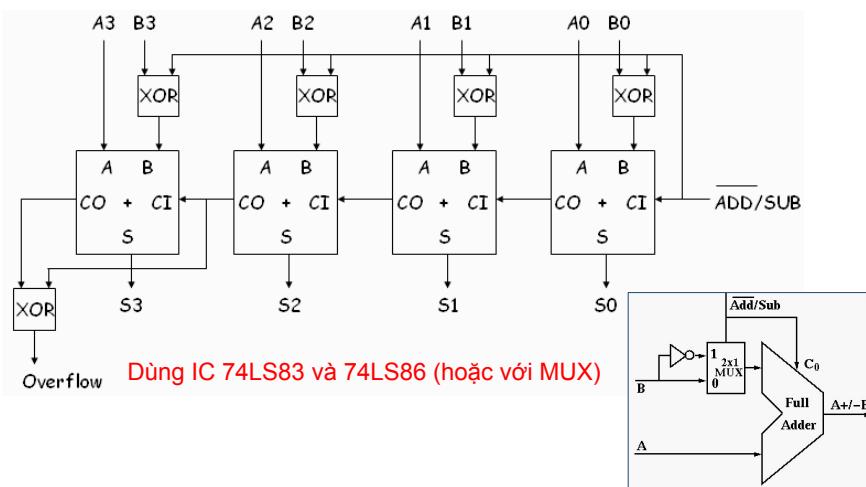


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BỘ TRỪ - SUBTRACTOR

$$A - B = A + (-B) = A + B_{\text{bù}} = A + \text{Inv}(B) + 1$$



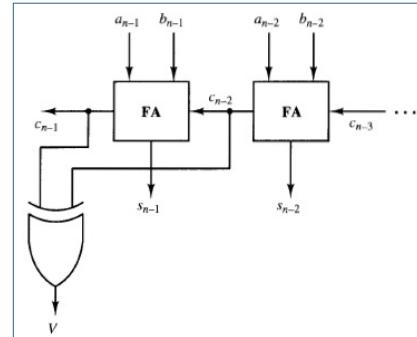
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MẠCH PHÁT HIỆN TRÀN – OVERFLOW DETECTION

Adder Inputs			Adder Outputs		Overflow
a_{n-1}	b_{n-1}	c_{n-2}	c_{n-1}	s_{n-1}	V
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

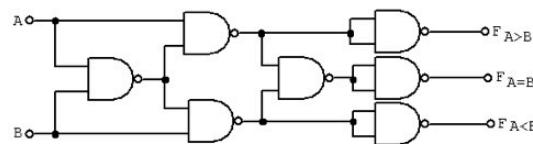
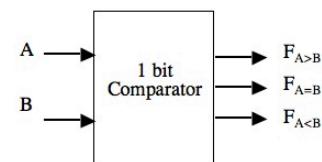
$$V = c_{n-2} \oplus c_{n-1}$$



BỘ SO SÁNH – COMPARATOR

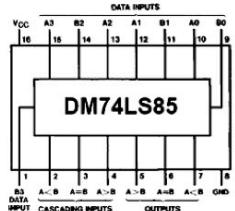
Thực hiện bộ so sánh 1-bit

A	B	$F_{A>B}$	$F_{A=B}$	$F_{A<B}$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0



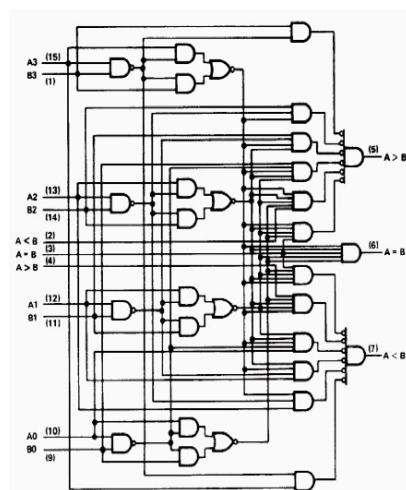
4-BIT MAGNITUDE COMPARATOR – 74LS85

4-Bit Magnitude Comparator

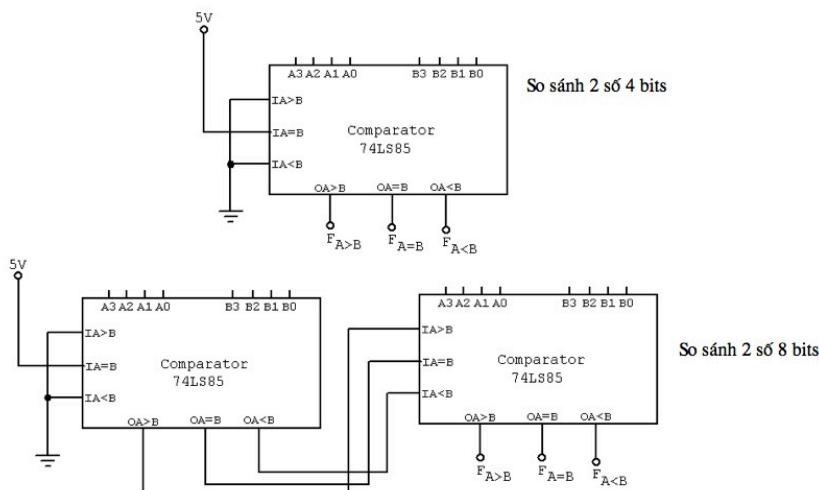


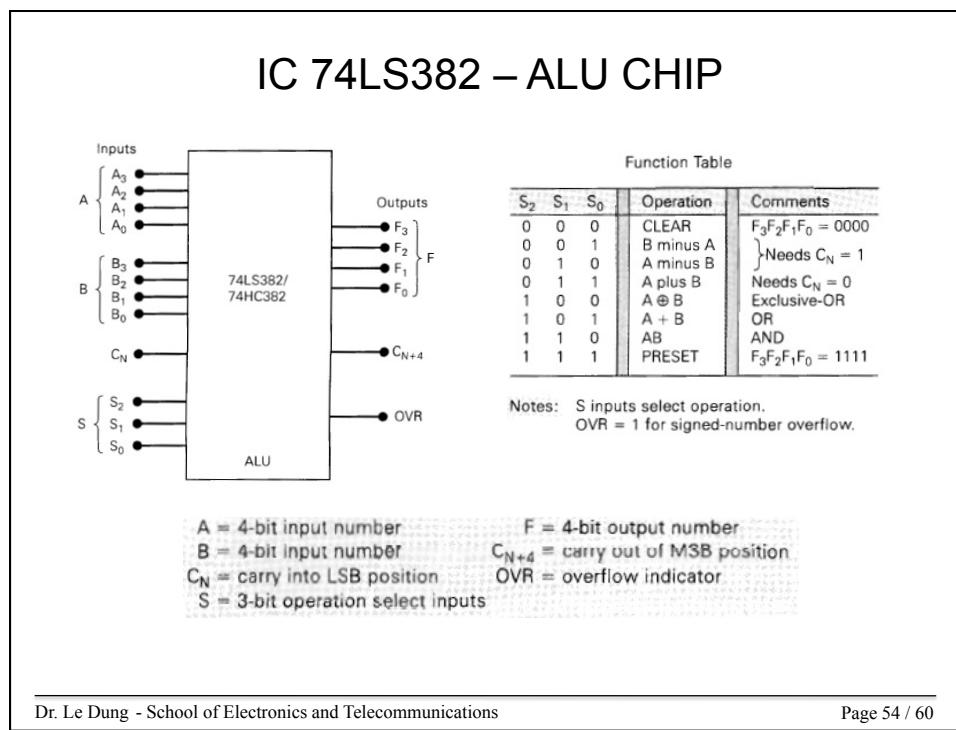
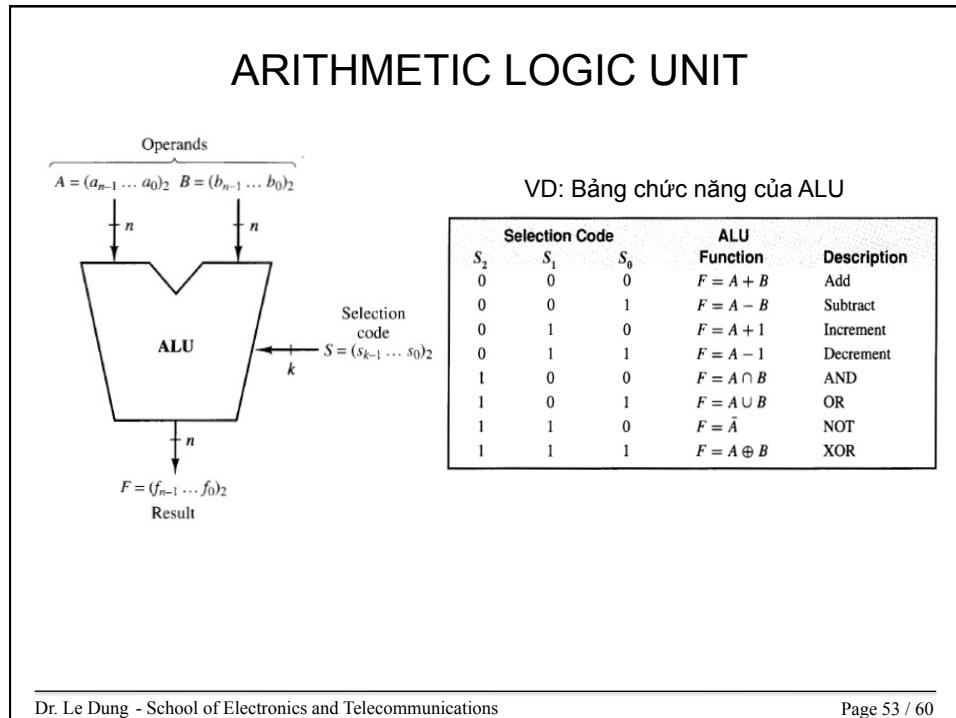
Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	H	L	L



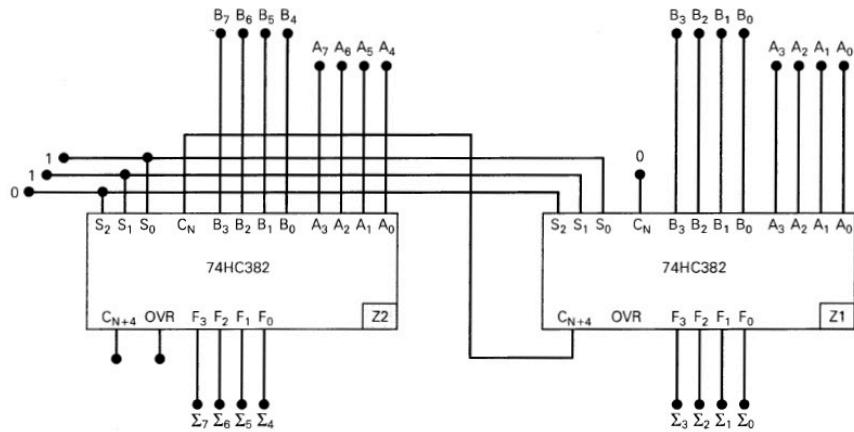
GHÉP NỐI CÁC IC 74LS85





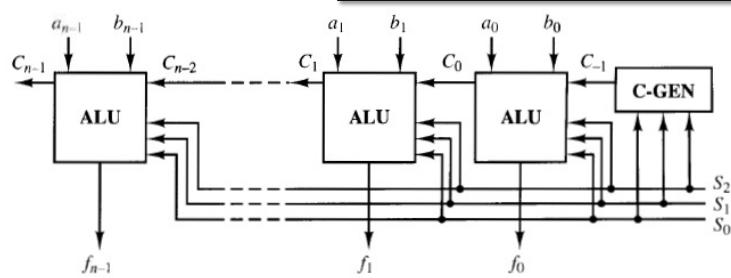
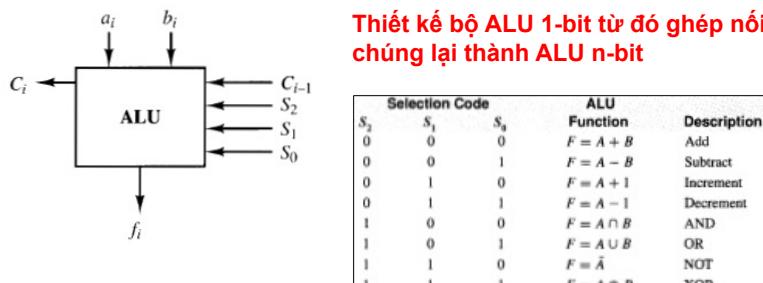
GHÉP NỐI IC 74LS382

VD: → Tạo bộ cộng 8-bit từ 2 IC 74LS382



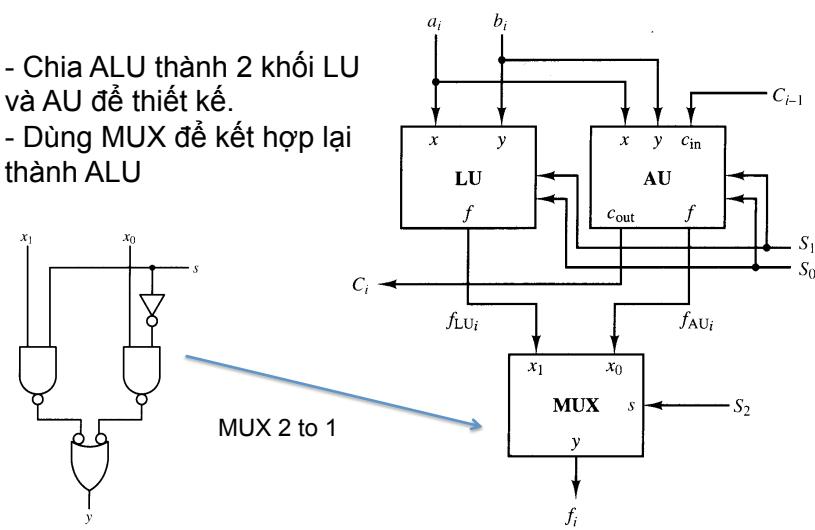
BÀI TẬP THIẾT KẾ ALU (1)

Thiết kế bộ ALU 1-bit từ đó ghép nối
chúng lại thành ALU n-bit



BÀI TẬP THIẾT KẾ ALU (2)

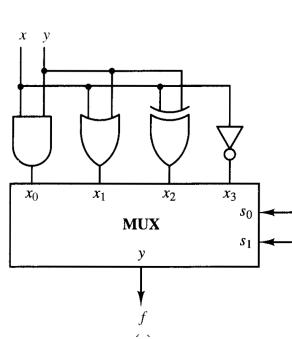
- Chia ALU thành 2 khối LU và AU để thiết kế.
- Dùng MUX để kết hợp lại thành ALU



BÀI TẬP THIẾT KẾ ALU (3)

Thiết kế khối LU (Logic Unit) với 4 hàm cơ bản

Function	S_1	S_0	f_{LU_i}
AND: $F = A \cap B$	0	0	$a_i b_i$
OR: $F = A \cup B$	0	1	$a_i + b_i$
NOT: $F = \bar{A}$	1	0	\bar{a}_i
XOR: $F = A \oplus B$	1	1	$a_i \oplus b_i$



S_1	S_0	x	y	F_{LU}
0	0	0	0	0
0	0	0	1	0 x AND y
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1 x OR y
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1 NOT x
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1 x XOR y
1	1	1	0	1
1	1	1	1	0

