Analysis Combinational Circuit

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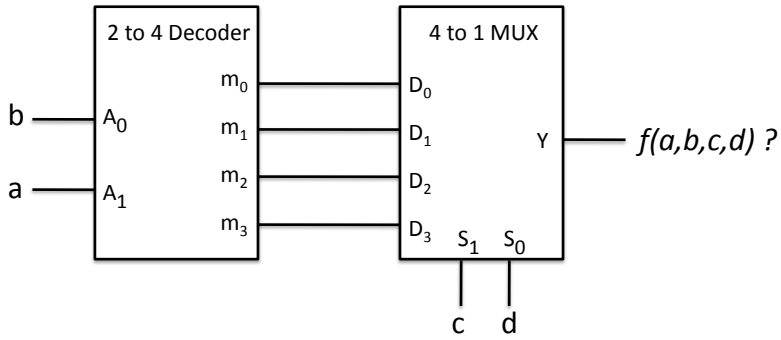
From a given combinational circuit to analysis

- Its function
  (Truth table, Expression forms)
- Timing diagram
  (Test vectors, Delay, Hazard/Glitch)

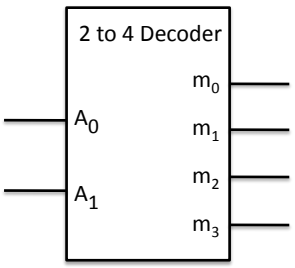
An example (1)

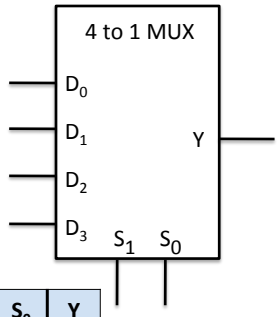
Analysis this combinational circuit



An example (2)

Modular understanding



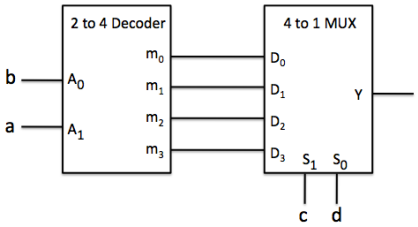


A_1	A_0	m_0	m_1	m_2	m_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

An example (3)

→ Truth table → Expression forms



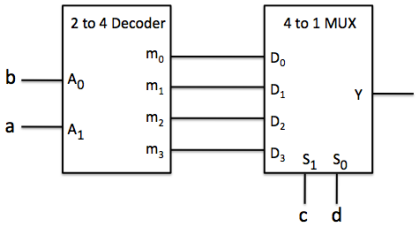
c	d	a	b	f	
0	0	0	0	**1**	$f=Y=D_0$
0	0	0	1	0	
0	0	1	0	0	
0	0	1	1	0	
0	1	0	0	0	$f=Y=D_1$
0	1	0	1	**1**	
0	1	1	0	0	
0	1	1	1	0	
1	0	0	0	0	$f=Y=D_2$
1	0	0	1	0	
1	0	1	0	**1**	
1	0	1	1	0	
1	1	0	0	0	$f=Y=D_3$
1	1	0	1	0	
1	1	1	0	0	
1	1	1	1	**1**	

→ $f = \sum_{cdab}(0, 5, 10, 15) = \sum_{abcd}(0, 5, 10, 15)$

$f = \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}b\bar{c}d + a\bar{b}c\bar{d} + abcd$

An example (4)

→ Expression forms



c	d	F = Y =
0	0	$D_0 = m_0 = a'b'$
0	1	$D_1 = m_1 = a'b$
1	0	$D_2 = m_2 = ab'$
1	1	$D_3 = m_3 = ab$

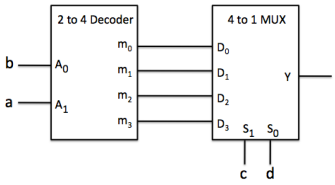
→ $f = m_0.\bar{c}\bar{d} + m_1.\bar{c}d + m_2.c\bar{d} + m_3.cd$

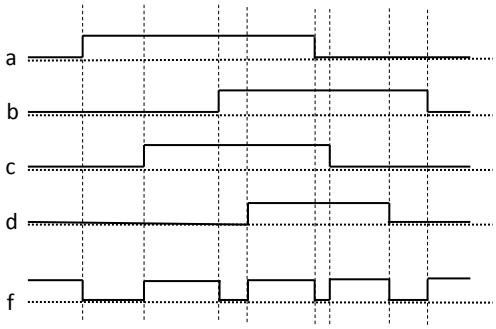
$= \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}b\bar{c}d + a\bar{b}c\bar{d} + abcd$

$= (a \odot c)(b \odot d)$ $= \overline{(a \oplus c) + (b \oplus d)}$

An example (5)

Timing diagram with no delay



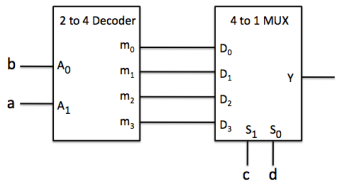


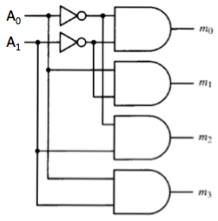
$f = (a \odot c)(b \odot d)$

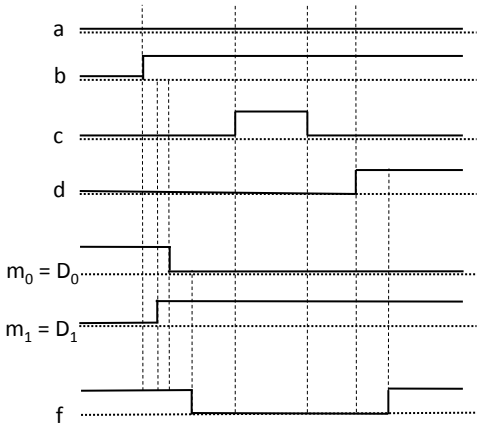
Test vectors : abcd = 0000→1000→1010→1110→1111→0111→0101→0100→0000

An example (6)

Timing diagram with delay





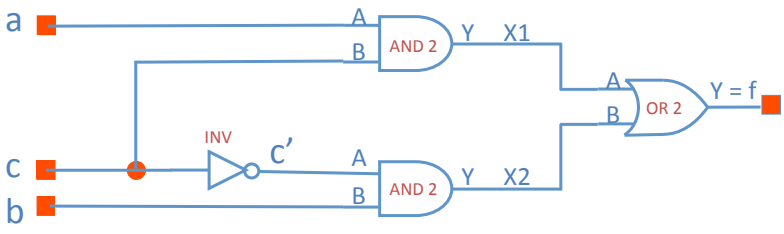


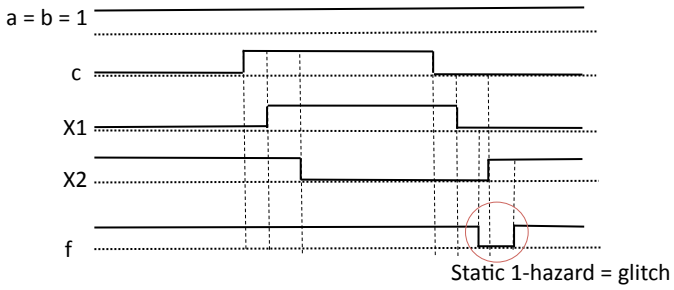
Test vectors : abcd = 0000 → 0100→0110→0100→0101

Static Hazard /Glitch

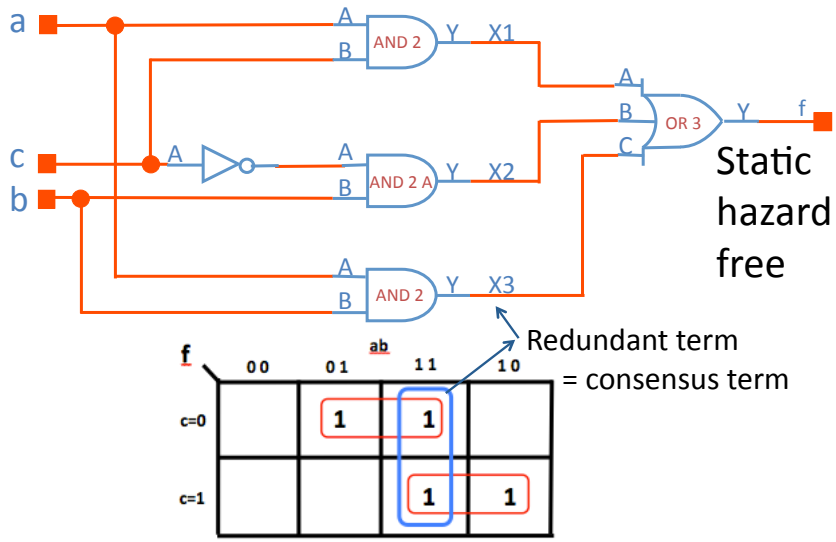
- Hazard condition: A single variable change causes a momentary output change when no output change should occur.
- Cause: different delay in two paths (see Example)
- Glitch: The momentary output change
  = unwanted transient pulse
  + Static 1-hazard = glitch $1 \rightarrow_0 \rightarrow 1$ (in SOP)
  + Static 0-hazard = glitch $0 \rightarrow_1 \rightarrow 0$ (on POS)
- Solution: Adding redundant terms (product terms or sum terms)

An example of static 1-hazard





Removing static 1-hazard



Dynamic hazard

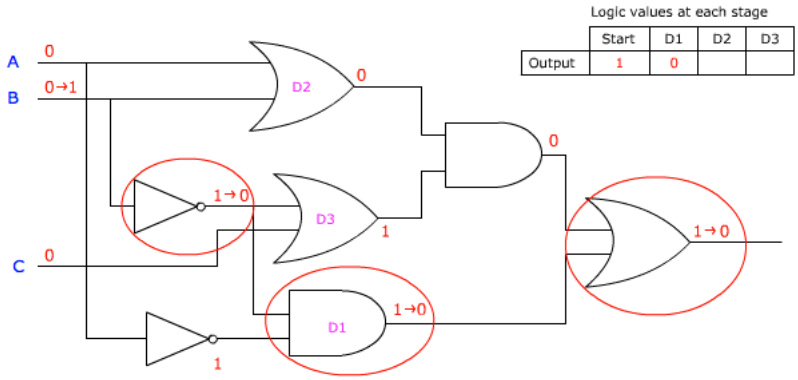
- A dynamic hazard is the possibility of an output changing more than once as a result of a single input change
- Cause: different delay in multiple paths

Dynamic Hazard on 0 → 1

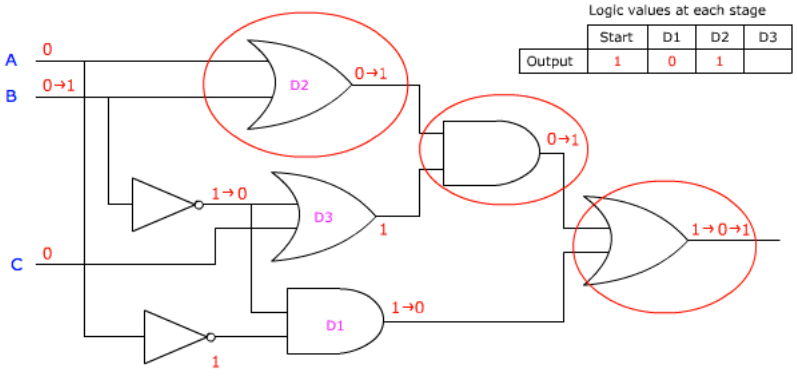
Dynamic Hazard on 1 → 0

- Any circuit that is static hazard free is also dynamic hazard free
- Any circuit dynamic hazard free

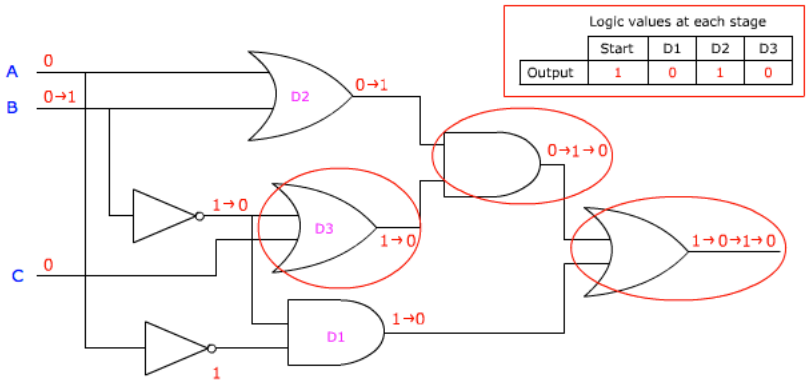
An example of dynamic hazard (1)



An example of dynamic hazard (2)



An example of dynamic hazard (3)



Function hazard

- Function hazards are non-solvable hazards which occurs when more than one input variable changes at the same time.

- Function hazards can not be logically eliminated with actual specification of the circuit. The only real way to avoid such problems is to restrict the changing of input variables so that only one input should change at any given time.

Hazard-free design

- Hazards are hard to detect by hand: importance of simulation
- The danger for hazards increases when rise times and fall times are not equal
- Are hazards a problem?
  - ❑ For synchronous circuits, they are not
  - ❑ Unless they control the clock of a memory element
  - ❑ For asynchronous circuits, they always are a problem