CÁC MẠCH LOGIC DÃY CƠ BẢN

(MODULAR SEQUENTIAL LOGIC CIRCUITS)

NỘI DUNG

I. THANH GHI (REGISTER)

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II. BỘ ĐẾM (COUNTER)

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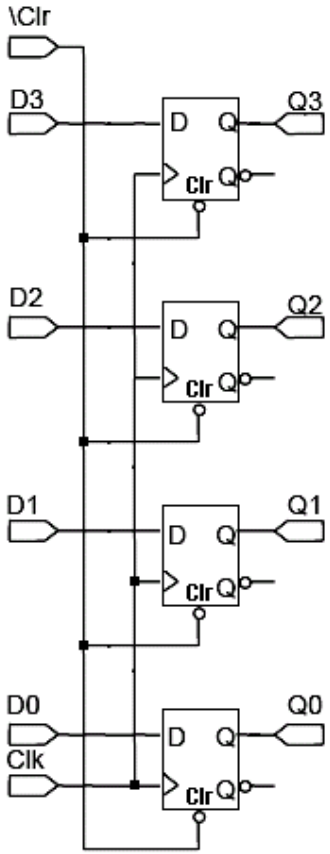
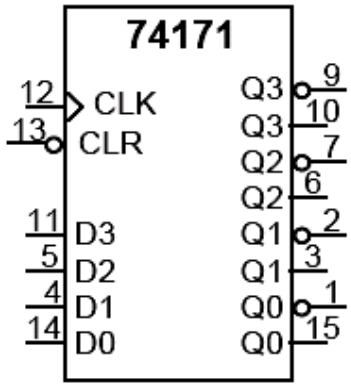
III REGISTER FILES, LIFO, FIFO

THANH GHI LƯU TRỮ (STORAGE REGISTER)



TTL 74171 Quad D-type FF with Clear



Ghi chú : .....
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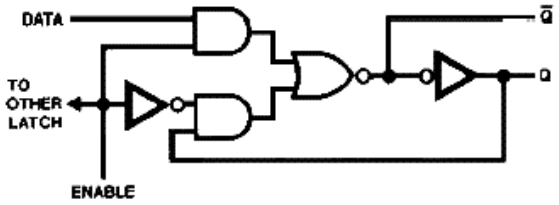
THANH GHI CHỐT (LATCH)

DM74LS75 Quad Latch

Logic Diagram

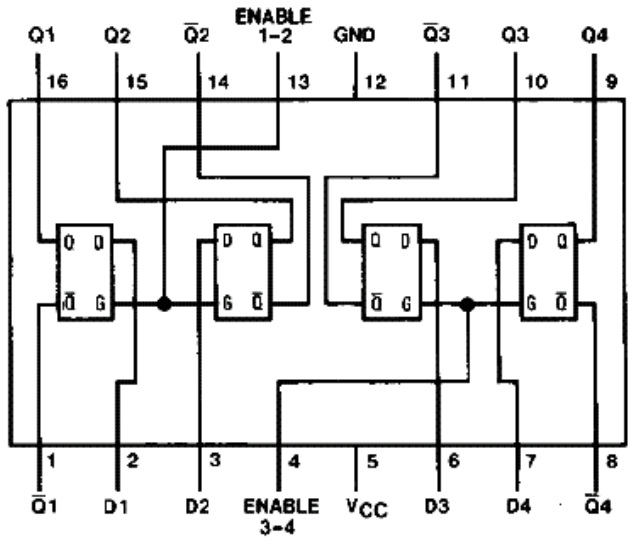
(Each Latch)



Function Table (Each Latch)

Inputs		Outputs	
D	Enable	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

Connection Diagram



Ghi chú : .....

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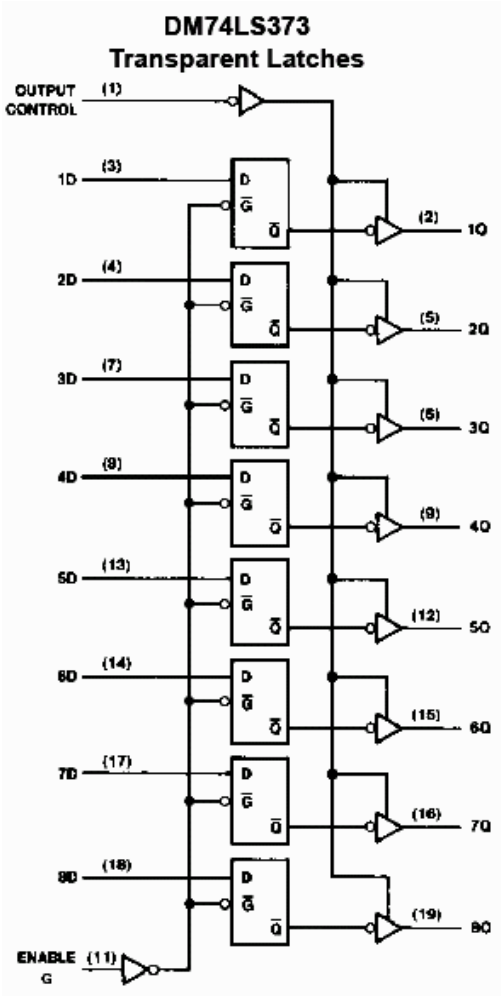
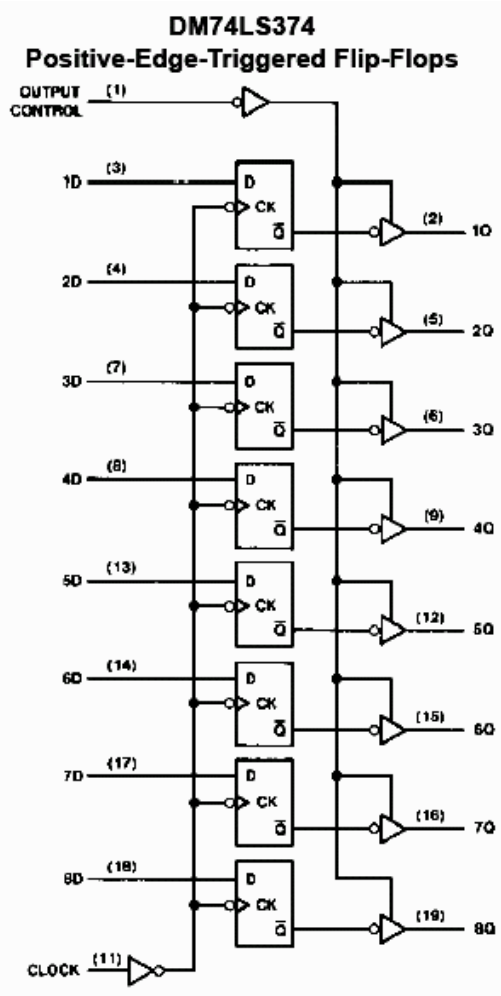
THANH GHI CHỐT CÓ ĐẦU RA 3 TRẠNG THÁI (TRI-STATES LATCH)





Ghi chú :

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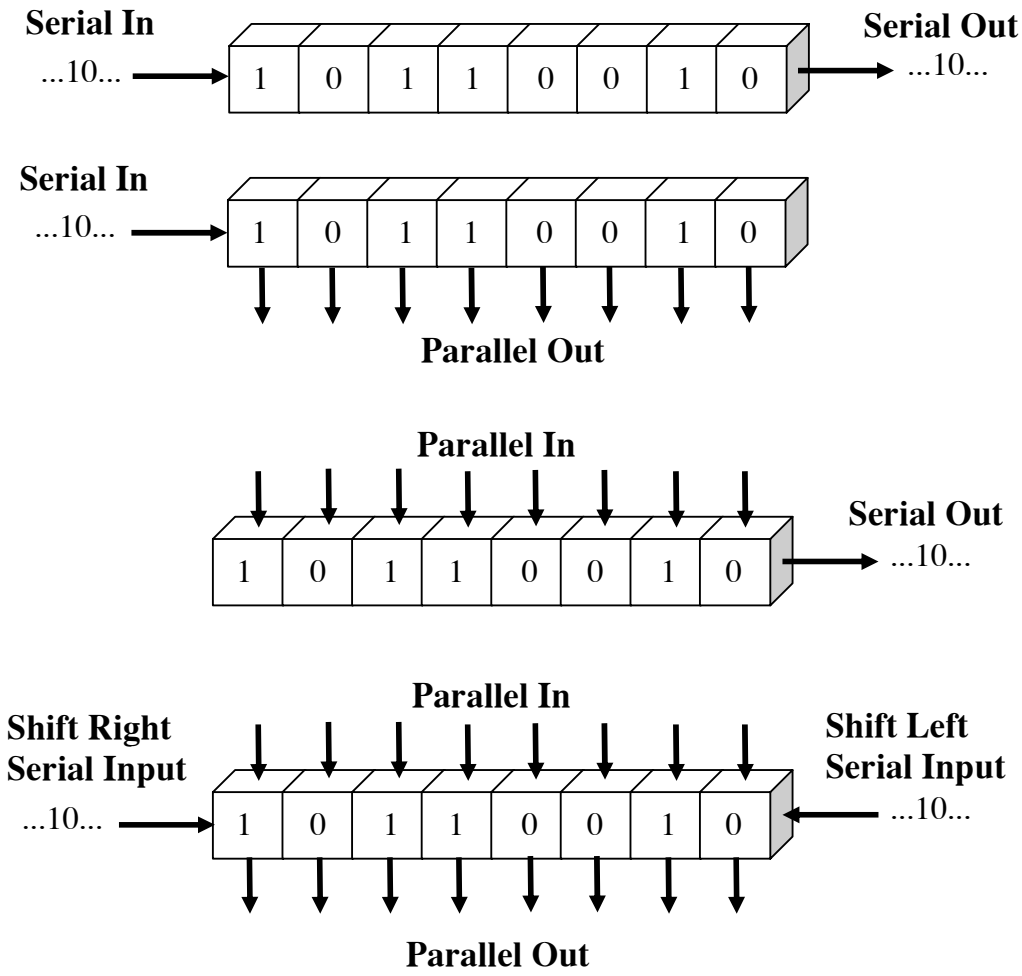
THANH GHI DỊCH (SHIFT REGISTER)



1. Serial-In Serial-Out Shift Register

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2. Serial-In Parallel-Out Shift Register

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3. Parallel-In Serial-Out Shift Register

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4. Shift Right Register

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5. Shift Left Register

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6. Bidirectional Shift Register

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7. Universal Shift Register

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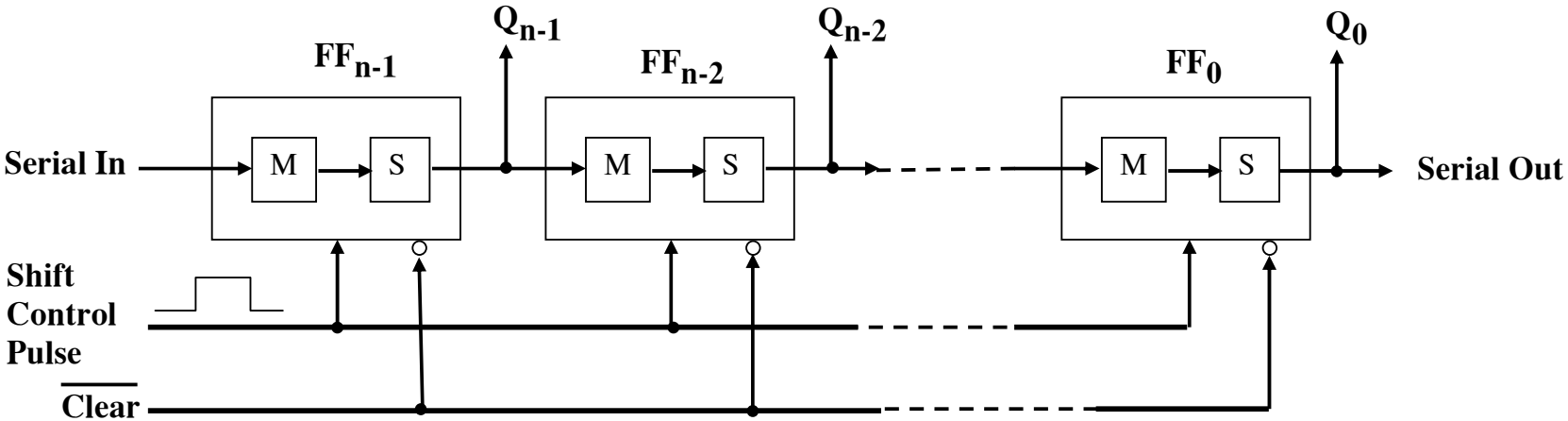
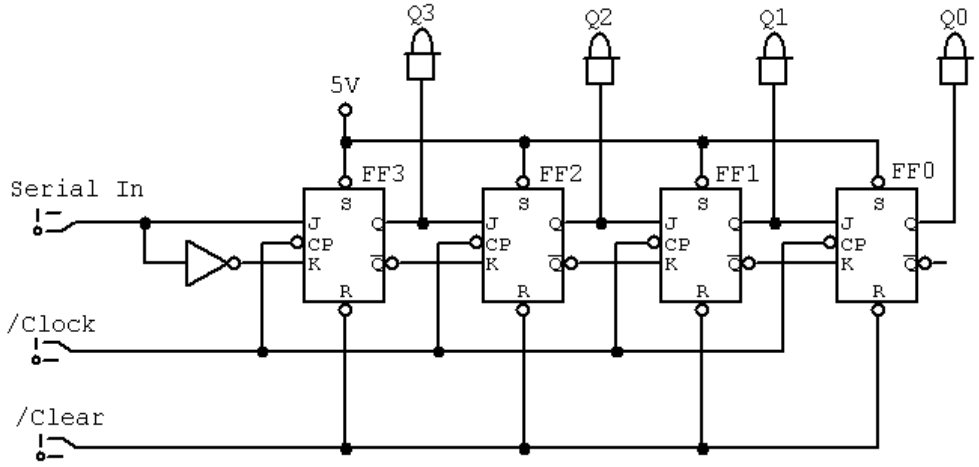
*** Shift Ring Register = Johnson Counter**

SERIAL LOAD SHIFT REGISTER





Ghi chú :

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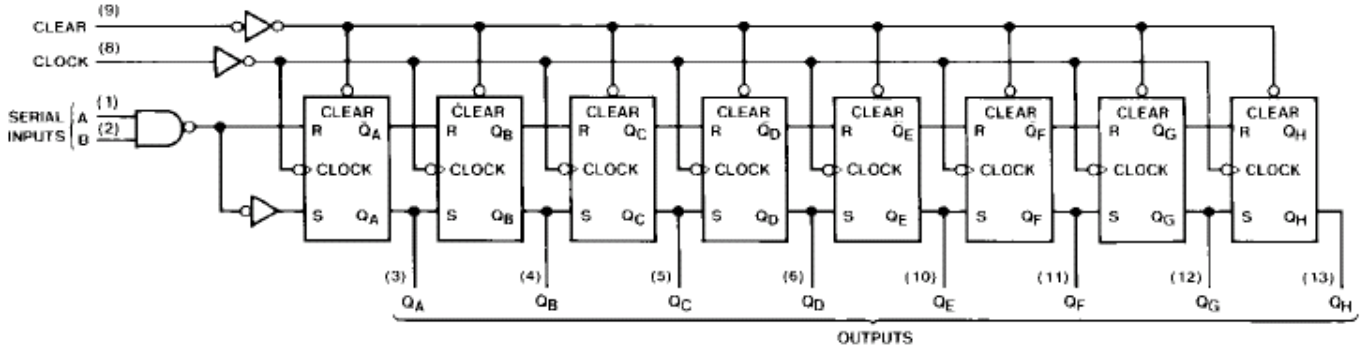
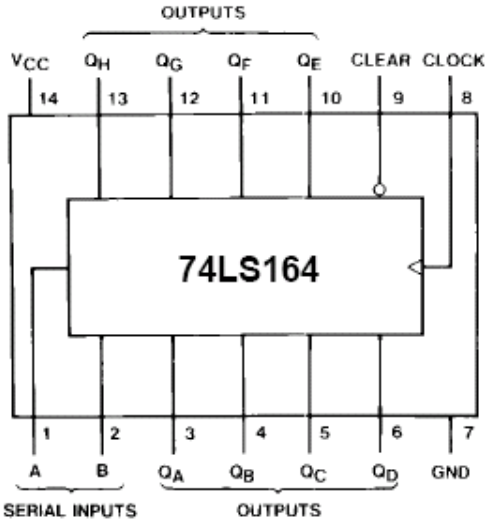
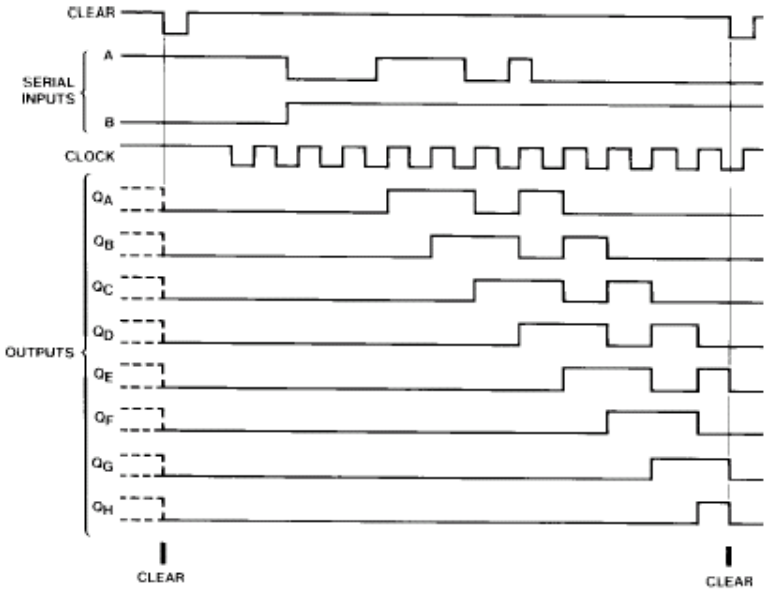
DM74LS164
8-Bit Serial In/Parallel Out Shift Register

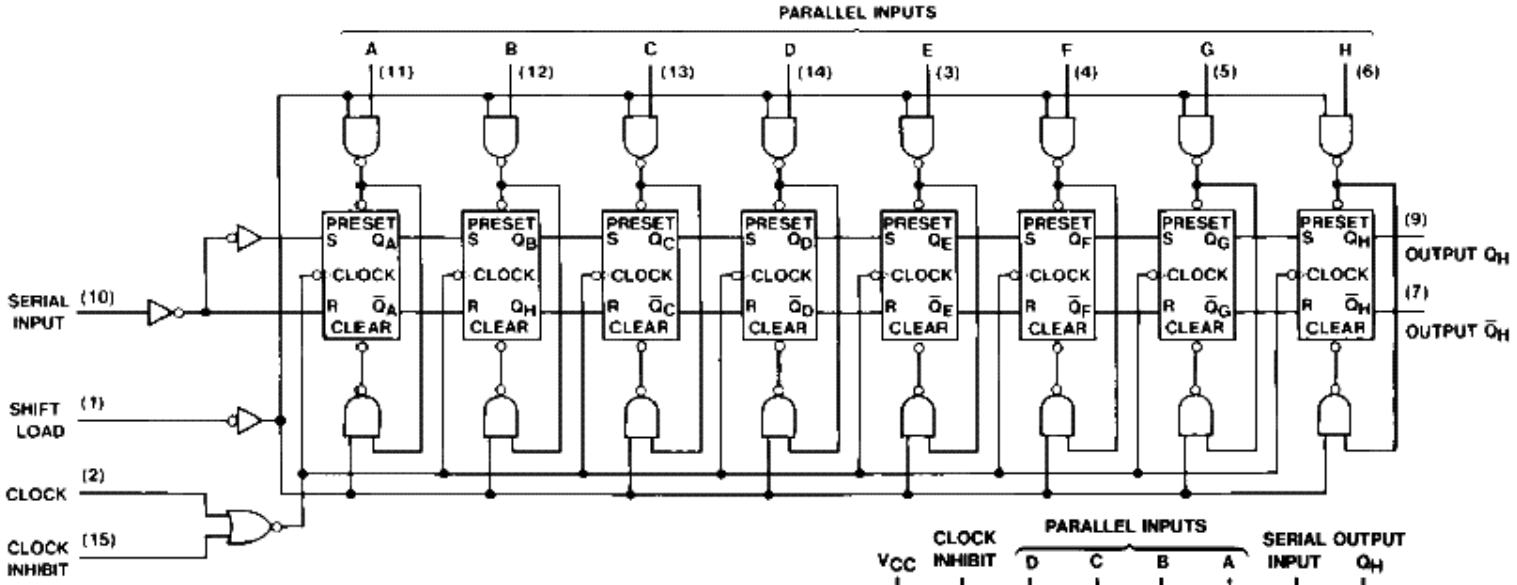


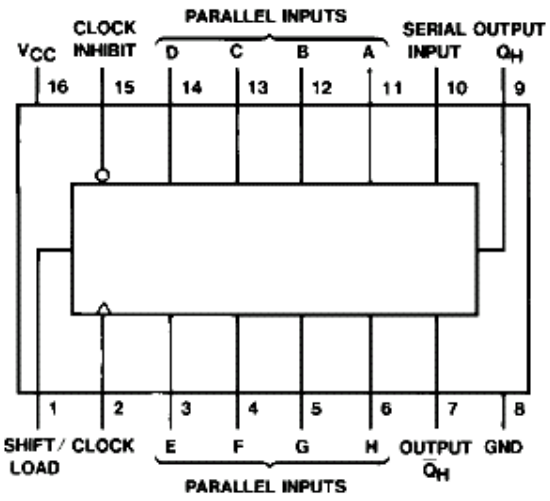


Timing Diagram



DM74LS165
8-Bit Parallel In/Serial Output Shift Registers

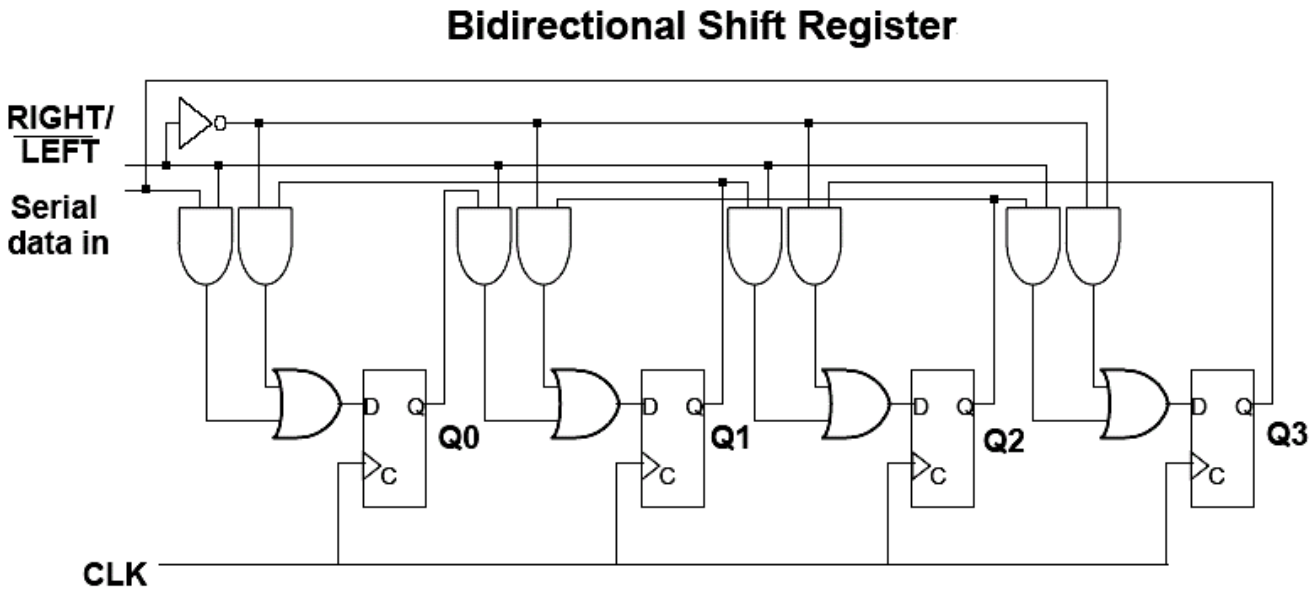




Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

THANH GHI DỊCH 2 CHIỀU



Ghi chú :

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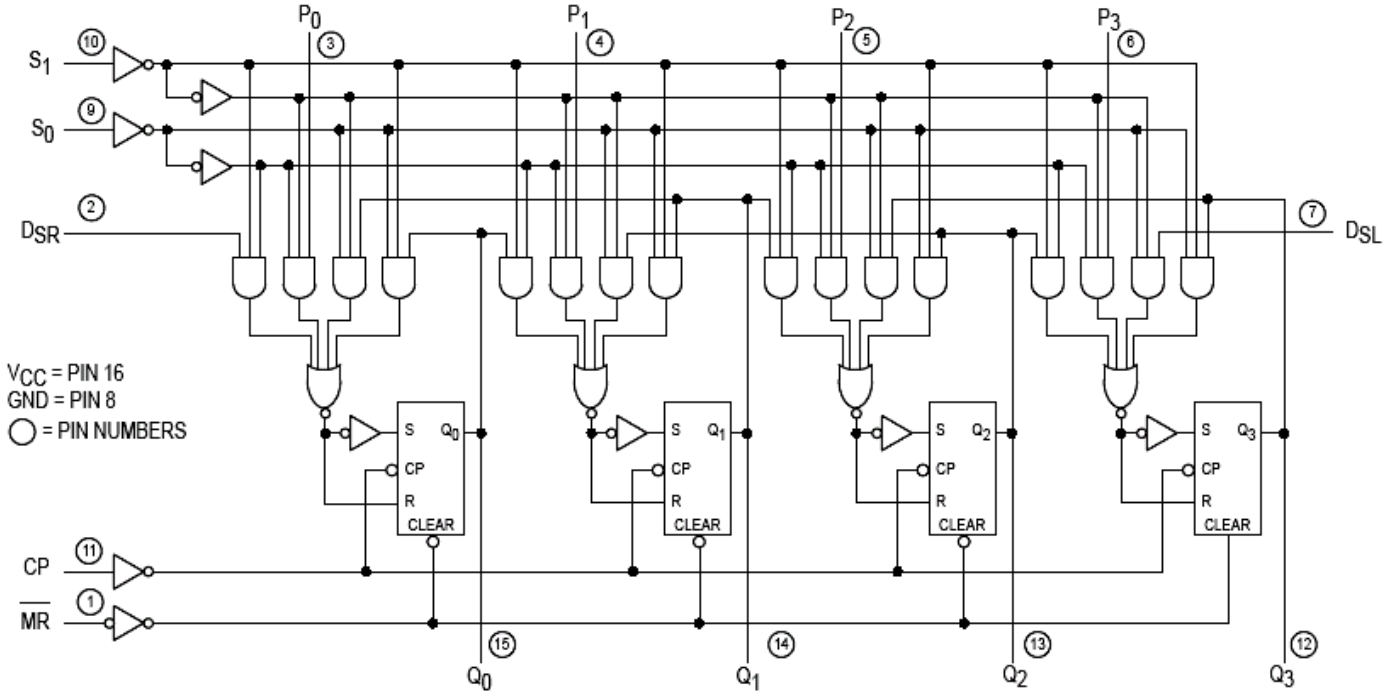
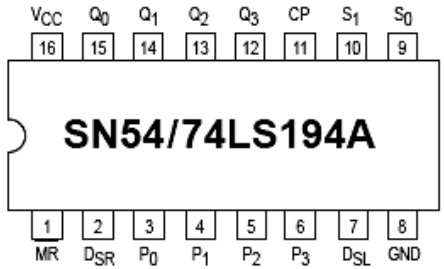
THANH GHI DỊCH ĐA NĂNG

MOTOROLA

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER **SN54/74LS194A**



THANH GHI DỊCH ĐA NĂNG (TIẾP)



PIN NAMES

S_0, S_1	Mode Control Inputs
P_0–P_3	Parallel Data Inputs
D_{SR}	Serial (Shift Right) Data Input
D_{SL}	Serial (Shift Left) Data Input
$\overline{CP}$	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q_0–Q_3	Parallel Outputs (Note b)

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	MR	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H H	h h	l l	X X	l h	X X	q_1 q_1	q_2 q_2	q_3 q_3	L H
Shift Right	H H	l l	h h	l h	X X	X X	L H	q_0 q_0	q_1 q_1	q_2 q_2
Parallel Load	H	h	h	X	X	P_n	P_0	P_1	P_2	P_3

Ghi chú :

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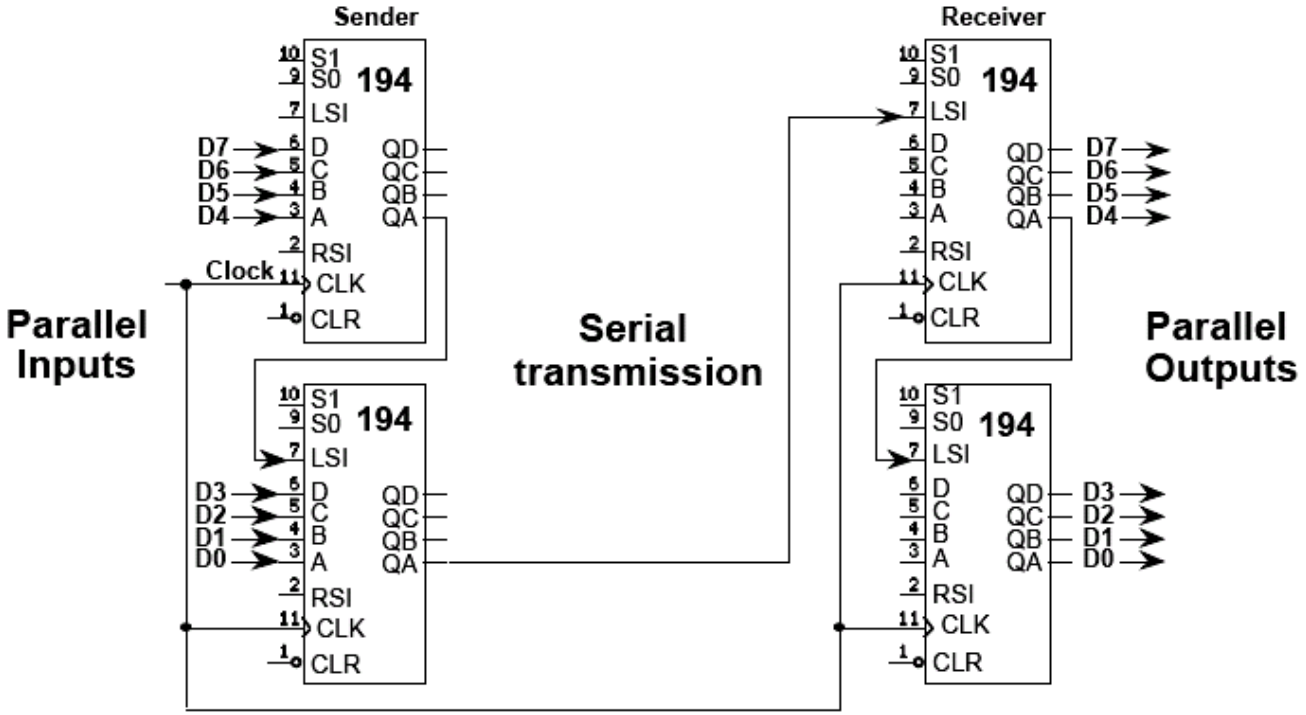
ỨNG DỤNG THANH GHI DỊCH

- **CHUYỂN ĐỔI SONG SONG/NỐI TIẾP VÀ NGƯỢC LẠI**
- **THIẾT KẾ BỘ NHÂN/CHIA**
- **TẠO THỜI GIAN TRỄ**
- **THIẾT KẾ MẠCH DÃY (TIẾT BÀI TẬP)**
- **TẠO CHUỖI TÍN HIỆU TUẦN HOÀN (TIẾT BÀI TẬP)**

CHUYỂN ĐỔI SONG SONG/NỐI TIẾP VÀ NGƯỢC LẠI

Parallel-to-Serial/Serial-to-Parallel Conversion



Ghi chú :

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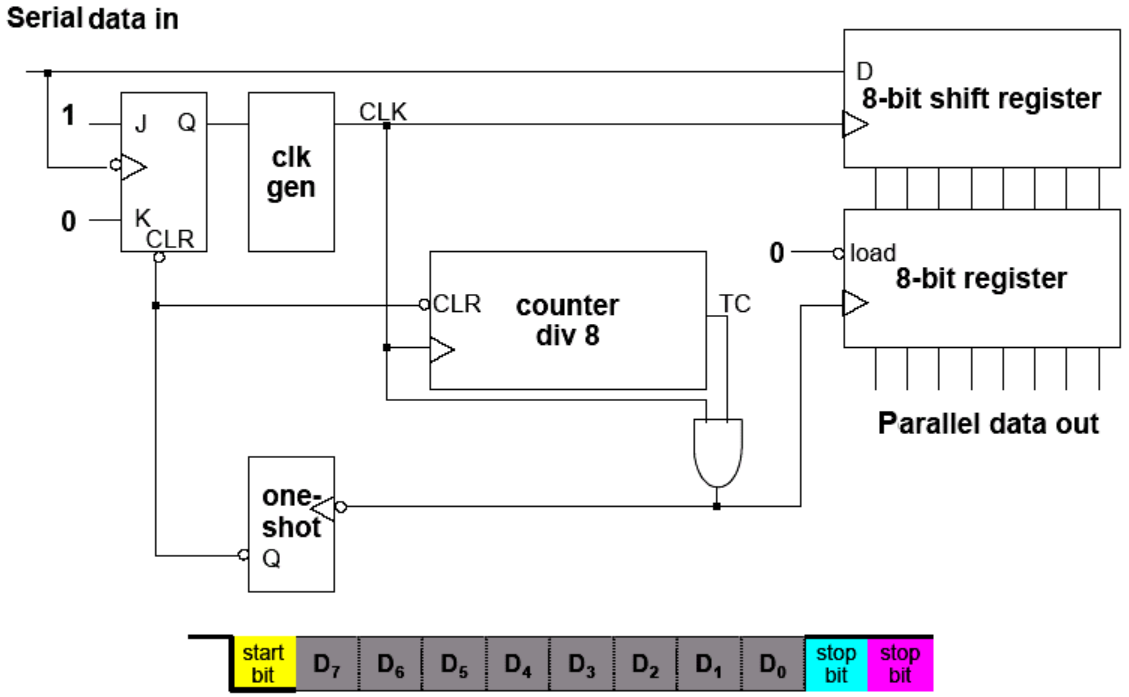
TRUYỀN TIN DI BỘ

Parallel to Serial Conversion for asynchronous communication



Ghi chú :

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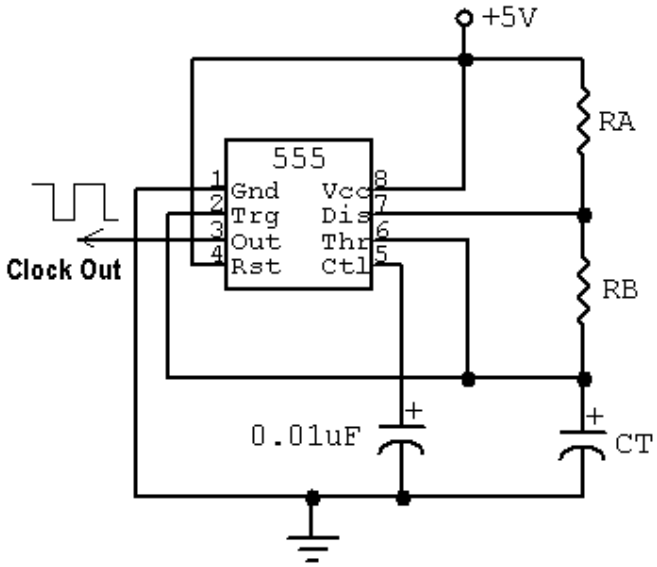
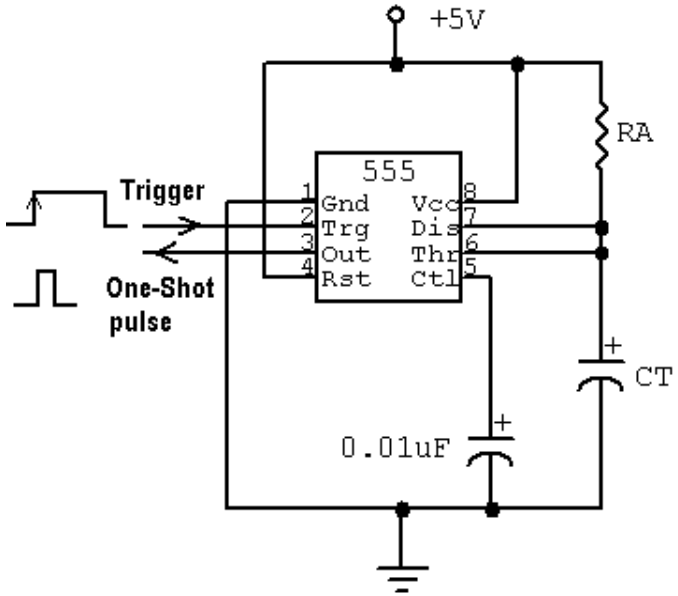
MẠCH TẠO CLOCK VÀ MẠCH MỘT XUNG (ONE-SHOT)





Thông số mạch tạo Clock :

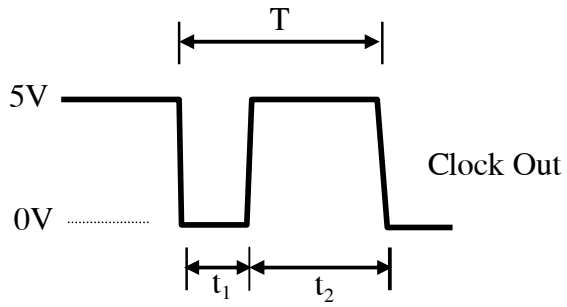
$t_1=0.693.R_B.C_T$

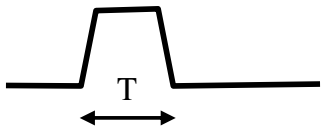
$t_2=0.693.(R_A+R_B).C_T$

$T= t_1 + t_2$

$R_A \geq 1K$, $R_A + R_B \leq 6.6M$

$C_T \geq 500pF$

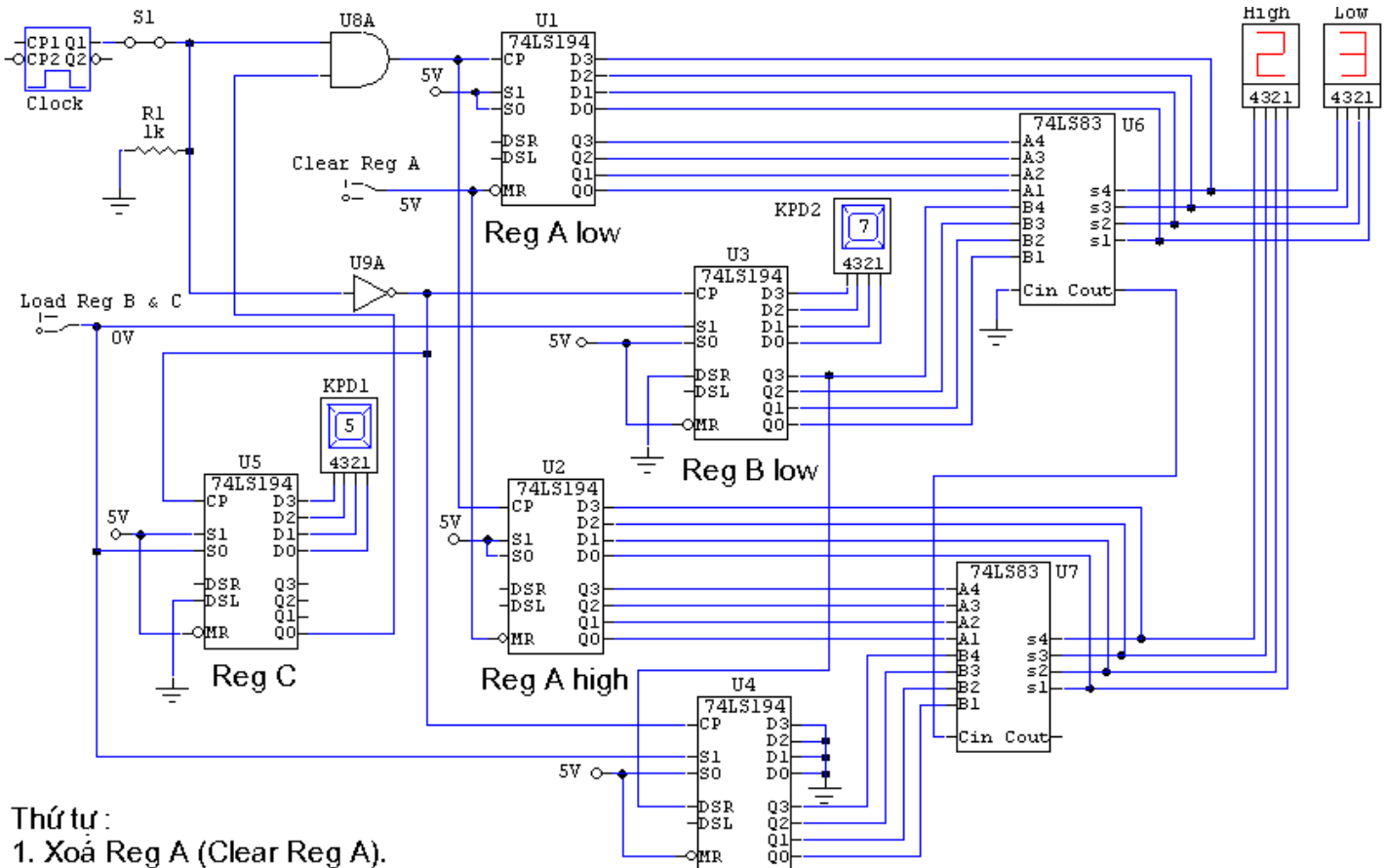


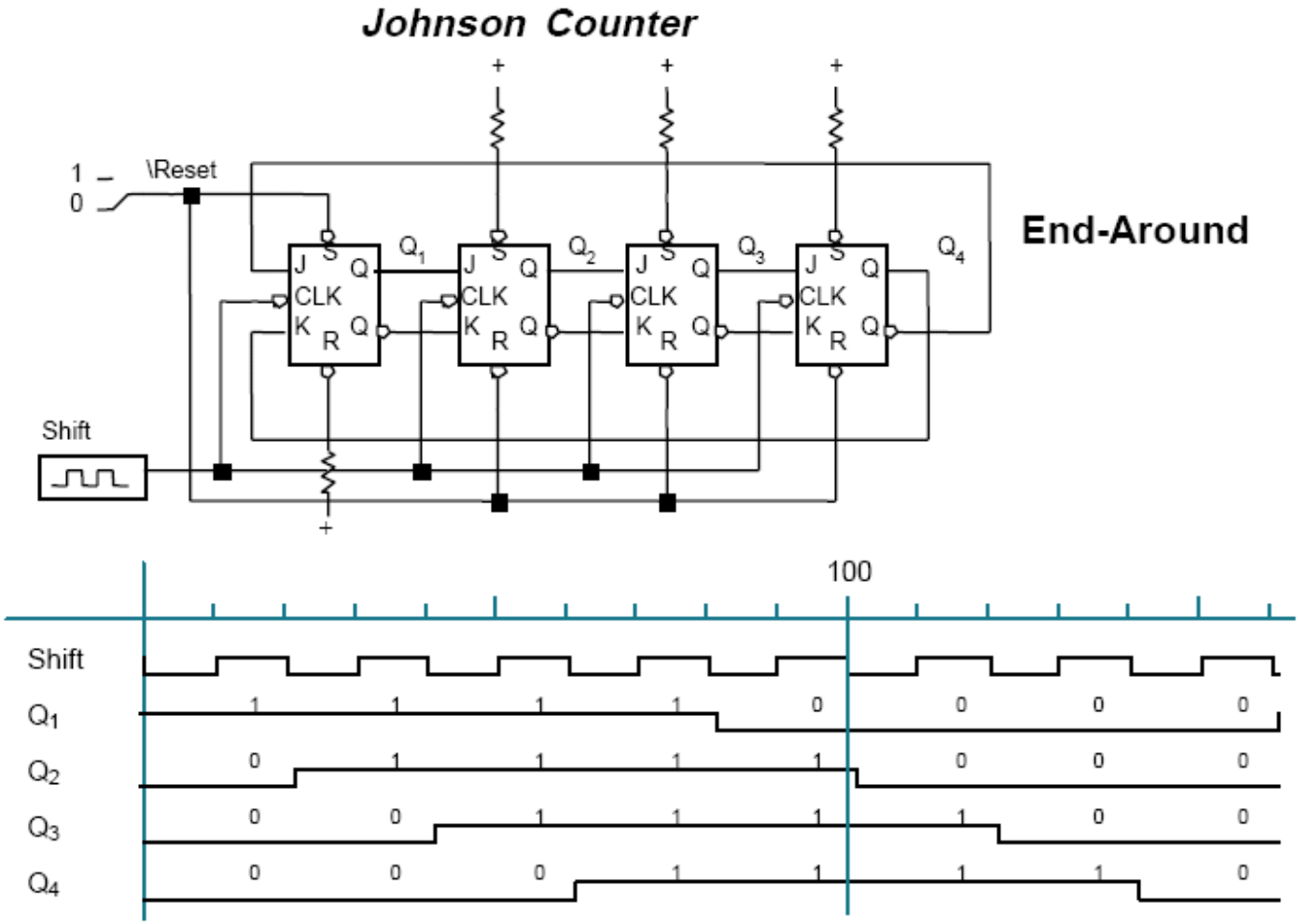


Độ rộng xung One-shot :

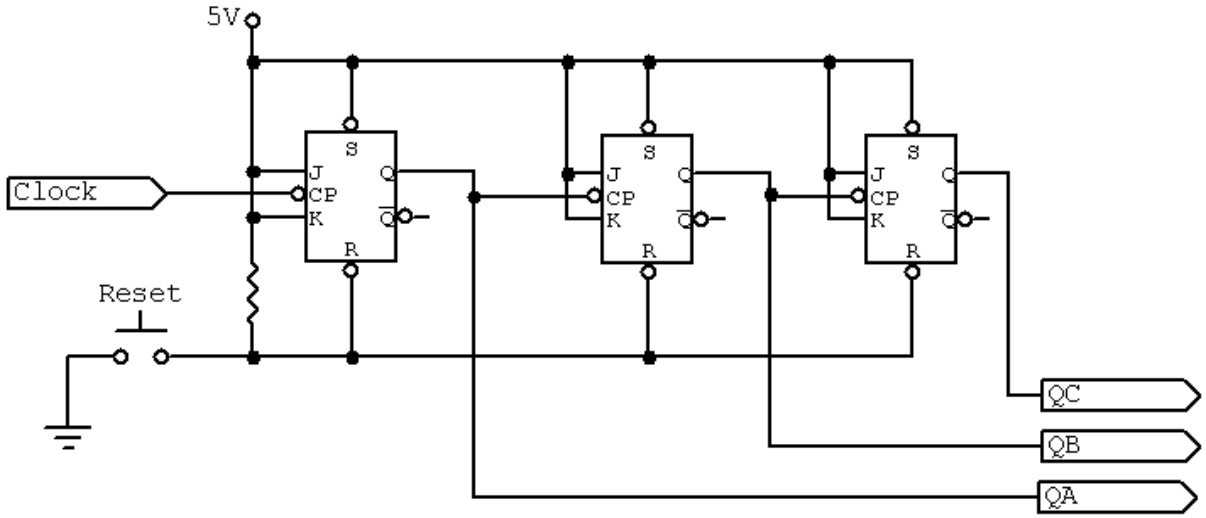
$T= 1.1\ R_A\ C_T$

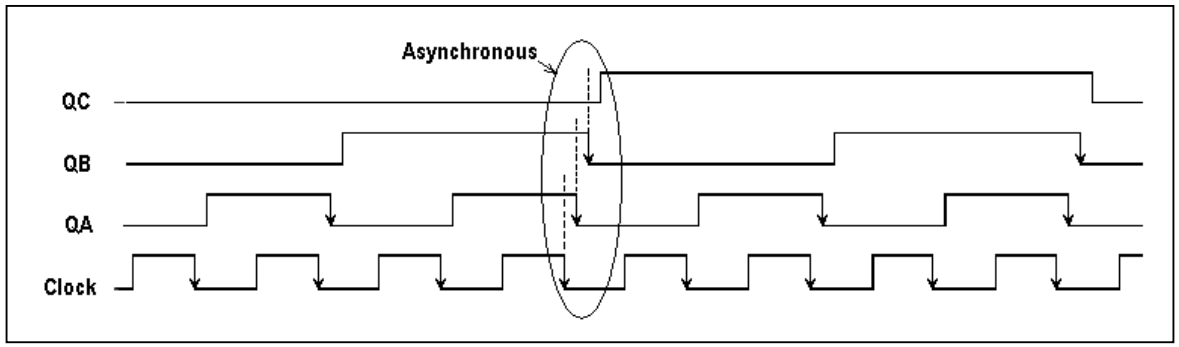
BỘ NHÂN 4 BITS DÙNG THANH GHI DỊCH



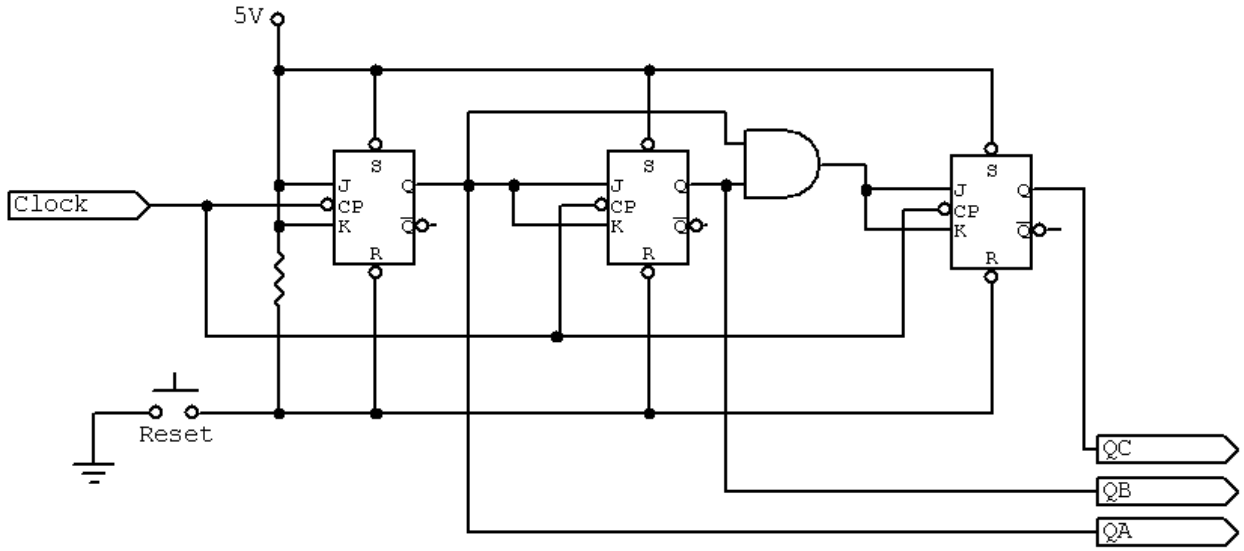

Johnson Counter
1
0
\Reset
Shift
J
CLK
K
S
R
Q
Q_1
Q_2
Q_3
Q_4
End-Around
100
Shift
Q_1
Q_2
Q_3
Q_4

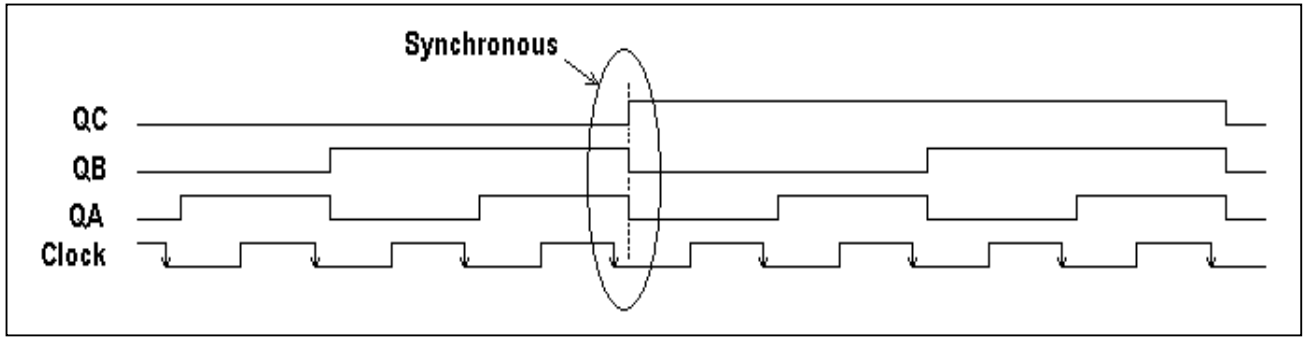
BỘ ĐẾM KHÔNG ĐỒNG BỘ (RIPPLE COUNTER)



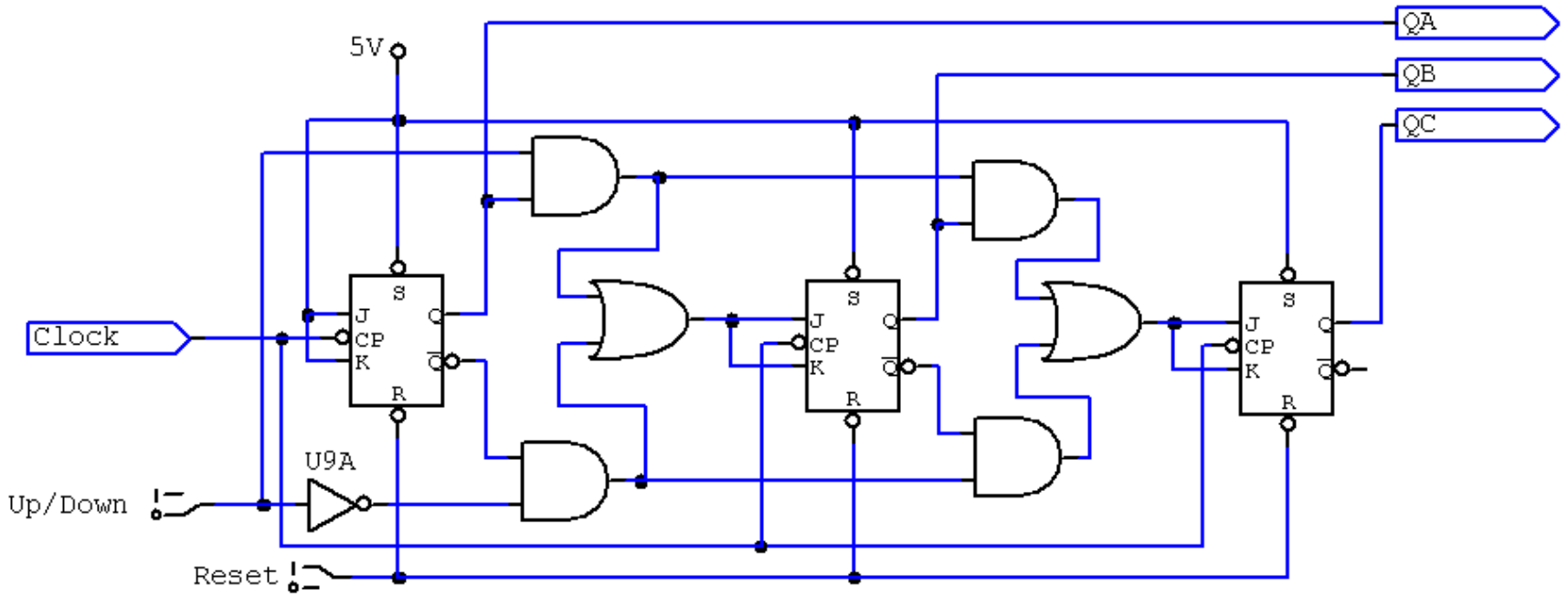


BỘ ĐẾM ĐỒNG BỘ (SYNCHRONOUS COUNTER)

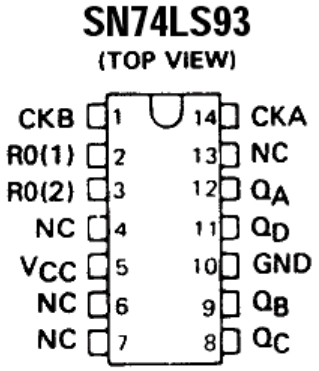




BỘ ĐẾM ĐỒNG BỘ TĂNG GIẢM (UP/DOWN COUNTER)

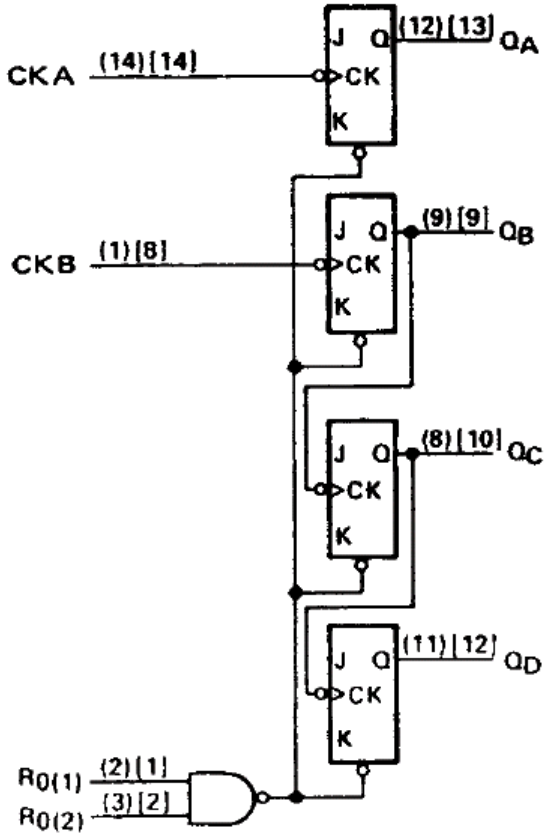


IC 74LS93 - BỘ ĐẾM NHỊ PHÂN 4 BITS KHÔNG ĐỒNG BỘ



RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			



74LS90 Decade and Binary Counters

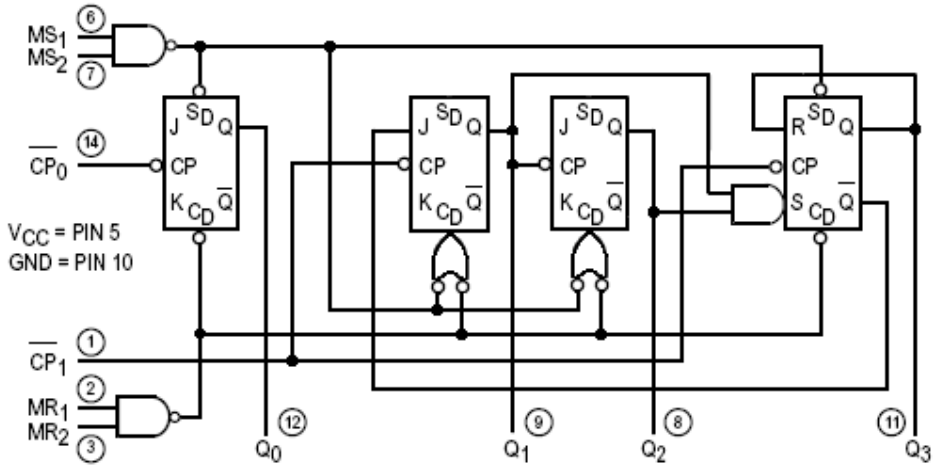
MODE SELECTION

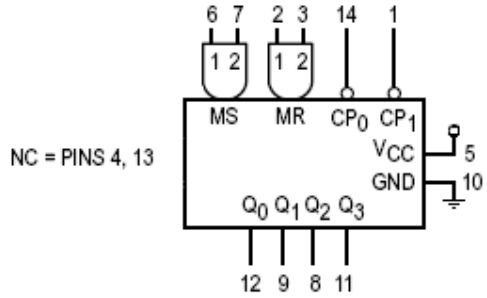
RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

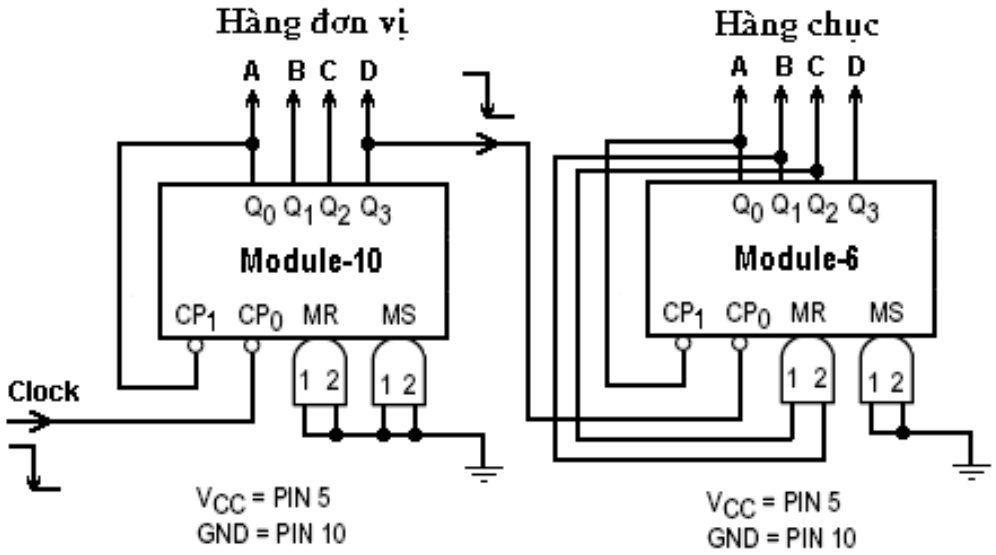


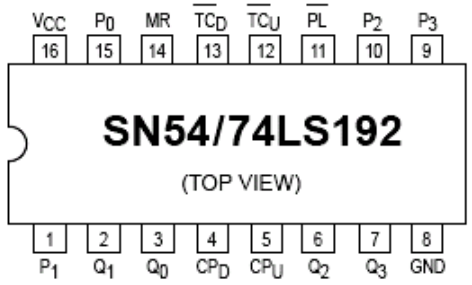


NC = PINS 4, 13

74LS90 TẠO BỘ ĐẾM MODULE-6 VÀ MODULE-10

(BỘ ĐẾM 60 DÙNG CHO MẠCH ĐỒNG HỒ ĐIỆN TỬ)



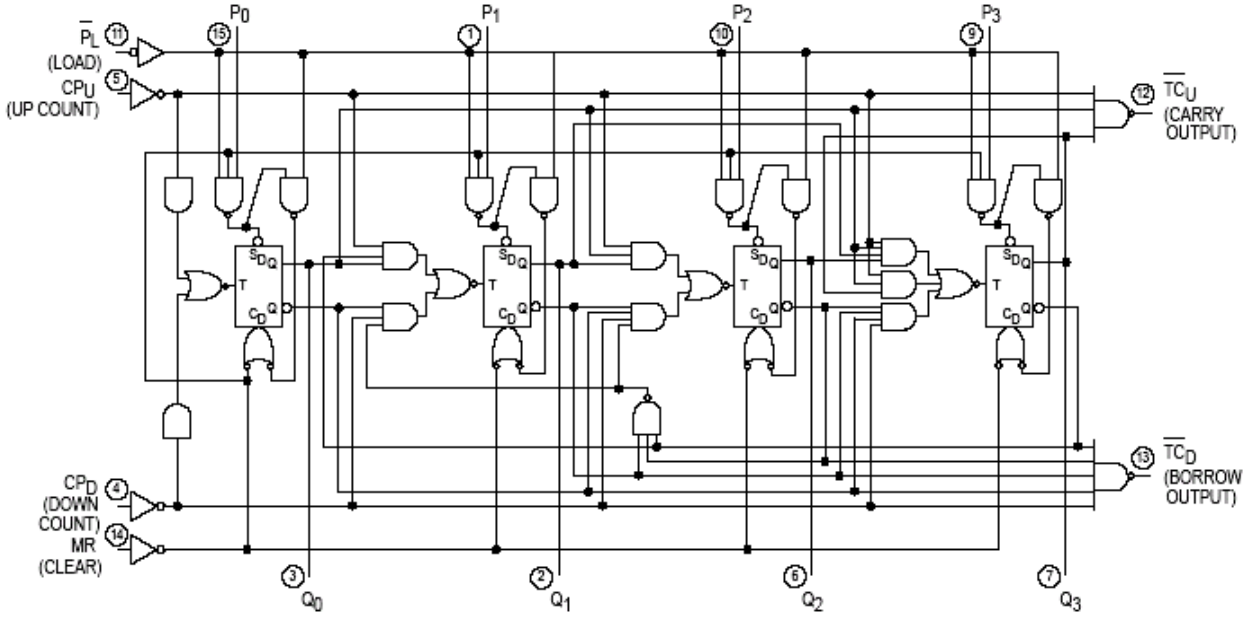


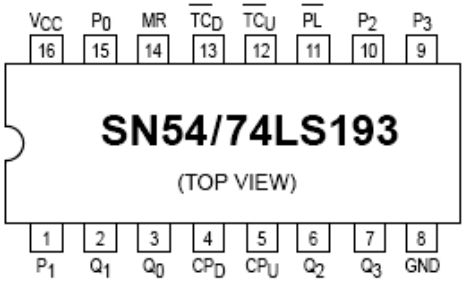
PRESETTABLE BCD/DECADE UP/DOWN COUNTER

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

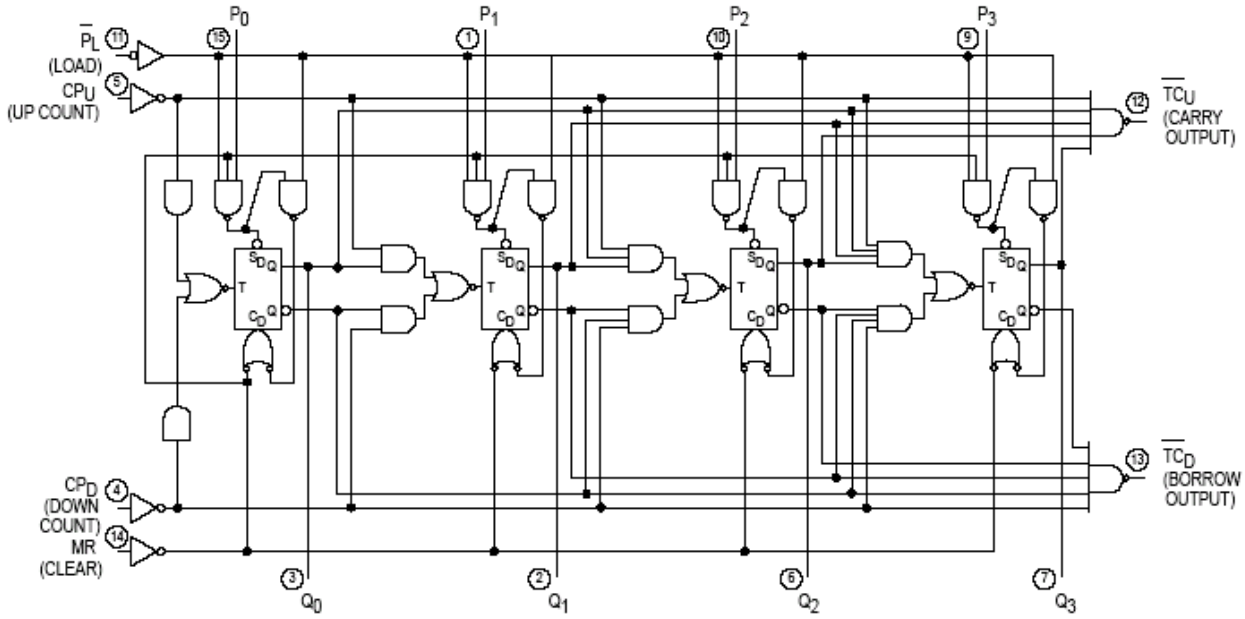
LOGIC DIAGRAMS



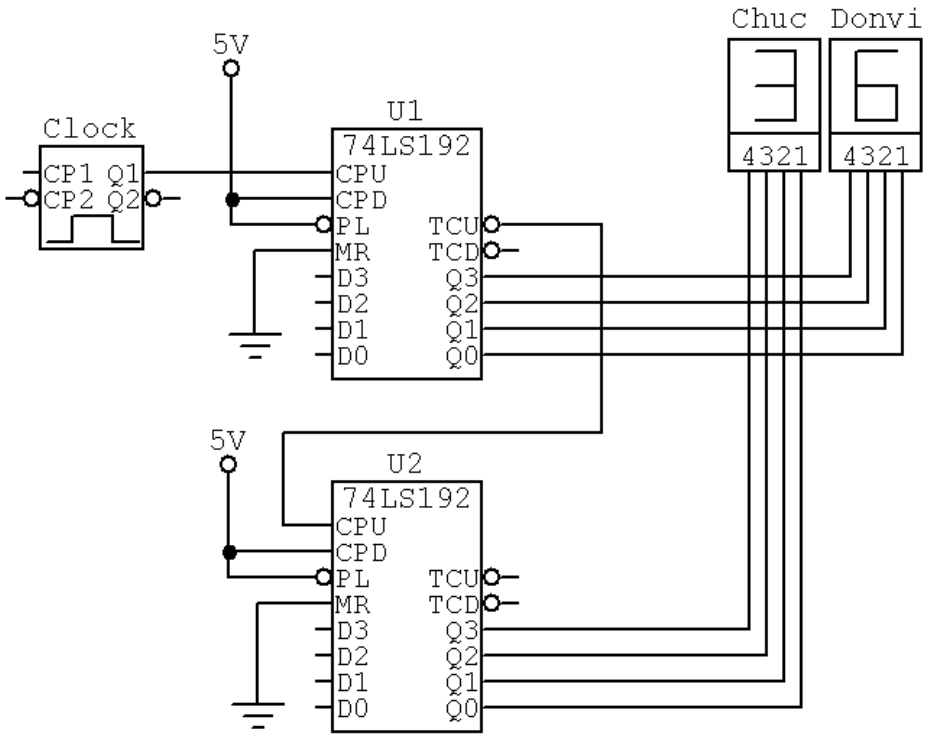


PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

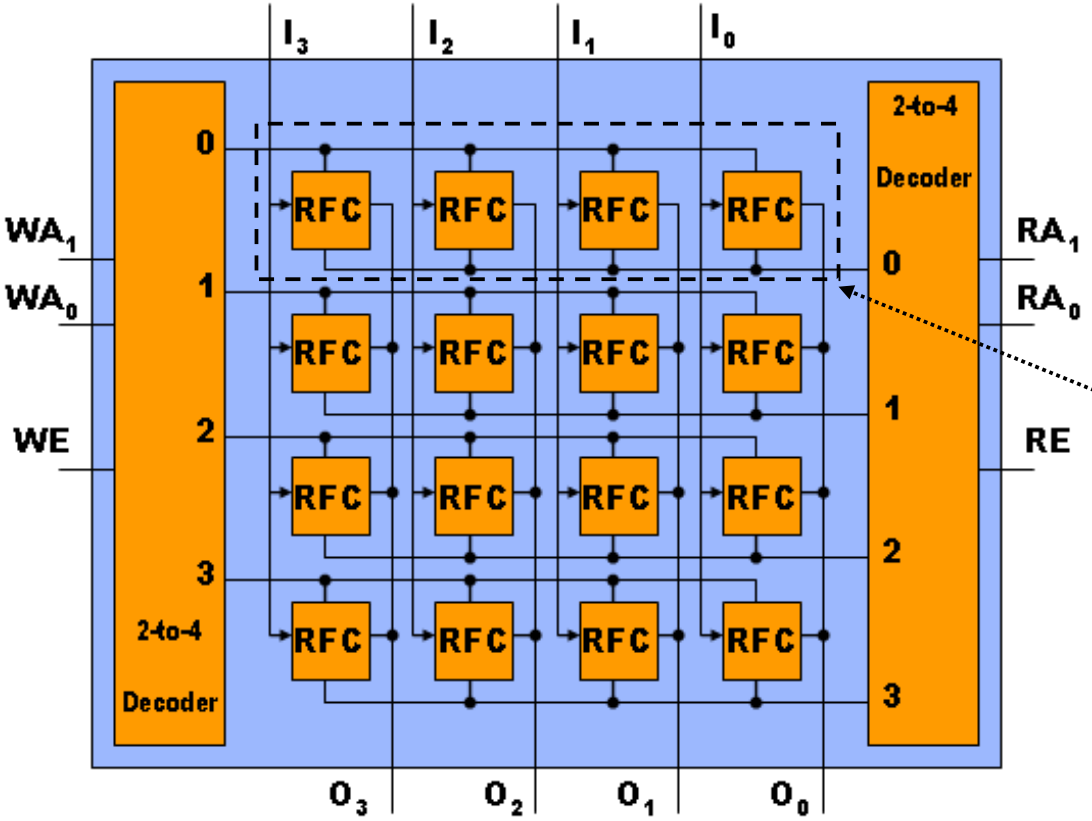
LOGIC DIAGRAMS



GHÉP NỐI MỞ RỘNG BỘ ĐẾM



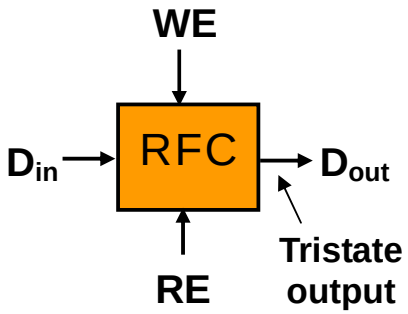
REGISTER FILES



Register Files with
4 x Register 4 bits

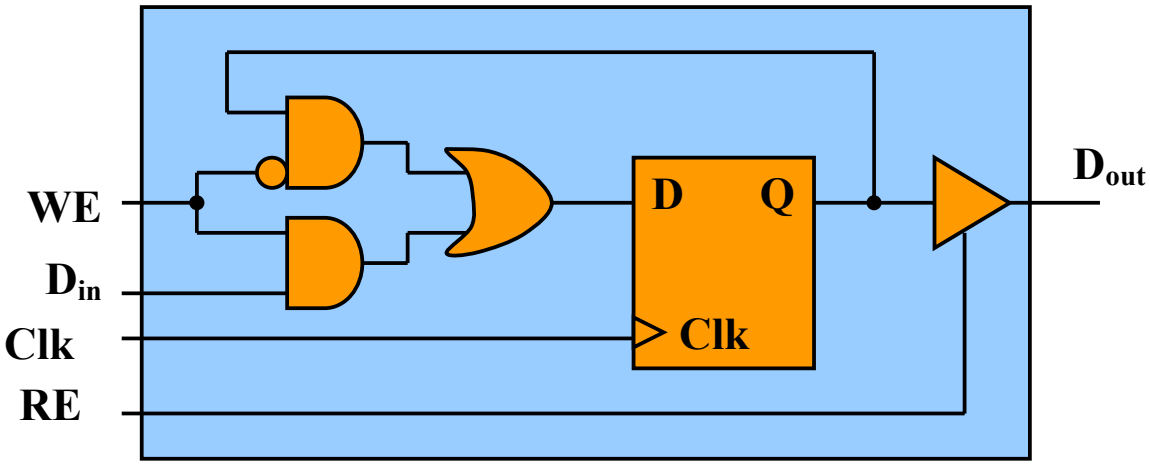
A register files is an array of processor registers in a CPU

Register **0** in the register files

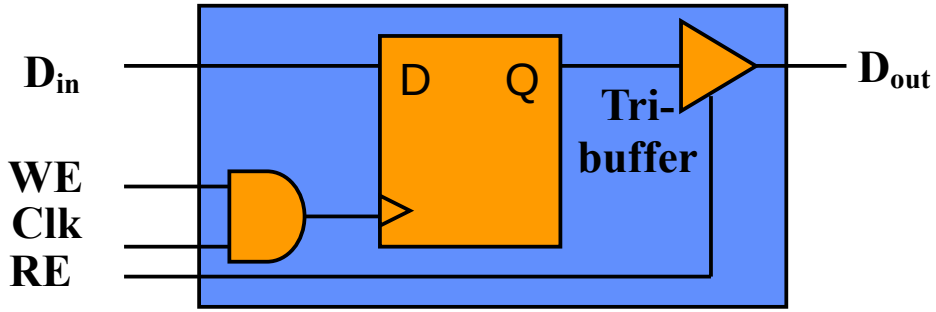


1 Register File Cell

IMPLEMENTATION OF REGISTER FILE CELL



Hoặc



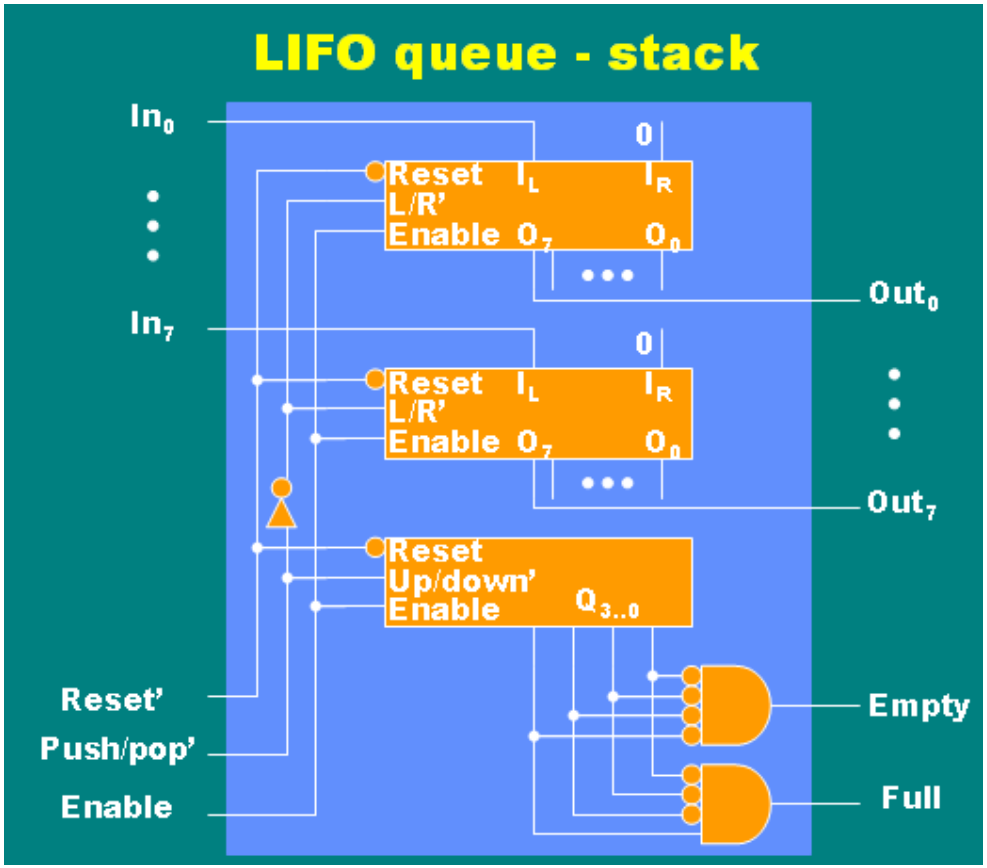
Thiết kế bộ nhớ hàng đợi (memory queue)

→ LIFO (last in first out)

→ FIFO (first in first out)

Dùng thanh ghi dịch, bộ đếm, Mux, SRAM

LIFO – LAST IN FIRST OUT



FIFO – FIRST IN FIRST OUT