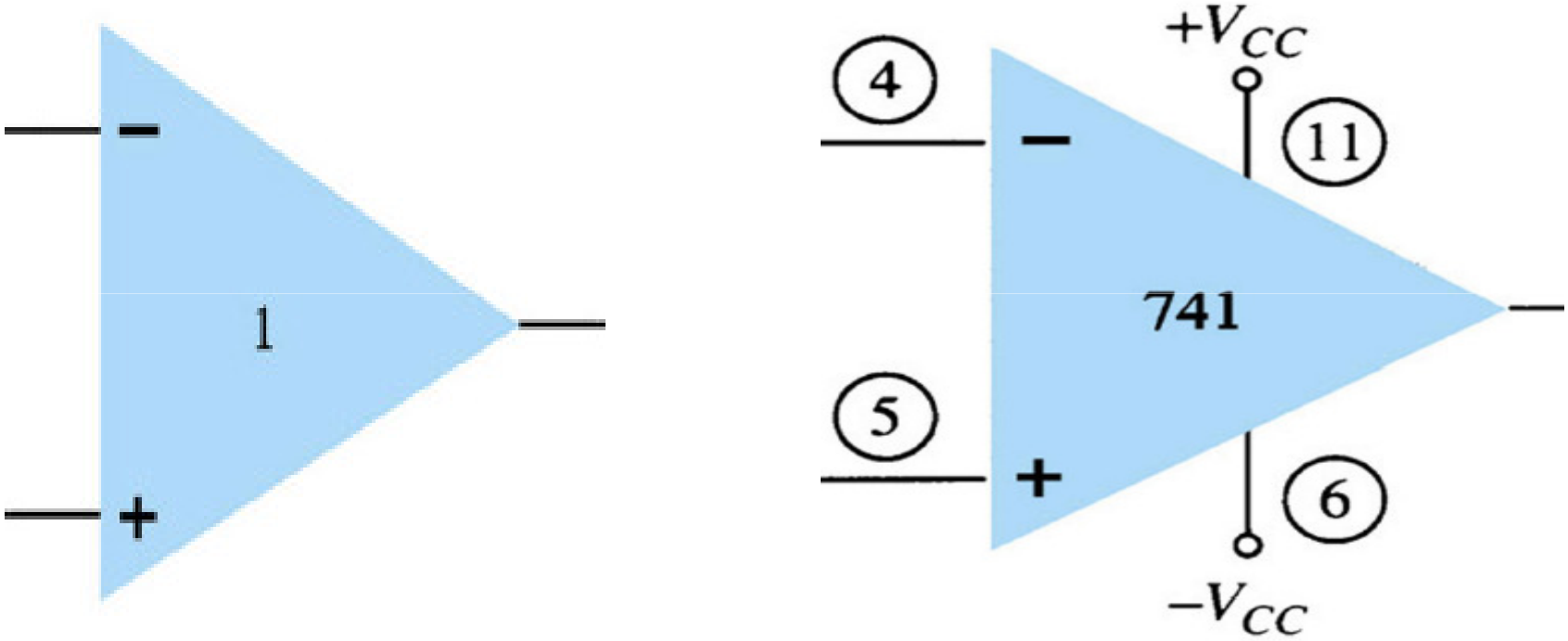
CHƯƠNG 9:
KHUẾCH ĐẠI THUẬT TOÁN

Contents

- Symbol
- Example
- Characteristics
- Structure
- Operation
- Applications
- µp 741

Symbol

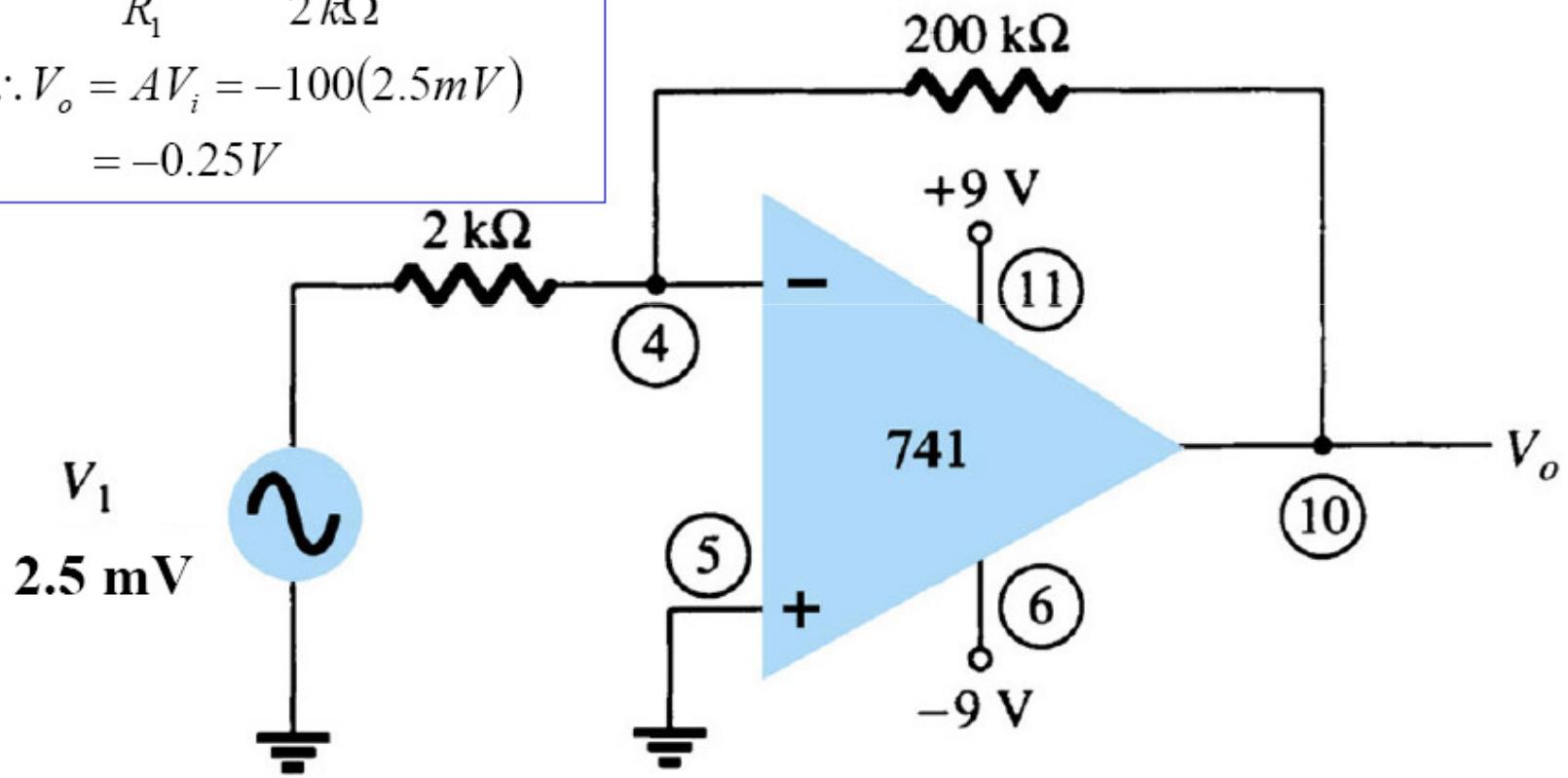


Example

$$A = -\frac{R_f}{R_1} = -\frac{200\,k\Omega}{2\,k\Omega} = -100$$

$$\therefore V_o = AV_i = -100(2.5mV)$$

$$= -0.25V$$



Characteristics

- Characters of circuits depend on outside circuit structure, not the opamp itself
- Gain A_V: very high, ideally ∞
- Zin: very large, ideally ∞
- Zout: very small, ideally 0
- Current entering the amp at either terminal: extremely small, ideally 0
- Voltage out (when voltages into each other are equal): small, ideally 0
- Bandwidth: broad, ideally infinite

Characteristics

- Input: 2 inputs (positive and negative)
  - Single-ended input: 1 input to signal source, 1 input to ground
  - Double-ended input: 2 different signal sources or 1 signal source apply between 2 inputs
- Output: 1 or 2 outputs, typically 1 output
- Mode gain:
  - Differential-mode gain A_{dm} - large
  - Common-mode gain A_{cm} - small
  - Common-mode rejection ratio CMRR=G=A_{dm}/A_{cm}, usually about 10^3-10^5

Structure

- Requirement:
  - Gain: large
  - Offset: small
  - Currents: small
  - Input impedance: large
  - Output impedance: small
  - Input: symmetric

Structure

- Input stage
- Intermediate stage
- Level shifting stage
- Output stage

- Example: 741 – at the end of chapter

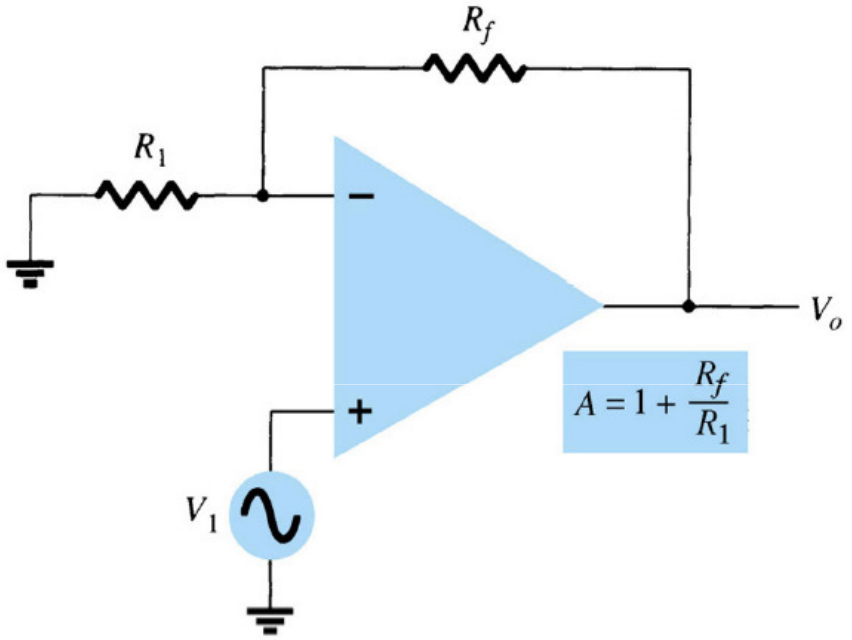
Applications

- Basic and advance applications
- Basic applications:
  - Inverting, non-inverting amplifier
  - Uni-gain circuit
  - Addition and subtraction circuits
  - Integration and differential circuits
  - Multi-stages circuit

Applications

- Advance applications
  - Current-controlled voltage source
  - Voltage-controlled current source
  - DC voltmeter
  - AC voltmeter
  - Driver circuit
  - Active filters
  - NIC
  - .etc.

Non-inverting fixed-gain amplifier



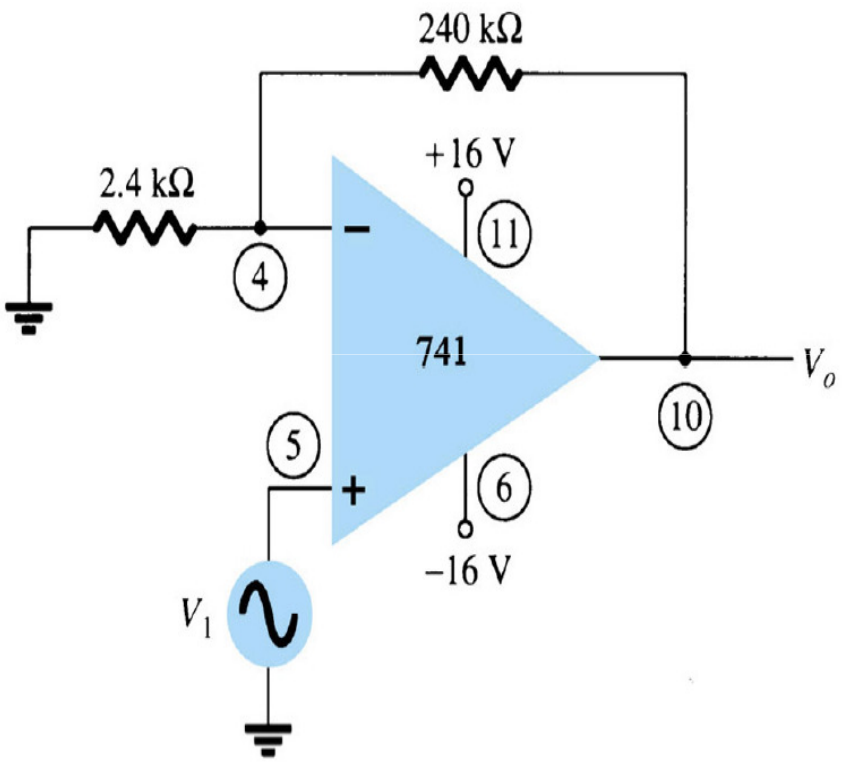
Prove:

- V- = V+ = V_1
- I- = I+ = 0

=>$I_{R1} = I_{rf} = V_1/R_1$

=>$A = 1+R_f/R_1$

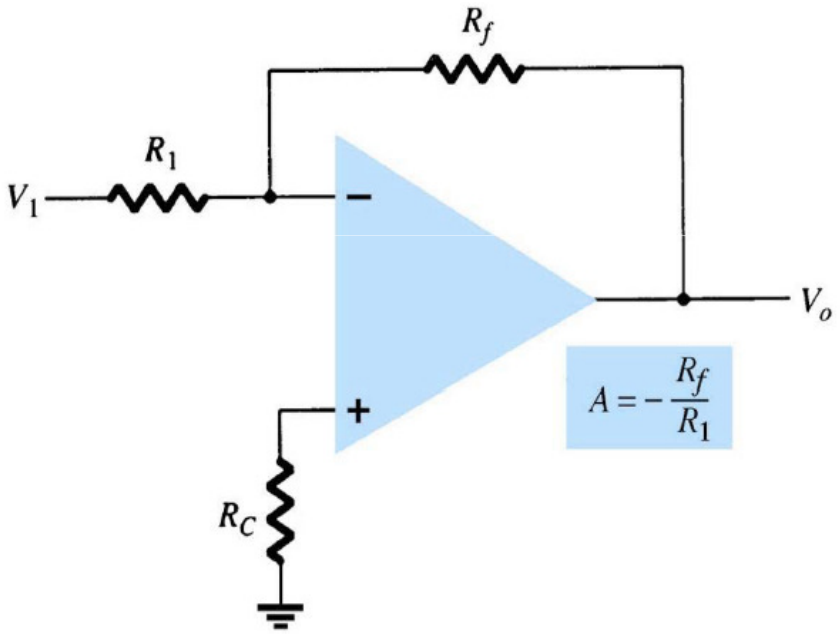
Non-inverting fixed-gain amplifier



$A = 1+R_f/R_1=101$

$V_o=101V_i$

Inverting fixed-gain amplifier



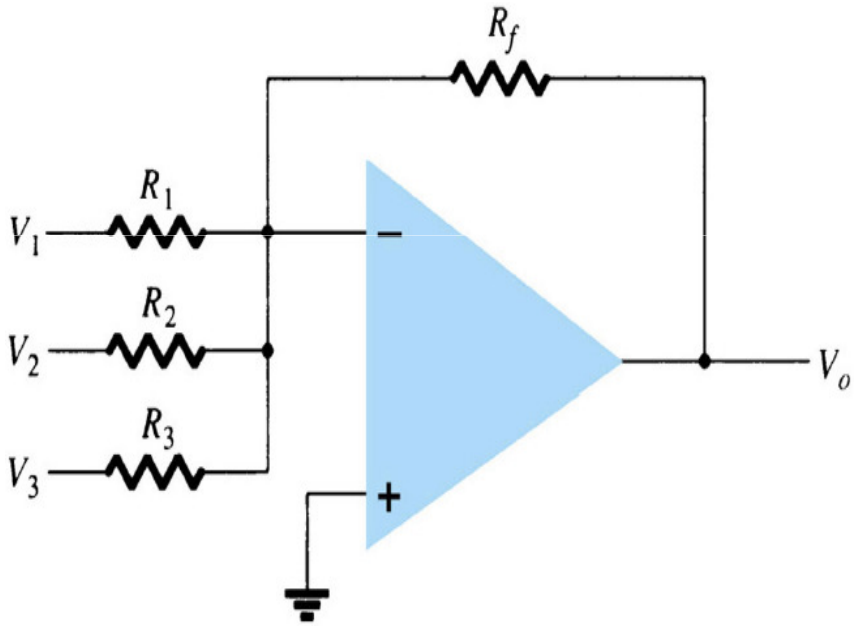
Prove:

- V- = V+ = 0
- I- = I+ = 0

$=>I_{R1} = I_{rf} = V_1/R_1$

$=>A = -R_f/R_1$

Voltage addition

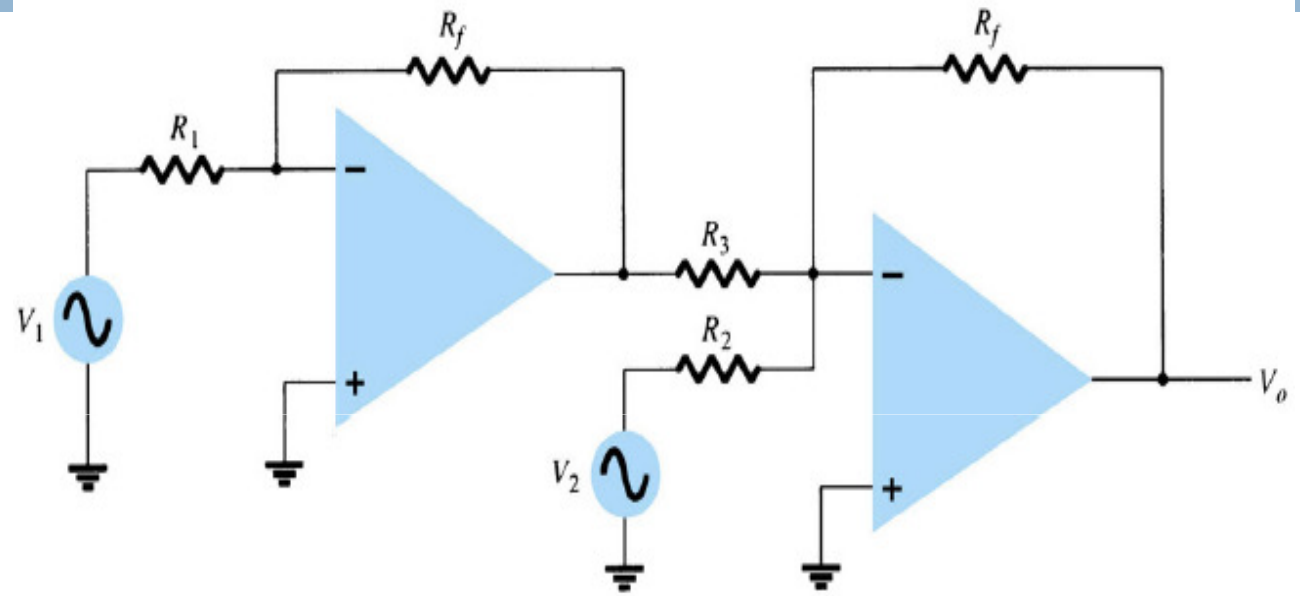


$V_o = -V_1R_f/R_1 - V_2R_f/R_2 - V_3R_f/R_3$

If $V_1 = V_2 = V_3$ then:

$A = -R_f/R_1 - R_f/R_2 - R_f/R_3$

Voltage subtraction

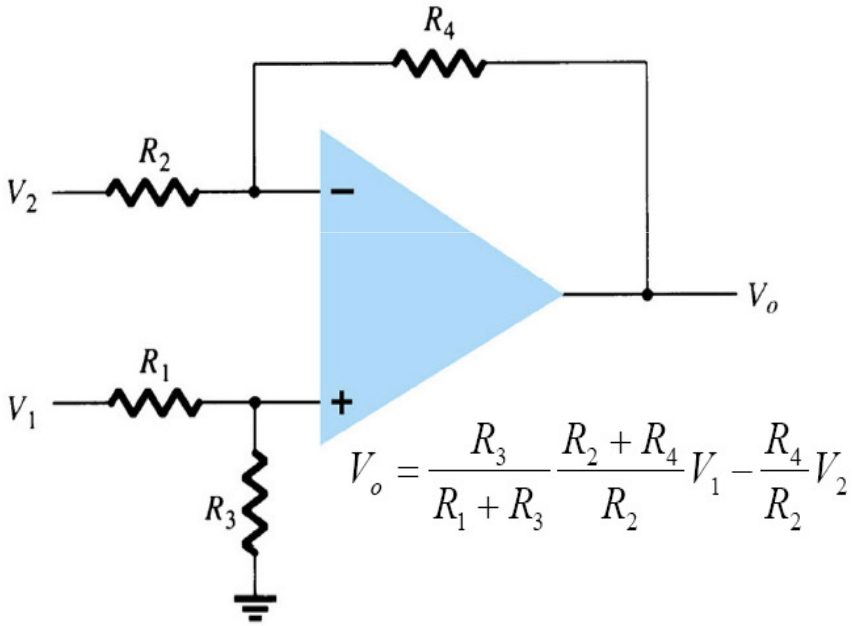


$V_{out1} = -R_f/R_1 V_1$

$V_{out} = -R_f/R_2 V_2 - R_f/R_2 V_{out1} = -R_f/R_2 V_2 + R_f/R_2 V_1$

$= -R_f/R_2 (V_1 - V_2)$

Voltage subtraction with 1 amp



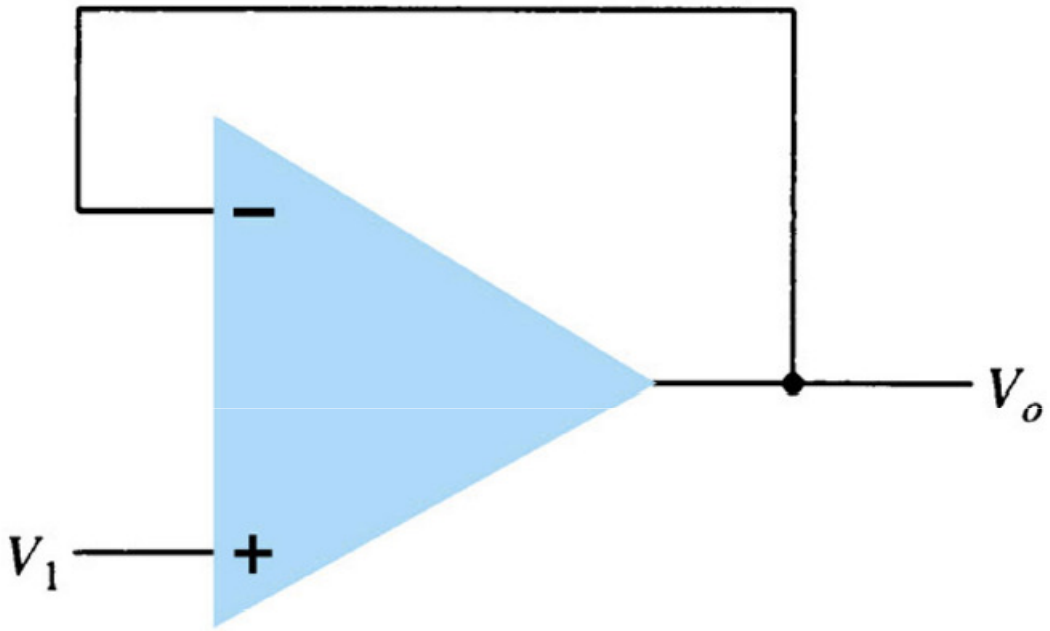
Prove:

- $V- = V+ = V_1 * R_3/(R_1+R_3)$
- $I- = I+ = 0$

$=> I_{R2} = I_{R4} = (V_2 - V_1 * R_3/(R_1+R_3))/R_2$

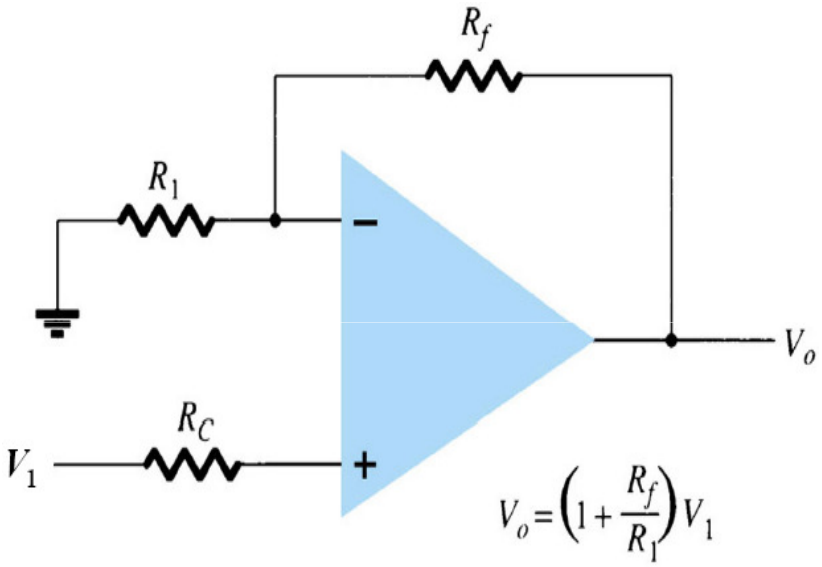
$=> Vo = V_1 * R_3/(R_1+R_3) * (R_2+R_4)/R_2 - V_2 * R_4/R_2$

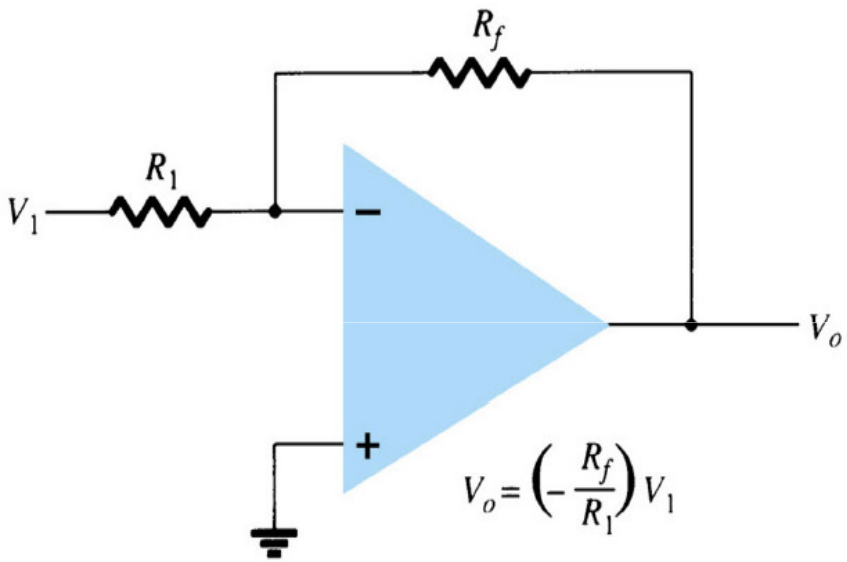
Uni-gain (buffer) amplifier



- Provide required input and output resistant stage
- Provide multiple identical output signals

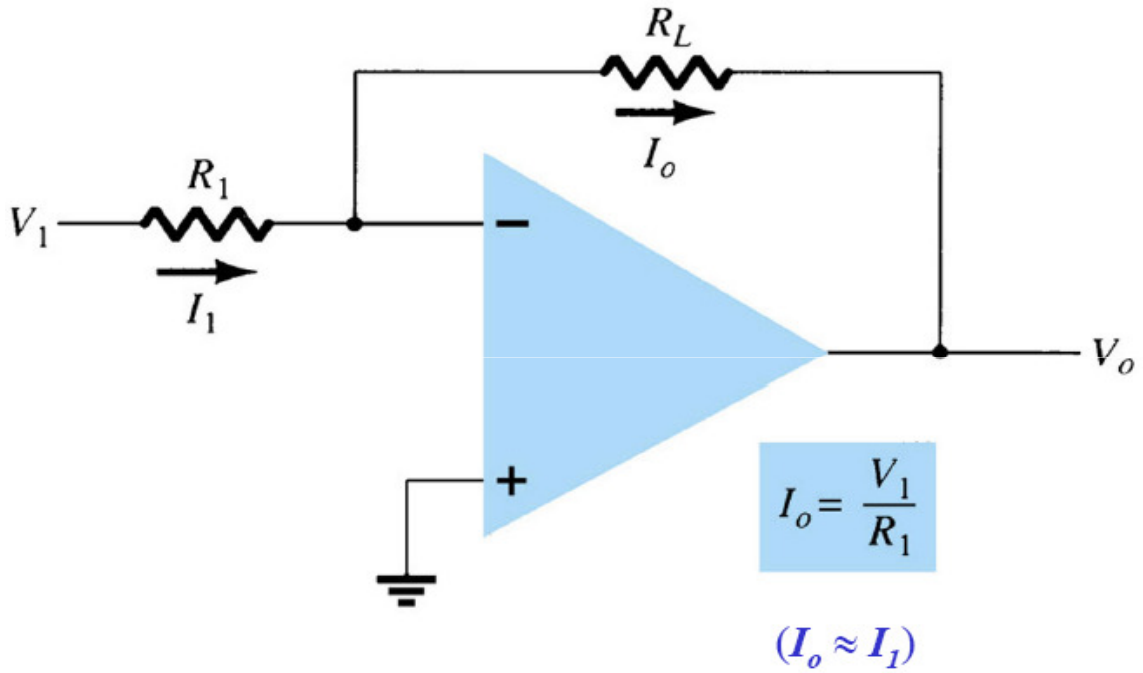
Voltage-controlled voltage source





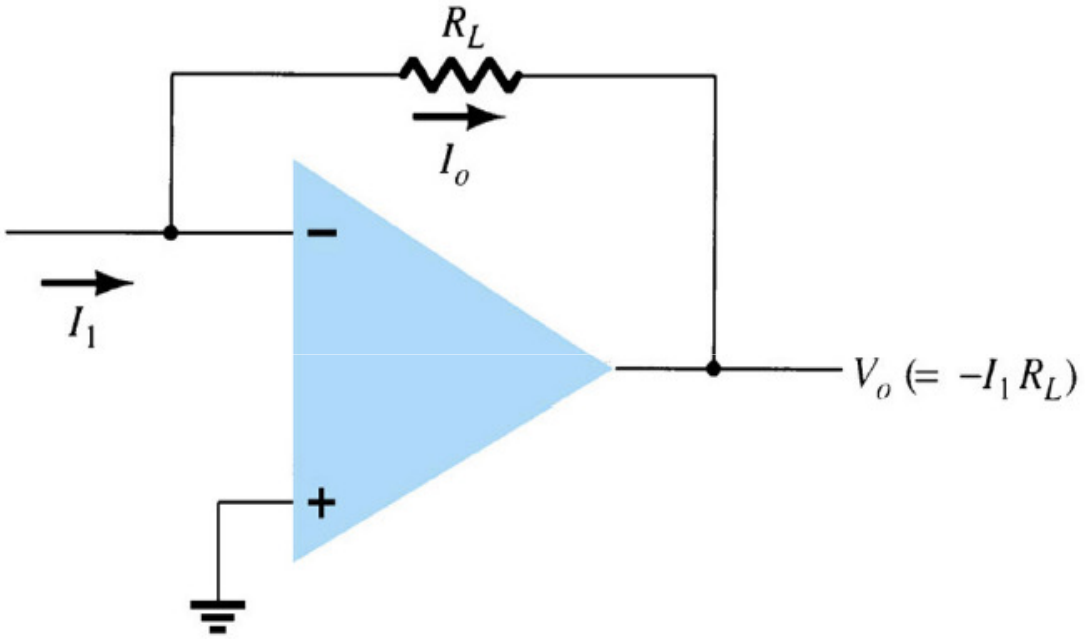
- $V_o=(1+R_f/R_1)V_1$
- $V_o=(-R_f/R_1)V_1$

Voltage-controlled current source



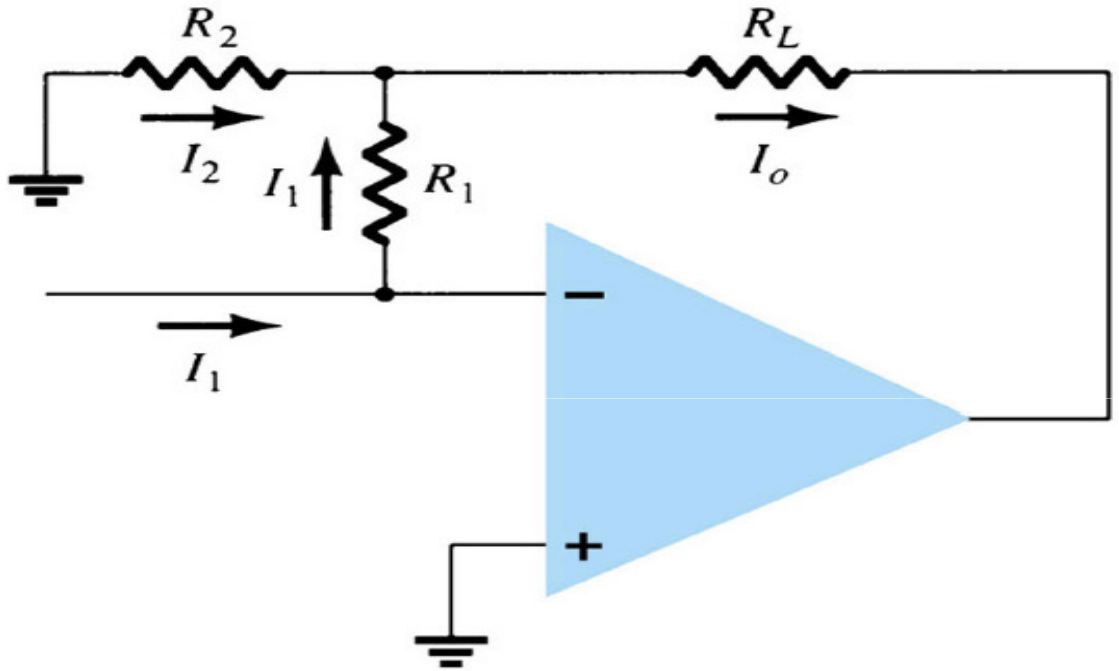
- $I_o = V_1/R_1$

Current-controlled voltage source



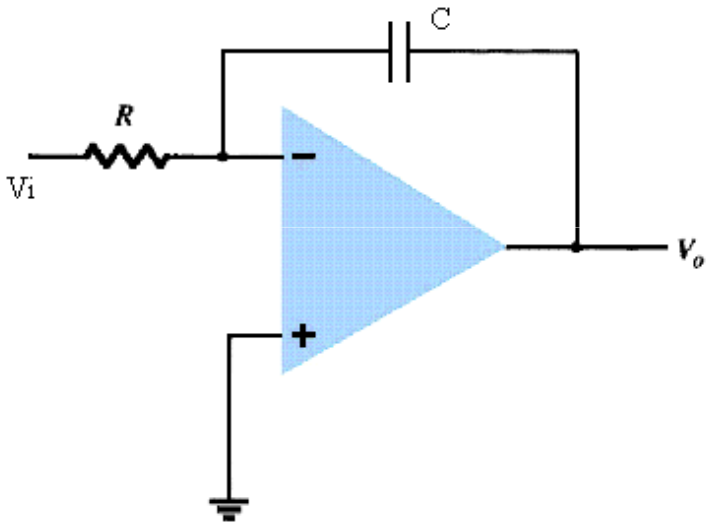
- $V_o = -I_1 R_L$

Current-controlled current source



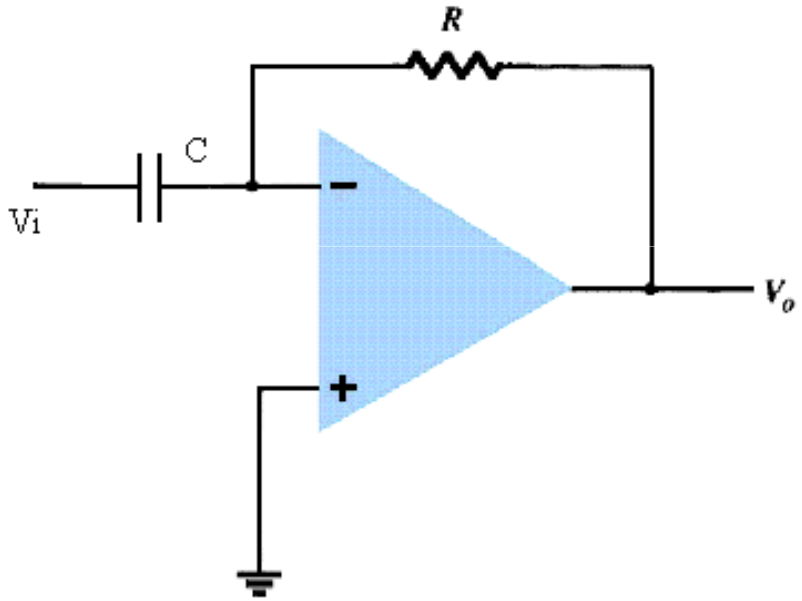
- $I_o=I_1(R_2+R_1)/R_2$

Integration circuit



- $V_o=(V_i/RC)_0 f^T V_i(t)dt+V_{out(t=0)}$

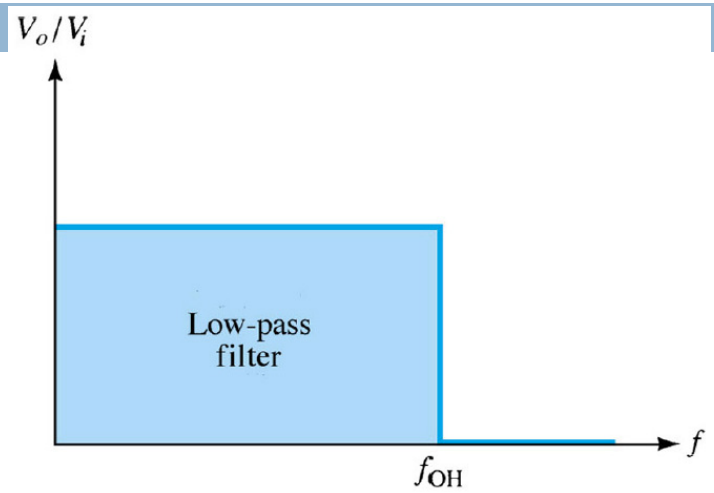
Differential circuit

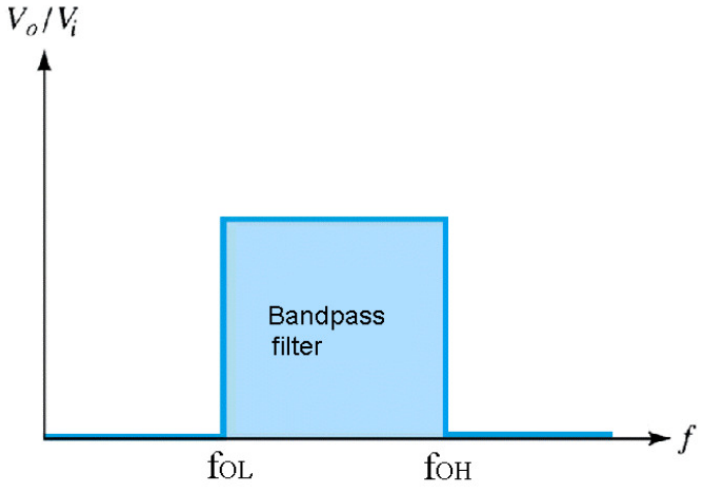


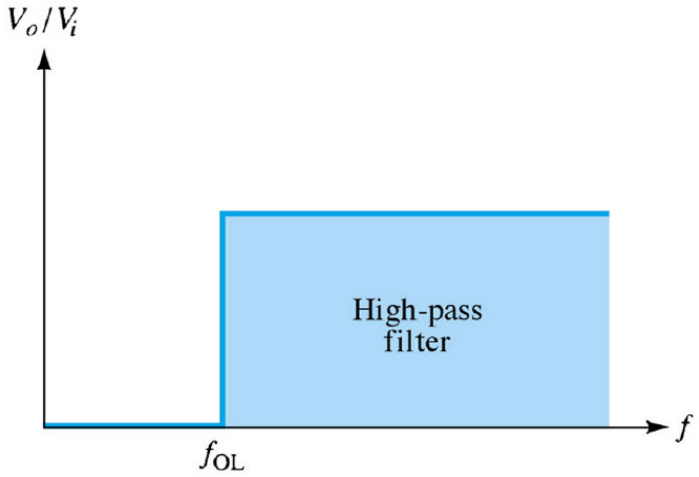
- $V_o = -RC\, dV_i/dt$

Filter

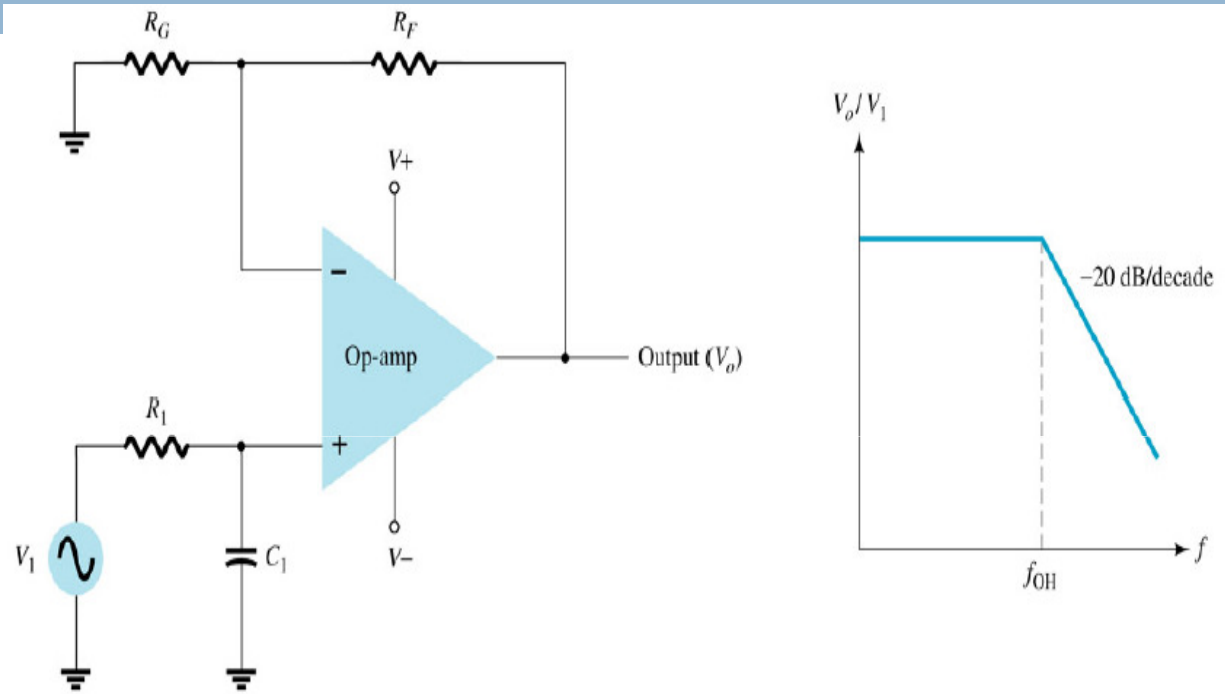
- Low pass filter
- High pass filter
- Band pass filter





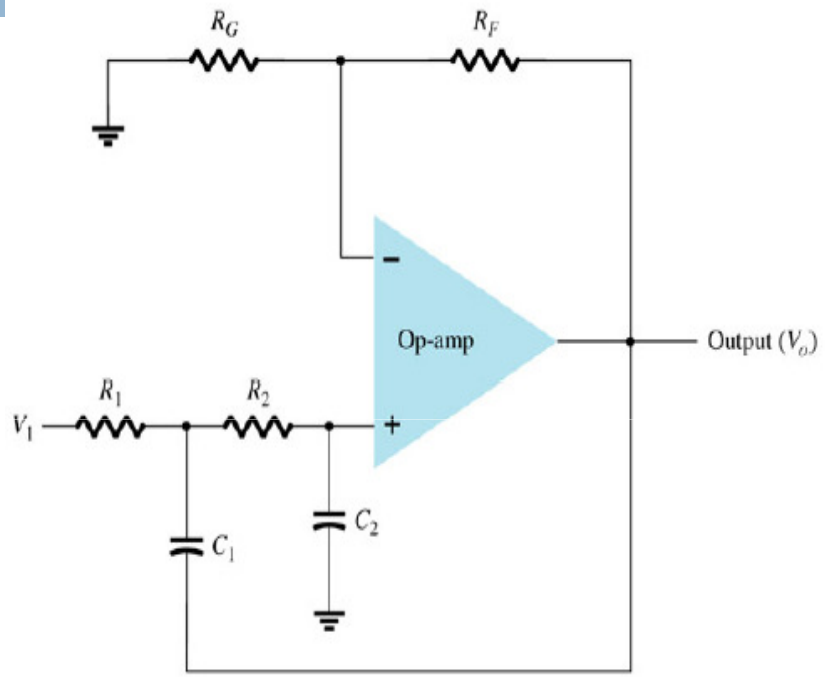


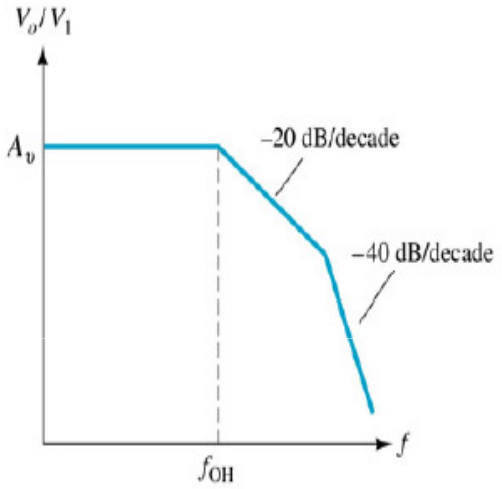
1st order low pass filter



- Cutoff frequency: $f_{OH}=1/(2\pi R_1 C_1)$
- Voltage gain below cutoff freq: $A_v=1+R_f/R_G$

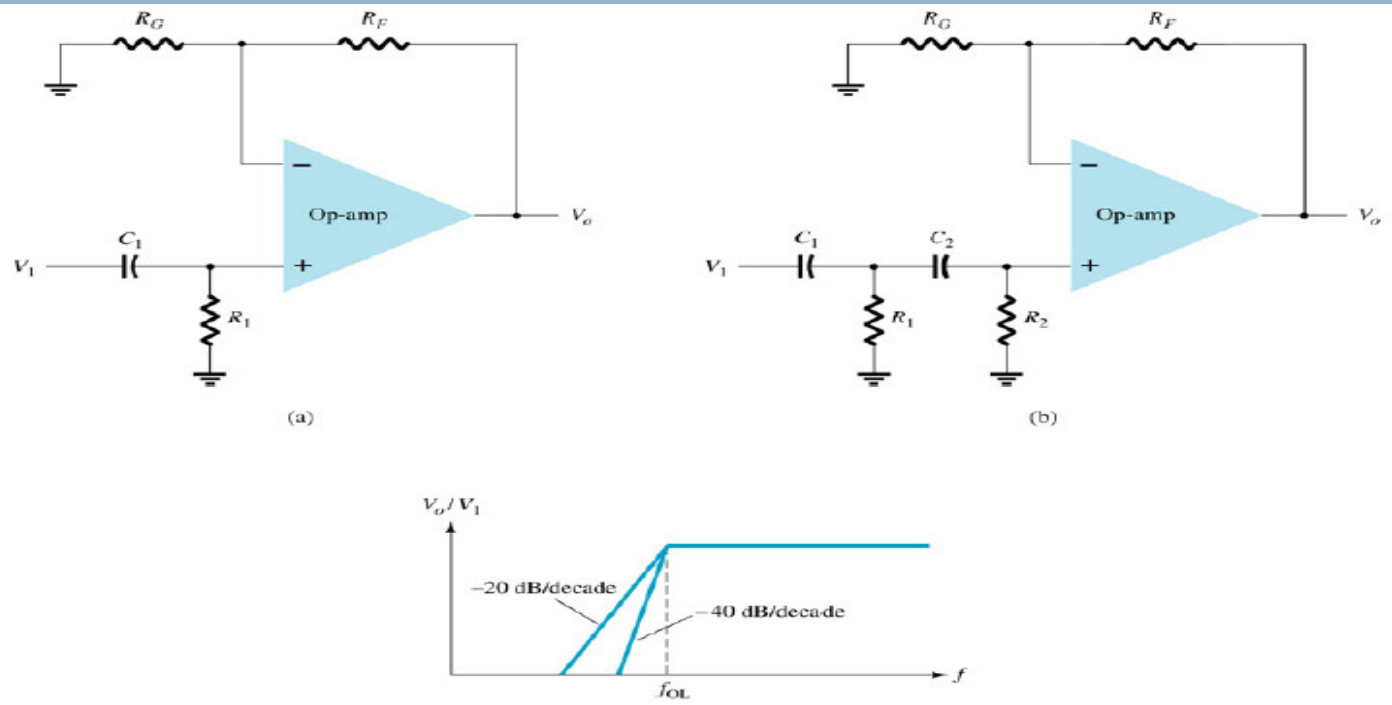
2nd order low pass filter





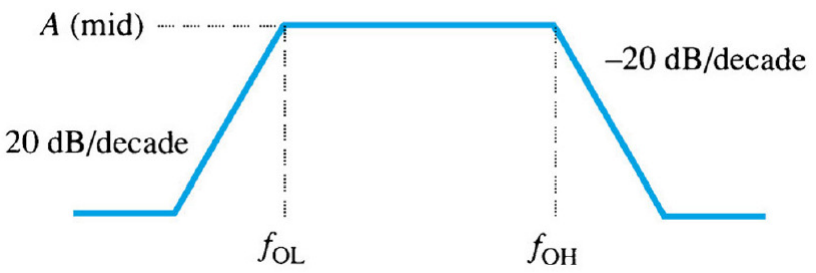
- Cutoff frequency: $f_{OH}=1/(2\pi R_1 C_1)$
- Voltage gain below cutoff freq: $A_v=1+R_f/R_G$

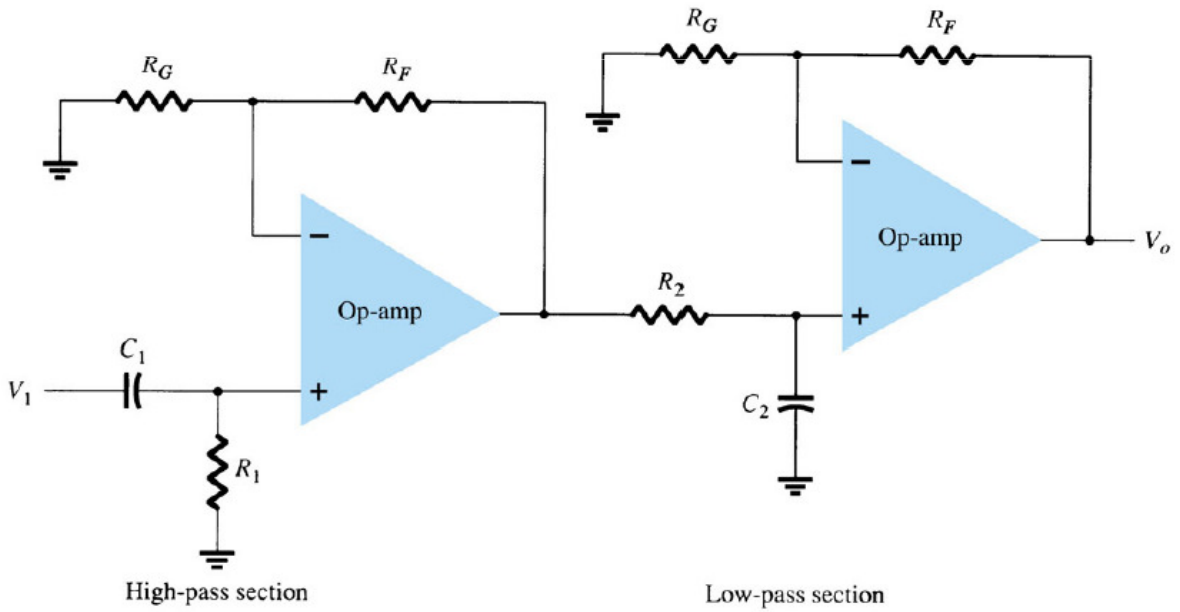
1st and 2nd order high pass filter



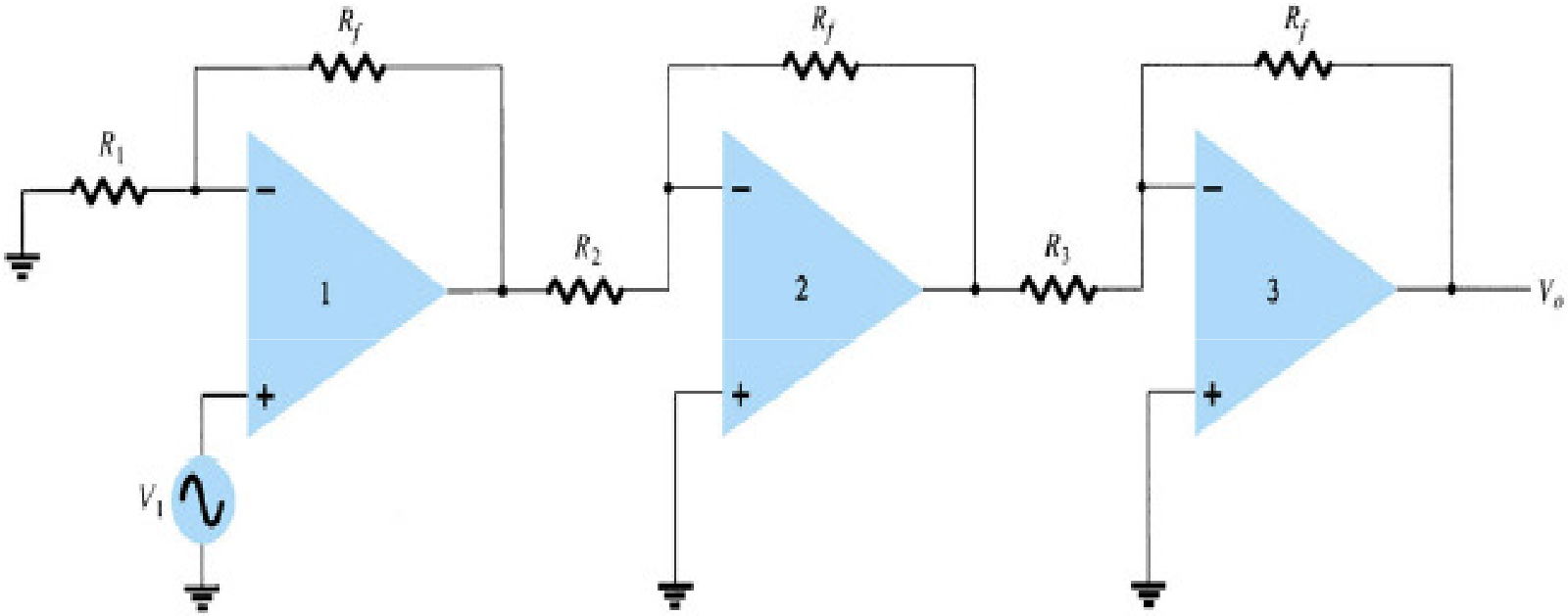
- Cutoff frequency: $f_{OL}=1/(2\pi R_1 C_1)$
- Voltage gain above cutoff freq: $A_v=1+R_f/R_G$

Band pass filter



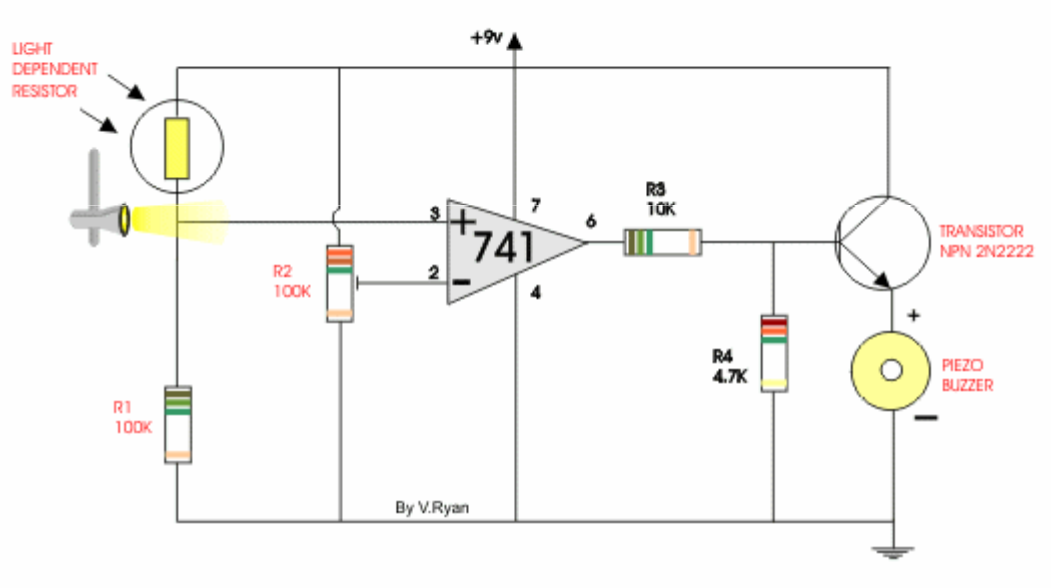


Multi-stages gain



$A = A_1 * A_2 * A_3$

741 application-Light activated alerter



12V battery monitor

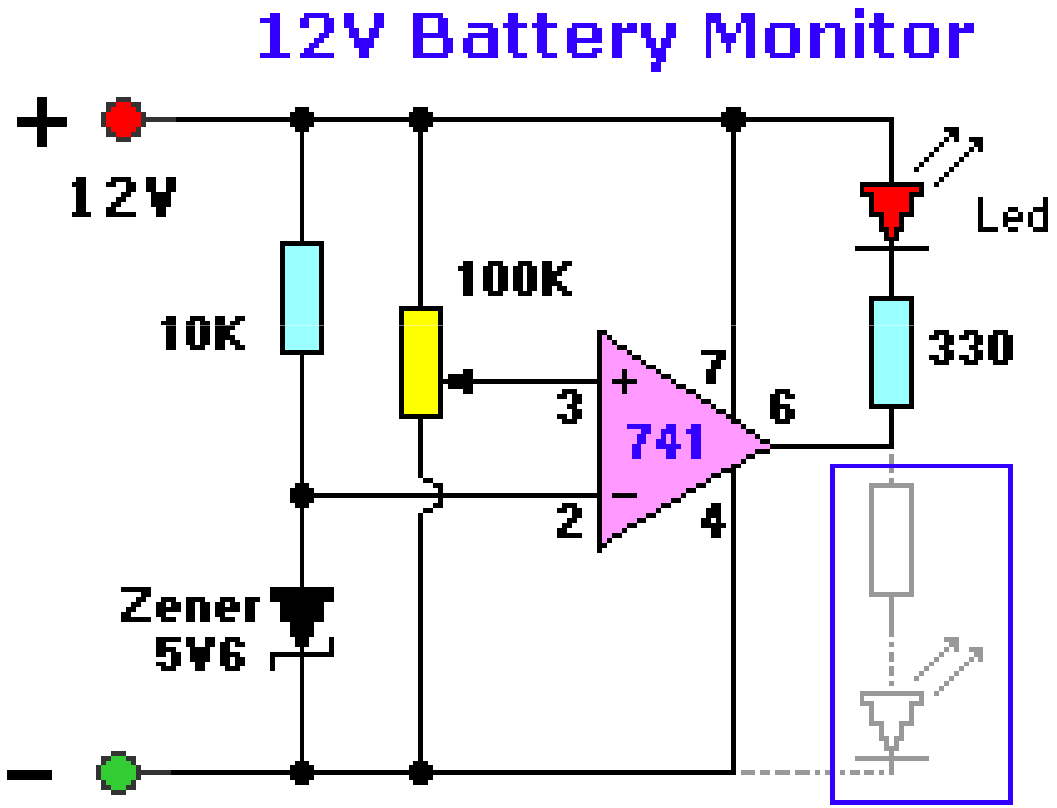


Fig. 14

Homework

- Chapter 14: 1, 4, 9, 10, 12, 15, 17, 18
- Chapter 15: 1, 6, 8, 11, 14, 16, 17

OpAmp 741

- Maximum ratings
- Inside structure

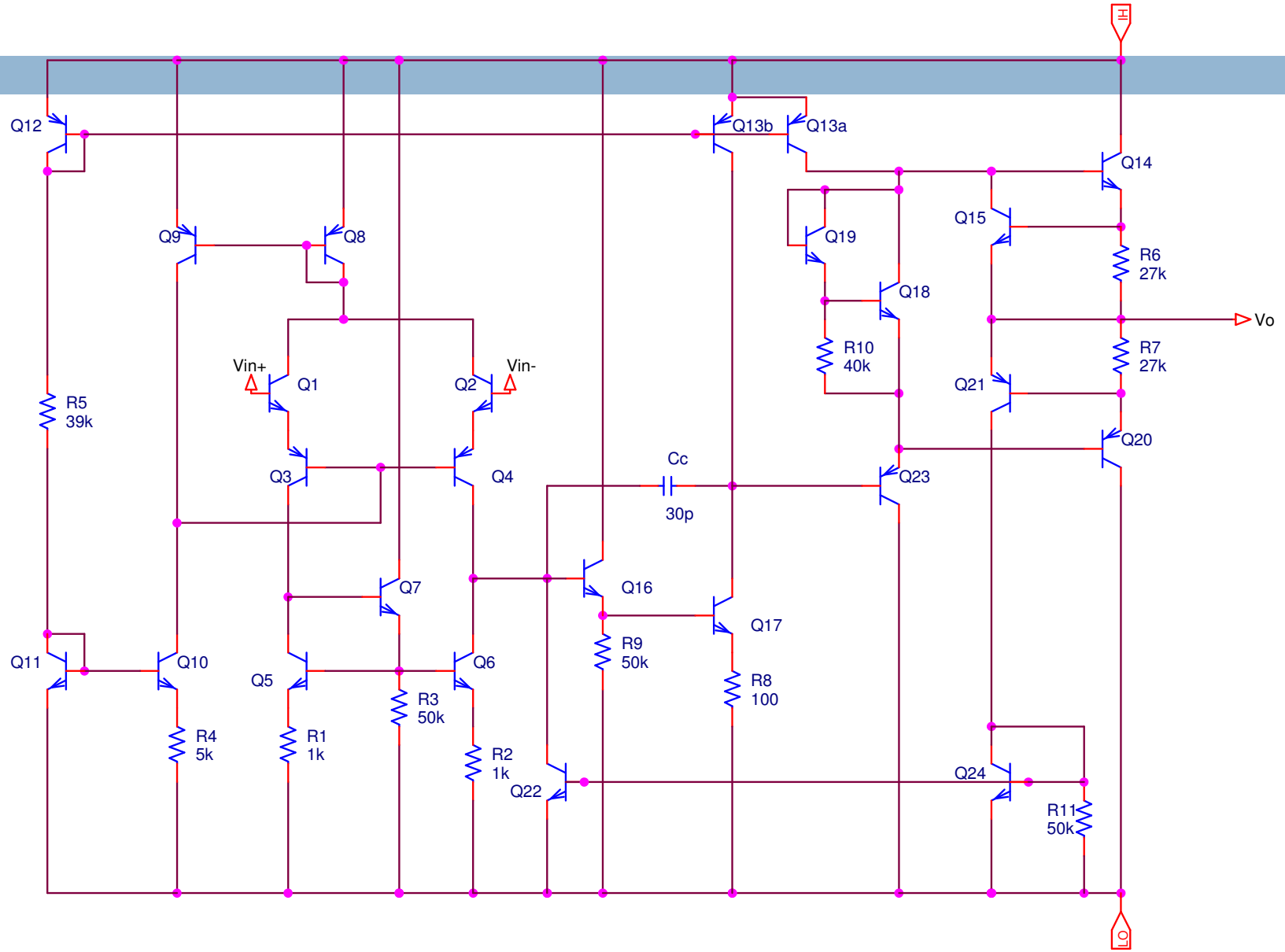
Maximum ratings

Max Ratings	Fig. 2
Supply voltage	±18Volts
Internal Power Dissipation	500mW
Differential Input Voltage	±30Volt
Input voltage	±15Volt
Voltage Offset Null/V-	±0.5Volt
Operating Temperature Range	0° to +70°C
Storage Temperature Range	-65° to +150°C
Lead Temperature, Solder, 60sec.	300°C
Output Short Circuit	Indefinite

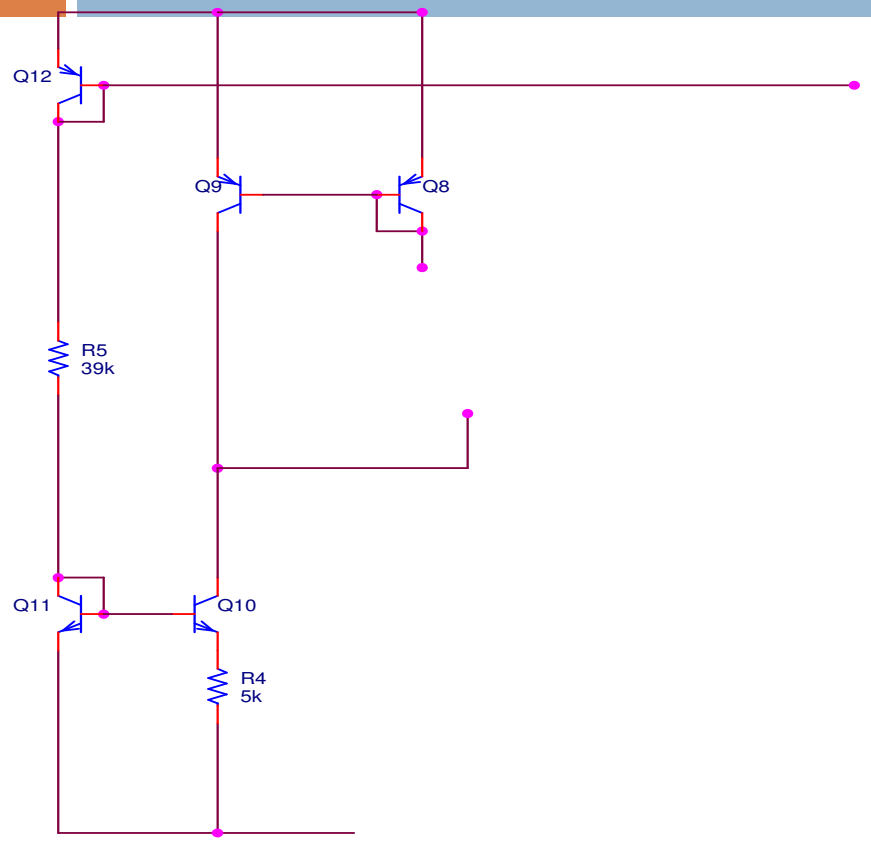
OpAmp 741 inside structure

- Biasing Currents
- Input Stage
- Second Stage
- Output Stage
- Short Circuit Protection

Inside structure: Schematic



Biasing Current Sources

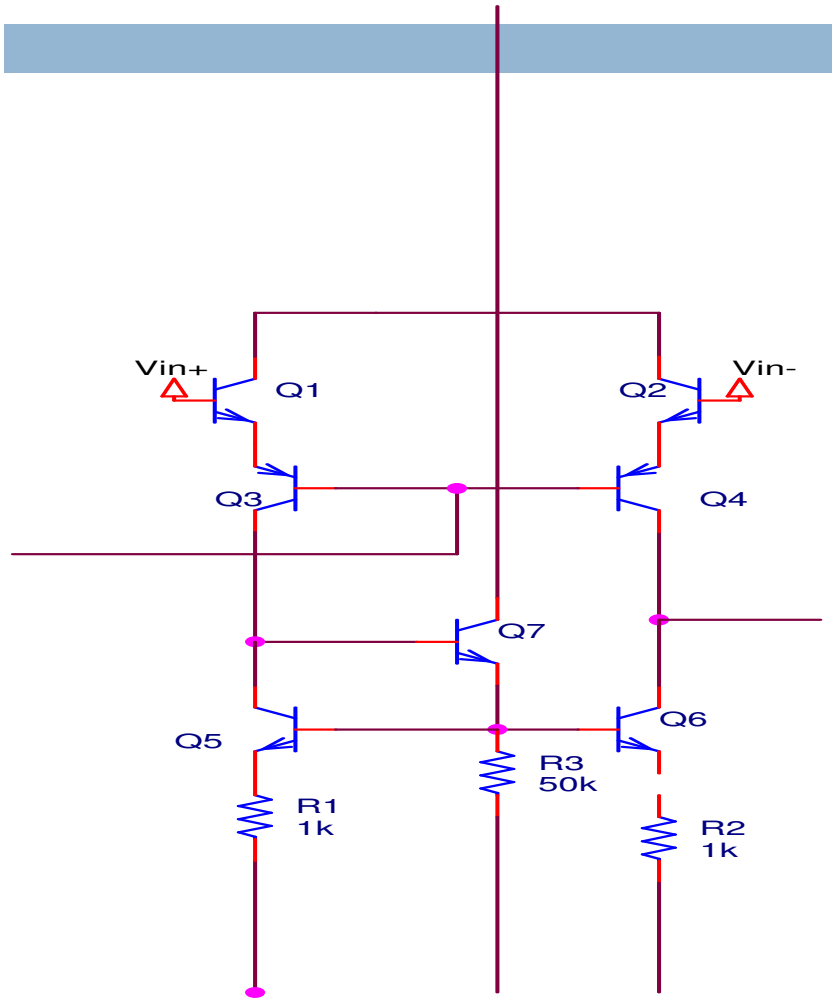


- Generates reference bias current through R_5
- The opAmp reference current is:

$I_{ref}=[V_{CC}-V_{EB12}-V_{BE11}-(-V_{EE})]/R_5$

- For $V_{CC}=V_{EE}=15V$ and $V_{BE11}=V_{BE12}=0.7V$, we have $I_{REF}=0.73mA$

Input Stage



- The differential pair, Q1 and Q2 provide the main input
- Transistors Q5-Q7 provide an active load for the input

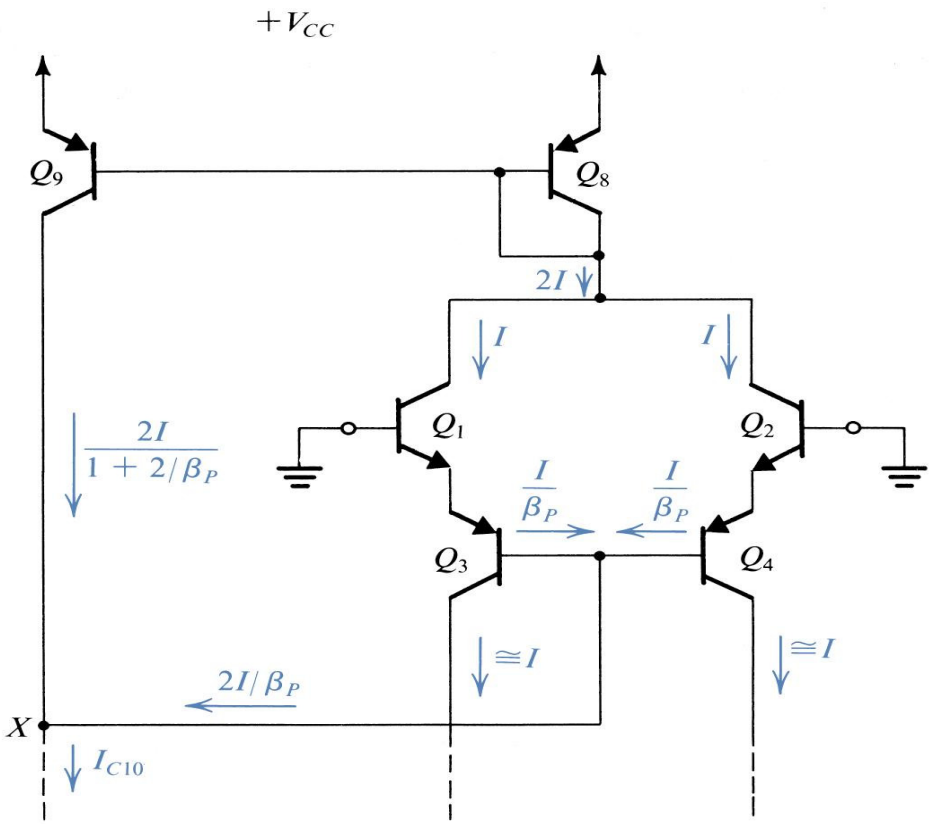
Input Stage:

DC Analysis - 1

- Assuming that Q10 and Q11 are matched, we can write the equation from the Widlar current source:

  - Using trial and error, we can solve for I_{C10}, and we get: $I_{C10}=19\mu A$

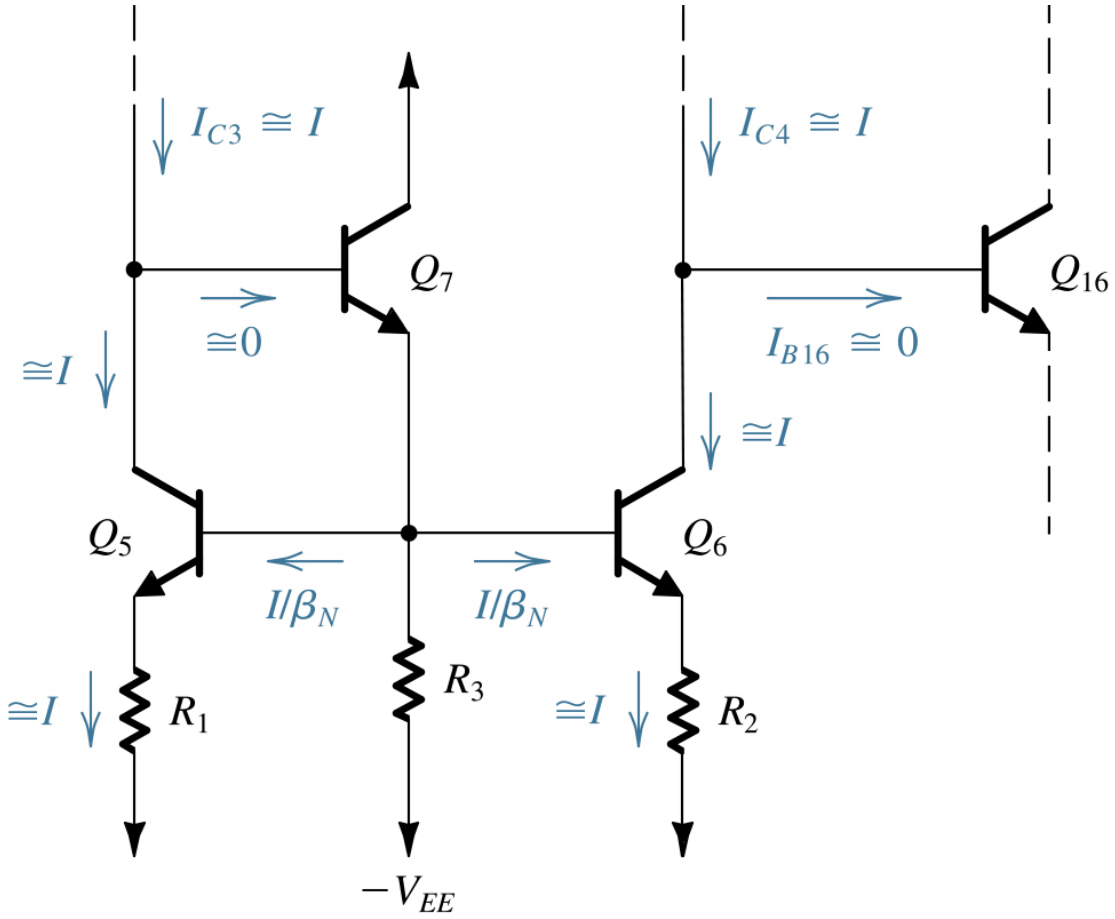
Input Stage: DC Analysis -2



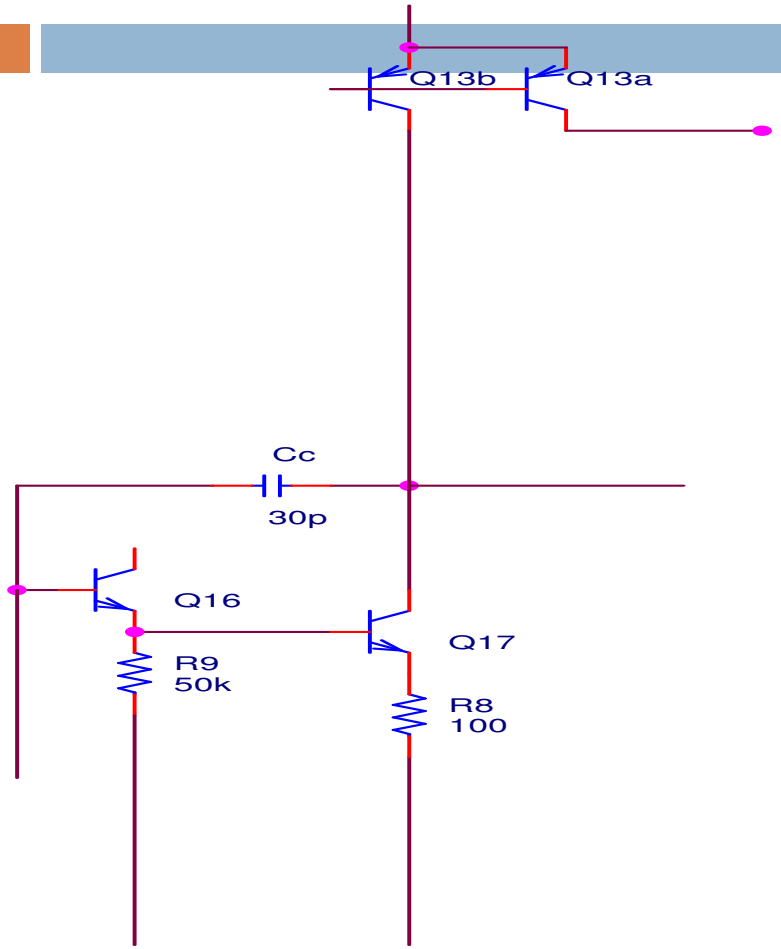
- From symmetry we see that $I_{C1}=I_{C2}=I$, and if the *npn* β is large, then $I_{E3}=I_{E4}=I$
- Analysis continues:

Input Stage: DC Analysis -3

- Analysis of the active load:



Second (Intermediate) Stage



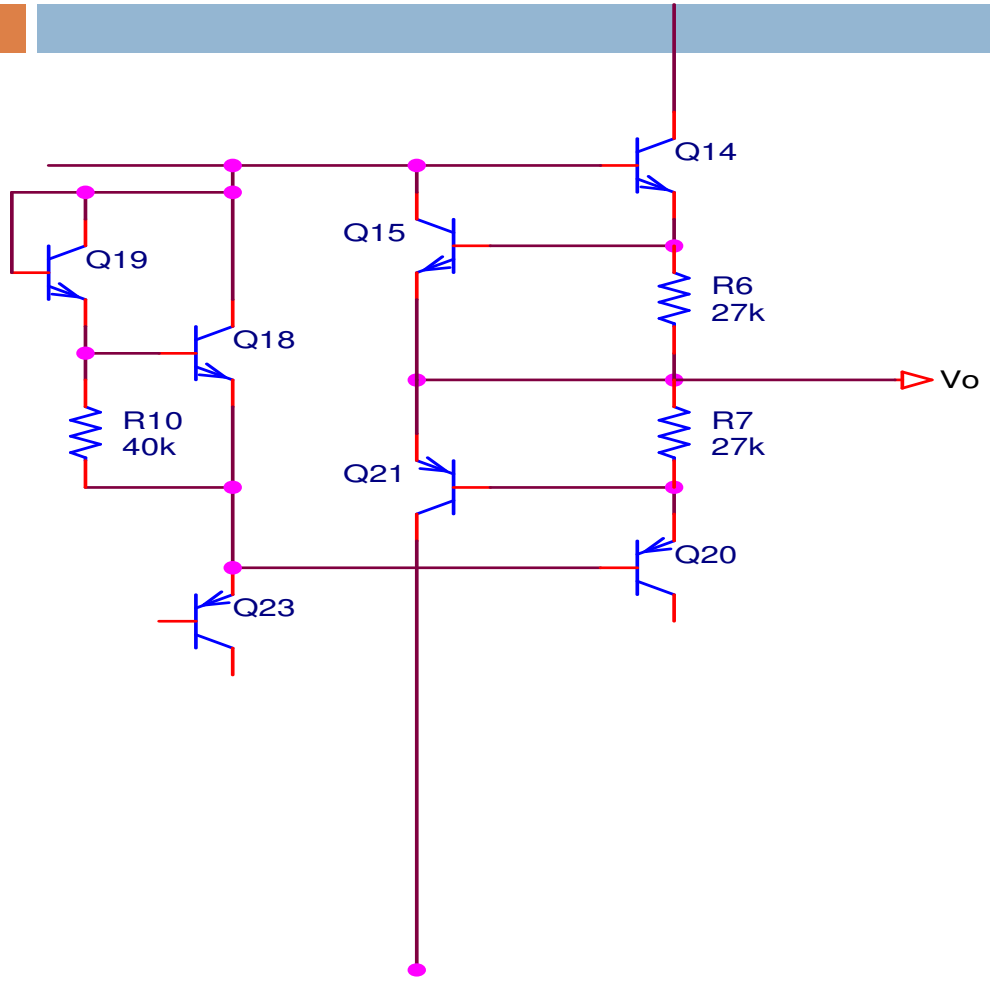
- Transistor Q16 acts as an emitter-follower giving this stage a high input resistance
- Capacitor Cc provides frequency compensation using the Miller compensation technique

Second Stage:

DC Analysis

- Neglecting the base current of Q23, I_{C17} is equal to the current supplied by Q13b
- $I_{C13b}=0.75I_{REF}$ where $\beta_P >> 1$
- Thus: $I_{C13b}=550uA=I_{C17}$
- Then we can also write:

Output Stage



- Provides the opAmp with a low output resistance
- Class AB output stage provides fairly high current load capabilities without hindering power dissipation in the IC

Output Stage:

DC Analysis

- Q13a delivers a current of $0.25I_{REF}$, so we can say: $I_{C23}=I_{E23}=0.25I_{REF}=180\mu A$
- Assuming $V_{BE18} = 0.6V$, then $I_{R10}=15\mu A$, $I_{E18}=180-15=165\mu A$ and $I_{C18}=I_{E18}=165\mu A$
- $I_{C19}=I_{E19}=I_{B18}+I_{R10}=15.8\mu A$

Short Circuit Protection

- These transistors are normally off
- They only conduct in the event that a large current is drawn from the output terminal (i.e. a short circuit)