Latches and Flip-Flops

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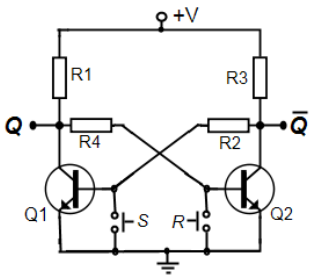
Content

- Memory element
- Latches
- Flip-Flops

A device with exactly two stable states

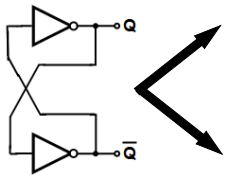
Bistable multivibrator circuit

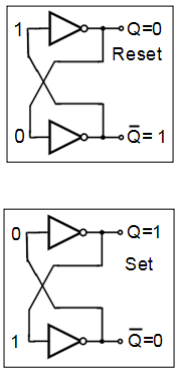


Q1 on → Q2 off

Q1 off → Q2 on

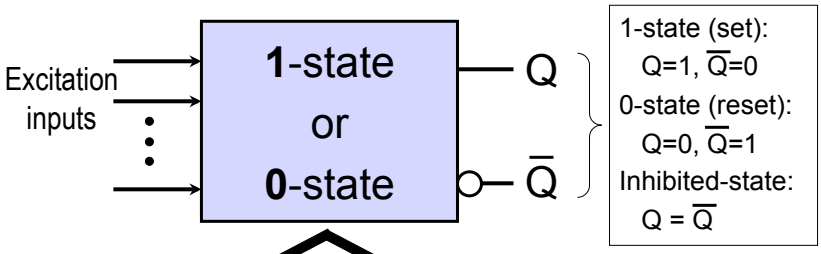
2 stable states





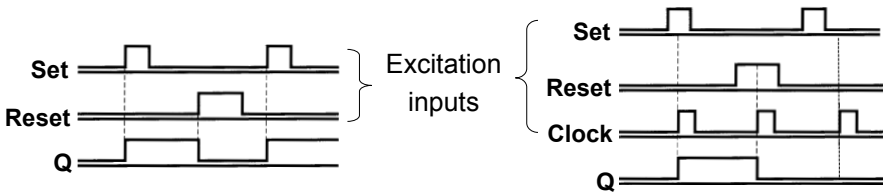
as
a memory element
can store one bit

Memory element



Latch

Flip-Flop (with clock)

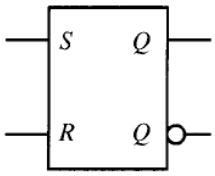


Latches

- SR latch (Set-Reset latch)
  - + with NOR structure
  - + with NAND structure
- Gated SR latch
- D latch (Delay or Data latch = transparent latch)

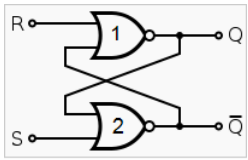
- Some applications of the latches (1) (2) (3)

Set-Reset Latch with NOR structure



SR latch

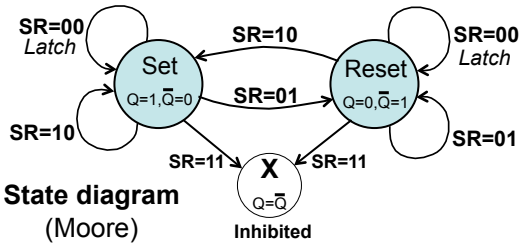
S, R active "High"



NOR structure

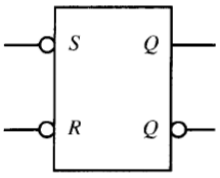
S	R	Q' (next)
0	0	Q (latch)*
0	1	0 (reset)
1	0	1 (set)
1	1	Q'=$\overline{Q}$'=0 (Inhibited)

*** Latch = No change**



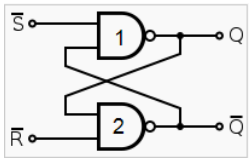
State diagram
(Moore)

Set-Reset Latch with NAND structure



SR latch

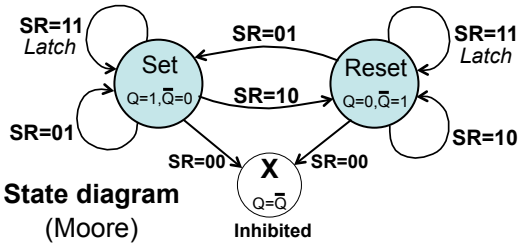
S, R active "Low"



NAND structure

S	R	Q' (next)
0	0	Q'=$\overline{Q}$'=1 (Inhibited)
0	1	1 (set)
1	0	0 (reset)
1	1	Q (latch)*

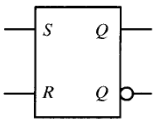
*** Latch = No change**



State diagram
(Moore)

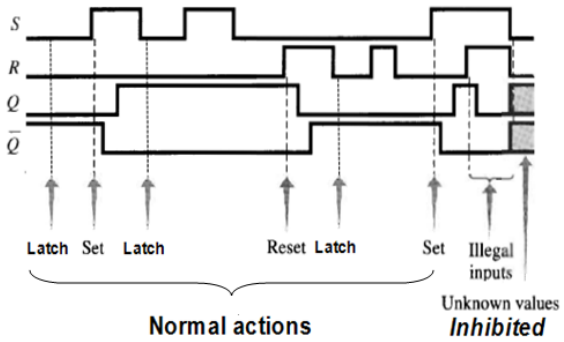
SR latch timing diagram

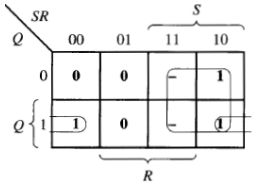
NOR SR Latch



S, R active "High"

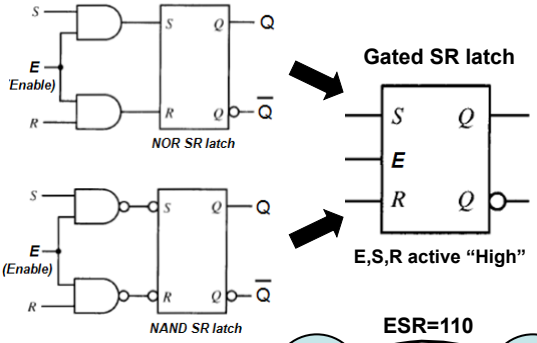
S	R	Q' (next)
0	0	Q (latch)*
0	1	0 (reset)
1	0	1 (set)
1 (Illegal)	1	Q'=$\overline{Q}$'=0 (Inhibited)





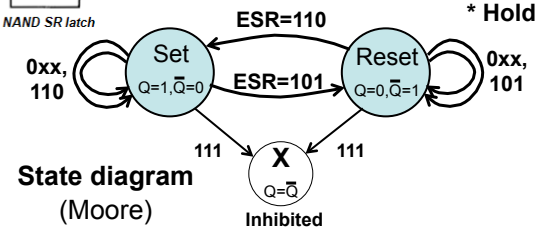
$Q' = S + \overline{R}Q$

Gated SR Latch



E	S	R	Q' (next)
0	x	x	Q (hold)*
1	0	0	Q (latch)
1	0	1	0 (reset)
1	1	0	1 (set)
1	1	1	Inhibited

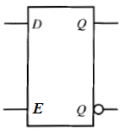
*** Hold = No action**

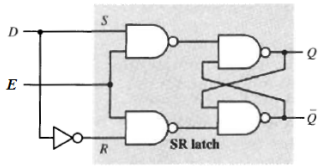


State diagram
(Moore)

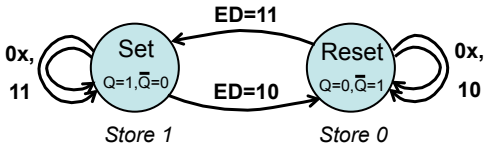
D Latch

Data or Delay latch
= transparent latch

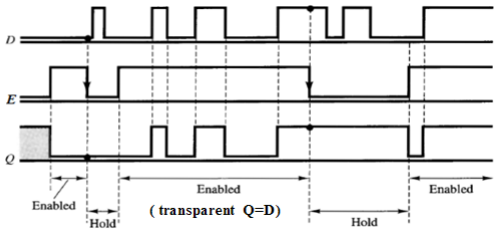




E	D	Q' (next)
0	x	Q (hold)*
1	0	0 (reset=store 0)
1	1	1 (set=store 1)

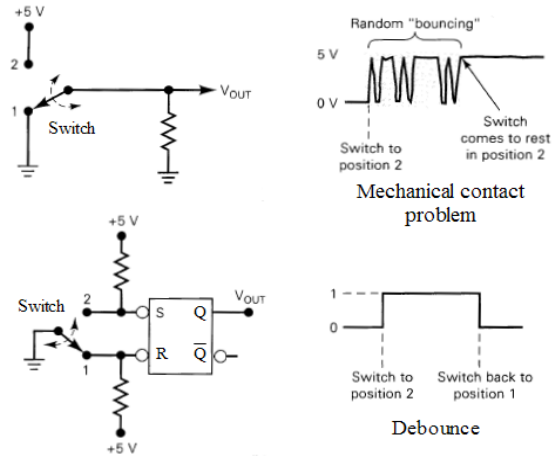


D latch
Timing
diagram



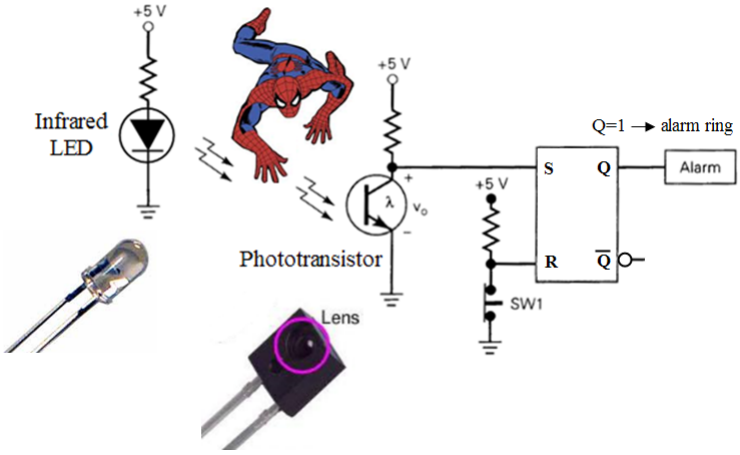
Some applications of the latches (1)

(App 1) Debounce a mechanical switch



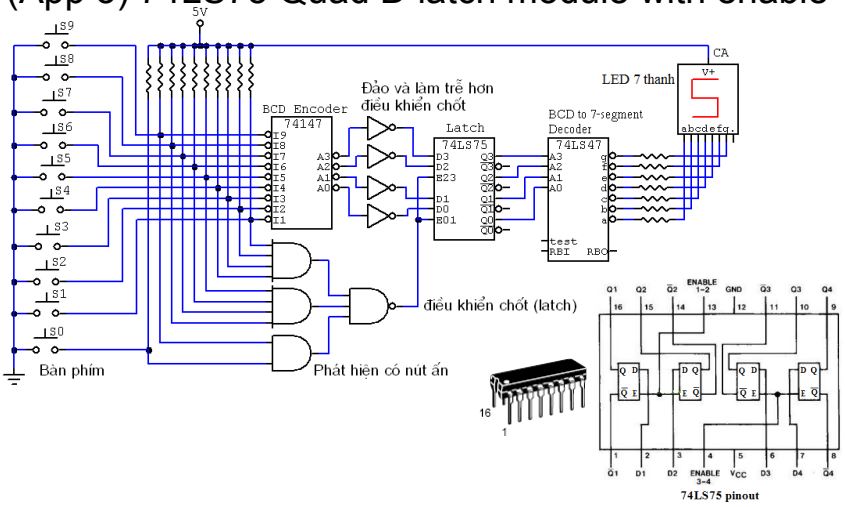
Some applications of the latches (2)

(App 2) LED detect alarm system



Some applications of the latches (3)

(App 3) 74LS75 Quad D latch module with enable



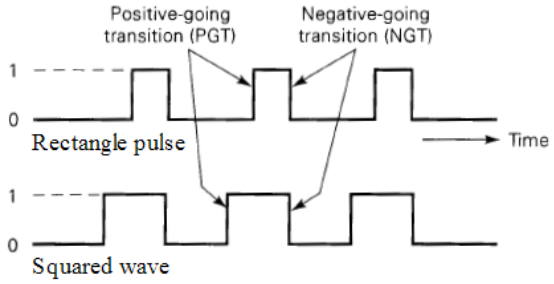
Flip-Flops

- Clock signals
- Clocked flip-flops
  - + Master-Slave Flip-Flop (Pulse-triggered FF)
  - + Edge-triggered Flip-Flop
- SR Flip-Flop
- JK Flip-Flop
- D Flip-Flop
- T Flip-Flop
- Asynchronous set and reset (Preset and Clear)
- Some applications of the flip-flops(1) (2) (3)

Clock signals

Với hệ thống đồng bộ, ngõ ra thay đổi trạng thái tại những thời điểm có cạnh xung clock.

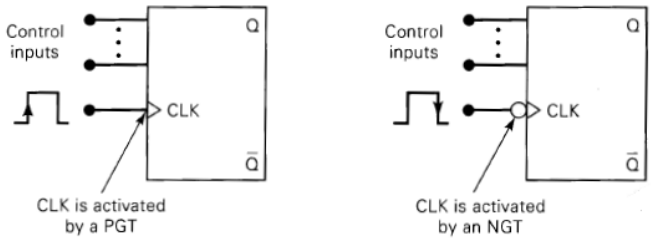
- Cạnh xung dương Positive-going transitions (PGT)
- Cạnh xung âm: Negative-going transitions (NGT)



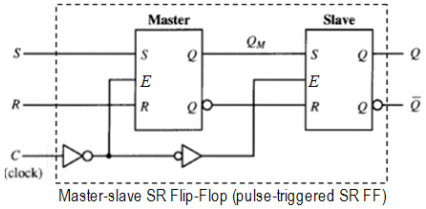
Clocked Flip-Flops

Trong các FF có ngõ vào xung clock (CLK)

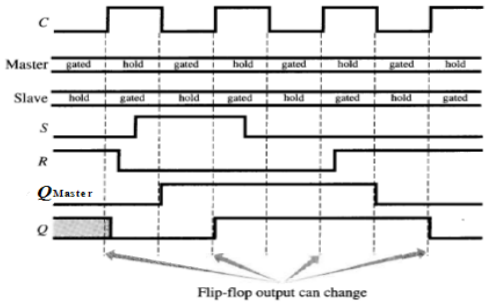
- (a) Xung clock tích cực cạnh dương
- (b) Xung clock tích cực cạnh âm



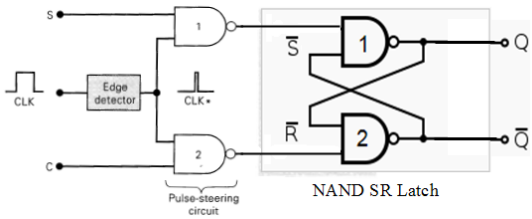
Master-Slave Flip-Flops

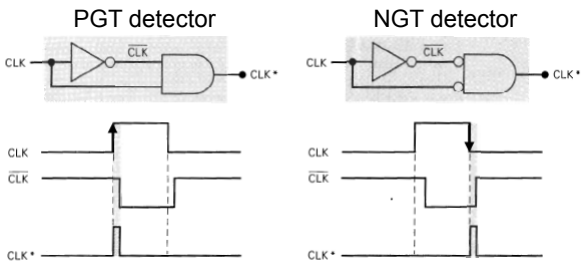


Master-slave SR Flip-Flop (pulse-triggered SR FF)

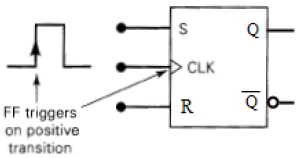


Edge-triggered Flip-Flops

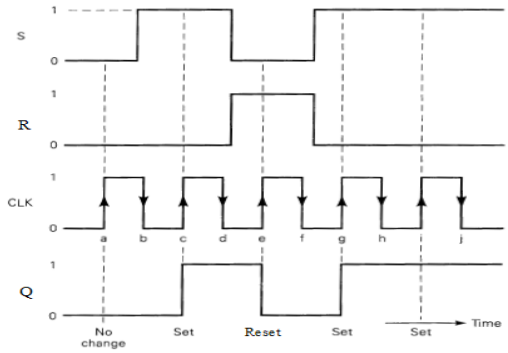




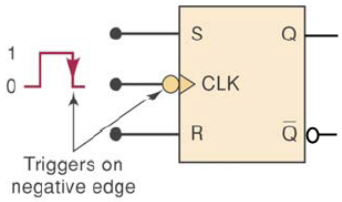
SR Flip-Flop (active with PGT)



Inputs			Output
S	R	CLK	Q' (next)
0	0	↑	Q (no change)
1	0	↑	1 (set)
0	1	↑	0 (reset)
1	1	↑	Inhibited



SR Flip-Flop (active with NGT)

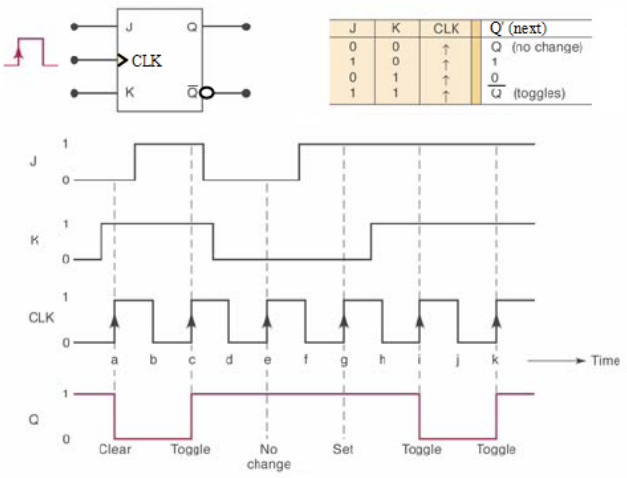


Inputs			Output
S	R	CLK	Q' (next)
0	0	↓	Q (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	(Inhibited)

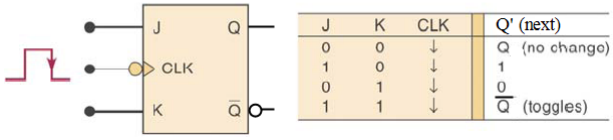
JK Flip-Flop

- Hoạt động giống SC-FF. J là ngõ set, K là ngõ clear
- Khi cả J và K đều ở mức cao, ngõ ra sẽ đảo trạng thái so với trạng thái trước đó.
- Có thể tích cực cạnh dương hay cạnh âm xung clock.

JK Flip-Flop (active with PGT)

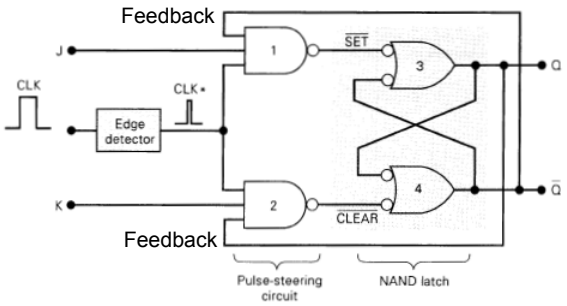


JK Flip-Flop (active with NGT)

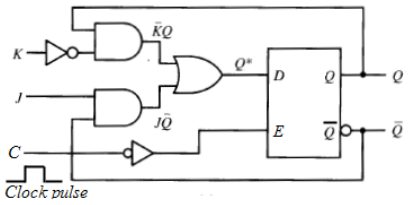


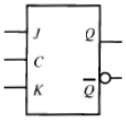
J	K	CLK	Q' (next)
0	0	↓	Q (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q}$ (toggles)

Internal Circuitry of JK Flip-Flop

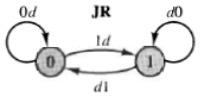


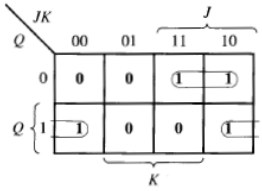
Pulse-triggered JK Flip-Flop





J	K	Q	C	Q'	
0	0	0	⎍	0	Hold
0	0	1	⎍	1	
0	1	0	⎍	0	Reset
0	1	1	⎍	0	
1	0	0	⎍	1	Set
1	0	1	⎍	1	
1	1	0	⎍	1	Toggle
1	1	1	⎍	0	

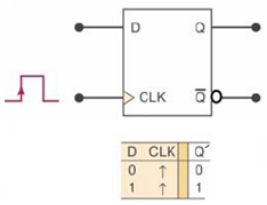




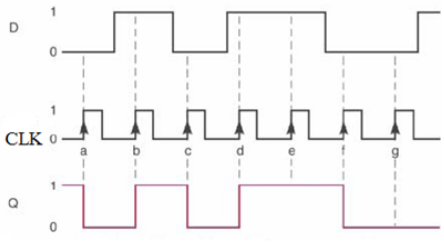
$$Q^* = \bar{K}Q + J\bar{Q}$$

D Flip-Flop

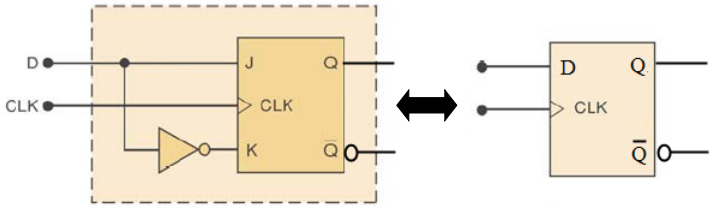
- Chỉ có một ngõ vào D, tương ứng với ngõ vào data.
- Ngõ ra Q sẽ có cùng giá trị với ngõ vào D khi có tác động của cạnh xung clock.
- Trong những thời điểm khác, D-FF sẽ lưu giá trị trước đó của nó.



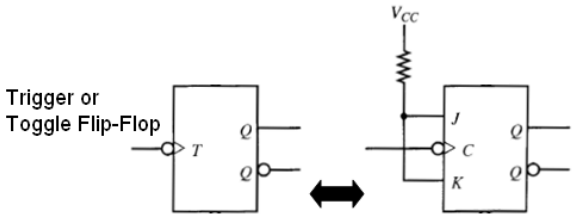
D	CLK	Q'
0	↑	0
1	↑	1



Make D Flip-Flop from JK Flip-Flop

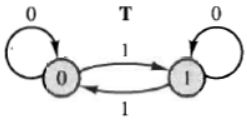


T Flip-Flop (active with NGT)

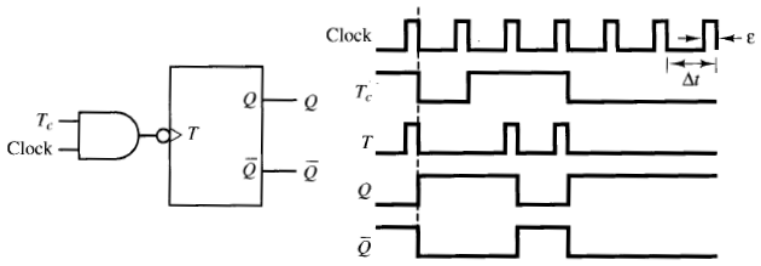


$\downarrow \Rightarrow Q^* = \bar{Q}$

T	Q	Q^*	
↓	0	1	Toggle
↓	1	0	Toggle



Clocked T Flip-Flop

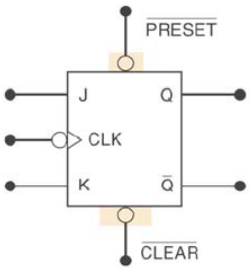


Asynchronous set and reset (1)

- S, R, J, K và D được gọi là những ngõ vào đồng bộ bởi vì ảnh hưởng của chúng đồng bộ với xung clock.
- Ngõ vào không đồng bộ hoạt động độc lập với những ngõ vào đồng bộ, chúng có thể set (1) hoặc clear (0) Flip-Flop vào bất kỳ thời điểm nào.

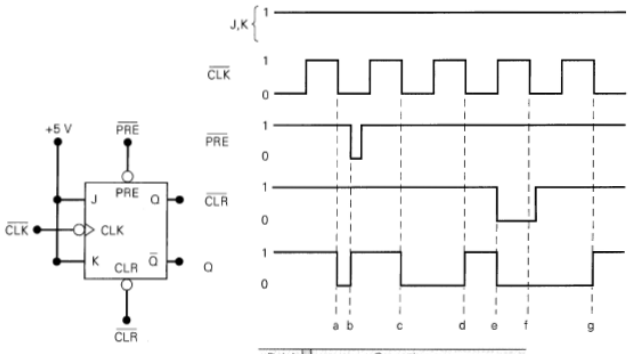
Asynchronous set and reset (2)

JK-FF with $\overline{\text{Preset}}$ and $\overline{\text{Clear}}$ inputs



J	K	Clk	$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	Q
0	0	↓	1	1	Q (no change)
0	1	↓	1	1	0 (Synch reset)
1	0	↓	1	1	1 (Synch set)
1	1	↓	1	1	$\overline{Q}$ (Synch toggle)
x	x	x	1	1	Q (no change)
x	x	x	1	0	0 (asynch clear)
x	x	x	0	1	1 (asynch preset)
x	x	x	0	0	(invalid)

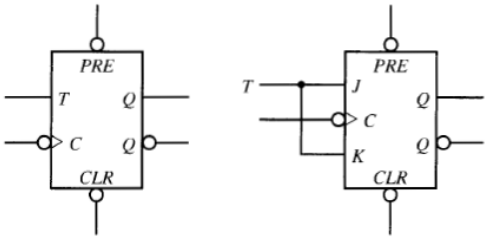
Asynchronous set and reset (3)



Point	Operation
a	Synchronous toggle on NGT of $\overline{\text{CLK}}$
b	Asynchronous set on $\overline{\text{PRE}} = 0$
c	Synchronous toggle
d	Synchronous toggle
e	Asynchronous clear on $\overline{\text{CLR}} = 0$
f	$\overline{\text{CLR}}$ over-rides the NGT of $\overline{\text{CLK}}$
g	Synchronous toggle

Asynchronous set and reset (4)

T-FF with $\overline{\text{Preset}}$ and $\overline{\text{Clear}}$ inputs



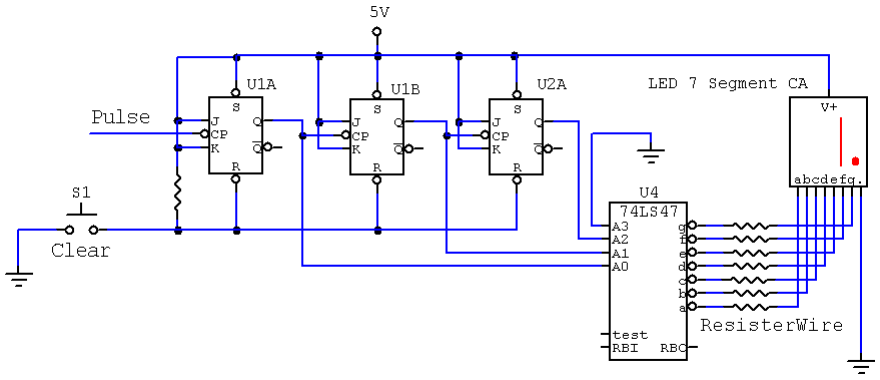
T	Q	C	Q^*	
0	0	↓	0	Hold
0	1	↓	1	
1	0	↓	1	Toggle
1	1	↓	0	

Applications of the Flip-Flop

+ Thiết kế các bộ đếm (Counter)
+ Thiết kế thanh ghi dịch (Shift register)
+ Thiết kế mạch dãy
+ Các ứng dụng khác

Some applications of the Flip-Flop (1)

3 bits Up-Counter



Some applications of the Flip-Flop (2)

Serial shift register