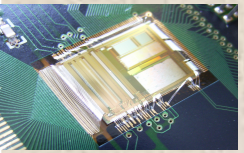
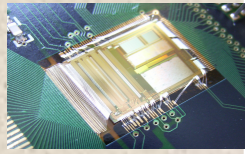


Set-up steps



1, Reading the chip ID

2, DAC scan

3, Calibrating the internal test pulse

4, Measuring noise – S-curves

5, Calibrating threshold

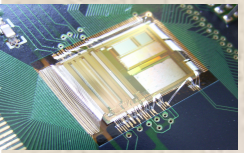
6, Trimming Threshold

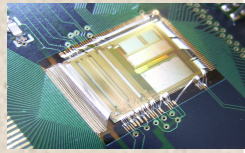
7, Taking Data

Most of this talk refers to the above set-up steps

Refer to the VFAT2 user manual for register functionality and address locations !!!

Functional routines that could be done once the set-up is complete





Noise characterisation of all channels in a single VFAT2 (with and without GEM) Study hybrid performance.

Noise characterisation and mapping of all VFATs on a chamber. Study GEB performance.

1, Reading the chip ID

2, DAC scan

3, Calibrating the internal test pulse

4, Measuring noise – S-curves

5, Calibrating threshold

6, Trimming Threshold

7, Taking Data

Estimation of detector channel capacitance.

Noise characterisation and mapping of all VFATs in the system. Study system performance.

Production test routines.

Data taking and MIP calibration. Test beams

Interface with CMS, Event house keeping etc

VFAT2 operation cycle

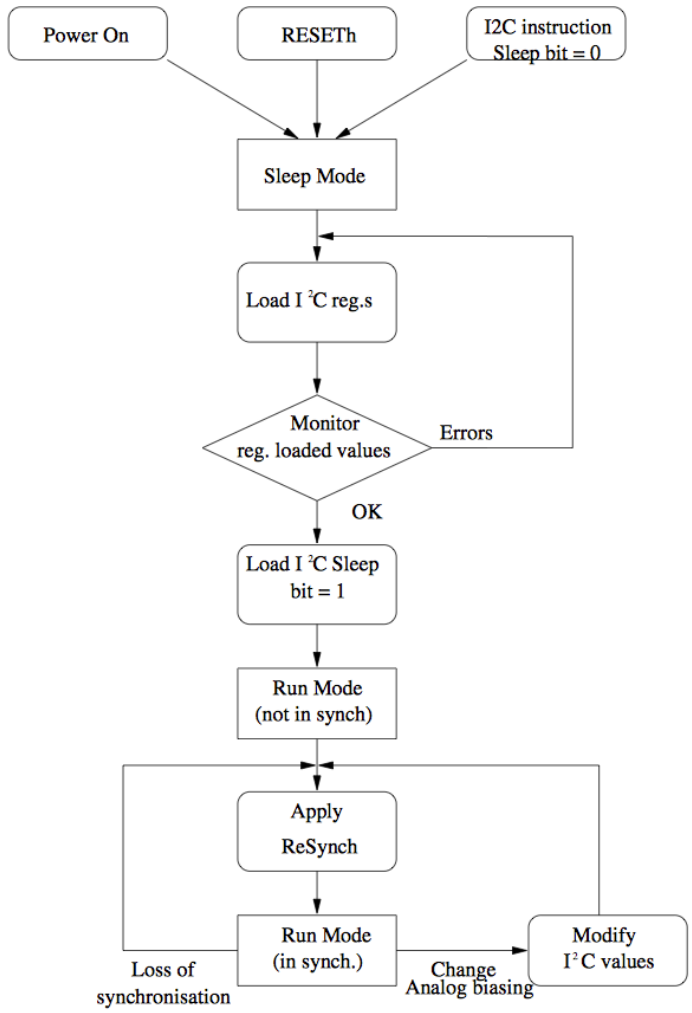


Figure 1: Flowchart of the operation cycle of VFAT2

VFAT2 internal registers

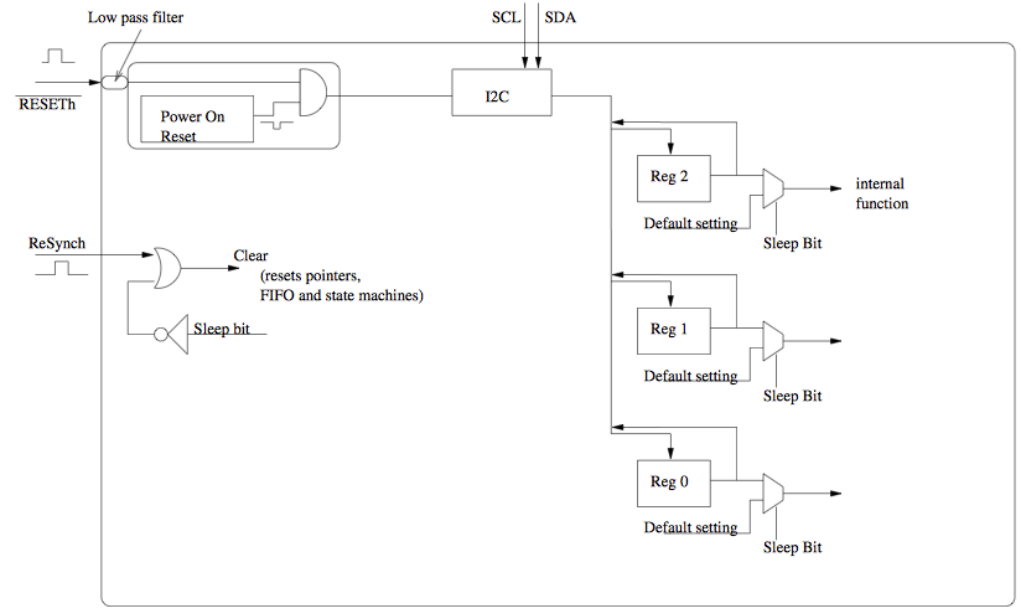


Figure 4: A schematic view of the programmable registers.

5.1 The Control Registers

VFAT2 has four "Control Registers" labelled Cont.Reg. 0, to Cont.Reg. 3 which have bit allocations as shown in tables 4, 5, 6 and 7.

7	6	5	4	3	2	1	0
CalMode ⟨1⟩	CalMode ⟨0⟩	CalPolarity	MSPolarity	Trigmode ⟨2⟩	TrigMode ⟨1⟩	TrigMode ⟨0⟩	SleepB Sleep/Run

Table 4: Control Register 0

7	6	5	4	3	2	1	0
ReHitCT ⟨1⟩	ReHitCT ⟨0⟩	LVDSPowerSave	ProbeMode	DACsel ⟨3⟩	DACsel ⟨2⟩	DACsel ⟨1⟩	DACsel ⟨0⟩

Table 5: Control Register 1

7	6	5	4	3	2	1	0
DigInSel	MSPulse-Length ⟨2⟩	MSPulse-Length ⟨1⟩	MSPulse-Length ⟨0⟩	HitCount-Sel ⟨3⟩	HitCount-Sel ⟨2⟩	HitCount-Sel ⟨1⟩	HitCount-Sel ⟨0⟩

Table 6: Control Register 2

Principal Registers :				
Reg. Name	Hardwired Sleep value	Software Default Value	Reg. Add.	Reg. type
Cont.Reg⟨0⟩	0000 0000	0000 0000	0	W/R
Cont.Reg⟨1⟩	0000 0000	0000 0000	1	W/R
IPreampIn	0000 0000	1010 1000	2	W/R
IPreampFeed	0000 0000	0101 0000	3	W/R
IPreampOut	0000 0000	1001 0110	4	W/R
IShaper	0000 0000	1001 0110	5	W/R
IShaperFeed	0000 0000	0110 0100	6	W/R
IComp	0000 0000	0111 1000	7	W/R
ChipID⟨0⟩			8	RO
ChipID⟨1⟩			9	RO
UpsetReg.			10	RO
HitCount0			11	RO
HitCount1			12	RO
HitCount2			13	RO
ExtRegPointer	0000 0000	0000 0000	14	W/R
ExtRegData	0000 0000	0000 0000	15	W/R
Extended Registers :				
Lat	1000 0000	1000 0000	⋆0	W/R
ChanReg⟨1 : 128⟩	0000 0000	0000 0000	⋆1 to ⋆128	W/R
VCal	0000 0000	0110 0100	129	W/R
VThreshold1	0000 0000	0000 0000	⋆130	W/R
VThreshold2	0000 0000	0001 1010	⋆131	W/R
CalPhase	0000 0000	0000 0000	⋆132	W/R
Cont.Reg⟨2⟩	0000 0000	0000 0000	⋆133	W/R
Cont.Reg⟨3⟩	0000 0000	0000 0000	⋆134	W/R
Spare⟨135⟩	0000 0000	-	⋆135	W/R

⋆ → addressed via Principal registers 14 and 15

Table 17: The VFAT2 Register Sleep settings

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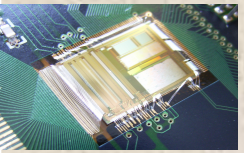
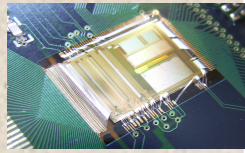
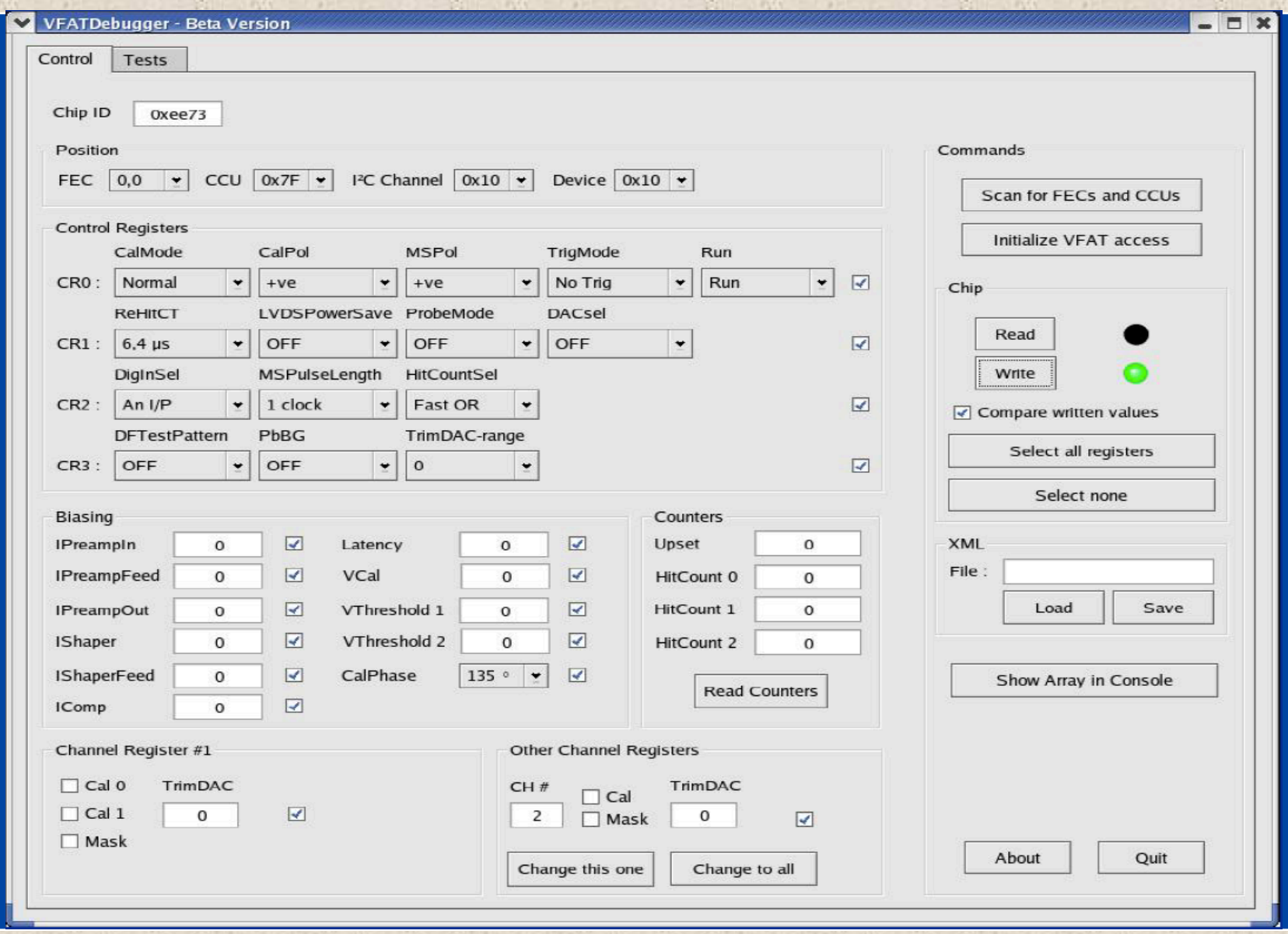
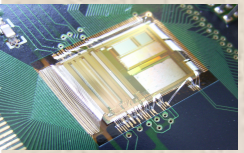
Example of TOTEM "set-up" control panel

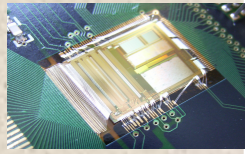








Read Chip ID



2.1 Power On

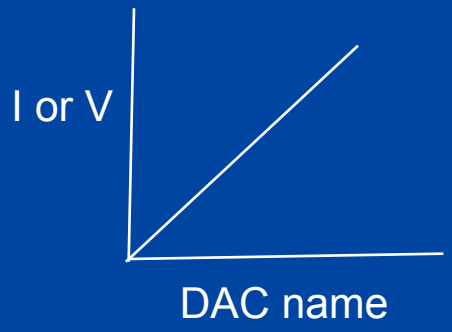
The chip will enter SLEEP mode directly on application of power to the chip.

2.1.2 Read ChipID

Each chip has a unique identifier hardwired inside that may be read via I2C through principal registers 8 and 9. The identifier should be used to create a directory in which the measured results of this particular chip can be stored.

DAC scanning

One by one, select DAC and scan it to obtain

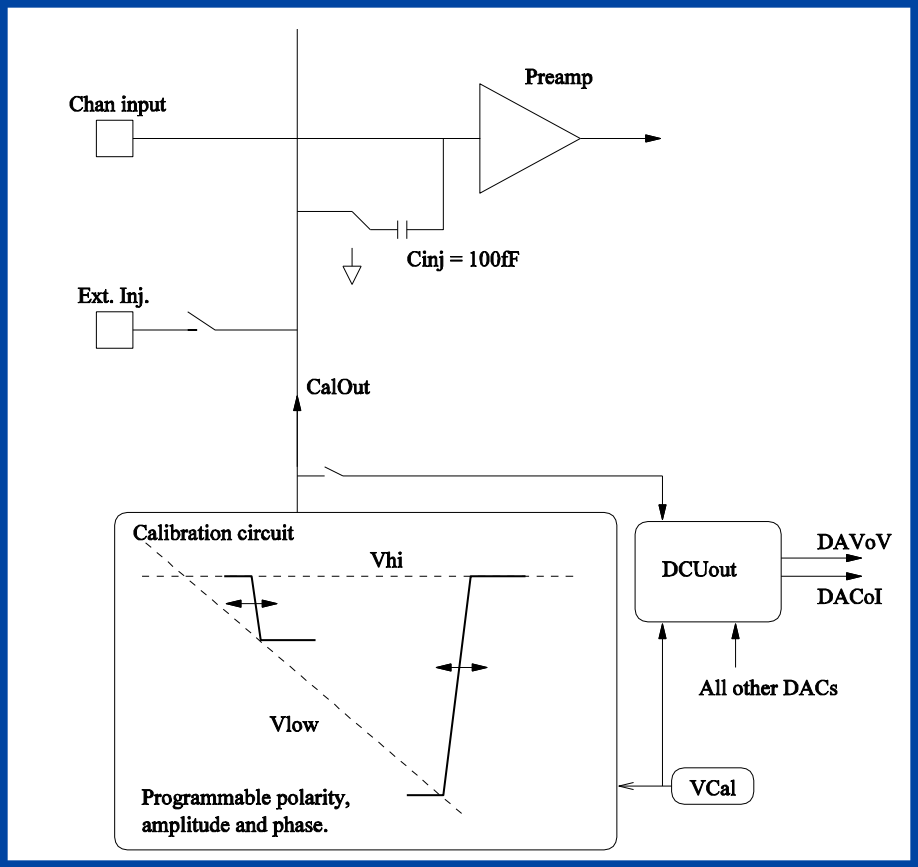


This can be stored and use as a lookup table for setting the required bias current or voltage

DAC Name	V or I	Exact V or I required	General DAC setting (bin)	General DAC setting (dec)
IPreampIn	I	168uA	10101000	168
IPreampOut	I	30uA	10010110	150
IPreampFeed	I	80uA	01010000	80
IShaper	I	30uA	10010110	150
IShaperFeed	I	20uA	01100100	100
IComp	I	60uA	01111000	120
VTh1	V			
VTh2	V			
VCal	V			

Table 28: Bias requirements and general DAC settings.

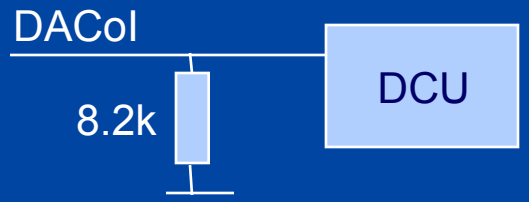
Calibration and noise measurements.



Qin = 100fF * (Vhi – Vlow)

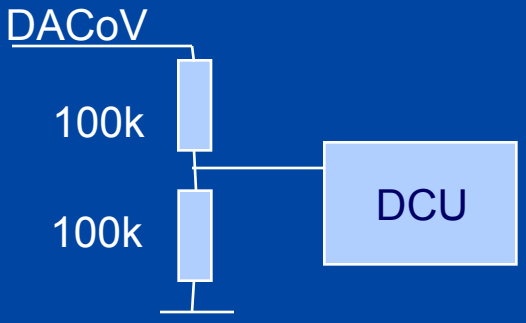
Qin = 0.1fC/mV of CalOut

DCU LSB = 463uV



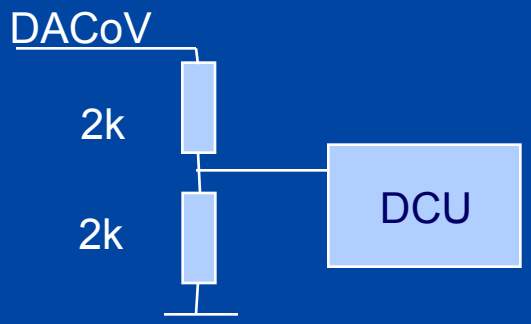
DACoI = (DCU_value * 463uV) / 8.2k

TOTEM hardware



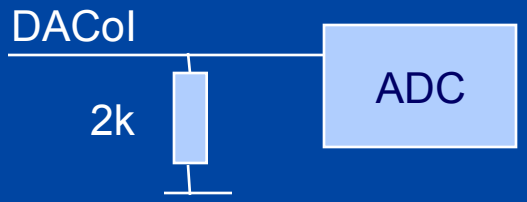
DACoV = DCU_value * 463uV * 2

ADC on OH v1

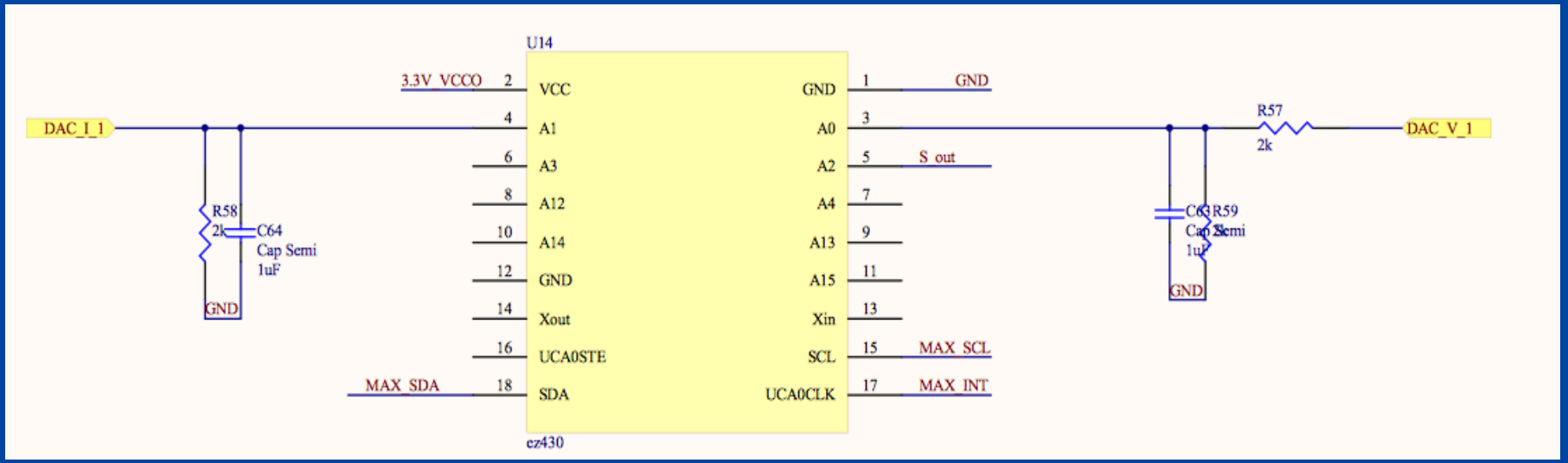


DACoV = DCU_value * xuV * 2

ADC LSB = xuV ??



DACoI = (DCU_value * xuV) / 2k



Calibrating VCal

After the DAC Scan you have Charge Injected vs VCal DAC vlaue

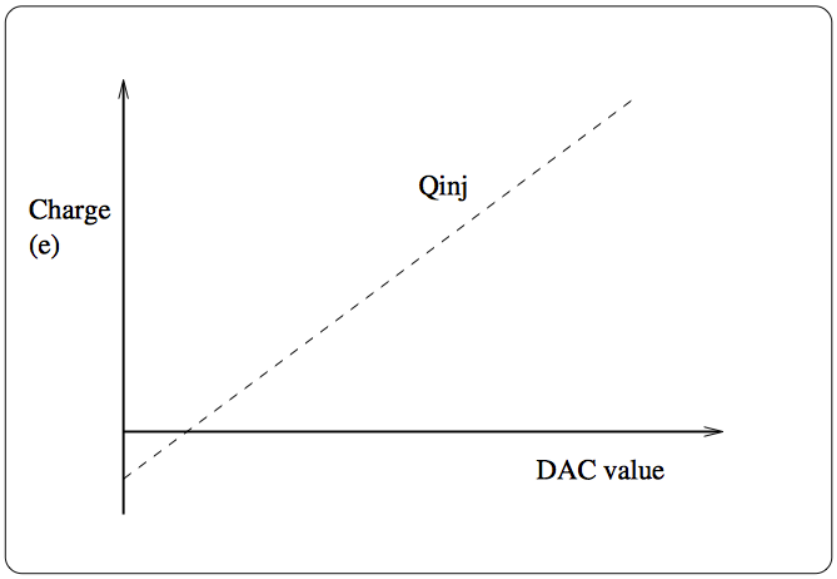
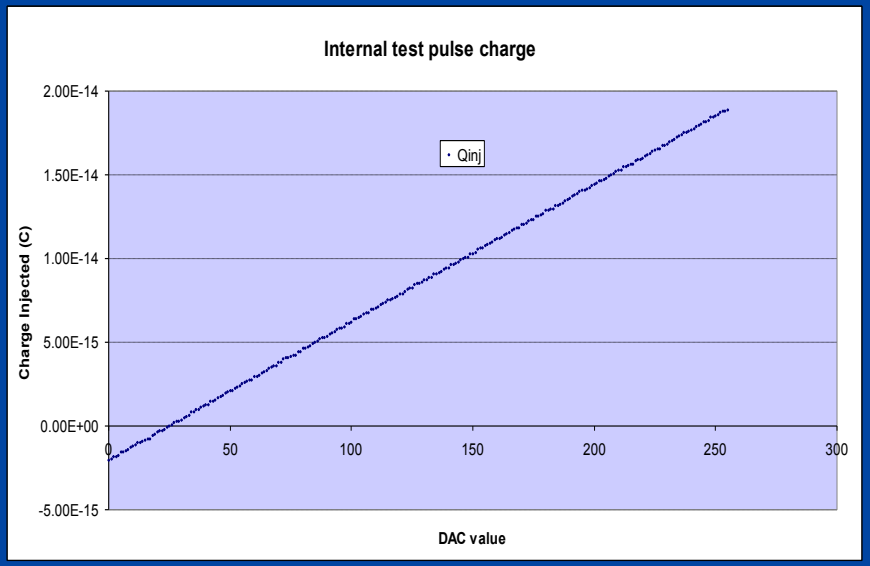


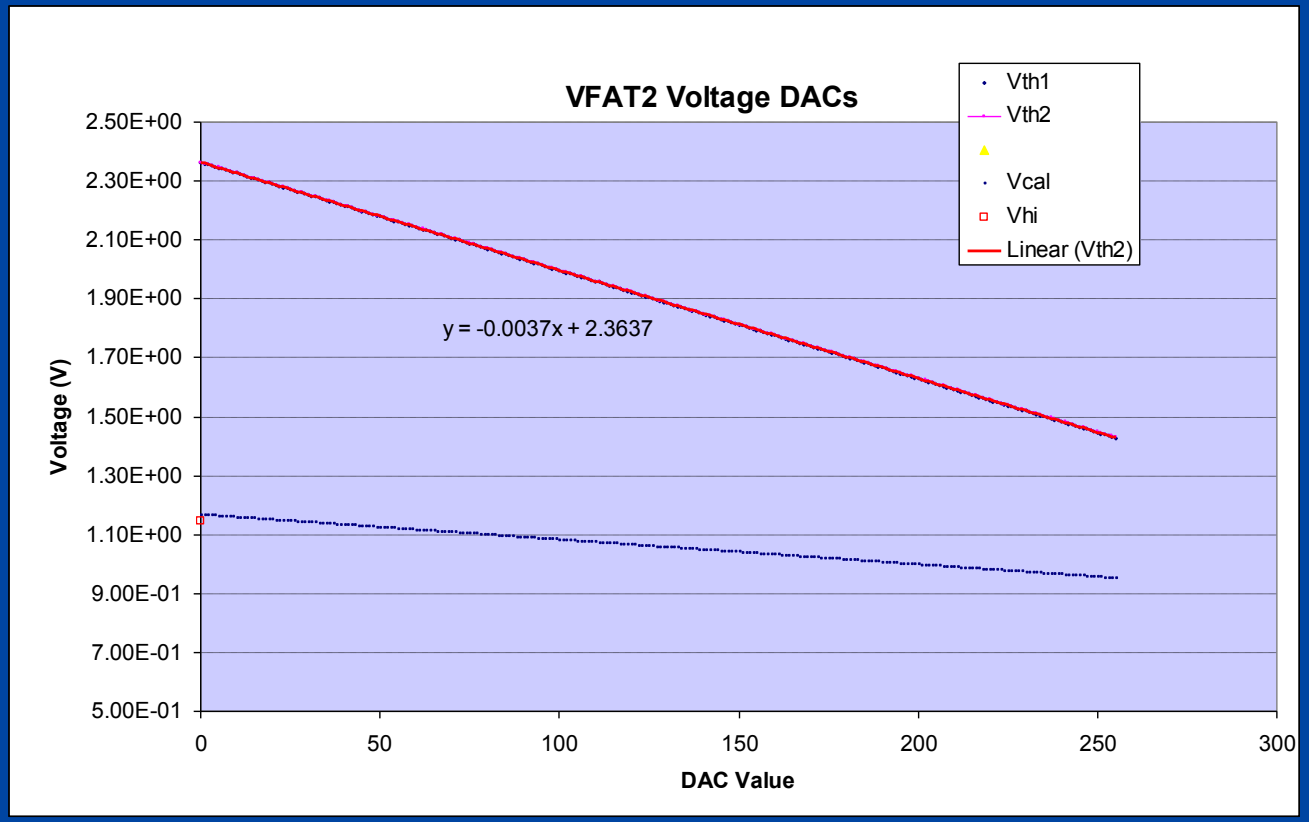
Figure 17: Injected charge



VCal

Calibrating Threshold range

Measure VCal, VT1 and VT2 DAC response via DCU



Vt1 and Vt2 DAC response

Total range of VT1 or VT2 = 0.9472 volts

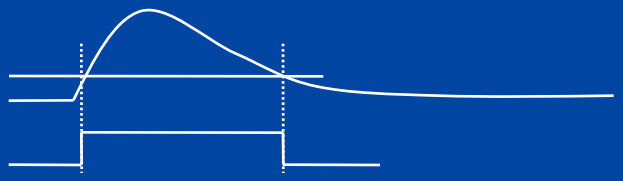
VFAT2 Thresholds (1)

VFAT has one main threshold control which is common for all channels.

Main threshold controlled by the difference between two voltages VT1 & VT2.

Roman Pot silicon
Positive signal charge
Requires a positive threshold

VT2 - VT1 > 0

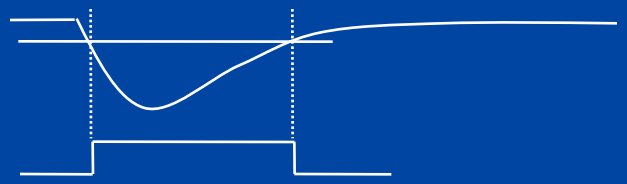


To increase threshold w.r.t. signal :

Increase DAC value (VT2-VT1)

GEM and CSC
Negative signal charge
Requires a negative threshold

VT1 – VT2 > 0



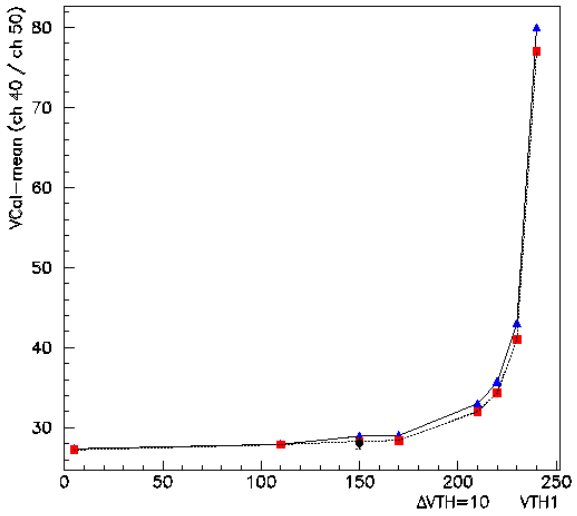
To increase threshold w.r.t. signal :

Increase DAC value (VT1-VT2)

Thresholds

Question : Does a given ΔVT always give the same threshold irrespective of VT1 and VT2 absolute values ???

Answer : No !!



Hence stick to the left of the curve.

Silicon :
For signals of positive charge :

VT1 = 0 constant, VT2 variable

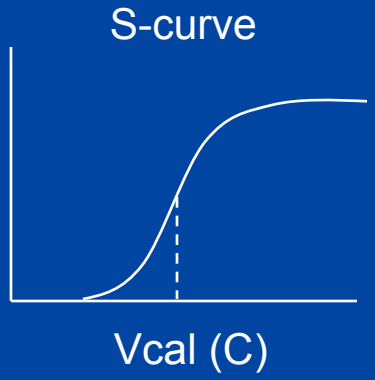
GEMs :
For signals of negative charge :

VT2 = 0 constant, VT1 variable

Positive Threshold	$VT1 = 0$	$VT2 = variable$
Negative Threshold	$VT1 = variable$	$VT2 = 0$

Table 29: Controlling thresholds

S-Curve



Error function fit
sigma = ENC (C)
Mean = threshold (C)

Convert to electrons :
Divide by 1.6*10^-19

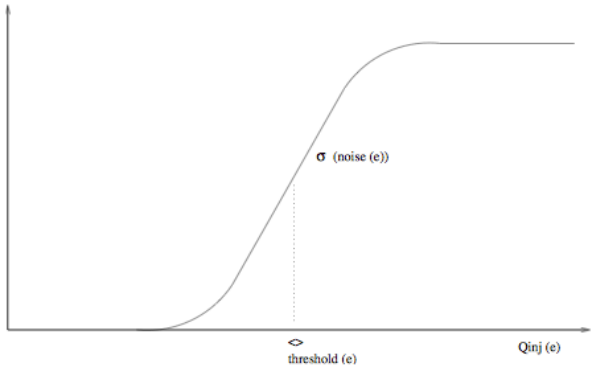
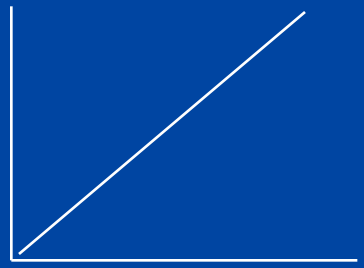
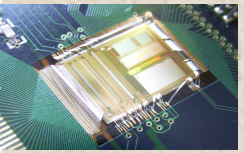
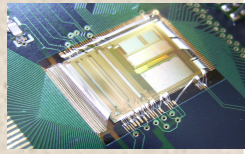


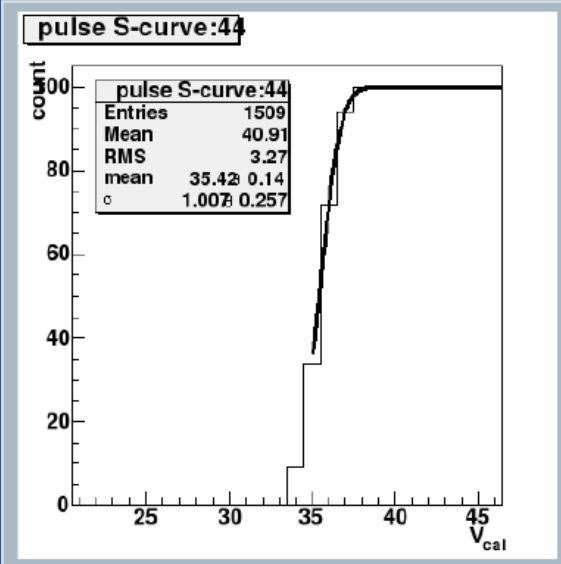
Figure 18: The S-curve

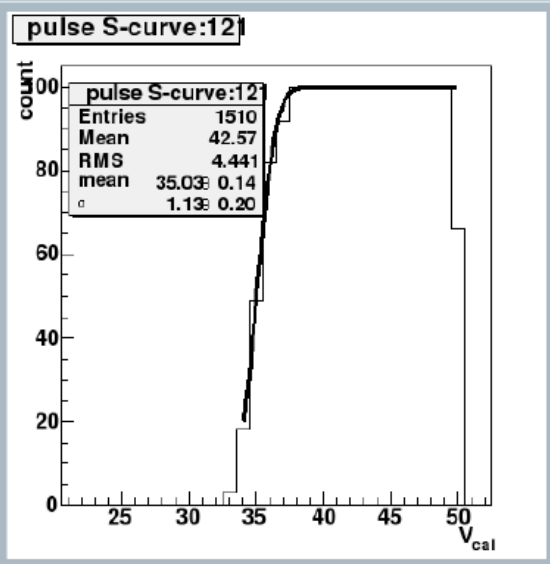


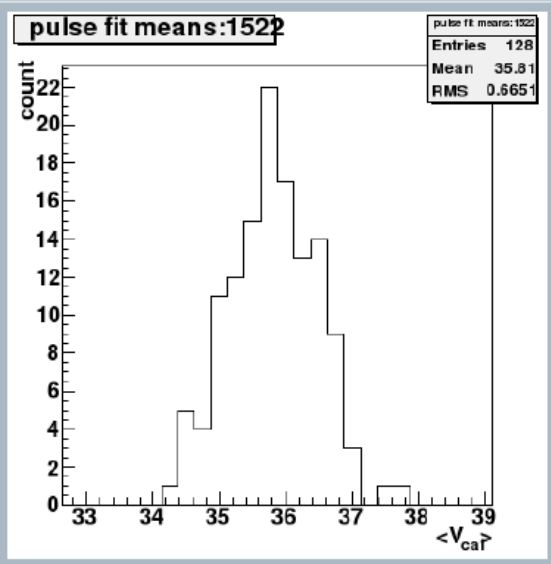


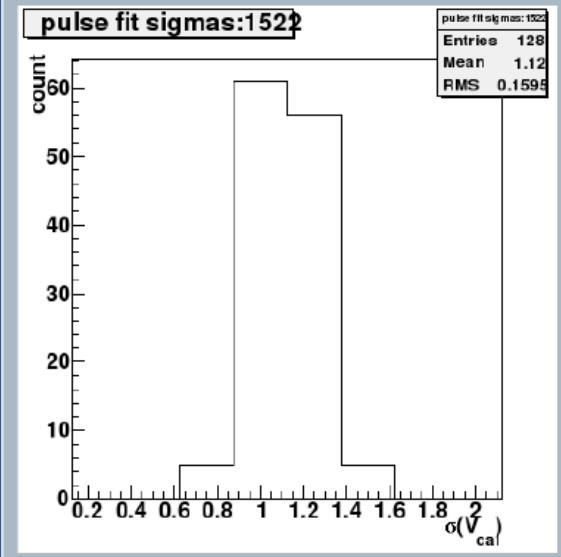
Example of TOTEM S-curves

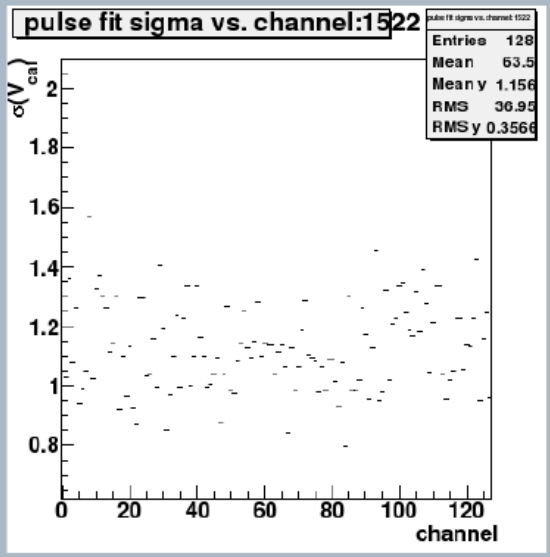


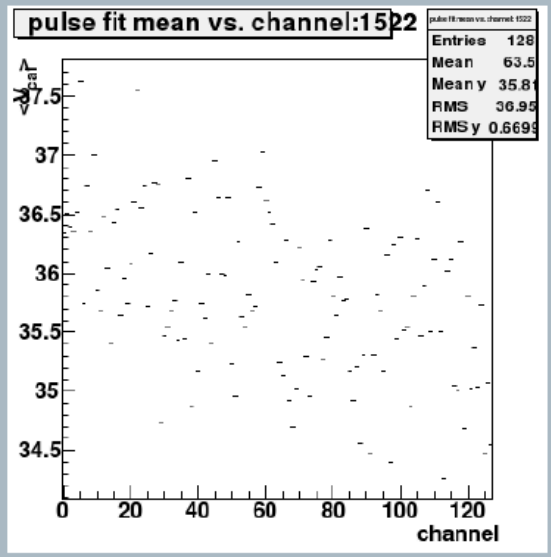






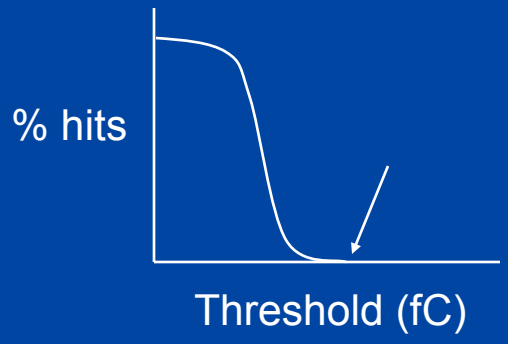


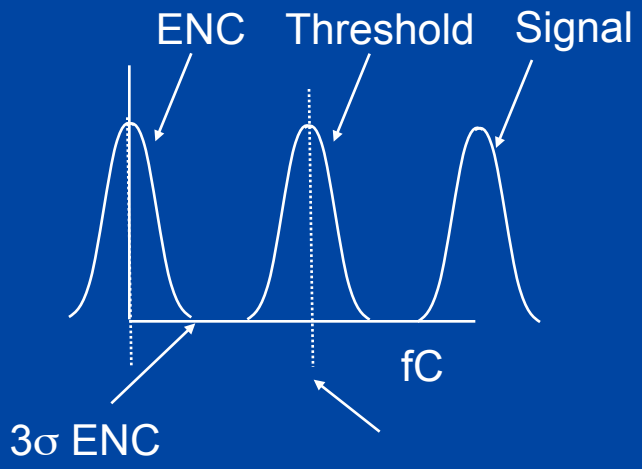




Minimum noise free threshold

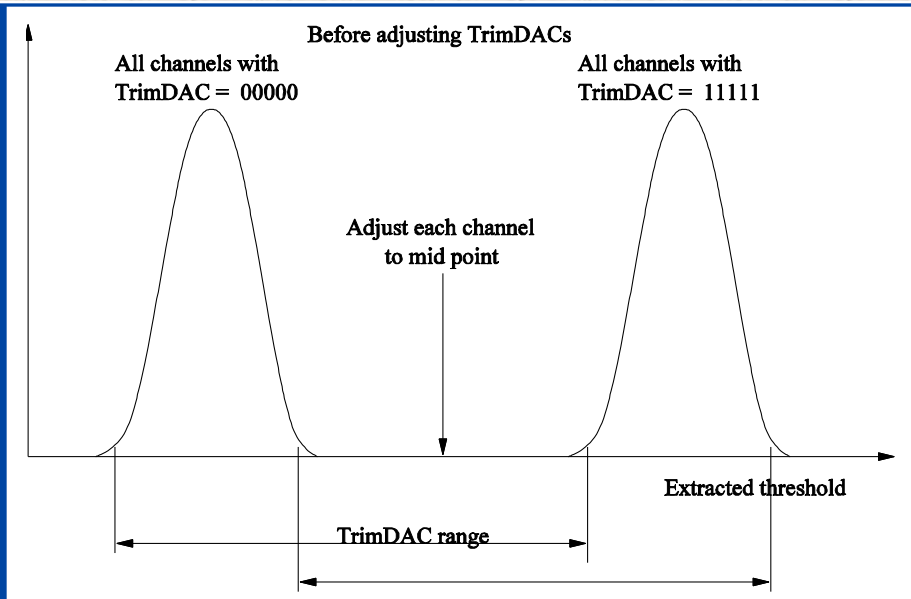
Sweep threshold and monitor hits on the S bits both with and without detector connected.

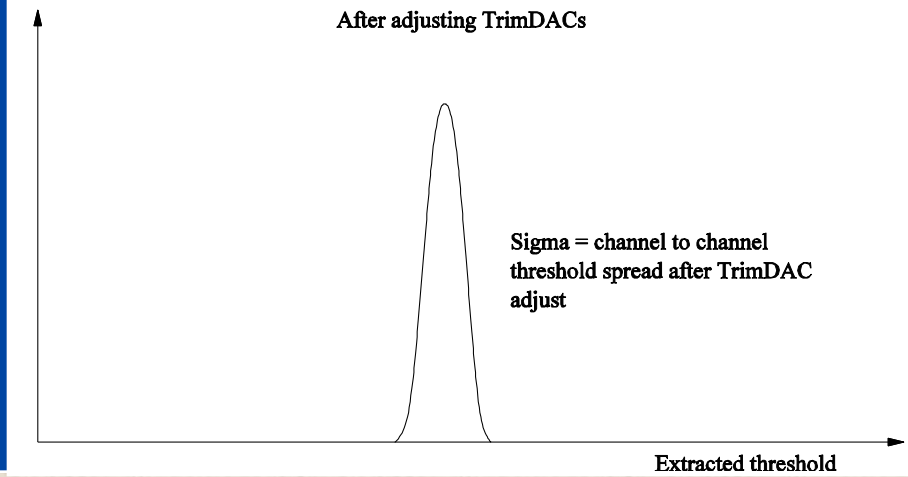




Minimum threshold $= \sqrt{(ENC^2 + Threshold\ \sigma^2)}$ * 6

Trim-DAC functionality





5 bit TrimDAC for each channel

3 bits for TrimDAC range settings

Constant threshold :

1, Measure thresholds for all channels with TrimDACs = 00000 & 11111

2, Select TrimDAC range to have the smallest gap possible between the two histograms.

3, For each channel, adjust TrimDAC to central point.

OR

Constant clarity :

1, Adjust TrimDAC for each channel to achieve constant

Threshold / (S/N)

Within limits, depends on the S/N variations of the detector.

Trimming thresholds

i)	For a given threshold setting two histograms can be made of measured thresholds for all channels, one with all TrimDAC settings = 00000 and the other with TrimDAC settings 11111.
ii)	If these histograms are well separated, the TrimDAC range should be adjusted so that the two histograms are as close as possible without overlap.
iii)	On a channel by channel basis; the TrimDAC should be adjusted to the midpoint between the two histograms.
iv)	A new histogram of extracted values with adjusted TrimDAC values should give a smaller sigma for the spread.

Table 30: Trimming of thresholds

Requires automated loop from thresholds measured from s-curves to adjusted trimDAC settings.

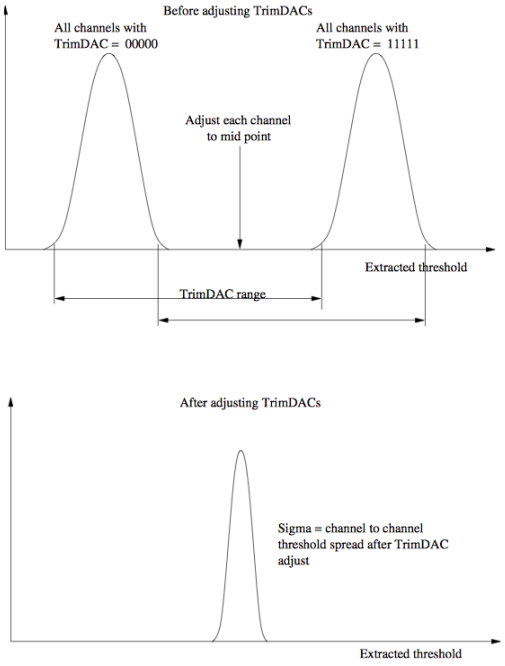
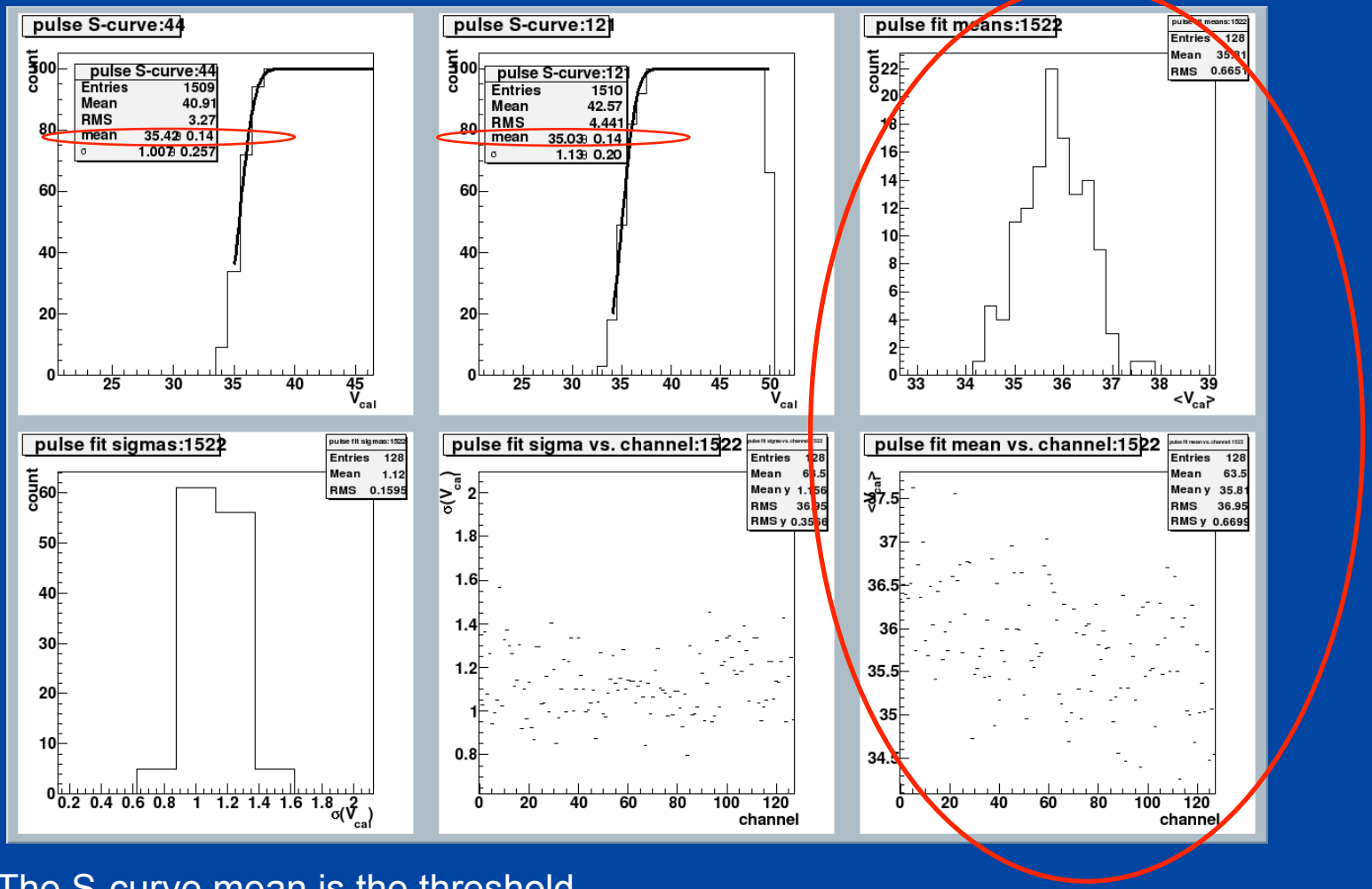


Figure 19: Trimming the thresholds

Measuring thresholds

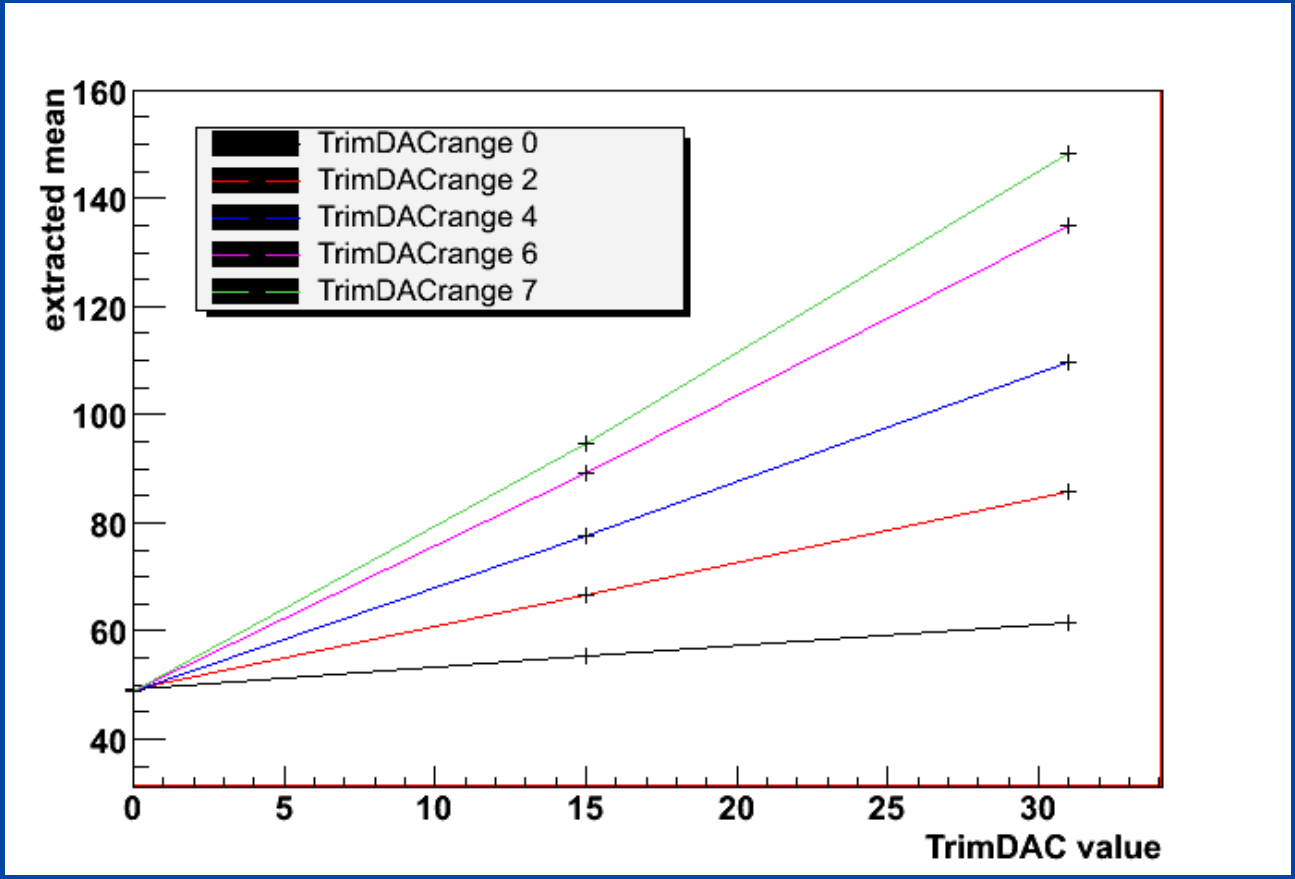


The S-curve mean is the threshold.

Note : VCal is on the x-axis in order to be able to express threshold in terms of input charge needed to go through the threshold.

TrimDAC range (measured)

Y-axis is VCal

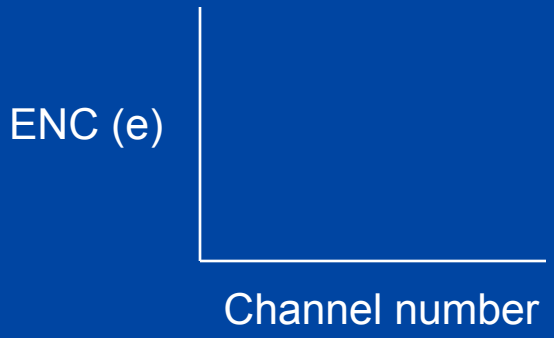


TrimDAC range 7, ΔVcal = ~ 100 ➔ 100 * 8^{-17} = ~ 8 fC for RP signals
(or ~ 40% of dynamic range)

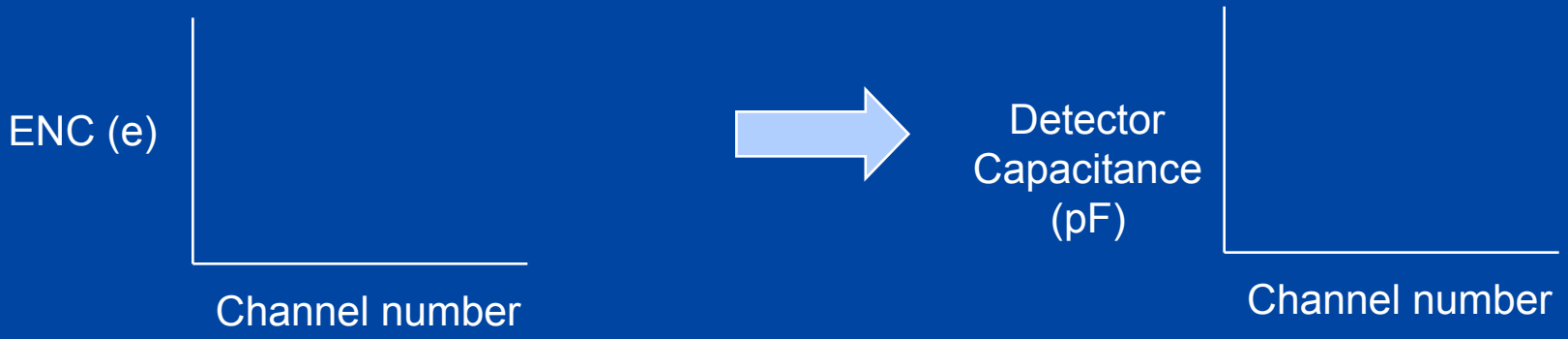
TrimDAC range 0, ΔVcal = ~ 5 ➔ 5 * 8^{-17} = ~ 0.4 fC

Extract detector capacitance

Do S-curves for all channels without detector connected.



Do S-curves for all channels with detector connected.



Detector capacitance => ENC (with det) – ENC (without det) / noise slope (~50 e/pF)