Unit 3. Hardware.

Internal / external components.

Part 2

Desarrollo de Aplicaciones Web
1er Curso
Curso 2020-2021
Autor: Vicent Bosch
vicent.bosch@ceedcv.es

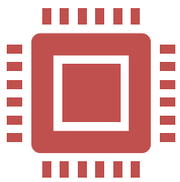
Recordatorio

ceedcv
CENTRE ESPECÍFIC D´EDUCACIÓ A DISTÀNCIA DE LA COMUNITAT VALENCIANA

Esta presentación no sustituye los apuntes disponibles en el aula virtual.

Las apuntes oficiales son los que tenéis en el aula virtual

Contents



Processors

Single Core vs Multi Core

Features

Memory

Features

RAM types

Memory Modules

Hard Disk

Interfaces

Magnetic - SSD

Addressing modes

1. Processors

ceedcv
CENTRE ESPECÍFIC D'EDUCACIÓ A DISTÀNCIA DE LA COMUNITAT VALENCIANA

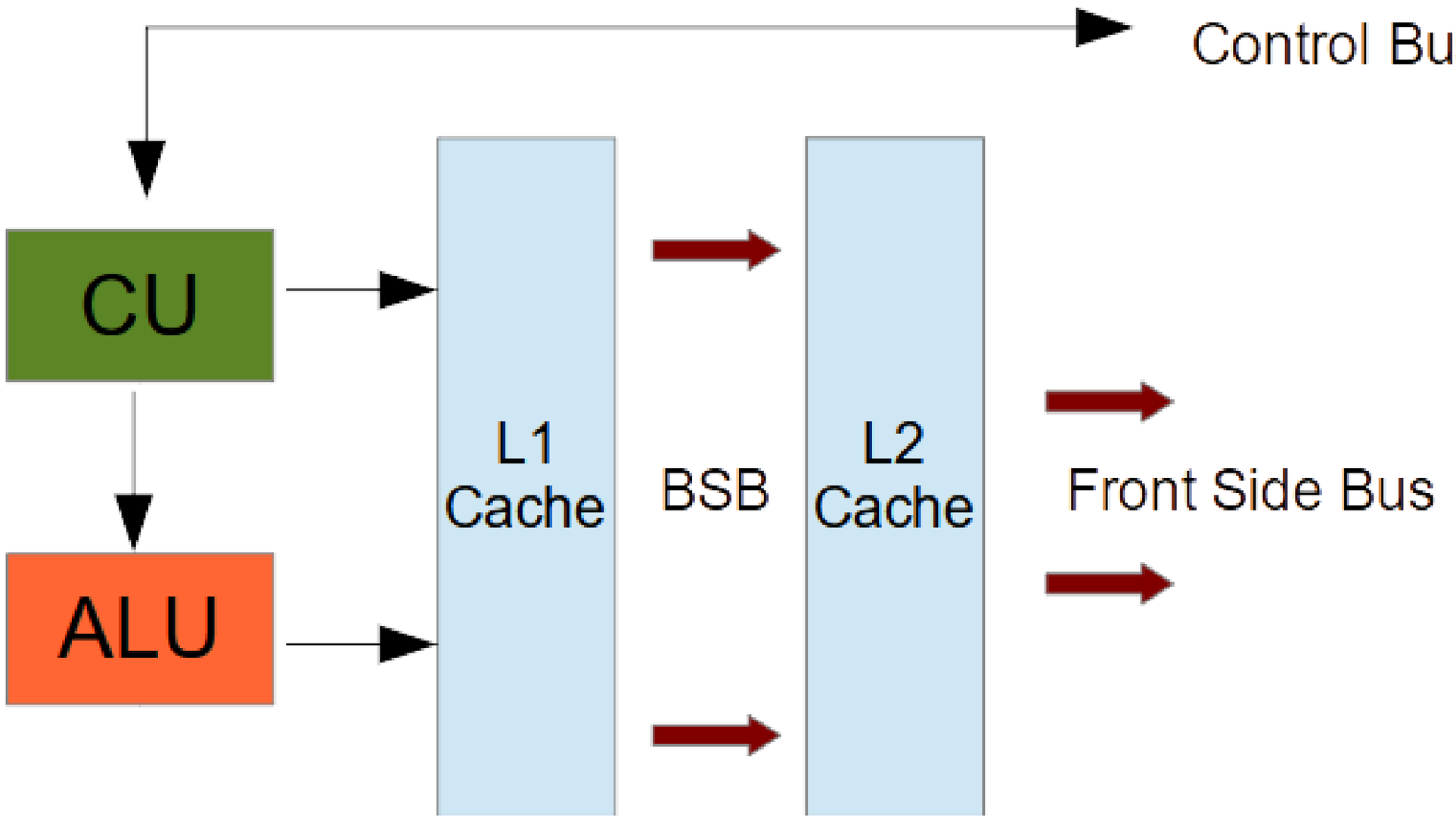
- ✓ **Frequency**:
  1 Hz → 1 operation / second
  1 MHz → 10^6 operations/second
  1 GHz → 10^9 operations/second

- ✓ **Bus speed:** *how quickly the computer can move data simultaneously. It has an effect on the computer speed*.

- ✓ **Cache:** L1, L2, L3

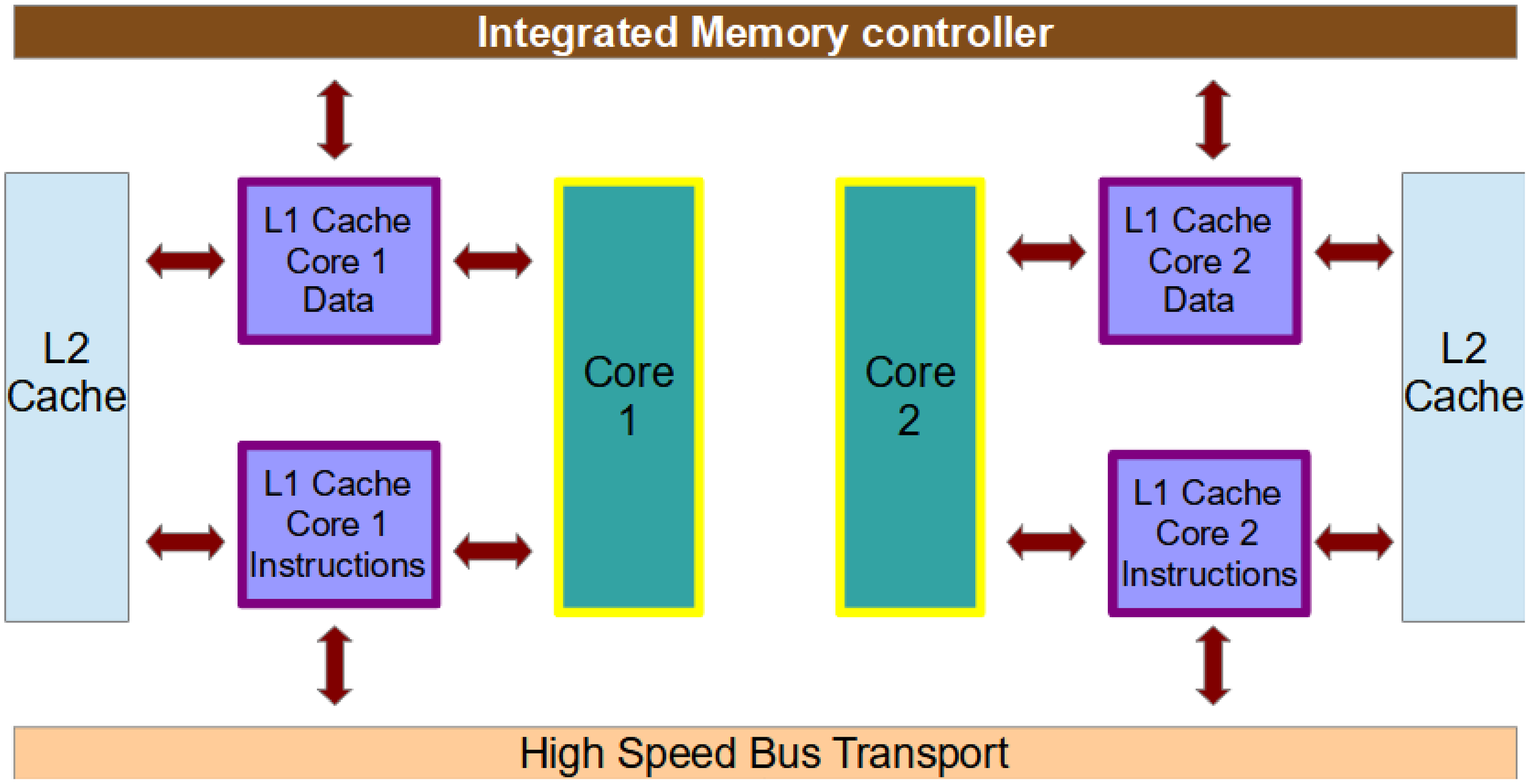
- ✓ **Example: Intel-Core i3-8100**

1. Processors. *Single Core*



1. Processors. *Multi Core*

ceedcv
CENTRE ESPECÍFIC D'EDUCACIÓ A DISTÀNCIA DE LA COMUNITAT VALENCIANA



Speccy

File View Help

ceedcv
CENTRE ESPECÍFIC D'EDUCACIÓ A DISTÀNCIA DE LA COMUNITAT VALENCIANA

- Summary
- Operating System
- CPU
- RAM
- Motherboard
- Graphics
- Storage
- Optical Drives
- Audio
- Peripherals
- Network

CPU

Intel Core i5

Cores	2
Threads	4
Name	Intel Core i5
Code Name	Skylake-U/Y
Package	Socket 1168 BGA
Technology	14nm
Specification	Intel Core i5-6200U CPU @ 2.30GHz
Family	6
Extended Family	6
Model	E
Extended Model	4E
Stepping	3
Revision	D0/K0/K1
Instructions	MMX, SSE, SSE2, SSE3, SSSE3, SSE4.1, SSE4.2, Intel 64, NX, VMX, AES, AV
Virtualization	Supported, Enabled
Hyperthreading	Supported, Enabled
Stock Core Speed	2400 MHz
Stock Bus Speed	100 MHz
Average Temperature	57 °C

Caches

L1 Data Cache Size	2 x 32 KBytes
L1 Instructions Cache Size	2 x 32 KBytes
L2 Unified Cache Size	2 x 256 KBytes
L3 Unified Cache Size	3072 KBytes

Cores

	Core Speed	Multiplier	Bus Speed	Temperature	Threads
Core 0	1497.1 MHz	x 15.0	99.8 MHz	56 °C	APIC ID: 0, 1
Core 1	1896.3 MHz	x 19.0	99.8 MHz	58 °C	APIC ID: 2, 3

Processors

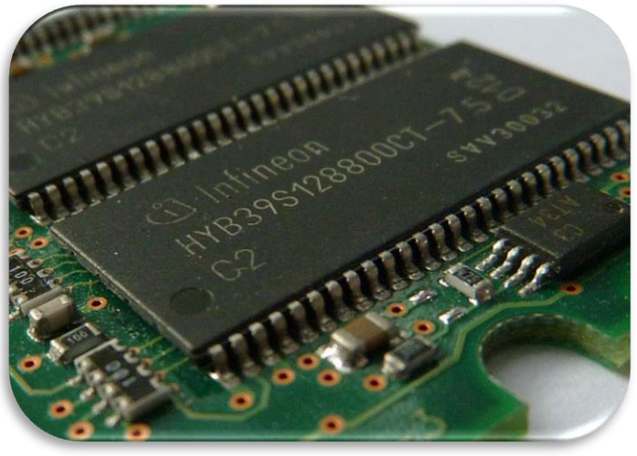
Example

v1.32.740

Check for updates...

2. Memory. *Organization*

- ✓ A memory cell stores 1 bit of information.
- ✓ Memory cells are organized in a form of a matrix (rows and columns), thus forming the memory chip. Ram_chip

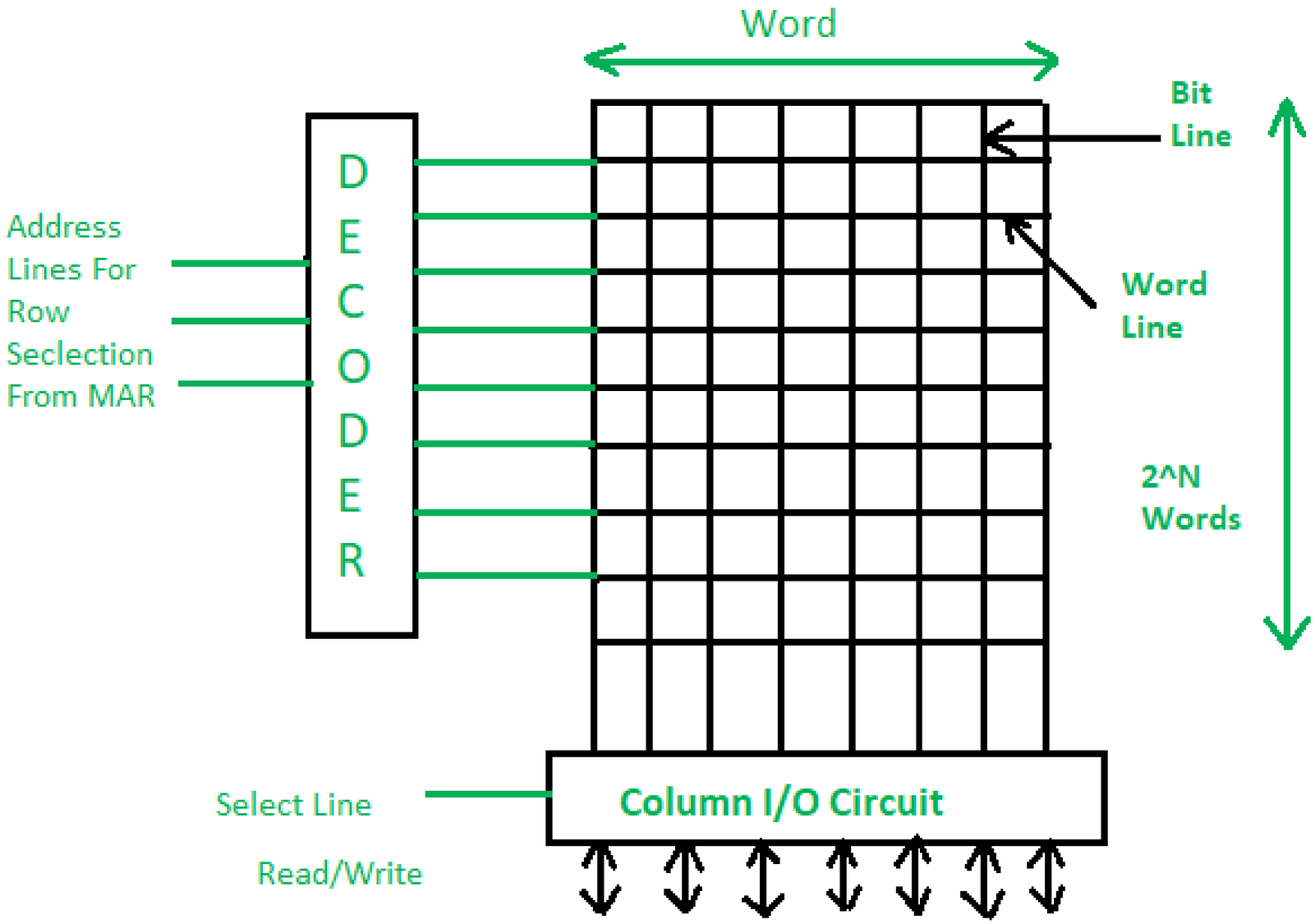


- ✓ Memory controller: *manages requests for data*
- ✓ Bus memory: address and data. *Do you want to know more?* here

2. Memory. *Organization*

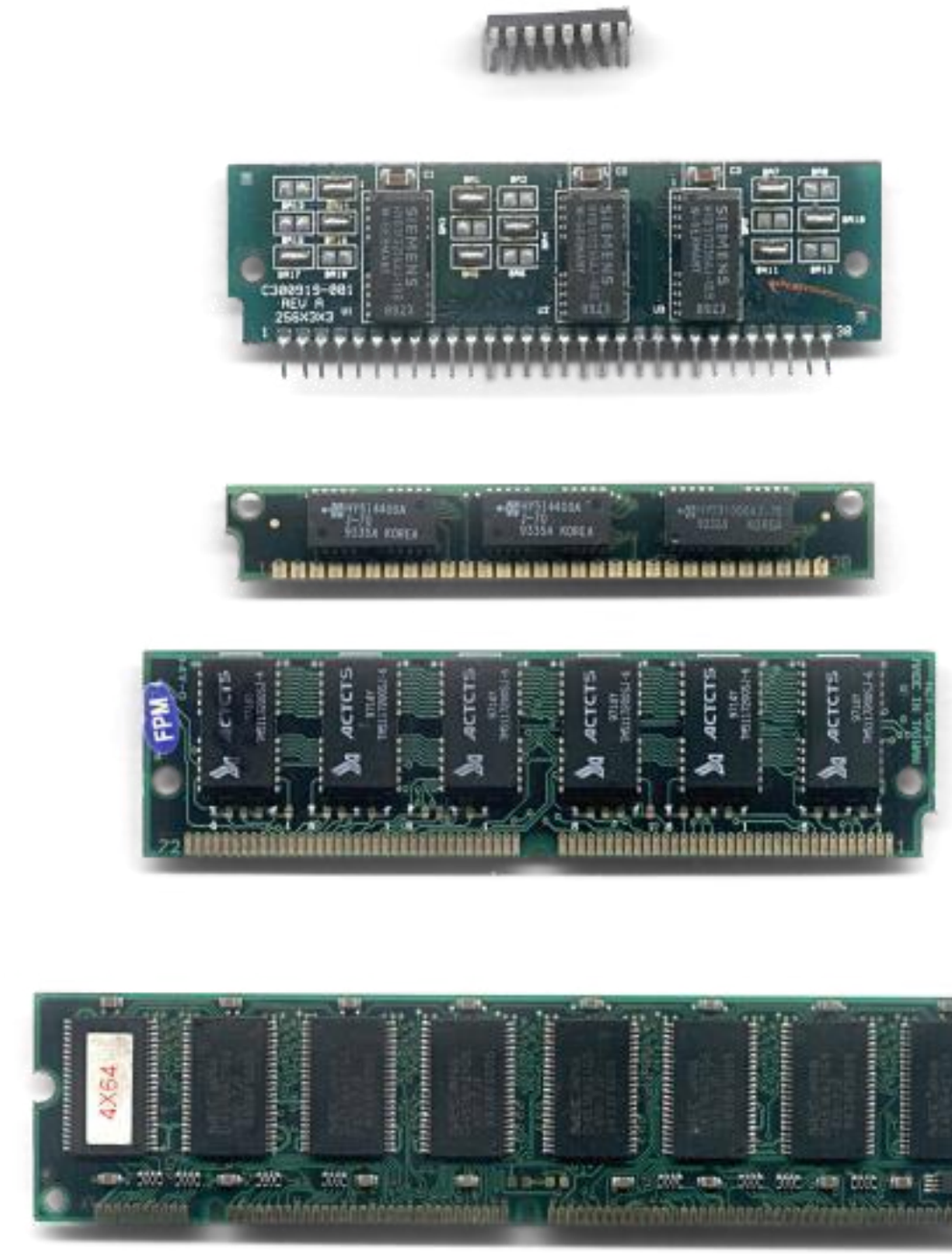
ceedcv
CENTRE ESPECÍFIC D'EDUCACIÓ A DISTÀNCIA DE LA COMUNITAT VALENCIANA

✓ *Do you want to know more?* here



2D Memory Organization

2. Memory.
RAM types



[Source]

2. Memory.

RAM types. DDR-DDR2

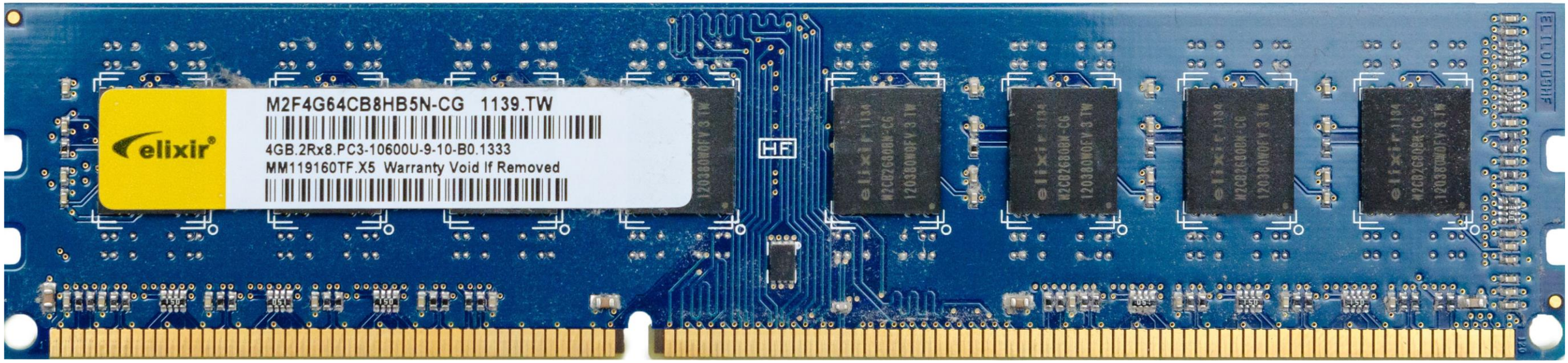
Source

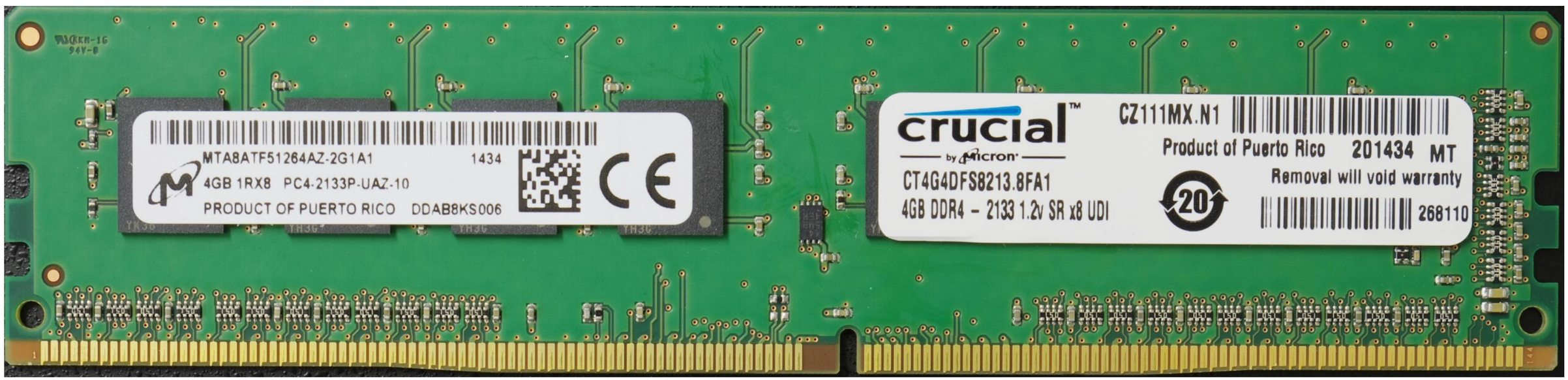
2. Memory.

RAM types. DDR3-DDR4

Source DDR3

Source DDR4





2. Memory. *DDR*

ceedcv
CENTRE ESPECÍFIC D'EDUCACIÓ A DISTÀNCIA DE LA COMUNITAT VALENCIANA

- ✓ Double transfer in one clock cycle.

  1Mhz → 2 x 10^6 transfers / second

- ✓ DDR4 ECC → detects errors and if possible, corrects.
- ✓ For example, DDR2-400 (400 MT/s)

  *(400*64 bits-bus)/8 → 3200 MB/s*

3. Hard Disk. *Interfaces*

ceedcv
CENTRE ESPECÍFIC D'EDUCACIÓ A DISTÀNCIA DE LA COMUNITAT VALENCIANA

- ✓ IDE:

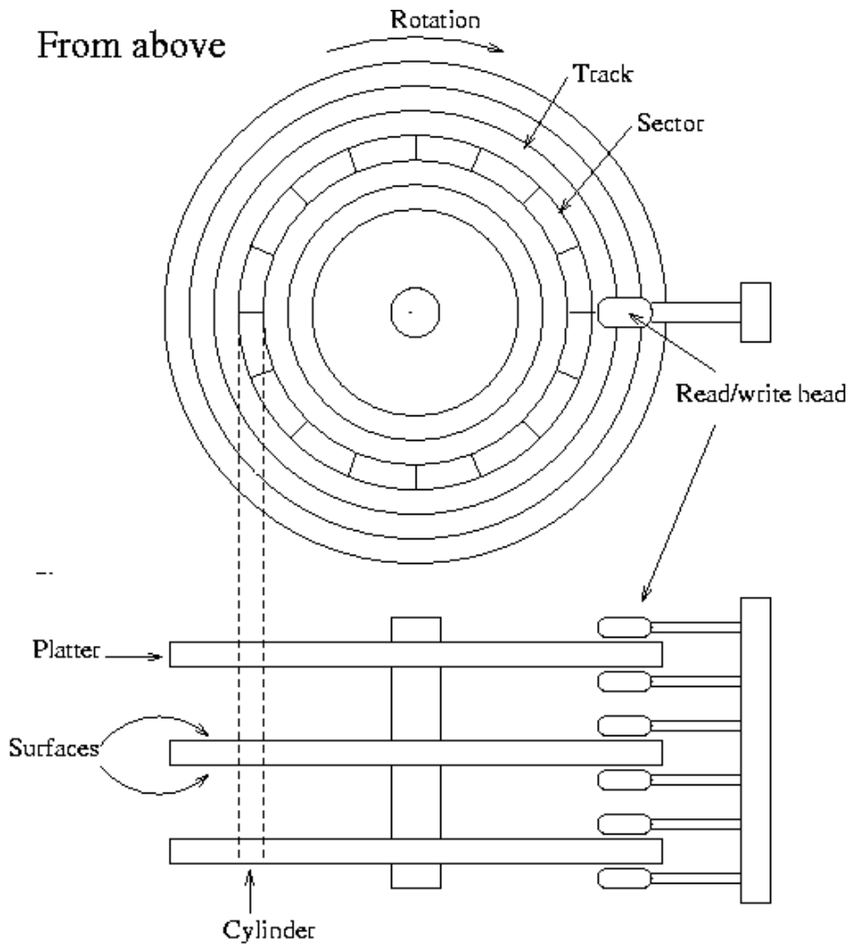
  https://www.computerhope.com/jargon/i/ide.htm

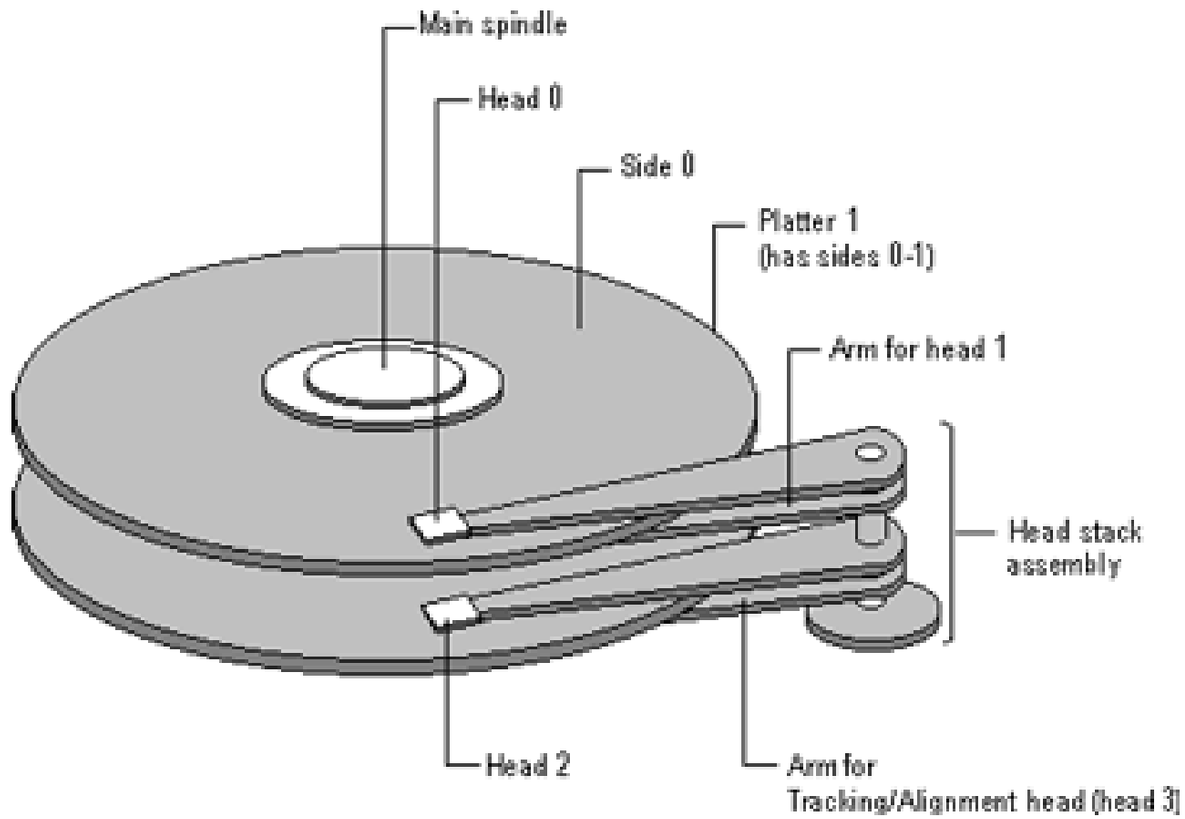
- ✓ SATA:

  https://www.computerhope.com/jargon/s/sata.htm

3. Hard Disk.
Magnetic

- ✓ Addressing modes: CHS and LBA
- ✓ CHS to LBA mapping

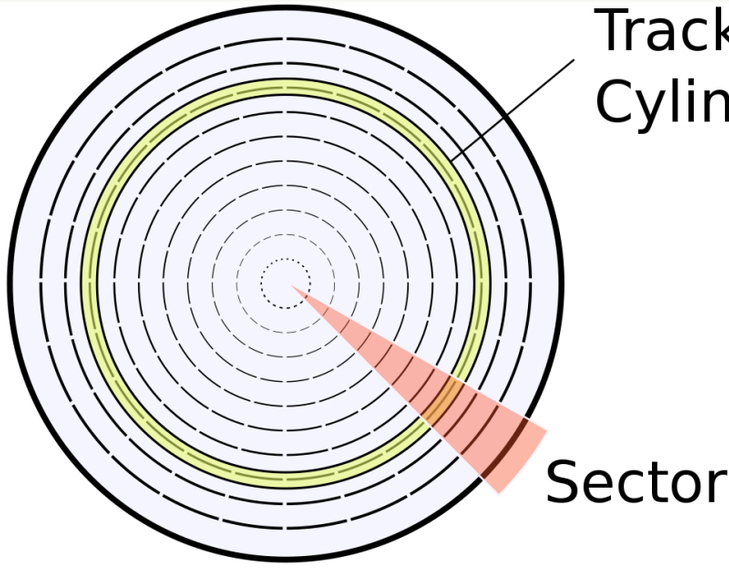


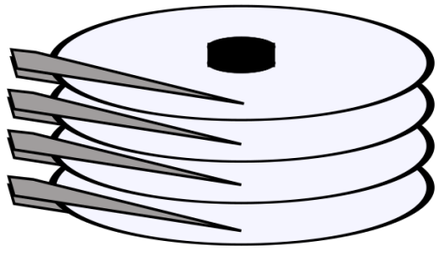


3. Hard Disk.
Magnetic

- ✓ Addressing modes: CHS

- ✓ **CHS addressing:** identifying individual sectors (physical block of data) on a disk by their position in a track, where the track is determined by the head and cylinder numbers.
- ✓ For a disk with **65536** cylinders, **16** heads and **256** sectors/track, with **512** bytes/sector:
- ✓ **65536** X **16** X **256** X **512** → *128 GB* (aprox.)





3. Hard Disk.
Magnetic

✓ Addressing modes: LBA

- ✓ **LBA addressing:** specify the location of the blocks of data stored in the hard disk.
- ✓ Blocks are located by an integer index.
  - First block→ LBA 0
  - Second block → LBA 1
  - And so on
- ✓ For a disk with a capacity of *128 GiB* (aprox.) and a sector size of 512 bytes:
  - First convert 128 GiB to bytes and then divide into 512 bytes.
  - *LBA*: *268435456* (sectors)
- ✓ **What's the capacity in GiB of this hard disk?**

3. Hard Disk.
Magnetic

✓ CHS to LBA mapping

✓ CHS tuples can be mapped to LBA address with the following formula:

LBA = (C × NH + H) × NS + (S − 1)

✓ For 1020 cylinders, 16 heads and 63 sectors of a disk → LBA 1028160 (sectors)

✓ The address CHS 10 12 51 is

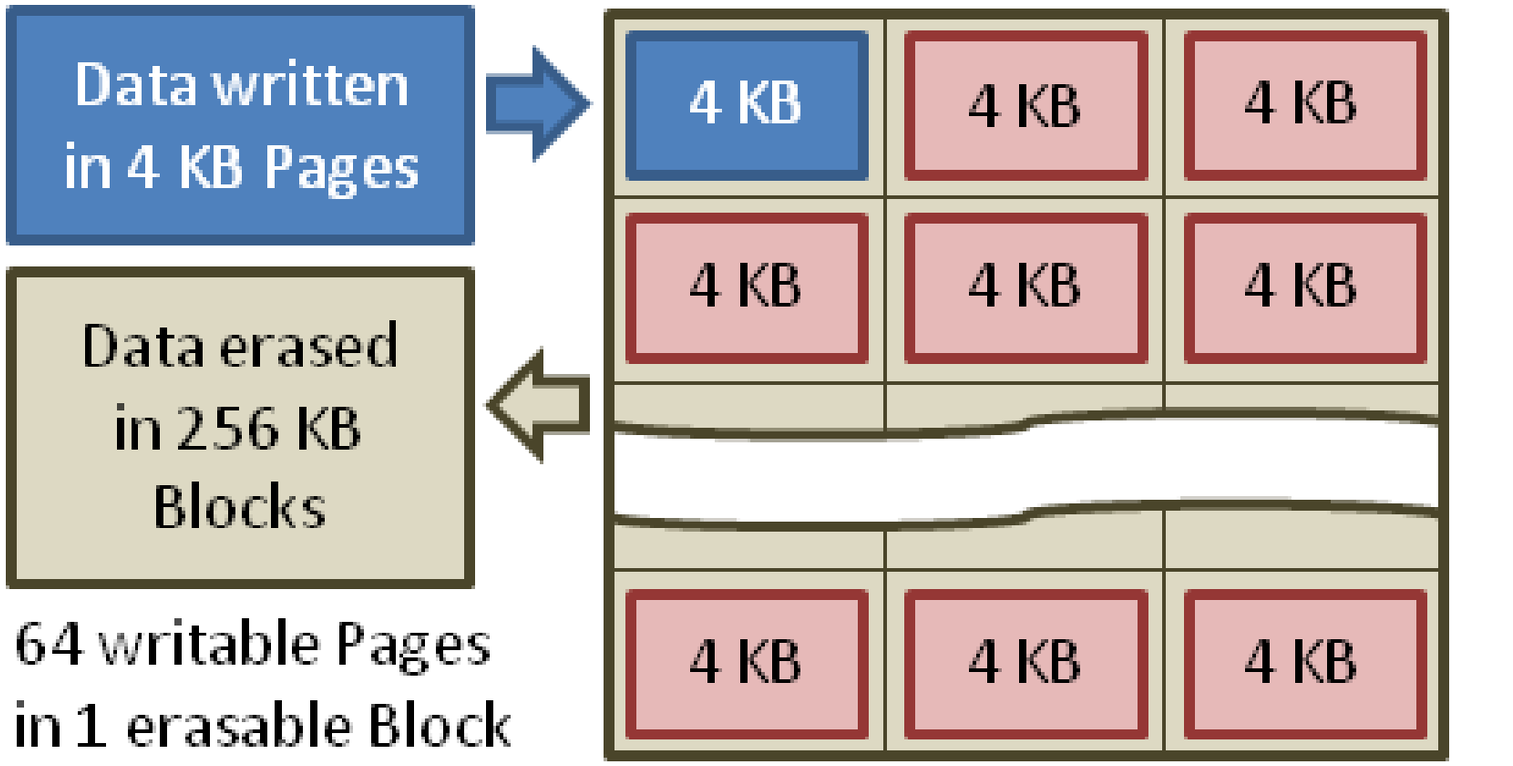
LBA=(10 × 16+12)× 63 + (51-1)

LBA=10886

https://en.wikipedia.org/wiki/Logical_block_addressing

3. Hard Disk.
SSD

- ✓ Flash technology
- ✓ Addressing mode: LBA
- ✓ More about addressing here: SSD Structure and basic working



Source

Questions?

ceedcv
CENTRE ESPECÍFIC
D´EDUCACIÓ A DISTÀNCIA DE
LA COMUNITAT VALENCIANA