Computer Architectures
lab 3
WinMIPS64 ILP

Considering the MIPS64 architecture presented in the following:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- FP multiplier unit: pipelined 8 stages
- FP arithmetic unit: pipelined 4 stages
- FP divider unit: not pipelined unit, 12 clock cycles
- branch delay slot: 1 clock cycle
- forwarding is enabled.

1) Using the program you wrote previously for the *winMIPS64* architecture, able to implement the following piece of code described at high-level:

```
for (i = 1; i <= 100; i++){
        v5[i] = v1[i]*v2[i];
        v6[i] = v2[i]/v3[i];
        v7[i] = v1[i]+v4[i];
}
```

   a. Assume that the vectors v1[], v2[], v3[], and v4[] are allocated previously in memory and contains 100 double precision floating point values; assume also that v3[] does not contain 0 values. Additionally, the vectors v5[], v6[], and v7[] are free vectors also allocated in memory.

   Compute by hand the number of clock cycles required to execute the program and compares the results obtained using the simulator.

2) Starting from the previous program and exploiting the optimization techniques *static scheduling*, *loop-unrolling*, and *register renaming*, and assuming that the *branch delay slot* is enabled, rewrite the initial program. Compute by hand the number of clock cycles required to execute the new program and compare the statistics values provided by the simulator.

3) Disable the *branch delay slot* and enable the *Branch Target Buffer*. Simulate once again the two programs used previously and compare the results. When the branch target buffer is enabled, is the behavior of the program as expected?

4) Write a new program for the *winMIPS64* architecture, able to implement the following piece of code described at high-level:

```
for (i = 1; i <= 100; i++){
        v5[i] = (v1[i]/v2[i] + v4[i]/v3[i] + v4[i]);
}
```

a. Assume that the vectors v1[], v2[], v3[], and v4[] are allocated previously in memory and contains 100 double precision floating point values; assume also that v2[] and v3[] does not contain 0 values. Additionally, the vector v5[] is a free vector also allocated in memory.

Compute by hand the number of clock cycles required to execute the program and compares the results obtained using the simulator.

5) Starting from the previous program and exploiting the optimization techniques *static scheduling*, *loop-unrolling*, and *register renaming*, and assuming that the *branch delay slot* is enabled, rewrite the initial program. Compute by hand the number of clock cycles required to execute the new program and compare the statistics values provided by the simulator.

6) Disable the *branch delay slot* and enable the *Branch Target Buffer*. Simulate once again the two programs used previously and compare the results. When the branch target buffer is enabled, is the behavior of the program as expected?