Schedule and Practical Cache 2

1. First Simulation:

```
---Dinero IV cache simulator, version 7
---Written by Jan Edler and Mark D. Hill
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---See -copyright option for details

---Summary of options (-help option gives usage information).

-l1-usize 128
-l1-ubsize 16
-l1-usbsize 16
-l1-uassoc 8
-l1-urepl l
-l1-ufetch d
-l1-uwalloc a
-l1-uwback a
-skipcount 0
-flushcount 0
-maxcount 0
-stat-interval 0
-informat d
-on-trigger 0x0
-off-trigger 0x0

---Simulation begins.
---Simulation complete.
l1-ucache
 Metrics                    Total          Instrn          Data          Read          Write          Misc
 -----------------          ------         ------         ------         ------         ------         ------
 Demand Fetches               1000            351            649            321            328              0
  Fraction of total          1.0000         0.3510         0.6490         0.3210         0.3280         0.0000

 Demand Misses                 873            311            562            277            285              0
  Demand miss rate           0.8730         0.8860         0.8659         0.8629         0.8689         0.0000

 Multi-block refs                 0
 Bytes From Memory            13968
 ( / Demand Fetches)         13.9680
 Bytes To Memory               4912
 ( / Demand Writes)          14.9756
 Total Bytes r/w Mem          18880
 ( / Demand Fetches)         18.8800

---Execution complete.
```

Overall Cache Performance:

- Total Demand Fetches: 1,000 memory accesses
- Total Demand Misses: 873 misses
- Overall Miss Rate: 87.3% (very high)

Access Type Breakdown:

Type	**Fetches**	**Misses**	**Miss Rate**
Instruction	351	311	88.6%
Data	649	562	86.6%
Read	371	277	74.7%
Write	328	285	86.9%

Memory Traffic Analysis:

- Bytes from Memory: 13,968 bytes (due to misses)
- Bytes to Memory: 4,912 bytes (write-backs)
- Total Memory Traffic: 18,880 bytes
- Traffic Amplification: 18.9x (18,880 ÷ 1,000 accesses)\

2. Second Simulation:

```
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---Summary of options (-help option gives usage information).

-l1-usize 128
-l1-ubsize 4
-l1-usbsize 4
-l1-uassoc 1
-l1-urepl l
-l1-ufetch d
-l1-uwalloc a
-l1-uwback a
-skipcount 0
-flushcount 0
-maxcount 0
-stat-interval 0
-informat d
-on-trigger 0x0
-off-trigger 0x0

---Simulation begins.
---Simulation complete.
l1-ucache
 Metrics                    Total          Instrn          Data          Read          Write          Misc
 -----------------          ------         ------         ------         ------         ------         ------
 Demand Fetches               1088              0            1088          1024             64              0
  Fraction of total          1.0000         0.0000         1.0000        0.9412         0.0588         0.0000

 Demand Misses                 152              0             152            88             64              0
  Demand miss rate           0.1397         0.0000         0.1397        0.0859         1.0000         0.0000

 Multi-block refs                 0
 Bytes From Memory              352
 ( / Demand Fetches)           0.3235
 Bytes To Memory                256
 ( / Demand Writes)            4.0000
 Total Bytes r/w Mem            608
 ( / Demand Fetches)           0.5588

---Execution complete.
```

Number of Misses and Hits:

a) Total Demand Misses: 152 Total Demand Hits: 1088 - 152 = 936 hits

Breakdown by type:

- Instruction Misses: 0 (all instruction accesses hit)
- Data Misses: 152

- Read Misses: 88
- Write Misses: 64

b) Miss Rate and Hit Rate: Overall Miss Rate: 13.97% (much better than previous 87.3%)
Overall Hit Rate: 86.03%

By access type:

- Instructions: 0% miss rate (100% hit rate)
- Data: 13.97% miss rate (86.03% hit rate)
- Reads: 8.59% miss rate
- Writes: 100% miss rate (all writes miss - indicates write-allocate policy)

Memory Traffic:

- Bytes from Memory: 352 bytes (due to misses)
- Bytes to Memory: 256 bytes (write-backs)
- Total Memory Traffic: 608 bytes
- Traffic per access: 0.5588 bytes/access

3. Third Simulation:

a) Change the block size to 8 words:

```
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---See -copyright option for details

---Summary of options (-help option gives usage information).

-l1-usize 128
-l1-ubsize 8
-l1-usbsize 8
-l1-uassoc 1
-l1-urepl l
-l1-ufetch d
-l1-uwalloc a
-l1-uwback a
-skipcount 0
-flushcount 0
-maxcount 0
-stat-interval 0
-informat d
-on-trigger 0x0
-off-trigger 0x0

---Simulation begins.
---Simulation complete.
l1-ucache
 Metrics                    Total          Instrn          Data          Read          Write          Misc
 -----------------          ------         ------         ------         ------         ------         ------
 Demand Fetches               1088              0          1088          1024             64              0
  Fraction of total          1.0000         0.0000         1.0000        0.9412         0.0588         0.0000

 Demand Misses                 136              0           136            72             64              0
  Demand miss rate           0.1250         0.0000         0.1250        0.0703         1.0000         0.0000

 Multi-block refs                0
 Bytes From Memory            1088
 ( / Demand Fetches)         1.0000
 Bytes To Memory               512
 ( / Demand Writes)          8.0000
 Total Bytes r/w Mem          1600
 ( / Demand Fetches)         1.4706

---Execution complete.
```

Number of Misses and Hits: Total Demand Fetches: 1088

- Demand Misses: 136

  → Demand Hits = Total Fetches - Misses = 1088 - 136 = 952

Access Type	**Fetches**	**Misses**	**Hits**
Instruction	0	0	0
Data	1088	136	952

Read	1024	72	952
Write	64	64	0

- All writes missed (100% miss rate).
- Read miss rate = 72 / 1024 = 7.03%
- Write miss rate = 64 / 64 = 100%
- Overall miss rate = 136 / 1088 = 12.5%

Metric	**Value**
Total Accesses	1088
Cache Hits	952
Cache Misses	136
Cache Hit Time	1 cycle
Cache Miss Time	10 cycles
Total Access Time	2312 cycles
Avg Access Time (AMAT)	2.124 cycles

b) Change the block size to 16 words:

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---Summary of options (-help option gives usage information).

-l1-usize 128
-l1-ubsize 16
-l1-usbsize 16
-l1-uassoc 1
-l1-urepl l
-l1-ufetch d
-l1-uwalloc a
-l1-uwback a
-skipcount 0
-flushcount 0
-maxcount 0
-stat-interval 0
-informat d
-on-trigger 0x0
-off-trigger 0x0

---Simulation begins.
---Simulation complete.
l1-ucache
 Metrics                    Total          Instrn          Data          Read          Write          Misc
 -----------------          ------         ------         ------         ------         ------         ------
 Demand Fetches               1088              0          1088          1024             64              0
  Fraction of total          1.0000         0.0000        1.0000        0.9412         0.0588         0.0000

 Demand Misses                 132              0           132            68             64              0
  Demand miss rate            0.1213         0.0000        0.1213        0.0664         1.0000         0.0000

 Multi-block refs                0
 Bytes From Memory            2112
 ( / Demand Fetches)         1.9412
 Bytes To Memory              1024
 ( / Demand Writes)         16.0000
 Total Bytes r/w Mem          3136
 ( / Demand Fetches)         2.8824

---Execution complete.
```

Metric	**Value**
Total Accesses	1088
Cache Hits	956
Cache Misses	132

Cache Hit Time	1 cycle
Cache Miss Time	10 cycles
Total Access Time	2276 cycles
Avg Access Time (AMAT)	2.092 cycles/access

4. Fourth Simulation:

a) Change the block size to 8 words:

```
---Dinero IV cache simulator, version 7
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---All rights reserved.
---Copyright (C) 1985, 1989 Mark D. Hill.  All rights reserved.
---See -copyright option for details

---Summary of options (-help option gives usage information).

-l1-usize 128
-l1-ubsize 8
-l1-usbsize 8
-l1-uassoc 16
-l1-urepl l
-l1-ufetch d
-l1-uwalloc a
-l1-uwback a
-skipcount 0
-flushcount 0
-maxcount 0
-stat-interval 0
-informat d
-on-trigger 0x0
-off-trigger 0x0

---Simulation begins.
---Simulation complete.
l1-ucache
 Metrics                    Total          Instrn          Data          Read          Write          Misc
 -----------------          ------         ------         ------         ------         ------         ------
 Demand Fetches               1088              0          1088          1024            64              0
  Fraction of total          1.0000         0.0000         1.0000        0.9412         0.0588         0.0000

 Demand Misses                  24              0            24            16             8              0
  Demand miss rate          0.0221         0.0000         0.0221        0.0156         0.1250         0.0000

 Multi-block refs               0
 Bytes From Memory            192
 ( / Demand Fetches)        0.1765
 Bytes To Memory               64
 ( / Demand Writes)         1.0000
 Total Bytes r/w Mem           256
 ( / Demand Fetches)        0.2353

---Execution complete.
```

b) Change the block size to 16 words:

```
---Dinero IV cache simulator, version 7
---Written by Jan Edler and Mark D. Hill
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---Copyright (C) 1985, 1989 Mark D. Hill.  All rights reserved.
---See -copyright option for details

---Summary of options (-help option gives usage information).

-l1-usize 128
-l1-ubsize 16
-l1-usbsize 16
-l1-uassoc 8
-l1-urepl l
-l1-ufetch d
-l1-uwalloc a
-l1-uwback a
-skipcount 0
-flushcount 0
-maxcount 0
-stat-interval 0
-informat d
-on-trigger 0x0
-off-trigger 0x0

---Simulation begins.
---Simulation complete.
l1-ucache
 Metrics                    Total         Instrn          Data          Read         Write          Misc
 -----------------          ------        ------        ------        ------        ------        ------
 Demand Fetches               1088             0          1088          1024            64             0
  Fraction of total         1.0000        0.0000        1.0000        0.9412        0.0588        0.0000

 Demand Misses                  12             0            12             8             4             0
  Demand miss rate          0.0110        0.0000        0.0110        0.0078        0.0625        0.0000

 Multi-block refs               0
 Bytes From Memory            192
 ( / Demand Fetches)        0.1765
 Bytes To Memory               64
 ( / Demand Writes)         1.0000
 Total Bytes r/w Mem          256
 ( / Demand Fetches)        0.2353

---Execution complete.
```

Metric	**8 words**	**16 words**
Total Accesses	1088	1088
Misses	24	12
Hits	1064	1076

Total Access Time	1304 cycles	1196 cycles
Average Access Time (AMAT)	1.199 cycles/access	1.099 cycles/access