B06602035

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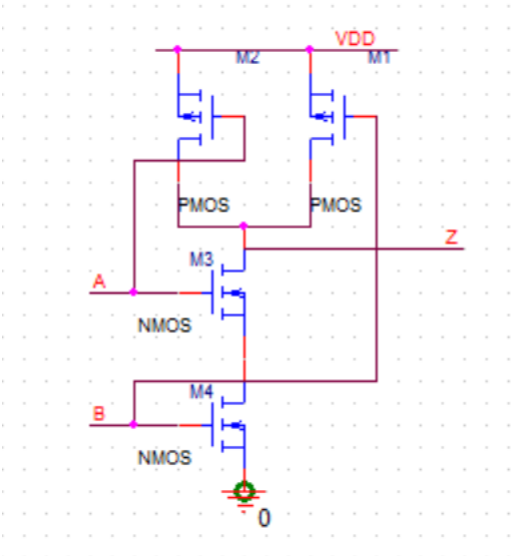
1.

(5)ND2

a.



b.

Inputs: A, B, VDD, GND

Outputs: Z

c. truth table

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

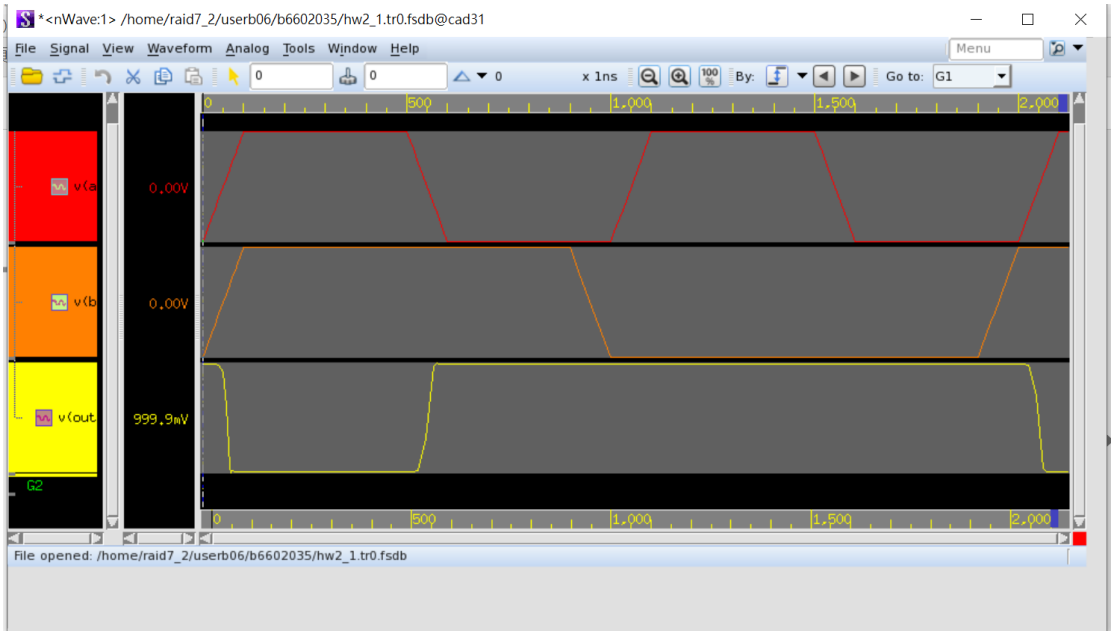
d.

hw2_1.sp

```
************************************************
.inc '90nm_bulk.l'
.SUBCKT Inv DVDD GND A B Out
*.PININFO DVDD:I GND:I A:I B:I Out:O
MM1             Out B DVDD DVDD PMOS l=0.1u w=0.5u m=1
MM2             Out A DVDD DVDD PMOS l=0.1u w=0.5u m=1
```

```
MM3                Out A N144540 N144540 NMOS l=0.1u w=0.25u m=1
MM4                N144540 B GND GND NMOS l=0.1u w=0.25u m=1
.ENDS
*********************************************
Vdd DVDD       0      1
Vss    GND           0      0

Vin A    0        pwl (0n 0v 100n 1v 500n 1v 600n 0v 1000n 0v 1100n 1v 1500n 1v 1600n 0v
2000n 0v 2100n 1v 2500n 1v 2600n 0v 3000n 0v 3100n 1v 3500n 1v 3600n 0v);

Vin1 B        0      pwl (0n 0v 100n 1v 900n 1v 1000n 0v 1900n 0v 2000n 1v 2900n 1v 3000n 0v
4000n 0v);


x1 DVDD      GND A B    Out          Inv

.tran 10n 2.1u
.op
.option post
.end
```

e.

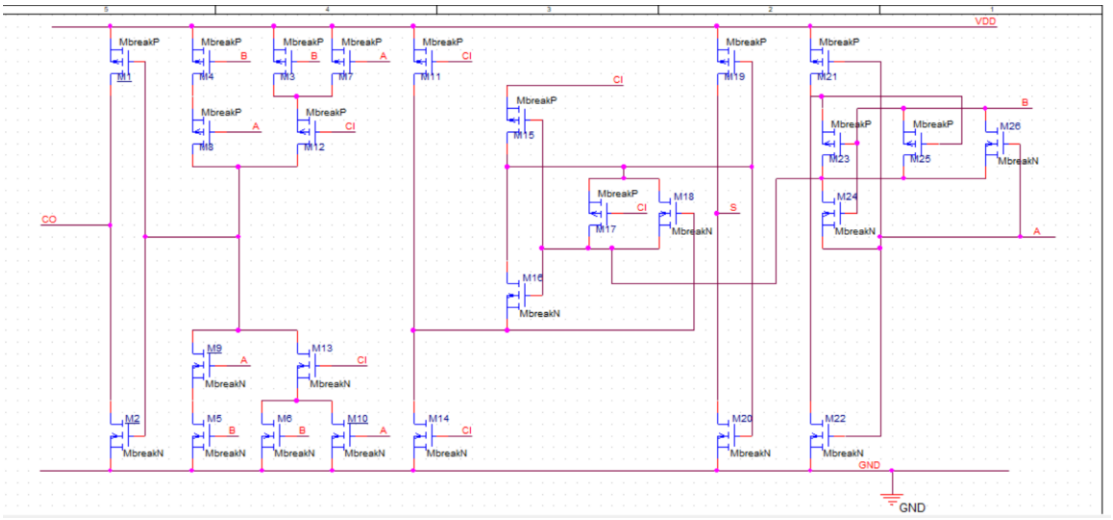


f.

這個算蠻簡單的，一開始開工作站卡了一下，其他都還好。

(10)FA1

a.



b.

Inputs: A, B, CI, VDD, GND

Outputs: CO,S

c. truth table

A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

d.

hw2_2_2.sp

```
**********************************************
.inc '90nm_bulk.l'
.SUBCKT Inv VDD GND A B CI CO S
*.PININFO VDD:I GND:I A:I B:I CI:I CO:O S:O
M_M1            CO N14413 VDD VDD PMOS l=0.1u w=0.5u m=1
M_M2            CO N14413 GND GND NMOS l=0.1u w=0.25u m=1
M_M3            N15145 B VDD VDD PMOS l=0.1u w=0.5u m=1
```

```
M_M4              N145962 B VDD VDD PMOS l=0.1u w=0.5u m=1
M_M5              N146352 B GND GND NMOS l=0.1u w=0.25u m=1
M_M6              N15185 B GND GND NMOS l=0.1u w=0.25u m=1
M_M7              N15145 A VDD VDD PMOS l=0.1u w=0.5u m=1
M_M8              N14413 A N145962 VDD PMOS l=0.1u w=0.5u m=1
M_M11               N15194 CI VDD VDD PMOS l=0.1u w=0.5u m=1
M_M12               N14413 CI N15145 VDD PMOS l=0.1u w=0.5u m=1
M_M13               N14413 CI N15185 GND NMOS l=0.1u w=0.25u m=1
M_M10               N15185 A GND GND NMOS l=0.1u w=0.25u m=1
M_M9              N14413 A N146352 GND NMOS l=0.1u w=0.25u m=1
M_M14               N15194 CI GND GND NMOS l=0.1u w=0.25u m=1
M_M15               N15385 N15755 CI VDD PMOS l=0.1u w=0.5u m=1
M_M16               N15385 N15755 N15194 GND NMOS l=0.1u w=0.25u m=1
M_M17               N15755 CI N15385 VDD PMOS l=0.1u w=0.5u m=1
M_M18               N15385 N15194 N15755 GND NMOS l=0.1u w=0.25u m=1
M_M19               S N15385 VDD VDD PMOS l=0.1u w=0.5u m=1
M_M20               S N15385 GND GND NMOS l=0.1u w=0.25u m=1
M_M21               N15830 A VDD VDD PMOS l=0.1u w=0.5u m=1
M_M22               N15830 A GND GND NMOS l=0.1u w=0.25u m=1
M_M23               N15755 B N15830 VDD PMOS l=0.1u w=0.5u m=1
M_M24               N15755 B A GND NMOS l=0.1u w=0.25u m=1
M_M25               N15755 N15830 B VDD PMOS l=0.1u w=0.5u m=1
M_M26               B A N15755 GND NMOS l=0.1u w=0.25u m=1
.ENDS
***********************************************


Vdd VDD       0     1
Vss   GND          0     0

Vin A         0       pulse (0 1 0 100n 100n 1.9u 4u)

Vin1 B       0      pulse (0 1 0 100n 100n 0.9u 2u)

Vin2 CI    0      pulse (0 1 0 100n 100n 0.4u 1u)

x1 VDD GND A B    CI CO S    Inv
```

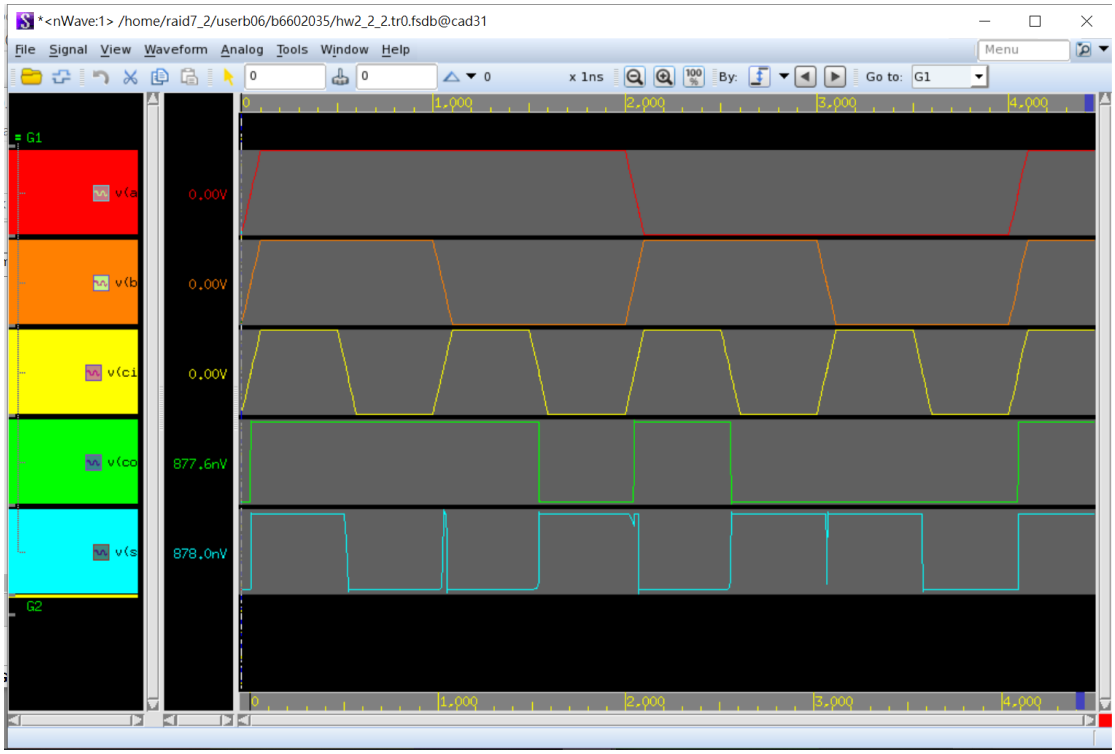
.tran 10n 4.4u

.op

.option post

.end

e.



f.

我覺得 layout 圖看懂了就不難，但畫成 pspice 很容易線沒接對，交錯在一起的時候不該 connect 的它偏偏要 connect 到一起，debug 的時候簡直氣到吐血。再來就是 creat netlist 改成.sp，這邊每次一改都要改很久，我最後找錯就是一個 mos 的 B 沒有改掉……花一個小時，真開心