IC Design

Homework # 3

(Due on 2019/12/13, 13:20. Verilog code and Report upload to CEIBA)

- ✧ Plagiarism is not allowed. 10% penalty for each day of delay.
- ✧ Any further questions, you can send e-mail to the TA (蘇倍陞)or leave messages on the board of the class website.
- ✧ TA email: r07943001@ntu.edu.tw , EE2-329

Specifications

In this homework, you are asked to design a **gate-level combinational circuit** that finds the average of nine given numbers. The inputs of this circuit are **nine 6-bit signed** digital values (in ***two's complement, the range is between -32~31***), denoted as *i0*, *i1*, *i2*, *i3*, *i4*, *i5*, *i6*, *i7*, *i8*. The output of the circuit, denoted as *average*, is also a **6-bit signed number**.

Following are some examples of the I/O:

Input									Output
i0	*i1*	*i2*	*i3*	*i4*	*i5*	*i6*	*i7*	*i8*	*average*
0x09	0x1c	0x1d	0x26	0x2f	0x17	0x02	0x0d	0x1a	0x0a
0x07	0x0a	0x35	0x2c	0x37	0x39	0x10	0x31	0x31	0x3b
0x1d	0x24	0x3a	0x36	0x26	0x2c	0x1b	0x21	0x2c	0x37

Since the sum of input may not be divisible by nine, **your average number should be rounded to the nearest integer.** For example, the sum of input for the first row is 87 in decimal form, the average of that is 87/9 = 9.667…, you should output 10(0x0a). The sum of input for the third row is -85 in decimal form, the average of that is -85/9 = -9.444…, you should output -9(0x37).

[**HINT**] You can use shift and add to implement divider.

There are some important things that you should notice:

- ➢ Your design should base on the **standard cells in the lib.v**. All logic operations in your design **MUST consist of the standard cells** instead of using the operands such as "+", "-", "&", "|", ">", and "<". **Note that the score of HW3 will be 0 if you use any of them.**
- ➢ Design your homework in the given "averager.v" file. **You are NOT ALLOWED to change the filename and the header of the top module (i.e. the module name and the I/O ports)**.
- ➢ If your design contains more than one module, don't create new file for them, just put those modules in "averager.v."

- The output waveform will be dumped to file "**averager.fsdb.**" You can use nWave to examine it.
- **For each set of input data, the test bench will allow your circuit to calculate the correct average number within 100ns.** Once exceeding 100ns or detecting the correct answer from your circuit, the test bench will soon provide the new data set to your design until all 10000 data sets have been simulated.

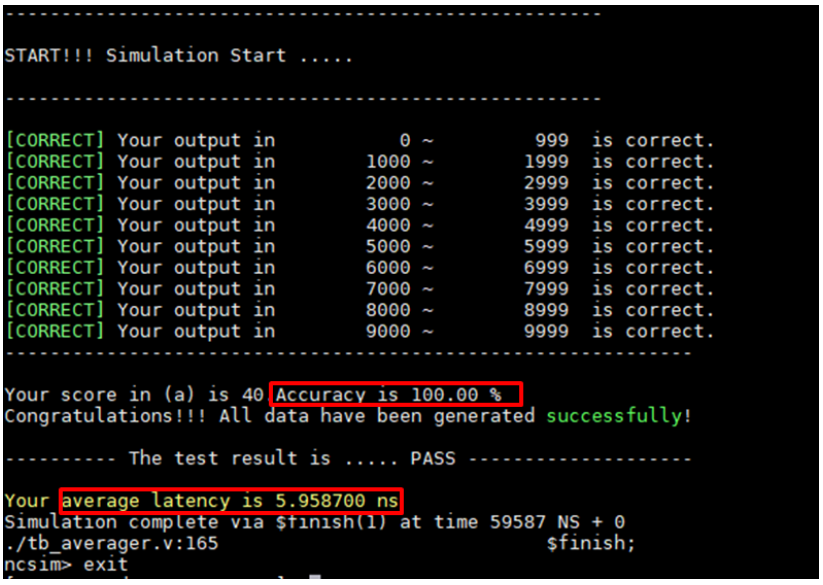
Grading

1. Gate-level design using Verilog (70%)

Your score will depend on both the correctness and performance of your design. We provide a "public" test bench with 10000 datasets. Following is the grading policy:

Correctness & Performance	Score
Fail to pass the test bench.	40 * (1-err #/10000)
Functionally correct	40
Average latency < 12ns	45
Average latency < 10ns	50
Average latency < 9ns	55
Average latency < 8ns	60
Average latency < 7ns	65
Average latency < 6ns	70
Using operands, not standard cell logic	0
Plagiarism	0

Testbench will provide related information for grading:



2. Report (30%)

You should also introduce and discuss about your design. Following are some requirements of your report.

- Circuit diagram (15%)
  Plot the circuit diagram of your design. You are encouraged to plot it hierarchically so that the reader can understand your design easily.
- Discussion (15%)
  Discuss about your design. For example, introduce you design, how do you divide nine in an efficient way, which technique is adopted in your design, how do you improve your critical path.

Notification

- Following are the files you will need (available on the class website)
  HW3.zip includes
  - **HW3_2019.pdf** : this document.
  - **HW3_tutorial** Verilog introduction
  - **averager.v**:
    Dummy design file. Program the design in this file.
    The header of the top module and the declaration of the I/O ports are predefined in this file and you are not allowed to change them.
  - **lib.v**: standard cells.
  - **tb_ averager.v**:
    Testbench for your design.
  - **i0.dat, i1.dat, i2.dat, i3.dat, i4.dat, i5.dat, i6.dat, i7.dat, i8.dat**:
    Input patterns for test bench. Please put these files in the folder that contains **tb_ averager.v** when doing simulation.
  - **golden.dat**:
    Output patterns of correct answers for test bench. Please put the file in the folder that contains **tb_ averager.v** when doing simulation.

- The following files should be compressed and uploaded to CEIBA by due time.
  - Report (PDF format)
  - averager.v
- File name rule : *HW3_(student id)_v#*
  Ex. HW3_b03901301_v1.zip
  Ex. HW3_b03901311_v2.zip

TA：蘇倍陞，EE2-329

TA email: r07943001@ntu.edu.tw or sam0108w@gmail.com

HW3 Office hours: 12/10 19:00-21:00 @ 博理 114

12/12 19:00-21:00 @ 博理 114

If you have no time at office hours, you can email TA to discuss another time for appointment.