Lakshya Rao

"Always love to do my own plumbing - pipelining is my passion"

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EXPERIENCE

Network Processor IC Design Intern
Huawei

05/2024 - 08/2024 *Ottawa, Canada*

Achievements/Tasks

- Worked on design of **new shared buffer/data cache** with multiple read/write interfaces accessed by multi-processor system.
- Worked as a team with a senior engineer - I was **responsible for coding top modules**, **read/writes modules** and **integrating key internal IP** into the block.
- Optimized pipeline to ensure **lowest latency and area.**
- Worked with verification team to debug RTL, and achieve **high functional coverage**, using **Synopsys VCS/Verdi** tool set.
- Running **Lint** and power tools (**Synopsys Spyglass**) to improve the quality of the RTL.
- Running synthesis (PLE and Physical) using **Cadence Genus**.
- Reviewing timing and adjusting RTL as required to meet timing targets. Working with the physical design team to ensure timing was met.

ASIC/FPGA Design Intern
Marvell

09/2023 - 12/2023 *Ottawa, Canada*

Achievements/Tasks

- Worked in the **ARM System Memory Management Unit (SMMU)** and **Compression Decompression (CDX)** design teams.
- **Took ownership** of the **Performance Monitor Counter Groups (PMCG)** sub-block within the SMMU and implemented several features as per the ARM spec**.**
- Led the **FPGA emulation** effort testing the CDX system.
- Created **top-level emulation architecture** and system-level design including **register definitions (error, status, control)**, **FSM design**, and **SW Interfacing.**
- Designed and implemented an **external-controller module** with several **concurrently operating FSMs with backpressure** as a top-level controlling entity.
- Implemented **AXI4-Lite** and **full AXI4** interface for status and control for communication with software via PCIe.

FPGA Design Intern
Evertz Microsystems

01/2023 - 04/2023 *Burlington, Canada*

Achievements/Tasks

- Developed a **new protocol from scratch** using **4b5b encoding** to **time-domain-multiplex SPI**, **UART**, and **Ethernet** data into a single high-speed data (SDL) line along with an **Ariber** (round-robin arbitration).
- Designed and implemented the **SPI receivers** and **transmitters** for host and receiver FPGAs in **VHDL.**
- Wrote **testbenches** for all modules created and simulated with **ModelSim**.

EDUCATION

BASc in Computer Engineering (Honours)
University of Waterloo

2021 - 2026

Waterloo, Ontario, Canada

Research

- Undergraduate Research Assistant @ **Waterloo Configurable Architectures Group** under Prof. Nachiket Kapre
- Mapping ML --> FPGAs

TECHNICAL SKILLS

Languages

SystemVerilog Verilog VHDL C/C++, Python MATLAB

Software

Cadence Genus, Synopsys Spyglass, Synopsys Verdi/VCS, Intel Quartus Xilinx Vivado, Lint

PROJECTS

NoX RISC-V Subsystem
(07/2024 - Present)

- Implementing instruction and data caches to an existing open source RISC-V core (NoX).
- Plan to make a sub-system out of many NoX cores.

INTERESTS

Watercolor Painting | Arm Wrestling | Weightlifting