Power Aware Embedded Test

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***Abstract*—In this paper we examine several embedded low power test schemes that we have proposed over the last few years. These solutions are aimed at reducing the switching activity during all scan-based test operations, particularly including those developed for BIST or deployed to perform on-chip test data compression.**

I. Introduction

Embedded test resources are being viewed increasingly as essential to reduce test cost. In particular, scan-based DFT schemes have gained broad acceptance as reliable test solutions. When it comes to energy consumption, however, scan-based test operations can dissipate much more power than low-power circuits were designed to function under. With overstressing devices beyond the mission mode, reductions in the operating power of ICs in a test mode have been recurring themes for years. A full-toggle scan pattern may draw several times the typical functional mode power, and this trend continues to rise, particularly over the mission mode's peak power. This so-called power-induced over-test may result in thermal issues, voltage noise, power droop, or excessive peak power over multiple cycles, which, in turn, cause a yield loss due to instant device damage, severe decrease in chip reliability, shorter product lifetime, or a device malfunction because of, for example, timing failures following a significant circuit delay increase.

Abnormal switching activity may also cause fully functional chips to fail during testing because of phenomena such as IR-drop, crosstalk, or di/dt problem. IR-drop refers to the power-rail voltage decrease due to higher current and the resistance of the devices between the rail and a circuit's node. Its large value increases path delays, and this degradation only worsens with elevated test frequencies or low supply voltages. Therefore, a device passing a slow speed scan test at nominal voltage may fail at-speed scan test where either the capture frequency is raised, the supply voltage is lowered, or both.

The underlying mechanism in crosstalk is related to capacitive coupling between IC's neighboring nodes. If the aggressor and victim nodes switch in the same direction, a delay on the victim node decreases, whereas it tends to increase, if they switch in opposite directions. Depending on the extent of coupling and a switching pattern during at-speed test, a failure can only be observed during testing, not in the functional mode.

The di/dt problem occurs in circuits using at-speed scan tests and is due to the sudden current changes within a few nanoseconds when applying the capture clock burst (typically a pair of launch and capture cycles) after a long pause where all clocks are inactive. Hence, the power distribution network may not be able to maintain the supply voltage in desired limits (the supply lines become unstable and reach levels below the ones encountered in a mission mode). The circuit might appear to be faster or slower than it actually is. It seems to be faster, if the clock stretching effect is dominant, and slower, if the combinational slowdown is forceful due to the supply variations.

The problem of excessive power dissipation during scan testing is typically split into two separate domains dealing with power reduction in shift and capture modes, respectively. Accordingly, numerous techniques for test power reduction and management have been proposed, focusing on test scheduling and reordering, partitioning and modifications of scan chains, scan cell reordering, as well as transition blocking and various forms of clock gating. Similar schemes have also been proposed for built-in self-test (BIST), including low-transition pseudorandom test pattern generators and gated scan cells.

Other solutions tailor patterns to the requirements of tests with the lowered switching activity, for instance, by reassigning certain non-random values to unspecified positions in test cubes causing power violations. It minimizes the number of transitions during scan loading, as done in power-aware ATPG. Deterministic test vectors can yield patterns leading to a reduced switching activity because of their usually low fill rates. Instead of random fill, don't care bits may assume (in the process of X-filling) values minimizing the amount of transitions during scan-in shifting. Other forms of X-filling decrease capture power by assigning particular values to unspecified bits so that the number of transitions at the outputs of scan cells in the capture mode is minimized.

On-chip test compression is facing similar test power problems. As on-chip decompressors expand and subsequently load test cubes into scan chains, don't care bits are typically filled with random values, and therefore the amount of flip-flop toggling during test may result in a power droop condition. The bulk of test power consumption can also be attributed to unloading test responses. Several low power test data encoding schemes were presented. Some of them rest on static LFSR reseeding techniques with certain extensions that allow reducing the scan-in transition probability. Other methods reduce test power in dynamic reseeding by using available encoding capacity to limit transitions in scan chains. These techniques freeze a decompressor in certain states by providing control data through external channels. It allows loading scan chains with decompressed patterns having low transition counts, and thus reduced scan-in power dissipation.

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