2012 IEEE 30th VLSI Test Symposium (VTS)

Test Generator with Preselected Toggling for Low Power Built-In Self-Test

Janusz Rajski, Jerzy Tyszer*, Grzegorz Mrugalski, Benoit Nadeau-Dostie
Mentor Graphics Corporation
Wilsonville, OR 97070, USA
*Poznań University of Technology
60-965 Poznań, Poland

Abstract – **This paper presents a new pseudorandom test pattern generator with preselected toggling (PRESTO) activity. It is comprised of a linear finite state machine (a linear feedback shift register or a ring generator) driving an appropriate phase shifter and armed with a number of features that allows this device to produce binary sequences with low toggling (switching) rates while preserving test coverage achievable by the best-to-date conventional BIST-based PRPGs with negligible impact on test application time.**

I. Introduction

Various forms of embedded test are increasingly viewed as essential to reduce test cost. Among them, scan testing has gained broad acceptance as a reliable solution. However, due to the high data activity associated with scan-based test operations, a circuit under test can dissipate much more power than it was designed to function under. With overstressing devices beyond the mission mode, reductions in the operating power of ICs in a test mode have been of concern for years. A full-toggle scan pattern may draw several times the typical functional mode power, and this trend continues to rise, particularly over the mission mode's peak power. This power-induced over-test may result in thermal issues, voltage noise, power droop, or excessive peak power over multiple cycles which, in turn, cause a yield loss due to instant device damage, severe decrease in chip reliability, shorter product lifetime, or a device malfunction because of timing failures following a significant circuit delay increase, for example. Abnormal switching activity may also cause fully functional chips to fail during testing because of phenomena such as IR-drop, crosstalk, or di/dt problem.

Numerous schemes for power reduction during scan testing have been devised [8]. Among them there are solutions specifically proposed for built-in self-test (BIST) to keep the average and peak power below a given threshold. For example, the test power can be reduced by preventing transitions at memory elements from propagating to combinational logic during scan shift. This is achieved by inserting gating logic between scan cell outputs and logic they drive [4], [9]. During normal operations and capture, this logic remains transparent. Gated scan cells are also proposed in [2] and [20]. A synergistic test power reduction method of [21] uses available on-chip clock gating circuitry to selectively block scan chains while employing test scheduling and planning to further decrease BIST power in the Cell processor. A test vector inhibiting scheme of [5] masks test patterns generated by an LFSR as not all produced vectors, often very lengthy, detect faults. Elimination of such tests can reduce switching activity with no impact on fault coverage.

The advent of low-transition test pattern generators has added a new dimension to power aware BIST solutions [3], [11], [15]. A device presented in [19] is comprised of an LFSR feeding scan chains through biasing logic and T-type flip-flop. Since this flip-flop holds the previous value until its input is asserted, the same value is repeatedly scanned into scan chains until the value at the output of biasing logic (e.g., a k-input AND gate) becomes 1. Depending on k, one can significantly reduce the number of transitions occurring at the scan chain inputs. A dual-speed LFSR of [18] consists of two LFSRs driven by normal and slow clocks, respectively. The switching activity is reduced at the circuit inputs connected to the slow-speed LFSR, while the whole scheme still ensures satisfactory fault coverage. Mask patterns are used in [14] to mitigate the switching activity in LFSR-produced patterns, whereas a bit swapping of [1] achieves the same goal at the primary inputs of CUT. A gated LFSR clock of [6] allows one to activate only half of LFSR stages at a time, thus reducing power consumption, as only half of the circuit inputs change every cycle. A scheme that combines the low transition generator of [19] (handling easy-to-detect faults) with a 3-weight PRPG (deployed to detect random pattern resistant faults) can also be used to reduce switching activity during BIST, as demonstrated in [17]. The schemes of [10], [13], and [16] suppress transitions in LFSR-generated sequences by either statistical monitoring or injecting intermediate and highly correlated patterns. Finally, a random single-input change generator can produce low power patterns in a parallel BIST environment, as shown in [7].

As the BIST power consumption can easily exceed the maximum ratings when testing at speed, scan patterns must be shifted at a programmable low speed, and only the last few cycles and the capture cycle are applied at the maximum frequency. In the burst-mode approach presented in [12], typically five consecutive clock cycles are used. The first four cycles serve shifting purposes, whereas the last one is designated for capture. The objective is to stabilize the power supply before the last shift and capture pulses are applied, which are critical for at-speed tests. To reduce the voltage droop related to a higher circuit activity, a burst clock controller slows down some of the shift cycles. It allows a gradual increase of the circuit activity, thereby reducing the di/dt effect. The controller can gate the shift clocks, depending on the needs for gradual warming up of the circuit.

In this paper, we propose a new pseudorandom test pattern generator (PRPG) for low power BIST applications. The generator is aimed at reducing the switching activity during scan loading due to its preselected toggling (PRESTO) levels. It can assume a variety of configurations that allow a

978-1-4673-1074-1/12/$31.00 ©2012 IEEE