A High Speed Embedded Cache Design with Non-Intrusive BIST

Steve Kornachuk†, Larry McNaughton††, Robert Gibbins†, Benoit Nadeau-Dostie††

†Northern Telecom, ††Bell-Northern Research
P.O. Box 3511, Station C, Ottawa, ON, Canada, K1Y 4H7

Abstract

This paper describes a 155 MHz wide-word cache design and its test integration features. Design techniques for high speed CAM with single ended match line sensing and highly integrated RAM are described. A new cache BIST algorithm based on the SMARCH [1] algorithm is presented. New techniques are described for the insertion of cache BIST access points into a high speed data path without compromising mission mode performance. Performance results of cache memory used for telecommunications microprocessor applications with 1Kb of CAM referencing a 5 Kb RAM are presented.

I. Introduction

With device gate counts and pin counts increasing and the cost of external functional testing rising, increases in hardware speed and functional complexity must be complemented by robust and complete self-test capability. The requirement to integrate special function macros into high speed data paths combined with the need to insert BIST for these components presents a potential conflict between performance and testability. One such macro, the cache design described here, provides high speed prefetched instruction storage and retrieval for a telecommunications processing application.

From its inception, the memory and BIST circuits were developed with the following objectives:

1) Accommodate the system cycle rate of 60 Mhz and various I/O overheads by completing the system address look-up compare cycle and the prefetched instruction RAM read within 12 ns, worst case (4.5V, 105°C).

2) Minimize active cycle power.

3) Incorporate into the cache's CAM and RAM blocks an interface that facilitates the connection of a cache BIST and is easily testable with functional vectors.

4) Design a BIST that has maximum memory fault coverage for both CAM and RAM blocks of the cache.

5) Insert the BIST circuitry into the high speed memory data path without incurring additional mission mode delay.

The memory performance and power objectives have been achieved by using a new self-timed CAM internal timing loop integrated tightly with the accompanying RAM read circuitry control signals. The self-timed nature of the cache give reasonable and predictable power consumption which increases linearly with frequency of operation. BiCMOS driver circuits used in the memories allow easy expansion from 4 to 256 rows and from 4 to 128 CAM compare data bits with no architectural change.

To achieve an easily testable cache interface, match line outputs are provided to the user to assist with on-chip diagnostics and cache BIST testing.

Cache BIST coverage is maximized by executing a complete SMARCH on the CAM read/write port while simultaneously running compare cycles on the compare port. Priority encoding of match line outputs ensures the correct hit/miss sequence. The CAM SMARCH sequence ends with a preload of the CAM with known states to

0-8186-6245-X/94 $04.00 © 1994 IEEE

address the RAM core in the subsequent RAM SMARCH tests, thus verifying the CAM-RAM match line to word line interconnection.

In the case of the cache memory, on board test signal generation circuitry such as BIST normally imposes a delay on the mission mode path due to multiplexing of memory inputs between mission mode and test mode signal drivers. To avoid this penalty, BIST control and serial data inputs were multiplexed with boundary scan signals which are already multiplexed into the input data path as part of the boundary scan test strategy [2].

II. Cache Architecture

The cache is comprised of a Content Addressable Memory (CAM) adjacent to and integrated with a static RAM, as shown in Fig. 1. Both the CAM and the RAM blocks have read/write ports with a synchronous clocked interface dependent upon addresses, select and write enable control signals. The modular, self-timed read/write port design of the CAM and RAM is taken from a family of SRAM described in [2]. The compare data input to the CAM, and the read-only outputs of the RAM as addressed by compare matches (hits) in the CAM, form a third I/O interface.

Cache Lookup Operation

The central cache function consists of detecting a bit for bit match between the compare data input word and any words stored in the CAM core. In the case of a match, a read occurs from the corresponding row in the RAM block. The tightly interlocked CAM and RAM internal timing paths allows a 3 ns CAM compare operation to immediately trigger a 3.5ns RAM read (at nominal process, 5V, 27° C). This self-timed operation, requiring only one user clock edge for complete compare and read operation, is independent of external clock duty cycle, saves power and yields a linear power vs. frequency characteristic.

The rising edge of the compare cycle clock raises the internal CAM control signals *ckbl*, *clml*, and *cml*. Gated by the rising edge of *ckbl*, compare bitline drivers drive the compare bitlines to correspond to the state of the compare data inputs. The rising edge of *cml* turns off the match line precharge devices.

For every bit in the CAM cell array, an exclusive-OR of the core cell state with the column compare bitline state occurs. If the cell state does not match the bitline state, a pull down device turns on to discharge the match line. Thus, there must be a bit for bit match between the

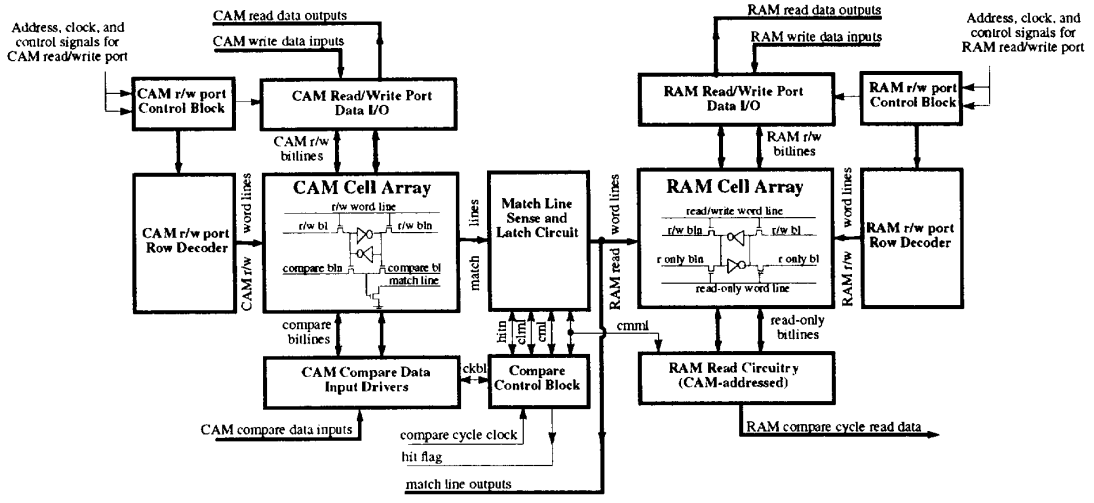

Fig. 1. Cache Block Architecture

compare word and the stored word for that row's match line to remain precharged to logic "one".

The rising edge of *clml* opens the match line sense and latch circuit, capturing the state of the match line and driving RAM word line inputs and user match line outputs. A transparent latch, biased by device ratioing to favor the detecting of falling edges, is used to sense the single ended match line.

A model timing path times compare events by executing a dummy worst case "miss". A model row of core cells has one core cell wired to mismatch the model column compare bitlines and pull down a model match line every cycle. The model match line falls at the same rate as the slowest miss, which is a mismatch of only one bit. The model matchline drives a dummy match line sensing circuit, whose output, *cmml*, falls to signify the end of the compare event.

The output of the CAM timing path, *cmml*, resets low the internal CAM clocks and initiates the RAM read cycle. As *ckbl*, *cml*, and *clml* fall, they shut down compare bitlines, activate match line precharge devices, and close the match line latch, respectively.

The RAM read-only port has its own self-timing loop, initiated by the falling edge of *cmml*. This RAM timing path gates word line drivers, activates the differential latching bitline sense amplifiers, then initiates word line shutdown and bitline precharge. Reads occur for the row addressed by the high match line in the case of a single hit. Multiple CAM hits address multiple RAM words simultaneously, resulting in ambiguous read data if the addressed RAM words have different values. A compare cycle without a cache hit results in no RAM word being addressed; unknown data is then sensed in the RAM.

If any rows register a hit, a shared precharged node, *hitn*, is pulled low. The precharge and evaluation of *hitn* happens on the opposite clock phase to the precharge and evaluation of the match lines. The cache hit flag output is simply an inversion of *hitn*.

Internal CAM events are gated by separate signals, which are slightly staggered in time to improve performance. For example, at the end of the compare cycle, the precharge of the match lines (*cml* fall) is delayed until the compare bitlines are driven low (*ckbl* fall). This prevents unnecessary current draw and precharge delay due to supply ground DC paths through the match line precharge devices and mis-matched core cells.

Another feature of the CAM is that each word has a validation bit implemented by modifying one core cell per word to be broadcast resettable to a low state in a single cycle. For an invalidated word, this cell discharges the match line as any mismatched bit would.

The cache has built in features to support testability. The read/write port test features support BIST and scan test strategy using input signal flip-flops with observable local outputs as well as an input to output shunt mode for direct memory output control. Test features specific to the compare function include access to the CAM compare circuitry via latched match line outputs, and test inputs to check the validation bits for each CAM entry.

III. Cache Memory BIST Algorithm

The objective of the cache memory BIST is to comply with system level test strategy by providing high speed and complete self-test capability of the cache memory and related interconnect, while minimizing the impact of the BIST interface on mission mode performance.

The BIST circuit for the cache memory is based on the serial interfacing technique and SMARCH algorithm described in [1]. Extensions to these methods take advantage of the properties of the SMARCH algorithm to test CAM and CAM/RAM combinations efficiently.

CAM Test

The CAM read/write port is tested as normal single port RAM using the SMARCH algorithm.

In test mode, compare and r/w data inputs are driven to the same state. A sample 3 word by 3 bit CAM element

with BIST interface is shown in Fig. 2. The first CAM r/w and compare data input bit is driven by a serial data input (SDI). For the other inputs the feedback path drives input bit n from CAM q(n-1), while the serial data output (SDO) is updated from the last memory output.

Table 1 shows one element of the CAM BIST march sequence for the sample circuit depicted in Fig.2. At the CAM compare input port, the SMARCH test performs read followed by write operations to uniquely test every bit within the CAM word one address location at a time. During the read, the data at the write input differs from the word being read from the core by a single bit. Every cycle, one bit is changed until each word has been changed from all ones to all zeroes or visa versa.

As the CAM SMARCH cycles proceed, a compare is also done using the same read/write word. Thus, the compare data inputs match the data presented to the read/ write port of the CAM. For every CAM word location, the BIST circuit checks for correspondence between encoded match lines and the read/write port address following write operations, and for no matches following read operations. A single bit miss condition is tested for every bit of every word in the CAM.

In general, a miss occurs for every CAM SMARCH read cycle with the following exceptions: The $(n+1)^{th}$ read cycle (n = bits/word) for a given word is used only to update SDO. Hits on this read cycle and the subsequent redundant write cycle are ignored. A read hit also occurs on the n^{th} read cycle for each word except the first one, due to previously filled words, and is also ignored.

Multiple hits occur on the n^{th} write cycle for each word except the first one, due to previously filled words. The match lines are priority encoded to return a hit address that corresponds to the current write address.

At the end of the CAM test portion of the cache BIST, unique values are written into the CAM core to facilitate the RAM test to follow.

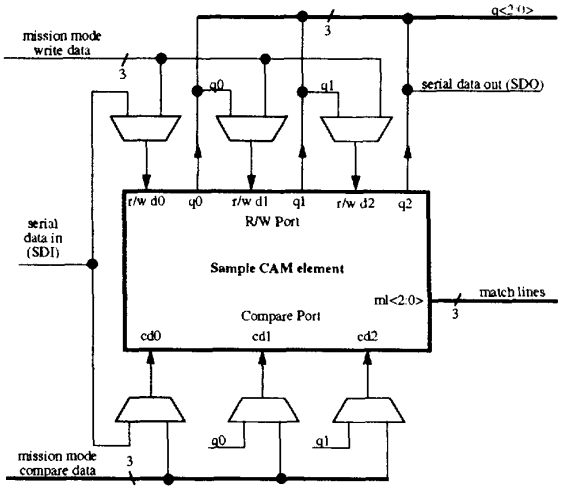

Fig. 2. Simplified CAM BIST Interface Example

SMARCH Operation	CAM Inputs D0 D1 D2	Core Contents			SDO	Compare Results D0D1D2 to Core
		Word 0	Word 1	Word 2		
Word 0 Addressed						
Read	100	000	000	000	0	Miss
Write	100	100	000	000	0	Hit Word 0
Read	110	100	000	000	0	Miss
Write	110	110	000	000	0	Hit Word 0
Read	111	110	000	000	0	Miss
Write	111	111	000	000	0	Hit Word 0
Read	111	111	000	000	1	Hit Word 0
Write	111	111	000	000	1	Hit Word 0
Word 1 Addressed						
Read	100	111	000	000	0	Miss
Write	100	111	100	000	0	Hit Word 1
Read	110	111	100	000	0	Miss
Write	110	111	110	000	0	Hit Word 1
Read	111	111	110	000	0	Hit Word 0
Write	111	111	111	000	0	Hit Word 0,1
Read	111	111	111	000	1	Hit Word 0,1
Write	111	111	111	000	1	Hit Word 0,1
Word 2 Addressed						
Read	100	111	111	000	0	Miss
Write	100	111	111	100	0	Hit Word 2
Read	110	111	111	100	0	Miss
Write	110	111	111	110	0	Hit Word 2
Read	111	111	111	110	0	Hit Word 0,1
Write	111	111	111	111	0	Hit Word 0,1,2
Read	111	111	111	111	1	Hit Word 0,1,2
Write	111	111	111	111	1	Hit Word 0,1,2

Table 1. CAM BIST March Element

RAM Test

The RAM read/write port is also tested using the SMARCH algorithm. The BIST circuit takes advantage of the unique values previously programmed into the CAM, presenting appropriate values at the compare data input such that a match occurs at the CAM row corresponding to the RAM location currently under test from the read/ write port. Thus, the values read from the RAM read/ write port during the SMARCH test correspond to those sampled from the RAM read-only port; both RAM ports are tested simultaneously.

IV. Cache Memory BIST Implementation

The aggressive system level performance requirements necessitate a BIST implementation optimized to minimize impact on the mission mode data path. A schematic of the cache implementation in a product code is shown in Fig.3.

In the product chip, the critical path is defined from the CAM compare data input pins, through the cache memory to the RAM read-only output pins. An IEEE 1149.1 [2] boundary scan is incorporated in these pins.

The boundary scan itself is re-used as the mechanism for controlling critical path signals during cache memory BIST. This re-use allows the user to avoid adding circuits to multiplex BIST data with mission mode data and increasing delay in the critical path. This technique is made possible by choosing a serial BIST compatible with the serial access provided by the boundary scan elements. The critical path must also have direct access between the pads and the critical macro inputs and outputs with no intervening logic.

During cache memory BIST, the BIST circuit overrides the standard IEEE 1149.1 Test Access Port (TAP) to gain serial access to the compare data and read-only output sections of the boundary scan registers. It then serially shifts appropriate data into the compare data inputs and samples the RAM read-only output signals for the CAM and RAM test algorithms discussed in section III.

This architecture takes advantage of boundary scan, cache memory BIST and ScanBist [5] testing to verify all

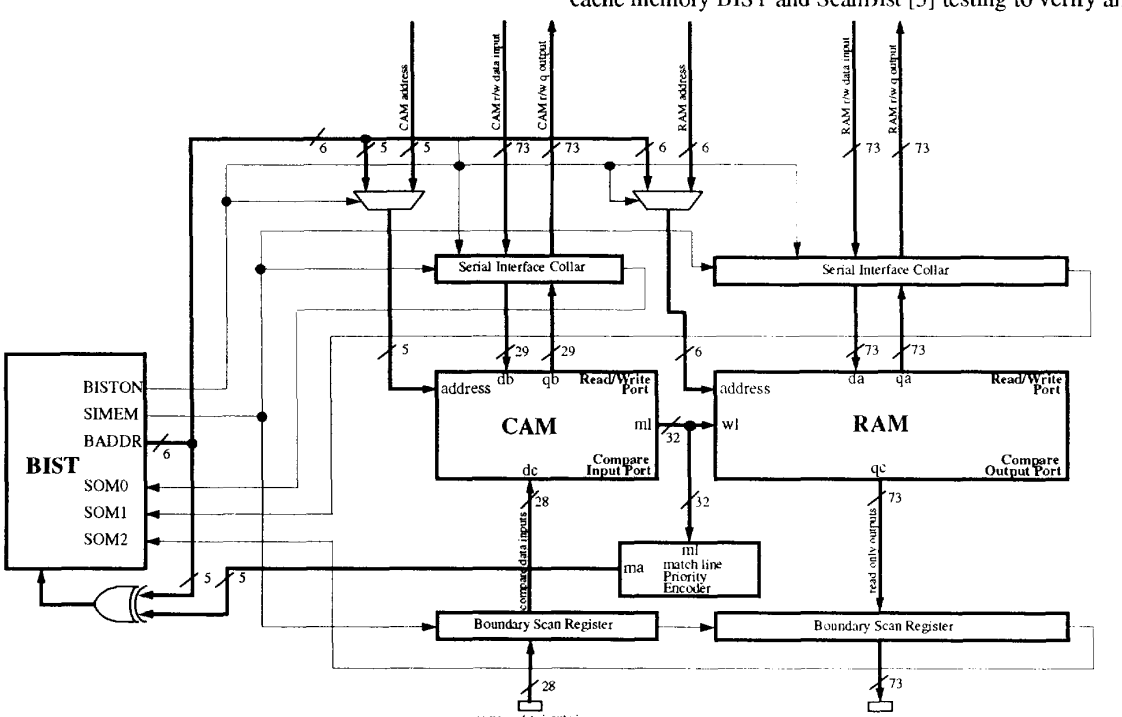

Fig. 3. Cache blocks with BIST circuit and Boundary Scan interface

interfaces to the cache. The chip scan test includes all memory input flip-flops, and uses the shunt modes of the CAM and RAM to verify the connectivity of the memory read/write outputs (*qa*, *qb*). The memory signals which do not have scannable flip flops or shunt mode access, such as the cache's *dc* inputs and *qc* outputs, are covered by the cache memory BIST as follows: during the last SMARCH pass of the RAM test, a set of non-homogeneous patterns designed to perform a counting test for shorts on the qc bus interconnect is loaded into successive RAM locations, and read out to the boundary scan chain.

V. Results

A prefetching cache-controlled memory management product chip containing a fully BISTed cache as described in this paper was manufactured in a 0.8 µm BiCMOS process. Cache BIST on this device runs successfully at the system rate of 60 MHz.

Waveforms are shown in Fig. 4 for the cache, comprised of 32 29-bit wide CAM words addressing 32 rows of 73-bit wide SRAM words, for conditions of nominal processing, 5.0V supply, and 27° C. The figure shows a cycle time of under 6.5 ns, RAM initialization (indicating completion of the compare cycle) under 3 ns, match line and hit flag access times of 3.5ns and 4.5 ns respectively, and CAM addressed RAM output access time of approximately 5.2 ns.

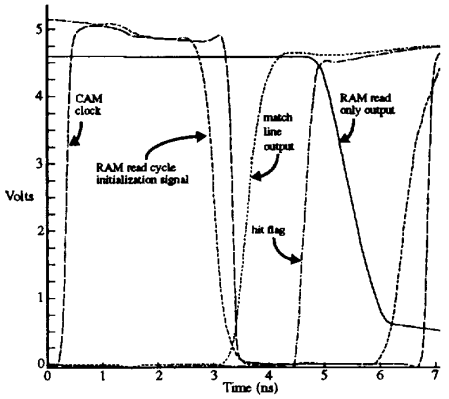

Fig. 4. Waveforms for cache compare/read cycle

VI. Conclusions

A high speed cache architecture with accompanying BIST algorithms and BIST integration techniques has been presented.

A cache BIST circuit is crucial to a thorough yet simple product test strategy. Complete memory coverage provided by an SRAM BIST serial interface can be extended to also test cache memory.

Implementation methods using the boundary scan circuitry to double as BIST signal input points minimize timing delays due to BIST integration into the high speed mission mode data path. The CAM is used to test the RAM; Boundary Scan, ScanBist, and memory BIST are combined to provide full memory interface coverage.

The performance of a cache with BIST implemented in product silicon exceeds the application's mission mode and test requirements.

Acknowledgement

The authors would like to thank James Fujimoto for his design of the cache RAM read-only port and help with technical questions during the creation of this manuscript.

VII. References

[1] Nadeau-Dostie B., Silburt A., Agarwal V.K., "A Serial Interfacing Technique for External and Built-In Self-Testing of Embedded Memories", IEEE Design and Test of Computers, vol. 7, no. 2, pp. 56-64, April 1990

[2] IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, Feb. 1990.

[3] Silburt A., et al., "A 180-MHz 0.8 µm BiCMOS Modular Memory Family of DRAM and SRAM," IEEE Journal of Solid-State Circuits, vol. 28, no. 3, pp. 122-132, Mar. 1993

[4] Giles G., Hunter C., "A Methodology for Testing Content Addressable Memories", Proceedings of the 1985 International Test Conference, pp. 471-474, 1985

[5] Nadeau-Dostie B., Hassan A., Burek D., "ScanBist: a Multi-frequency scan-based BIST method ", IEEE Design & Test of Computers, vol. 11, no. 1, pp.7-17, March 1994