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[54] **METHOD AND APPARATUS FOR TESTING MULTI-PORT MEMORY USING SHADOW READ**

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Related U.S. Application Data

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[51] **Int. Cl.**[7] **G11C 7/00**

[52] **U.S. Cl.** **365/201**; 365/230.05

[58] **Field of Search** 365/201, 230.05, 365/189.04, 220, 221; 371/21.1, 21.2

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[57] **ABSTRACT**

A method of and apparatus for testing multi-port memory performs a shadow read to an adjacent memory cell concurrent with a write operation associated with typical read-write testing. In the presence of a bit wire short or a word wired short, the concurrent read of an adjacent memory cell will cause the value of that cell to be corrupted. The corrupted value is then found by the read-write testing. Consequently, the testing takes no longer than read-write testing. In addition, the testing scheme can be modified for memory with read only ports. An embodiment of the apparatus employs and exclusive OR gate on the least significant bit of the test row address line to generate the shadow read address.

21 Claims, 4 Drawing Sheets