Transitioning eMRAM from Pilot Project to Volume Production

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***Abstract*—Embedded non-volatile RAM technology, and in particular Magneto-resistive RAM (MRAM), continues making great progress in read/write speed and cycling endurance, now rivaling traditional memory technologies. This advancement together with their low-energy consumption and non-volatility opens huge application markets. While stand-alone MRAM products are already being deployed, the first pilot applications for embedded MRAM are just starting to emerge. The availability of Design-for-Test (DFT) tools is key in the transition from low-volume technology exploration and pilot projects to high-volume production. In this paper we explore a new aspect of a Memory Built-In Self-Test (MBIST) tool for eMRAM, namely Error Correcting Code (ECC)-aware test and repair technology. This new MBIST capability provides the ability to make in-system, user-programmable trade-offs concerning the eMRAM repair resources. Having extra control over the repair resources in turn increases both manufacturing yield as well as the longevity of the product in its application.**

Keywords—eMRAM, trimming, ECC, ECC tuning, ECC-aware test, memory fault injection, memory test, memory repair, memory yield, memory aging, DFT, MBIST

I. Introduction

The rapidly growing IoT market creates a huge demand for embedded non-volatile memories. For example, IoT devices [1], with AI technology [2], require high density and high performance, low power memory operation. However, scaling traditional eFlash memories has limitations going below 28nm due to its high cost. The industry offers several alternative embedded non-volatile memories such as MRAM, CBRAM (Conductive Bridge Random-Access Memory), FeRAM (Ferroelectric Random-Access Memory), ReRAM (Resistive Random-Access Memory), etc. Recent MRAM technology announcements by Samsung [3] and IBM [4] show very promising results. MRAMs manufactured at 14nm FinFET technology sustained a sub 100ns write speed with 1E14 cycles of endurance. This is very impressive compared to eFlash technology which offers micro-second to milli-second write speed with 1E5 cycling endurance [5]. It also promises downscaling capability to fill the embedded NVM market needs beyond the 28nm node. This type of high speed, high endurance, and high-density MRAM is expected to replace some of the cache memories in the near future.

In this Industrial Short Paper, we describe a new MBIST solution for eMRAM. This MBIST solution provides the same fully integrated implementation environment to build MBIST DFT logic for both SRAMs as well as MRAMs. Furthermore, much of a standard solution for SRAM transfers directly, so the same MBIST methodology can be used for testing both SRAM and MRAM. Accordingly, Section II introduces first the standard MBIST test and repair flow for SRAM. In Section III we will develop this flow into a production-ready test and repair flow for eMRAMs highlighting only the differences. For completeness, this section also summarizes eMRAM specific fault models and the necessary trimming used in the experimental setup outlined in Section IV. The focus in Section IV is however on "ECC-Aware Test and Repair". This combines the power of the ECC, which every emerging NVM requires, with the power of repair for the purpose of improving yield and durability of the memory in the product application. The data presented in Section IV clearly demonstrates the applicability of the ECC-aware test and repair technology to eMRAMs. Lastly, Section V concludes the paper.

II. Standard Memory BIST Overview

Figure 1 illustrates a widely used standard MBIST test and repair manufacturing flow. The same manufacturing flow can be used for SRAMs implementing redundancy (repair) or ECC logic. ECC is not typically used for SRAMs during manufacturing test, but it can be used during in-system testing to ensure tolerance of soft errors.

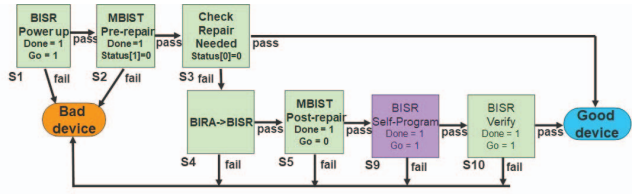

Fig. 1. MBIST test and repair manufacturing flow

The Built-in Self Repair (BISR) power-up step (S1) of the flow emulates a power-up event. The BISR chain is loaded with a repair solution previously calculated and stored in a fuse box. All spare resources of repairable memories are flagged as unused when executing the flow for the first time. The MBIST pre-repair step (S2) calculates a new repair solution based on the previous one. It tests all memories in the design and

2023 IEEE International Test Conference (ITC) | 979-8-3503-4325-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/ITC51656.2023.00021

2378-2250/23/$31.00 ©2023 IEEE
DOI 10.1109/ITC51656.2023.00021