A New Procedure for Weighted Random Built–In Self–Test

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Abstract

A procedure for determining weight distributions and implementing weighted random pattern generation in built–in self–test circuits is examined. Test lengths orders of magnitude shorter than those encountered in conventional pseudorandom testing are recorded.

1. Introduction

In an attempt to address the unreasonable test times encountered using conventional pseudorandom testing, this paper describes a procedure for incorporating weighted random pattern generation into self-testing circuits.

At the root of most common test pattern application mechanisms used today is stored pattern testing, pseudorandom pattern generation and the inevitable hybrid of both. Stored pattern testing involves the application of specific test vectors, each of which provides an incremental level of coverage. Externally applied, this approach may require large storage capability and expensive test units. The technique is straightforward and suitable for many *present* testing needs. However, considering that the specifications of a test unit are static, upper limits are physically imposed on such variables as test frequency, the number of I/O channels and the size of input (pin) buffers. On the other hand, circuit attributes are dynamic, that is various technology advancements can result in higher operating speeds, higher pin counts, and progressively larger test sets. This conflict ultimately implies costly test equipment upgrades or replacement. Therefore, it is questionable if long term economical testing is feasible with a standard stored pattern approach [Bas89].

Uniform random pattern or pseudorandom testing relaxes the functional and memory requirements of the external tester used. Often, relatively simple sequential circuits, such as linear feedback shift registers (LFSRs) [Gol67][Bar87] or cellular automata (CA) [Hor89], can be used to pseudorandomly generate test inputs such that there is an equal probability of assigning a 1 or 0 value to an input. The intention is that after a large number of these "pseudorandom"[1] vectors, a reliable level of fault coverage will be achieved. Unfortunately, experience has shown that with current circuit densities, an excessive number of test patterns may be needed to attain this goal. Moreover, only a relatively small number of the initial vectors cover a large portion of the detectable single stuck-at faults, leaving the majority of the sequence to be wasted in an attempt to detect random pattern resistant faults. In fact, most of the time penalty associated with random pattern testing is due to the application of these unnecessary patterns.

An obvious alternative is to use a joint test strategy – apply a reasonable number of pseudorandom test patterns and supplement this with stored pattern testing. However, it has been found that in many cases, the size of the stored test set needed nears 70% of the full deterministic set [Bas89]. Thus, this approach does not quite address the problem of limited storage in external testers.

The idea of incorporating test circuits on-chip, i.e. that of built–in self–test (BIST), offers numerous advantages, such as increased test portability, more efficient low level (probe) tests and easier diagnosis of failed chips at the board level. Of course, there are shortcomings which must be considered, for example an increase in area, and potential speed degradation if test circuitry is inserted in a critical path.

A refinement of conventional pseudorandom testing is the application of a non-uniform distribution of 1's to 0's as test inputs. This idea of *biased* or *weighted* random pattern (WRP) generation can result in a much higher rate of coverage than that of uniform random pattern testing alone. One drawback though is that proposed schemes to determine weights are quite complicated and the associated on-chip weighted pattern generators have, so far, been much more area "hungry" than their uniform random counterparts [Wun87][Sch75][Brg89].

This paper examines a built–in self–test (BIST) imple-

[1] In the course of this text, "pseudorandom" or "random" patterns refers to those which are pseudorandomly generated with a device such as an LFSR [Bar87].

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