US 20050028059A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0028059 A1**

(43) **Pub. Date: Feb. 3, 2005**

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(54) **PROCESSOR INTERFACE FOR TEST ACCESS PORT**

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(21) Appl. No.: **10/892,203**

(22) Filed: **Jul. 16, 2004**

Related U.S. Application Data

(60) Provisional application No. 60/491,558, filed on Aug. 1, 2003.

Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/724**

(57) **ABSTRACT**

A processor interface for test access port comprises a write buffer for storing data output by a processor and having a command field, a data field, and a serial output connected to a serial input of the test access port, a read buffer for storing data output by the test access port for access by the processor and having a data field, and a serial input connected to a serial output of the test access port; and a control circuit responsive to a command stored in the command field for generating test access port control signals for transferring test data from the write buffer to the test register and from the test register to the read buffer via test access port serial input and serial output.