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[54] **CLOCK SKEW MANAGEMENT METHOD AND APPARATUS**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-François Cote**, both of Aylmer, Canada

[73] Assignee: **LogicVision, Inc.**, San Jose, Calif.

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[58] **Field of Search** 713/500, 501, 713/502, 503

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Primary Examiner—William Grant
Assistant Examiner—Ronald D Hartman, Jr.
Attorney, Agent, or Firm—Fields and Johnson, P.C.

[57] **ABSTRACT**

A method of testing an integrated circuit having core logic with two or more clock domains and at least one signal path originating in one clock domain and terminating in an other clock domain, each signal path having a source control element in the one clock domain and an associated destination control element in the other clock domain, each the control element being a scannable memory element, the method comprising the steps of, for each the control element shifting a test stimulus into all scannable elements in the core logic; placing an associated source control element in a hold mode for a predetermined number of clock cycles prior to a capture operation so that the source control element holds its output constant during the predetermined number of clock cycles; performing a capture operation for capturing the data output in response to the test stimulus by the control element and by all other scannable elements which are not control elements; maintaining an associated source control element in a hold mode for a predetermined number of clock cycles following a capture operation so that the source control element holds its output constant during the predetermined number of clock cycles; shifting out data captured in the capturing step; and analyzing the data captured in the capturing step. An integrated circuit for use with the method comprises a source control element and an associated destination control associated with each signal path for exchanging data between the one and the other of the clock domains, the source control element being located in the one clock domain and the associated destination element being located in the other domain; each control element being a scannable memory element having an input and an output and being configurable a SHIFT mode for shifting data from its input to its output and a CAPTURE mode for capturing data applied its input, each the source control element being further configurable in a HOLD mode for holding its output constant; and the control elements being configurable in the modes in response to predetermined combinations of a Scan Enable signal for enabling or disabling shifting of data therethrough and a Capture Disable signal having a one value to cause a recipient control element to enable the capture mode and another value to cause a recipient control element to suppress the capture mode.

43 Claims, 12 Drawing Sheets