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(54) **METHOD AND APPARATUS FOR CONTROLLING POWER LEVEL DURING BIST**

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(56) **References Cited**

U.S. PATENT DOCUMENTS

4,503,537		3/1985	McAnney	371/25
4,969,148		11/1990	Nadeau-Dostie et al.	371/21.1
5,329,533		7/1994	Lin	371/22.3
5,349,587		9/1994	Nadeau-Dostie et al.	371/22.3
5,614,838		3/1997	Jaber et al.	324/765
5,655,127	*	8/1997	Rabe et al.	395/750.04
6,037,813	*	3/2000	Eto et al.	713/501 X

* cited by examiner

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(57) **ABSTRACT**

An improvement in a method of testing a digital circuit or system, having a plurality of scannable memory elements, in accordance with conventional BIST methods in which, at a reference clock, a test stimulus is shifted into the memory elements, the response of the elements is captured and the captured data is shifted out of the elements and analyzed, the improvement comprising controlling the average power consumption of the circuit during the test by suppressing clock pulses from the reference clock during phases of the test that do not require the maximum level of activity or in which the performance of the circuit is not to be evaluated; and, suppressing no clock pulses from the reference clock in phases of the test in which the performance of the circuit is to be evaluated, so that the conditions are substantially as those of normal mode of operation of the circuit.

23 Claims, 3 Drawing Sheets