A BIST Algorithm for Bit/Group Write Enable Faults in SRAMs

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Abstract

The use of group (or bit) write enable in memories is becoming very common in embedded memories. The circuitry used to achieve these functions need be thoroughly tested for different kind of defects using specific test sequence. However, most BIST algorithms assume that these write enables are forced active during the global write cycle in the BIST run. This paper presents a serial interface BIST algorithm that is used to test defect on bit/group write enables of these memories.

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1. Introduction

Static Random Access Memories (SRAM) is being extensively used in system on chip (SOC) designs. It is common to see tens or even hundreds of SRAMs integrated into chips to perform different functions [1]. With the wide used of SRAMs new functionalities are being added to the memories to address specific design requirements. Among those is the ability to perform partial write operation where only specific portion of the memory word is written. This is achieved by disabling the memory internal write circuitry from writing the whole word by using write enable control ports. These write enable ports may control individual bits or a group of bits in a word. However, using the bit or group write enables does not necessarily replace the need for global write enable. Most memories maintain the global write enable port to initiate a write operation to the memory.

The existence of bit and group write enable functionality in SRAMs present new testing challenges. Treating these ports as global write enable surely reduces the fault coverage on the circuitry associated with them.

This paper presents a BIST algorithm and test circuit architecture for detecting defects in bit and group write enable that are internal to the memory. In section 2 we present the defects of interest and the fault models used. The algorithm for detecting bit write enable defects is presented next. Section 4 extends the algorithm for the detection of the group write enable faults. The memory interface circuit architecture is introduced in section 5. Conclusions are provided in section 6.

2. Bit and Group Write Enable Defects and Fault Models

Figure 1 shows a typical memory implementation to support bit write enable function. The active high write enable logic is implemented at the input data path (before the bit line decode circuit).

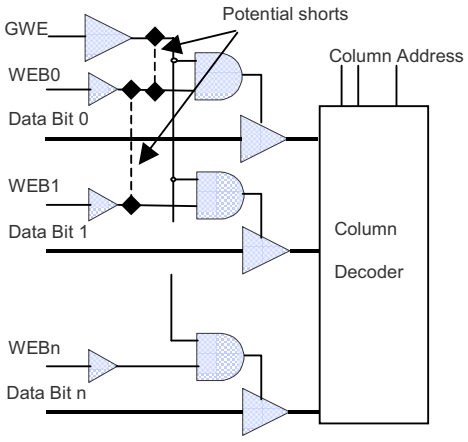

Fig. 1 A Bit write Enable implementation

Here the global write enable (GWE) is used to control all bit write enables (WEB). A data bit is written to the memory only when the global write enable and the specific bit write enable are active.

Controlling the WEBs and the GWE from one source in test mode will mask stuck active faults on the WEBs. Shorts between the WEB will also be masked. Furthermore, shorts between GWE and any WEB will not be detected, Wired-OR (for active low write enable signals); Wired-AND (for active high write enable signals) short between the Global Write Enable (GWE) and the bit write enable of the Most Significant Bit (MSB) will not be tested.

The coverage is further reduced if the write enable circuitry is implemented after the column decoder. The defects in this case will affect all bit lines in the memory array.

Traditionally test engineers use functionally generated patterns to test for these defects. The patterns perform read and write operations with different data and bit write enable values. However, generating these patterns is becoming too complicated for deeply embedded memories.

3. Detection Algorithm for Bit Write Enable

To detect the defects of interest, GWE and WEBs are controlled independently. The detection of these defects is achieved using a serial interfacing technique [2]. The memory data inputs and outputs are connected to form a shift path from one bit to the next. The first bit receives a single bit of data that will be used to apply the test data. Data is shifted from the LSB to the MSB.

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