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[54] **INTEGRATED CIRCUIT TESTING METHOD AND APPARATUS AND INTEGRATED CIRCUIT DEVICES FOR USE THEREWITH**

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[52] **U.S. Cl.** **371/68.1**; 371/15.1; 371/22.3; 371/24; 371/25.1

[58] **Field of Search** ..... 371/22.3, 68.1, 68.3, 371/71, 67.1, 25.1, 24, 22.1, 22.5, 22.6, 22.4, 15.1; 364/200 MS File, 900 MS File

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[57] **ABSTRACT**

In a so-called "scan-design" arrangement for testing integrated circuits, whether at the device level or at system level, problems associated with the storage and handling of vast amounts of data from increasingly complex devices are addressed by testing a pair of identical integrated circuits simultaneously and using the binary vector generated by scanning one of these integrated circuits as the reference against which to compare the binary vector produced by scanning the other integrated circuit. A plurality of "scan-designed" integrated circuits may be connected in series, possibly in a ring, and each compared with its predecessor. Zero-display coupling across each device may be employed to allow each successive integrated circuit to be compared with the same reference circuit in the chain or ring.

11 Claims, 1 Drawing Sheet