Structural test with functional characteristics

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Abstract

A novel structural test clocking architecture is proposed to reproduce characteristics of the functional mode of operation that are essential to a high-quality test. Bursts of functional mode clocks are controlled to provide accurate timing tests taking into account functional timing constraints such as multi-cycle paths and false paths. Any mix of asynchronous and synchronous clocks is supported. Long term (Idd, temperature) and short term (IR-drop) power characteristics related to circuit activity are independently controlled.

I. Introduction

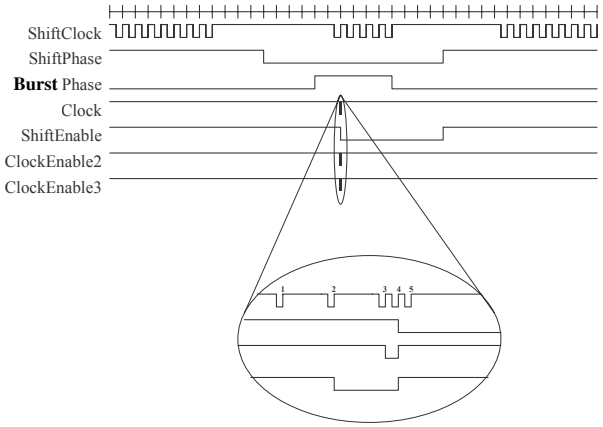
Defects that affect circuit speed are becoming more prevalent and it is important to provide a thorough at-speed test. Another trend is the replacement of functional test by structural test methods to implement all tests. However, it is not trivial to implement an at-speed structural test. Circuits have several characteristics that complicate the task. Functional clocks can cover a wide frequency range. These clocks can be asynchronous (ie non-integer frequency ratio and/or unknown relative phase) or synchronous (ie their frequency ratio is fixed as well as their relative phase) to each other. Cross-domain paths must be correctly handled to prevent false timing violations caused by false paths while providing proper test of the interface logic. Within each domain, multi-cycle paths are sometimes used, instead of pipelining, to implement functions at a lesser cost. Gated clocks are used for low power designs. PLLs are used to control groups of synchronous clocks and/or multiply external reference clocks. Other aspects of the design affect the implementation of an at-speed test. The circuit is designed to perform at a certain temperature and supply voltage. The circuit activity has a direct influence on the local temperature and reduction of supply voltage (IR-drop) which in turn influence the timing. An at-speed structural test should be implemented such that the supply current, temperature and supply voltage drops can be controlled in a way that physical limits are not exceeded and, preferably, approach the conditions of the functional operation. An at-speed test method must be such that a minimum number of test-specific timing constraints are added to the design. These constraints must be easy to meet so that timing closure is not impacted.

II. Clocking scheme

The clocking scheme proposed in this paper addresses these issues. Clock bursts are applied to the circuit to reproduce characteristics of the functional mode of operation. The burst length is programmable. Burst lengths longer than 2 are needed to test multi-cycle paths [1] and deal with issues related to IR-drop. In [2], it was reported that the results of at-speed tests were different when using a burst of length of 2 as opposed to a free-running clock (ie “infinite” burst length). It is our experience as well that modifying the burst length will cause variations of the supply voltage and change the circuit timing. Some timing defects can only be identified if the burst length is sufficiently long to cause a supply variation that is comparable to the one observed during functional operation. The burst is modifiable at run-time to adjust the number of at-speed clock pulses applied.

However, the total number of clock pulses is kept constant so that the circuit response also remains constant. An example is shown in figure 1. The clock burst is nominally 5-cycle long but 2 clock cycles have been slowed down. The instantaneous frequency of these 2 cycles is 1/4th of the nominal frequency. The remaining 3 cycles are applied at the nominal frequency. Note that all these clock cycles are derived from the same clock by gating a free-running clock.

Fig. 1. Example clock burst waveform



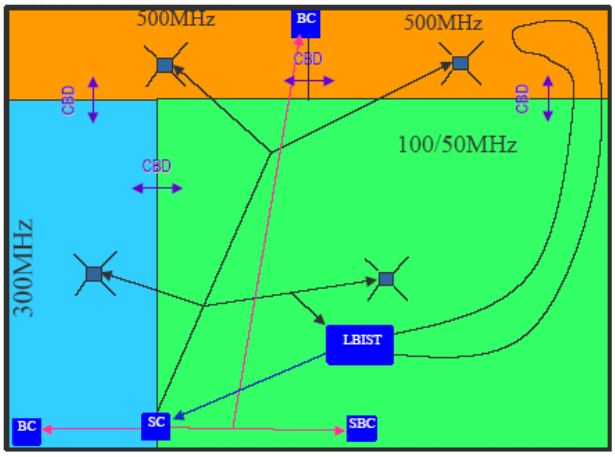
In order to maximize the coverage of delay defects, including cross-talk, a launch-from-shift methodology is preferred to perform an at-speed test. In [3], it is shown that for a same transition fault coverage, 10 times as many patterns are required using launch-from-capture with a burst length of 2 capture cycles compared to the launch-from-shift methodology. Longer burst lengths would require even more patterns. This is clearly unacceptable when considering test time or tester storage, even with compressed patterns.

III. Chip architecture

A general view of the clocking architecture is illustrated on figure 2 on an example circuit. A shift clock controller (identified SC) and a number of burst clock controllers (identified BC or SBC) which are connected to clock gating logic located at the base of each clock domain are shown. Each clock domain also includes a small sequencer (small square in the middle of each domain) to generate "critical" control signals such as scan enable and, optionally, clock enable(s) that are local to the domain. The Scan enable signal is pipelined locally in each clock domain to easily meet timing. Clock enable signals are needed for a small fraction of flip-flops that are source of multi-cycle paths or false paths. The handling of multi-cycle paths is similar to the one described in [1] by configuring the source flip-flops in hold mode for a number of clock cycles before the capture operation as shown in figure 1. The flip-flops are identified in design constraints files already needed by physical design tools and static timing analysis tools. The test timing is identical to the one used during static timing analysis.

The sequencer contain a number of flip-flops that corresponds to the burst length minus one as well as a handful of gates. Pipeline flops might be needed for control signals (Scan Enable and Clock Enable) depending on the fanout.

Fig. 2. Example circuit with multiple domains



An Embedded Test controller applying random patterns or decompressing deterministic patterns can be present or the various controllers can be driven directly from a tester applying uncompressed ATPG patterns.

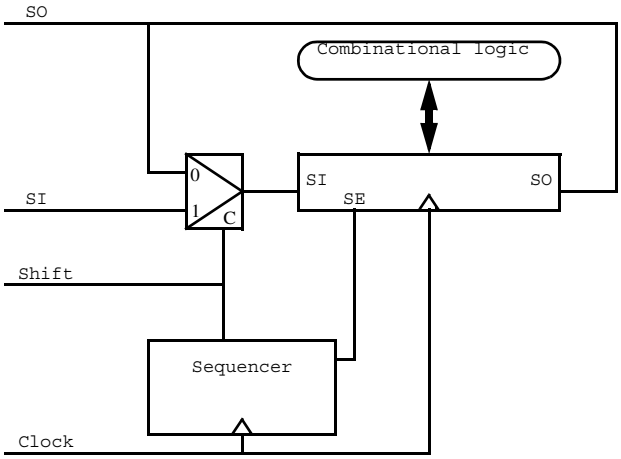
IV. Intra-domain clocking

For the launch-from-shift methodology, the scan chains are configured in shift mode for all but the last clock cycle of the burst (except for the multi-cycle path sources as explained above). This would normally require to have a test controller that can provide serial test data at potentially very high frequencies. We avoid this situation

by adding a multiplexer at the beginning of each scan chain that selects between a serial input coming from the test controller or from its own serial output (see figure 3).

During the shift phase, test data is transfered at reduced speed from the embedded test controller to the scan chain. During the burst phase, the test data is rotated until the capture operation occurs. This method allows to put the controller on any clock domain or even on its own domain if desired. Simple 2-edge timing can be used to transfer test data to/from scan chains that are on different clock domains than the controller. The controller is put in hold mode during the clock burst so that no additional timing constraints are necessary for the embedded test controller even if it happens to be on a high speed clock domain.

Fig. 3. Rotating chain segment and sequencer



V. Inter-domain clocking

The architecture allows to have a same controller handle any number of clock domains of different frequencies. Cross-domains paths (identified as CBD in figure 2) between asynchronous clock domains are tested using a method similar to the one described in [1]. However, setup and hold times are relaxed even more to make sure that no artificial timing constraints are introduced. An analysis tool identifies at the RT level the flops located at the source and destination of cross-domain paths. For each scan load, a control signal decides which of the source or destination flip-flops will be allowed to capture during the burst. If destination flip-flops are selected, the source flip-flops are configured in hold mode for the duration of the burst in their clock domain so that destination flip-flops can perform a capture operation during the burst. If source flip-flops are selected, they perform the normal burst including the capture operation and the destination flip-flops will also go through all operations of the burst except for the capture. Only few flip-flops have their capture suppressed at any given time and the test time impact is negligible. It is sufficient to test these cross-domain paths at reduced speed because they are typically going through asynchronous interfaces that are delay-insensitive and relatively few gates are tested at reduced speed.

The embedded test controller, shift clock controller, burst clock controllers and sequencers are all on different clock domains but none of the signals between them are timing critical. This greatly simplifies timing closure.

The handling of cross-domain paths between synchronous clock domains is addressed in a companion paper [4].

VI. Results

A subset of the clocking scheme described in this paper was used to collect data and understand the power requirements for a circuit projected to work nominally at 200MHz. The average current (Idd) and maximum frequency (Fmax) were measured at different temperatures and supply voltages. The experiments were performed on a qualification lot of 25 samples. A very small fraction of the results obtained are given here. The ones presented illustrate the application of the clocking architecture to yield learning and delay testing.

In this particular circuit, the burst length during the burst phase was limited to 2. During the shift phase, the method of [5] was used to generate the clock as it met the requirements and the new shift clock controller was not available at the time the circuit was designed. According to this method, short bursts of the functional clock are used to shift in the scan data. For example, for the shift rate identified “LBIST Core 1/4 Shift”, a short burst of 2 clock cycles derived from the functional clock is enabled and the next 6 clock cycles are suppressed. This is repeated until the scan chain are loaded. Similarly, for

"LBIST Core 1/2 Shift", bursts of 4 cycles followed by 4 suppressed cycles are applied. For the 1/8 shift rate, one out of 8 pulses is enabled. For "Full shift", the clock is free-running. All shift rates are compared to a functional test (MARCH4CLS_CONT) and an ATPG test with transition fault coverage comparable to the subset of the BIST patterns used to conduct the experiments. The ATPG test uses a launch-from-capture approach (burst length of 2).

Figure 4 demonstrates the necessity to control the circuit activity when performing an at-speed test. Fmax is plotted as a function of Vdd for the various tests. The "1/2 Shift" and "Full Shift" tests indicate a lower Fmax because of excessive IR-drop occuring during the shift phase. However, the 1/4 and 1/8 Shift tests match very closely the reference functional test. The reasons for the strange ATPG results at low temperatures are not understood. The results at high temperatures are more linear but the Fmax predicted is always optimistic by 15-20%.

Fig. 4. Fmax as a function of Vdd

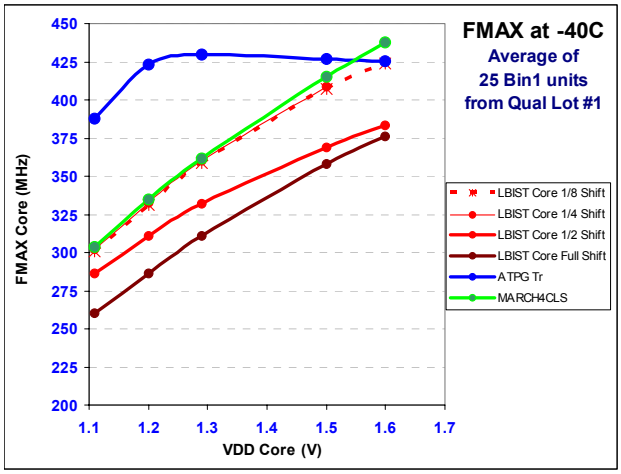
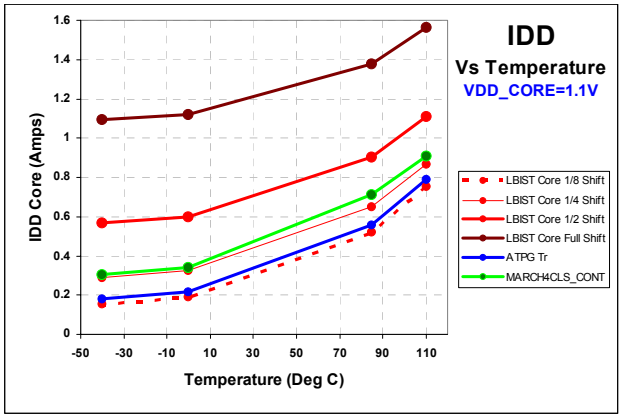


Figure 4 shows the variation of Idd as a function of the temperature for the same tests. The "1/2 Shift" and Full Shift rates are clearly above the reference Idd indicating that the average circuit activity is higher than the functional test. However, the "1/4 Shift" test is very close to the reference functional test. The ATPG pattern was shifted at an equivalent rate of 1/6 and could not match the reference Idd. The ability to control Idd independently from the maximum frequency (Fmax) measured during the burst phase where the capture operation takes place is very valuable to characterize the power grid characteristics. As the maximum frequency of circuits increase, it is becoming necessary to use an Embedded Test controller that can shift data at higher speed than a tester.

Fig. 5. Idd as a function of temperature



VII. Conclusions

We described a novel structural test clocking architecture capable of reproducing characteristics of the functional mode of operation that are essential to high-quality test and yield learning. Bursts of functional mode clocks are controlled to provide accurate timing tests taking into account functional timing constraints such as multi-cycle and false paths. The test timing is identical to the one used during static timing analysis. Any mix of asynchronous and synchronous clocks is supported. Test patterns can be applied from a BIST controller, an embedded pattern decompressor or a tester.

Various features allow to control the average current as well as the amount of IR-drop in the circuit under test allowing to measure more precisely the maximum frequency during yield learning and production test.

References

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