A Scan-Based BIST Technique Using Pair-Wise Compare of Identical Components

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Abstract

This paper addresses the problem of efficiently testing scannable ASICs in a board-level and system-level environment. The method makes use of a serial testability bus (ETM or IEEE 1149.1) and takes advantage of the presence of identical components on the boards. The main benefits of the method are a significant reduction in test time and test data to be stored. Results obtained for an actual system show a reduction in test time of about 20 times for a module with 50 ASICs. The extra board area required was less than 2% for all boards of the module.

Introduction

This paper addresses the problem of efficiently testing scannable Application Specific Integrated Circuits (ASICs) in a board-level and system-level environment. A new Scan-based BIST technique is described and the results of its application to an actual system are presented. The method makes use of a serial testability bus (IEEE 1149.1 or ETM) and takes advantage of the presence of identical components on the boards.

The paper is organized as follows. The first section describes the system used as the test vehicle for the new testing method and its main test features. The second section presents a possible test procedure and highlights the issues associated with conventional scan testing at the board and system level. The third section describes the key components of the proposed test and diagnosis procedure (Pair-Wise Compare or PWC method) which is detailed in section 4. The fifth section discusses the costs and benefits of the procedure in general and for the particular system described in the first section. Conclusions are drawn from that experience in the last section.

1) System and test features

The system module to be discussed is composed of 4, or optionally 5, Printed Circuit Boards (PCBs), backplane and a processor card (see figure 1). A complete system consists of dozens of such system modules. The Port boards perform the Input/Output operations of the system. The module contains of order 50 ASICs but with less than 10 unique types. On figure 1, each fill pattern can be associated to an ASIC type (the number of instances is not necessarily exact). The main boards have 15 to 20 ASICs each.

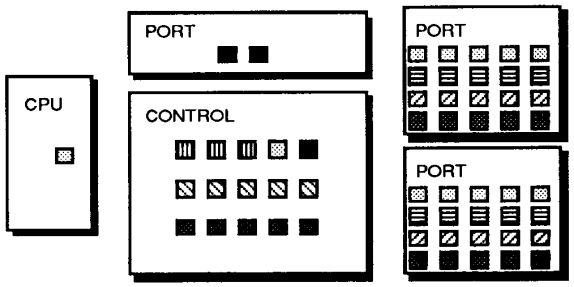

Figure 1 Schematic view of the module showing the ASIC distribution

The ASICs are scan-testable designs, with boundary scan as an integral component. Memories are tested using specialized self-test methods described in [1]. A standard serial slave interface on each chip is used for test access and control. The five-pin testability bus is similar to the Element Test and Maintenance