An Embedded Technique For At-Speed Interconnect Testing

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Abstract

A new embedded test technique which provides full at-speed testing of board level interconnect is described. The proposed technique is fully compatible with the IEEE 1149.1 boundary scan standard. The technique extends the standard's architecture to provide for synchronized at-speed timing control of the boundary scan cells so that test data can be applied and captured across the interconnect at system speeds.

1. Introduction

Rapid advances in silicon, packaging and board technologies have created new opportunities and challenges for equipment manufacturers. Indeed, the complexity and speed of today's boards are creating severe manufacturing test challenges. This is particularly true when it comes to testing for delay related defects in the board interconnect.

Many companies today perform interconnect testing using in-circuit test (ICT) techniques [10]. Testers that provide this capability typically contain hundreds to thousands of physical probes (often called a "bed-of-nails") that are used to contact chip pins and board test points to perform the interconnect tests. However, the continued practicality of ICT is severely challenged by advances in packaging technology. Dense, double-sided boards require thousands of probes, and modern surface-mount chip packages leave most chip pins physically inaccessible. In addition, testing for interconnect delay faults is not practical due to the inability of the tester hardware to apply at-speed signals through the probes.

ICT's physical access problem drove the creation and subsequent industry-wide acceptance of the IEEE 1149.1 Boundary Scan Standard [1-9] as a foundation for probeless interconnect testing. Unfortunately, the IEEE 1149.1 standard is not designed for applying and capturing data across interconnects at application speed. Because of the standard's serial control approach, a minimum of 2.5 test clock (TCK) cycles are required between the time test data can be launched from one chip and captured at another. So for example, with a TCK operating frequency of 25 MHz, the effective interconnect test frequency available from 1149.1 becomes 10 MHz, clearly much lower that typical board application speeds.

In light of the above limitations, the method most commonly used to achieve at-speed interconnect testing is through functional testing at the board or system level. Functional testing though has some strong limitations. The time and resource required to develop the functional tests can be very high. Perhaps even worse is the time needed to diagnose the physical location of a fault once it is detected.

In this paper, a new embedded test technique which provides full at-speed testing of board level interconnect is described. The proposed technique builds upon the standard IEEE 1149.1 test approach. The technique uses new at-speed boundary scan cells as well as embedded timing control for these cells. A key feature of the proposed technique is that it is compatible to IEEE 1149.1 based testing. A board design can incorporate a mixture of chips incorporating the technique described in this paper and chips simply compliant to the IEEE 1149.1 standard. Any existing boundary scan test hardware as well as test and diagnostic software tools can still be used without modification.

The remainder of this paper is organized as follows. Section 2 describes the high level architectures at both the chip and board levels required to implement the proposed technique. Section 3 describes the new at-speed boundary scan cells while the at-speed timing controller is described in section 4. Section 5 describes the use model of the proposed technique in the context of boundary scan based testing. Section 6 concludes the paper.

2. High Level Architectures

The diagram in Figure 1 illustrates the chip level architecture required to implement the proposed technique. Shown are the standard IEEE 1149.1 TAP and controller together with at-speed boundary scan cells and an at-speed interconnect (ASI) controller. The at-speed boundary scan cells consist of IEEE

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