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(54) **SCAN TEST METHOD FOR PROVIDING REAL TIME IDENTIFICATION OF FAILING TEST PATTERNS AND TEST BIST CONTROLLER FOR USE THEREWITH**

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(58) **Field of Search** 714/726–739; 324/765, 46, 16

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,652,814	A	*	3/1987	Groves et al.	714/738
4,801,870	A		1/1989	Eichelberger et al.	
5,732,209	A		3/1998	Vigil et al.	
5,831,992	A	*	11/1998	Wu	714/732
5,930,270	A		7/1999	Forlenza et al.	

* cited by examiner

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(57) **ABSTRACT**

A method of scan testing an integrated circuit to provide real time identification of a block of test patterns having at least one failing test pattern comprises performing a number of test operations and storing a test response signature corresponding to each block of test patterns into a signature register; replacing the test response signature in the signature register with a test block expected signature; identifying the block as a failing test block when the test response signature is different from the test block expected signature; and repeating preceding steps until the test is complete.

70 Claims, 8 Drawing Sheets