Improved Core Isolation and Access for Hierarchical Embedded Test

Benoit Nadeau-Dostie, Saman M.I. Adham, and Russell Abbott
LogicVision

Editor's note:
IEEE Std 1500 enables automation and hence allows for easier and faster integration of embedded cores into an SoC. This article describes an automated test development system based on the concept of embedded test.
—Erik Jan Marinissen, IMEC

IEEE Std 1149.1 is a widely accepted testability standard that has been in use since the early 1990s.[1] Although the standard was primarily focused on board-level assembly verification testing via the boundary scan register, its test access port (TAP) and many optional provisions make it usable for a broader range of applications. Since its inception, researchers have proposed numerous extensions and applications that allow designers to use the standard's TAP for general system-level test and maintenance tasks and for accessing chip-level testability features.

Until the late 1990s, chip-level applications used TAP for accessing a chip's scan design or on-chip BIST features. However, it became apparent that increasing chip complexity would force new design and test methods. On the design side, circuits are now partitioned into blocks to facilitate synthesis and layout. Iteration turnaround times can be maintained at a reasonable level. Concurrent engineering enables several design teams to develop the various blocks in parallel. Some preexisting blocks can be reused, especially for standard functions, such as the PCI bus interface. Finally, several circuits exploit the architecture's regularity by using several instances of the same block.

These new design methods have introduced completely new test constraints.[2,3] Unlike ICs, cores can't be manufactured and tested individually. Direct access to core ports is virtually impossible. The problem is similar to testing a fully assembled printed circuit board (PCB) without having previously tested the individual components. Test and diagnosis of such a board is possible only if each IC comes with a standard test interface such as IEEE Std 1149.1, which has internal and external test modes. IEEE P1500 was proposed to similarly address the testing of core-based circuits. The internal test information is encapsulated in the form of scan test vectors or BIST procedures, and no design knowledge is necessary. This is especially useful when the core is provided by a third party. Each core's external test information makes it possible to test the connections and logic between cores.

In this article, we describe a new hierarchical embedded-test methodology developed at LogicVision for core-based designs. The wrapper serial port (WSP) of IEEE Std 1500 is at the heart of the test architecture.[4] Each core is equipped with a WSP and controlled by the top-level TAP to provide access to all core test controllers. An improvement to the standard, called *shared isolation*,[5] makes it possible to significantly reduce core isolation costs while enabling at-speed testing of core interface signals. Our methodology provides a fixed core test interface regardless of the number of test resources under its control. The star architecture allows verification and testing of cores independently, enabling concurrent engineering and better diagnostic resolution.

Hierarchical test architecture

Figure 1 shows an example IC using LogicVision's hierarchical test methodology. This simple circuit

0740-7475/09/$25.00 © 2009 IEEE Copublished by the IEEE CS and the IEEE CASS