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(54) **METHOD AND PROGRAM PRODUCT FOR MODELING CIRCUITS WITH LATCH BASED DESIGN**

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(58) Field of Search **716/6, 3, 5, 21**

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(57) **ABSTRACT**

A method of and computer program product for modeling a logic circuit having combinational logic and latches, in which the latches are clocked by one of a first clock phase, a second clock phase or a pulse derived from the second clock phase, a subset of latches being scannable, comprises, for each latch in the logic circuit, associating the latch with one of the first and second clock phase; and when latch is associated with the first clock phase, modeling the latch as a buffer connected between the data input and output of latch; and when the latch is associated with the second clock phase, modeling the latch as an edge-triggered flip-flop having the same data input, data output and clock input as the latch.

25 Claims, 4 Drawing Sheets

