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(54) **MASKING CIRCUIT AND METHOD OF MASKING CORRUPTED BITS**

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(57) **ABSTRACT**

A masking circuit for selectively masking scan chain inputs and/or outputs during scan testing of an integrated circuit, comprises a mask register having at least two mask register elements for each scan chain to provide a plurality of masking modes; and an input and output mask control circuit for each scan chain, each mask control circuit being connected between a test pattern source and a signature register and between a serial input and a serial output of an associated scan chain and being responsive to mask control data stored in the register elements for configuring the associated scan chain in one of the plurality of masking modes during a scan test of the circuit.