Complete, Contactless I/O Testing – Reaching the Boundary in Minimizing Digital IC Testing Cost

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Abstract

Embedded test of memory and random logic can enable very low cost ATE to test large, high speed ICs because high quality at-speed tests can be generated on-chip. However, it is also necessary to test the DC and AC parameters of the input/output (I/O) circuitry. This paper describes how most I/O pin characteristics can be tested cost-effectively with a variety of novel techniques that exploit the 1149.1 and 1149.4 test standards. The techniques measure VOL/IOL, VOH/IOH, VIH, and VIL at DC, perform at-speed I/O wrap, and test on-chip power rail impedance, all via minimum pin-count (MPC) access. The 1149.4 bus is also suitable, of course, for testing mixed-signal functions. The paper then discusses costs and benefits of MPC testing of high pin-count ICs on a low cost tester to show that testing costs can be reduced to insignificance.

1. Introduction

Reduced pin-count (RPC) testing has been proposed [1], [2], [3] to facilitate low-cost probe testing of high pin-count ICs – it can also facilitate multi-site testing. These techniques contact between 10 and 64 digital pins, including at least the four or five IEEE 1149.1 Test Access Port (TAP) pins. Conventional probe cards limit robust digital test frequencies to less than 10 MHz, however, probe cards are available that can handle much higher frequencies for a smaller number of probes or a higher cost. Of course, the tester must be able to accurately deliver these higher frequencies (or more accurate signal edge timing).

Although the reported RPC probe techniques test the logic core and embedded memories via scan or BIST, and test the basic structure of wrap-around input/output (I/O) circuitry, the I/O pin DC and AC parameters are not tested, with the exception of pin leakage current as reported in [3][9]. The resultant yield dropout in the subsequent full pin-count (FPC) Final test, due to insufficient I/O parametric performance, will usually be less than 1% as suggested in [2], so not probe testing I/O parametric performance would appear to have minimal cost impact. However, I/O parametric tests are often regarded as essential at Wafer Sort, for several reasons: Wafer Sort and Final (package) tests are typically performed at different temperatures to improve fault coverage; parametric tests during Wafer Sort provide an early indication of processing quality; some ICs are only ever tested at the wafer level, i.e., those destined for chip scale packaging (CSP) or multi-chip modules (MCM).

BIST is widely used for testing embedded SRAM because the quality of simple scan-access testing is inadequate, the number of memories is too many for direct access, the fault coverage of some BIST algorithms has been demonstrated to be equivalent to direct access, the patterns can be applied at higher speed by BIST, and the number of test patterns is too many for single-site testing by conventional ATE. Programmable BIST for embedded DRAM offers the same benefits, plus new algorithms can be applied if new defect mechanisms are found after silicon fabrication. The test time for memory BIST which applies the patterns at-speed is therefore the minimum possible (or very nearly). For example, a megabit of SRAM, partitioned as four 8Kx32b SRAMs, can be tested sequentially by one BIST controller having a 22N algorithm, and operating at 25 MHz, in 70 ms.

Recent experiments by Prof. McCluskey and his students [22] provide an interesting conclusion regarding BIST for random logic: the only combinational logic test that achieved zero test escapes, relative to an exhaustive test, was pseudo-random patterns applied at-speed until every stuck-at fault had been detected at least fifteen times.

Therefore, one can conclude that random logic and embedded memories could be structurally tested by BIST, and that functional tests for these functions might no longer be necessary to achieve zero test escapes (if the BIST is applied consistent with the above experiment). The test time for BIST of logic can be reduced, almost arbitrarily, by reducing the length of the scan chains and increasing the number of scan chains. In practice, the number of scan chains is limited to several hundred per pseudo-random pattern generator (PRPG) to minimize interconnect. Circuit macro-blocks tend to contain less than 50,000 scan bits, so a hierarchical approach that uses one PRPG per macro block is sufficient to reduce all scan chains to less than 300 bits, and many blocks can be tested in parallel. If each pseudo-random scan pattern is shifted at half-speed (to consume power that is comparable to normal operation) but applied at-speed for a few clock cycles around the mission-mode cycle, then test times can be near minimum (for example: 500 bits × 50K vectors / 50MHz = 500 ms).

It has previously been reported [20] that BIST for PLLs can be implemented digitally, and that the test time

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for jitter, lock range, lock time, and loop gain, can be reduced to about 50 ms, compared to the 500 ms or more required for conventional testing of a subset of this parameter list.

The preceding four paragraphs illustrate that a small number of low frequency signals from a low cost tester could test a large IC in less than 2 seconds. Low cost testers can cost less than $0.02 per second (see Appendix), thus test cost could be reduced to a few cents for a multi-million gate, megabit IC that also contains a PLL. If embedded test could also address I/O pin AC and DC parameters, with similar efficiency, then many devices could easily be fully tested in parallel, and this would approach the "boundary" to minimizing the cost of testing digital ICs.

This paper will describe some new methods for testing the I/O pin DC and AC parameters via a combination of digital and analog techniques that use the 1149.1 and 1149.4 test access standards. The paper starts by describing typical parametric pin tests. It next introduces 1149.4 and then discusses how to test DC parameters, via a modified 1149.4 access, for high pin-count ICs. Next, at-speed testing of AC parameters is described using the core clock and embedded clock generation so that any low frequency tester can be used to test I/Os at-speed. The impact of power rail quality on AC performance is discussed, together with a novel test circuit that measures this impact. After considering the value of 1149.4 for testing the inevitable mixed-signal functions on a "digital" IC, we describe hardware verifications, limitations, and discuss the economics of the test strategy.

2. I/O parameters

I/O pin DC parameters that are typically tested at Wafer Sort (with FPC access) include the output voltages and currents (VOL, IOL, VOH, IOH), the input voltage logic levels (VIL, VIH), and the pin leakage currents (IIL, IIH, IOZ). Testing these parameters typically requires a DC parametric measurement unit (PMU) to be connected to the pins, via relay switches. The PMU applies a voltage or current, and the resultant current or voltage is compared to a threshold to determine pass/fail. For testers with a DC PMU per pin, test time can be as little as 5 ms per parameter, limited by a 1~5 ms relay settling time and the PMU speed. For testers with a PMU shared among several pins, the test time is proportionally longer. Most test programs do *not* test leakage for all pins simultaneously, to ensure detection of shorts between the pins – this further increases the test time. Of course, appropriate patterns need to be loaded prior to each DC test – these patterns are simplest when 1149.1 boundary scan is used. Typical test programs require 200~900 ms to test all I/O DC parameters for ICs with more than 256 signal pins.

I/O pin AC parameters typically include propagation delay, setup and hold times, and rise and fall times. These tests are performed using a timing parametric unit (TMU) or by comparing an output signal, after a precise time interval, to an expected voltage, or by applying an input signal at a precise time interval after a clock edge. Sometimes a binary search is performed to find the time of a signal transition. The AC parameters can normally be tested in less than a few hundred milliseconds, but may require longer if a different time-set and initialization pattern is required for each pin tested. Boundary scan access does not typically help for these tests.

3. Testing I/O DC Parameters

Designing a digital IC with boundary scan and "I/O wrap" permits basic contactless structural test of I/O pins. I/O wrap means that the pins are made bi-directional (the signal wraps around), including pins which functionally need to be only inputs or only outputs. The added cost of making a pin bi-directional is usually insignificant (e.g., a minimum-sized driver is added to an input-only), and some companies design most pins to be bi-directional to simplify board-level testing anyway. The bi-directional pins need to have appropriate boundary scan, as shown in figure 1, i.e., scan cells that control the output enable signals.

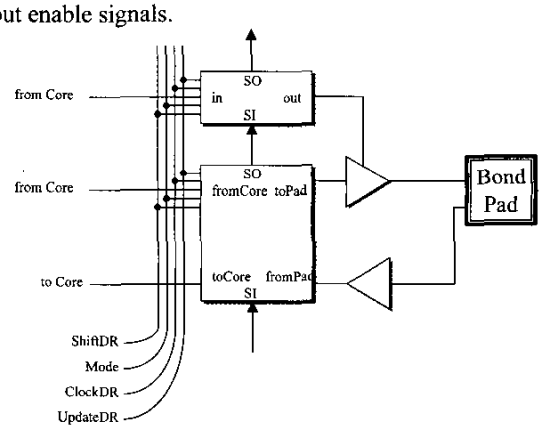

Fig. 1 I/O wrap with 1149.1 boundary scan

During IC test, a basic I/O structural test can be performed by driving (updating) each I/O pad to a logic value, and then latching (capturing) the received value and shifting it out through the boundary scan register. All pins can be tested in parallel, however, adjacent pins should be driven to different values to permit detection of pin-to-pin shorts. This is a relatively slow wrap-around interval because the time between update and capture is a minimum of 2½ TCK cycles, and the TCK frequency is typically much slower than the I/O functional clock rate. For example, f_{TCK} is typically about 10 MHz, whereas function mode I/O operation might be 200 MHz.

An 1149.1-controlled basic structural test can be extended to test for leakage current (IIL, IIH, IOZ), using the technique described in [3][9] and shown in figure 2. In that technique, each I/O pad is first driven to a logic

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value, and then the driver is disabled (tri-stated) so that the pad voltage floats and discharges at a rate determined by the pad capacitance and the leakage current. The pad's logic value is captured a precise time later (e.g., 3 µs), as controlled by f_{TCK} and the number of Run-Test/Idle states inserted between updateDR and captureDR. Test time is one or two milliseconds for almost any number of pins.

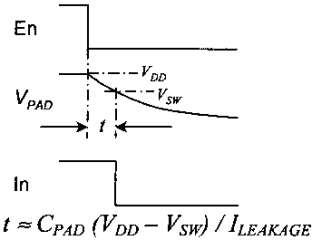

Fig. 2 Principle of leakage current test

3.1 1149.4 for testing digital ICs

To test other I/O DC parameters, analog access to the pins is necessary. The IEEE 1149.4 Standard for a Mixed Signal Test Bus [4] specifies an analog extension to 1149.1 digital boundary scan [5]. Briefly, 1149.4 simply adds two analog buses to an IC that has 1149.1 (JTAG) boundary scan, and routes them to some or all of the IC's pins, as shown in figure 3, so that an analog stimulus signal can be applied to each pin, and an analog response signal can be measured at a pin, possibly the same pin. Therefore, this infrastructure can enable measurement of the output drive of a digital pin without contacting the pin. It can also facilitate monitoring on-chip voltages in voltage converters, back-bias generators, or differential logic.

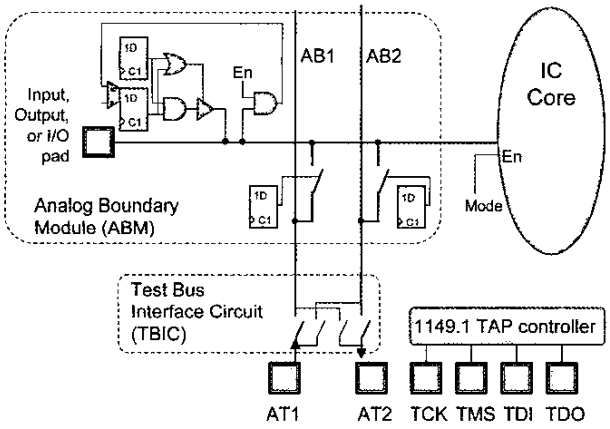

Fig. 3 1149.4 circuitry: ABM, analog buses, TBIC, TAP

Designers typically have two major concerns with the 1149.4 scheme, but these now have new solutions.

Problem: It has been reported [6][7] that adding 1149.4 to an IC that already has 1149.1 boundary scan would increase the IC's area by 3%.

Solution: Fortunately, the additional area is decreasing predictably with each shrink in technology. For example, it is about 3% for a 1 cm die in 0.8 µm technology relative to a non-pad-limited design with boundary scan, but less than 0.8% for 0.25 µm. This paper will show how the benefits of adding 1149.4 can exceed the silicon cost for 0.18 µm, and thus reduce IC cost. The favorable economics of this approach is implied in a recent patent by Intel [8] that describes a technique for contactless pin leakage testing via one or two analog buses routed to each pin.

Problem: The 1149.4 analog bus is specified to have a minimum frequency range (-3dB) of 100 kHz, which is insufficient to test most digital signals and many analog signals. In any case, an analog bus that carries high frequency signals would cause interference problems on an IC.

Solution: Most commercial LCR meters perform impedance measurements at frequencies below 10 kHz to minimize noise effects. The techniques described in this paper will use sub-megahertz frequencies on the analog bus.

Benefits of 1149.4 are increasing as new techniques arise, however, the standard was initially aimed at providing benefits for board-level test and mixed-signal IC test so there is no published material on using 1149.4 for digital ICs, except for one paragraph in [7] which states,

> "DC parametric tests are required to verify that all of the parallel transistors are defect-free in output drivers, and that input switching points and leakage currents are correct. The P1149.4 bus allows testing of these parameters without requiring a probe for each pad. For example, a current can be delivered to a pad whose output driver (controlled via the boundary scan data register) is driving a logic 'low'. If the driver is specified to deliver 16 mA at 0.4 V, then 2 mA should cause <50 mV output. This can be measured via AT2, thus verifying the transistors are intact. Likewise, leakage current at inputs or tri-state outputs can be measured. Lastly, a voltage ramp could be delivered via AT1 to each function input pin to determine its switching point. Thus, a lower cost probe card and tester, with perhaps only 50 probes (mostly power) could test a 500 pin IC."

3.2 Testing I/O Current

A technique for testing IOL and VOL for many pins, via an 1149.4 analog bus, may be summarized as follows:

1. via boundary scan, drive a pin to logic 0, and enable the two analog bus switches for the pin;
2. apply a known source current (e.g. 1 mA) to the pin via one of the analog buses;
3. monitor the voltage at the pin via the second analog bus, and compare the voltage to a threshold to determine pass/fail;
4. repeat steps 1~3 for each pin to be tested.

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The CMOS transmission gates used to route the bus current to each pin are optimally designed to have between 300 and 1000 ohms resistance, and so the stimulus current is typically limited to less than 5 mA. The 1149.4 standard only requires that the bus be able to convey at least 100 µA and that the total series resistance be less than 10 kΩ. Therefore, to determine the pass/fail threshold voltage for a 16 mA output pin, using a 1 mA load, it is necessary to first characterize the driver to statistically correlate the driver's output voltage at 1 mA to its output voltage at IOL, e.g. 16 mA.

The procedure is repeated to test IOH and VOH, by updating all pins to drive logic 1 and applying a known sink current.

Each I/O must be measured individually to ensure that all of the known stimulus current is applied to each pad in turn. Fortunately, each measurement time can be quite fast. The source impedance will be about 1000 ohms (largely due to the access transmission gate) and the total bus capacitance will be about 100 pF (including off-chip bus capacitance), so the time constant is approximately 100 ns and therefore permits an accurate measurement in 1 µs. If all pins are tested sequentially, the voltage of the (100 pF) monitoring analog bus will change only minimally as each pin is accessed in turn.

A conventional PMU may not be fast enough – instead the analog bus voltage could be sampled by a comparator or by a high impedance (>1 MΩ) digital channel whose input switching point can be set with millivolt accuracy. When testing a 50Ω output driver with a 1 mA stimulus, achieving 1% accuracy requires measuring the resultant 50 mV (i.e., V_{SS}+50mV or V_{DD}–50mV) with better than ±0.5 mV uncertainty at 1 MHz – this is quite practical for many digital testers. Alternatively, an on-chip comparator can be connected to the analog bus, however, comparators that are accurate at voltages very close to the power rails are non-trivial.

The time to reload the boundary scan register can become the most significant consumer of test time in this procedure. For a 50 signal-pin IC, and f_{TCK} = 10 MHz, the time to re-load the 200-bit boundary scan register (1149.4 requires 4 scan bits per pin) would be about 20 µs, and the time to perform this 50 times would be 1 ms. However, for a 500 signal-pin IC, the time for boundary scan loading would be 200 µs per scan load, and 100 ms to perform this 500 times. The test time is proportional to the square of the number of pins.

A novel improvement, shown in figure 4, is to update the analog switch controlling bits (B1 and B2) of the boundary scan register, separately from each ABM's data and enable control bits (D and C) and TBIC bits, and to suppress Capture entirely. With this arrangement, after updating the necessary bits into the D and C latches, the boundary scan shift register is re-loaded with all logic 0's, and two logic 1's at the B1 and B2 bits corresponding to the first pin to be measured. Then, a partial update-only updates all B1 and B2 latches. After performing the measurement, the boundary scan shift register is clocked 4 times to shift the two logic 1's to the next pin's B1 and B2 register bits, and the partial update is repeated. This needs only four shift clock cycles between updates, as shown in figure 5, and means that the boundary scan load time will grow only linearly with pin count. The load time for each additional pin then becomes about 1 µs, and the time for 50 pins becomes 50 µs. For 500 pins, the time becomes 500 µs. Adding the 1 µs measurement time for each pin, and performing the test for both logic 1 and logic 0, increases the total test time to 2 ms for 500 signal pins. Increasing the measurement time ten-fold, to 10 µs, only increases the test time to 20 ms.

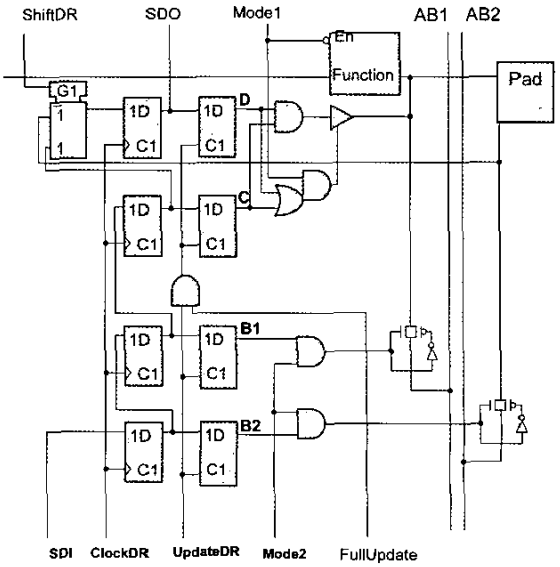

Fig. 4 ABM with partial/full update capability

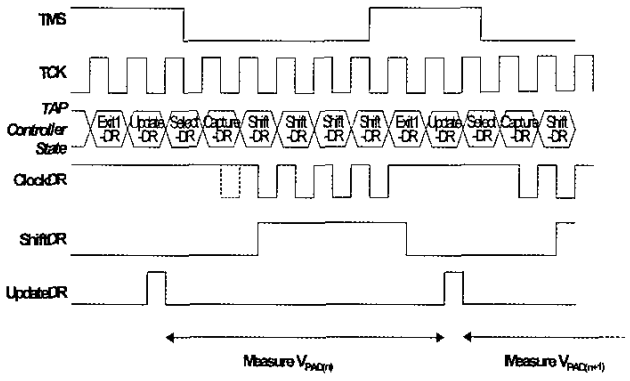

Fig. 5 Timing diagram for fast sequential analog access, regardless of length of boundary scan register

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3.3 Testing Input Voltages

Another important test verifies the maximum logic 0 input voltage (VIL) and the minimum logic 1 input voltage (VIH). In summary, this test can be performed, using 1149.4, as follows:

1. via boundary scan, enable the B1 (and/or B2) analog switches for all pins
2. apply the VIL (or VIH) voltage via the analog bus
3. via boundary scan, capture the resultant logic value at each input, and shift out the expected logic 0's (or 1's).

While it is possible to apply a single voltage to a large number of inputs simultaneously (that are specified to have the same VIL), via the 1149.4 bus, this is not practical because the sum of the input leakage currents might not be negligible. For example, if the series transmission gate resistance is 500 ohms, each pin's leakage current is 500 nA, and 500 pins are tested in parallel, the voltage drop across the transmission gate will be 25 mV. If the number of pins tested simultaneously is reduced, the accuracy improves.

For pins that have more than 1 μA leakage current, perhaps due to a pull-up resistance that cannot be disabled, the VIL/VIH test can be applied to one pin at a time. It may be necessary to monitor the voltage that is actually delivered to the pad, via the second analog bus. Typical PMUs have separate force and sense terminals [27] – the force terminal can be connected to one of the analog buses, and the sense terminal can be connected to the other bus. Using the analog buses as force/sense lines is a powerful and general technique for ensuring accurate delivery of AC and DC voltages to any on-chip circuit node.

Testing IIL and IIH can be done with a procedure similar to that used for testing IOL and IOH. All pins are put in tri-state mode, and a 1 μA sink current is applied, in turn to each pin via one analog bus. The voltage at the pin is monitored via the same analog bus (or via the second bus using an on-chip comparator). For a pin that has 1.1 μA source leakage current (IIL), the time for the 100 nA difference current to charge the 100 pF analog bus, and cause a 100 mV change, is $t=Cv/i$ = 100 μs. Testing 500 pins this way will require about 50 ms. This method is significantly slower than the method described in [3] but facilitates higher accuracy diagnostic measurements when needed.

Differential pins are becoming more common to accommodate increasing frequencies and decreasing power rails voltages. The 1149.4 test access standard requires the same test approach for all pins, including those that are half of a differential pair. This means that four boundary scan bits and a single-ended input buffer are needed for each pin (i.e., eight bits for a differential pair). The two analog buses may each be differential (i.e., four bus wires in total) to improve noise tolerance and diagnosability. An interesting test case is a low-voltage differential signal (LVDS) driver. To test this type of output, more than 3.5 mA is required to verify that the current sourcing capability is intact, but a lower current can be used to test the current sinking capability. For an LVDS receiver, a true differential stimulus is needed to verify the offset voltage and switching point, hence a differential analog bus may be essential (it is possible to use the two-single-ended analog buses to deliver a differential signal, but then the actual voltage delivered can not be monitored simultaneously).

In summary, embedded testing of a DC parameter for 500 pins, requires less than 10 ms. VOL/IOL, VOH/IOH, VIL, VIH, IIL, and IIH can all be tested in 10~100 ms, which is up to 10~100X faster than typical FPC testing.

4. Testing I/O AC Parameters

A technique for at-speed testing of board-level interconnect was reported in [10][11]. The key principle of the technique is using the high-speed core clock for each output pin signal to clock a short sequence of inverted-data, data, inverted-data. The TCK clock would not be suitable for such a test because its maximum frequency is typically too low, and its edges have too much timing uncertainty (TCK is not typically routed with clock tree synthesis). As seen in figure 6, at each input pin, data is captured using the system core clock and a function-mode flip-flop, and only when the non-inverted data is expected, thus testing that the board-level interconnect transferred the data within one core clock cycle. The technique uses an existing board-level signal common to the ICs involved for coarse synchronization – the scheme is transparent to 1149.1 mode.

The same principle can be used to perform at-speed I/O wrap, with or without contacting the pad. The pad is driven with a data burst (101 or 010) at the core clock rate, and the pad value is captured using the same clock. This verifies that the delay from one clock edge to Q-out, to pad, to D-in, to the next clock edge is less than one core-clock period. For an uncontacted pad, most delay faults in either the output driver, or the input receiver will cause this test to fail, especially since the driver must also pass the DC parametric tests previously described.

A more stressing at-speed I/O wrap test can be performed during Final test by connecting a capacitive and/or resistive load to the outputs, within 1 or 2 cm of the DUT to avoid transmission line problems. For a package test, this can also serve to test for a defect-free bond wire connection. For example, if a 100 pF capacitor load is used, then the I/O-wrap path delay for an 8 mA output driver will increase by 20 ns compared to no connected capacitance. Then, if the pad's logic value were captured 10 ns after being updated, no logic change would be expected – if the pad's logic value has changed, then no capacitance is connected and the bond wire must be defective.

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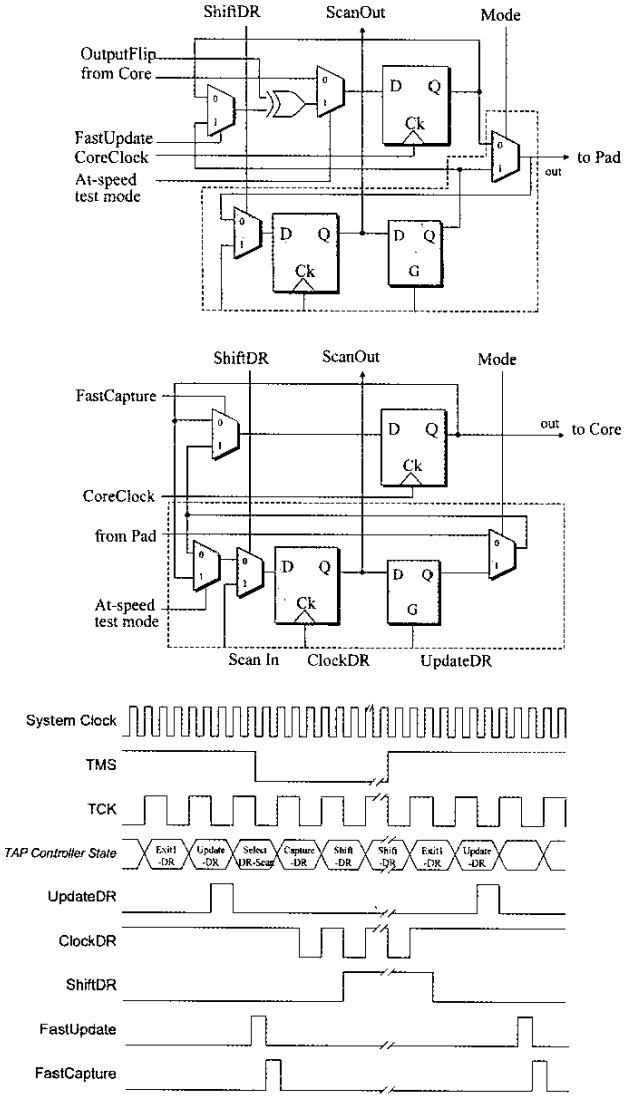

Fig. 6 **Boundary scan cells** (shaded logic gates) **and waveforms for at-speed I/O wrap** (unshaded logic gates are part of core function and scan path)

4.1 HF Clocking with a Low Frequency Tester

The high frequency core clock is typically generated by a PLL whose input frequency is a lower frequency, typically less than 50 MHz. For many testers, a 50 MHz clock to the DUT presents problems: the frequency is beyond the capability of many PC-based testers, and the interface board is significantly more expensive than for frequencies less than 10 MHz. Three practical solutions are described next.

To generate a DUT input clock frequency greater than the ATE/hardware capability, the PLL within the DUT can be designed to handle a lower input frequency during test. This typically means increasing the PLL's feedback divider count (if it is not already possible). Adjusting the PLL's output frequency for testing portions of the on-chip logic has also been reported [12]; many other variations are possible.

A second approach is to place a free-running crystal oscillator on the device interface board, a minimum distance from the DUT. This may not be suitable for scan-based testing because the crystal clock will be asynchronous with respect to the ATE. Some logic BIST approaches [13][25] are able to run asynchronously with respect to the tester and yet deliver results synchronously via the TAP.

A third approach is to provide a free-running clock generator on-chip. A digitally tunable ring oscillator can be used for this purpose, preferably one that is synthesizable such as that described in [14]. For a process with 30 ps nominal inverter delays, oscillation period increments will typically be 50 ps which corresponds to 1% for a 200 MHz oscillator (T=5 ns). The delays added by multiplexers, and worst/best case delay range can reduce this accuracy to 5%. Smaller increments can be achieved by connecting tri-state buffers in parallel and selectively enabling one or both of them. Higher oscillation frequencies, with the same accuracy, are possible by using multiple ring oscillators, designed with overlapping, narrow frequency ranges, as shown in figure 7. A binary search algorithm can determine the optimal delay setting to achieve any target frequency. Occasional trimming of the oscillation frequency can be performed using TCK as the reference frequency (during intervals when it has a constant frequency), or any other accurate low frequency source, to maintain the frequency within one or two percent of the target frequency. A digital ring oscillator is not known for low jitter, however, its output would normally be the input to the core clock's PLL whose output would have low jitter. As discussed for the crystal oscillator solution, this approach is only suitable for scan or logic BIST that can accommodate asynchronous clocking relative to the TAP clock.

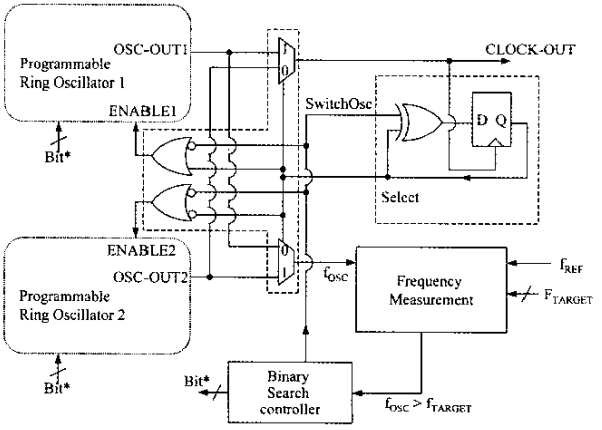

Fig. 7 **Embedded clock generator**

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Another approach, denoted "delay I/O wrap test" [15] uses separate launch and capture clocks generated by the ATE or on-chip. This approach can address delays shorter than a clock cycle, but is more complicated to implement because it requires additional precise clocks.

For gigahertz I/O pins, a clock frequency might not exist on-chip for updating and latching the output, or else it might be impractical to clock a flip-flop at gigahertz rates. For these pins, an alternative low-cost approach was proposed in [23] in which a high speed output pin is connected to an off-chip, passive, low pass filter to introduce data-dependent jitter in the data stream before the signal is connected back into an input of the IC. This is not I/O wrap on a single pin (and hence not suitable for contactless probing), but quite similar, and does not involve the ATE. Many ICs that have high speed I/Os also have built-in pseudo random pattern generators and pattern comparators so that they can perform built-in bit error rate testing (BERT), e.g., Texas Instruments' SLK2501 and National Semiconductor's SCAN921023.

4.2 Power rail impedance

A troublesome source of I/O path delay defects is the power rail inductance and resistance, as has been reported extensively, e.g., [16]. A typical high pin-count IC has a large number of power pins, comparable to the number of signal pins. The many power pins are needed to reduce the amplitude of power rail glitches during switching of I/Os (and core logic) due to the rapid *di/dt* of CMOS logic combined with the inductance and resistance in the power rail. Variations in power rail impedance can also be a significant contributor to skew between output signal edges. Functionally testing signal skew is relatively time-consuming and requires high performance ATE.

The need to test power rail quality has been discussed in the literature. One paper [17] highlighted the impact of faulty power pin connections at the board-level – the defects are relatively common and are very difficult to diagnose or detect. X-ray laminography was proposed as a practical way to detect unsuccessfully soldered power pins. Another paper [18] proposed an analog technique for measuring the voltage drop in any power rail line while a known current flow is being induced, but the approach can be area intensive (1% of IC).

Unfortunately, measuring the resistance (or inductance) of the power rail does not prove that glitch amplitudes will be sufficiently small. It has been recently proposed [19] that signal line overshoot be measured using an analog comparator to compare the signal to a clean V_{DD}. This could be considered for power rail glitches, however, glitches of interest can be less than 100 ps in duration (too fast for most comparators), the glitch amplitude needs to be adjustable during test, and a suitably quiet reference V_{DD} can be difficult to obtain.

A novel way to test for power rail glitches is to implement a conventional set-reset NAND-gate flip-flop that has one input connected to an analog bus, as shown in figure 8. By driving the input DC voltage to just above the logic gate's switching point voltage, the logic gate is made programmably sensitive to power rail glitches. As shown in figure 8, any increase in V_{DD} or V_{SS}, relative to the analog bus voltage, will set (change the state of) the flip-flop. Its value can be scanned out, before it is reset by a scan bit, and scanned out again to verify the reset. A NOR flip-flop can be used also, with an analog bus voltage set just below the input switching point voltage, to detect decreases in V_{DD} or V_{SS}.

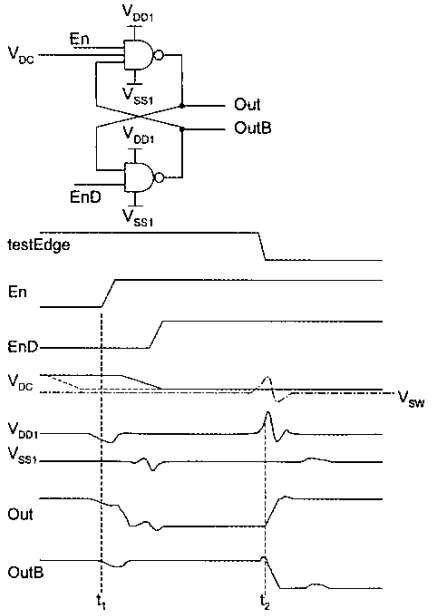

Fig. 8 NAND flip-flop for detecting positive-going power rail glitches (and waveforms)

This power rail quality test circuit can detect any sub-nanosecond glitches that would affect digital delays. The amplitude of glitches that is detected can be adjusted by varying the analog bus voltage (limited by the noise on the analog bus). Stimulus glitches on the power rail can be instigated by updating an output pin to cause a logic transition. One of each flip-flop type can be physically located near each power pin to detect whether that pin has been successfully soldered to a circuit board.

Silicon area increase for power rail DFT is negligible: two scan flip-flops and four combinational gates per sensor (NAND flip-flop and NOR flip-flop); the number of sensors is equal to the number of V_{DD}/V_{SS} pairs.

In summary, embedded testing of AC performance for all pins can be performed in negligible test time (a few tens of milliseconds). At-speed I/O-wrap testing, using the core clock, will detect most delay faults. When using a low speed tester, it is possible to generate any core clock frequency by using the function's PLL, an embedded clock generator, and/or an interface board-mounted

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crystal oscillator. Power rail quality can be tested by initiating output pin signal transitions while monitoring the power rail voltage with a "hair-trigger" set-reset flip-flop whose input is connected to a near mid-rail voltage from the 1149.4 analog test bus.

5. Mixed-signal testing

Many digital ICs contain a small amount of mixed-signal circuitry, such as a low speed ADC, DAC, comparator, or reference voltage. It is likely that "random analog" has no general test solution; all that can be hoped for is that expensive-to-develop tests can be re-used when the circuitry is placed in another IC design. Tests that are implemented via the 1149.4 analog test bus are re-usable – only the position of scan bits that enable analog access switches (transmission gates) changes from design to design. In many cases, IC designers must provide analog access to these functions anyway [26], so using a standard analog bus for all such access becomes simpler and might not increase the pin count. The analog bus design is simplest for low frequency (<1 MHz) analog signals, but it can be designed to handle higher frequencies. To minimize digital access times, control bits for the analog switches, or digital access to ADCs or DACs should be part of a dedicated, TAP-addressable, short scan path.

6. Hardware verification

A general purpose 1149.4 chip [21] is available from National Semiconductor, in sample quantities, and it allows verification of the above concept for existing ICs by connecting pins of the 1149.4 IC to pins of an IC under test. This 1149.4 chip was used to verify the 1149.4 DC measurements described in this paper. The output drive for a typical digital pin was measured at various load currents to see whether testing at 1mA was representative of output impedance measured at the rated IOL. A typical relationship is shown in figure 9.

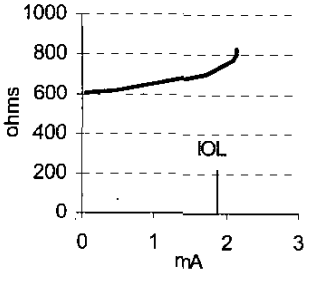

Fig. 9 Output impedance (measured) vs. load current for the 1149.4 IC (0.25 µm n-channel transistor, logic 0)

At-speed, on-chip, I/O wrap was verified using a laser-programmed gate array (LPGA). It was also implemented by connecting an output-only pin, that had at-speed interconnect test capability, to an input-only pin that was similarly equipped, via an off-chip wire. The at-speed interconnect test was verified on various ICs, including one with a 400 MHz core clock.

An embedded clock generator was verified on the above LPGA – it used two ring oscillators, with adjustable loop delays, and each ring oscillator targeted a different (overlapping) frequency range to allow high frequency operation and yet maintain frequency increments of a few percent. The clock generator achieved 250 MHz operation in 0.6 µm CMOS at room temperature, which translated to over 100 MHz, with ±2% accuracy under all conditions – accuracy is easier to achieve for oscillators designed for lower frequencies or in finer geometry processes.

Power rail quality testing was verified using an FPGA. An analog voltage was applied to a pin, which was the input to a set-reset flip-flop, and an adjacent pin was toggled. Power rail glitches of a few nanoseconds were visible using an oscilloscope, and were sufficient to trigger the flip-flop. Simulations were performed using finer geometries and 1 nH power rail inductances. The capacitance of the on-chip analog bus to many AC grounds generally helps to make the bus voltage stable; it will nevertheless experience noise that is significant but less than the power rails.

7. Limitations

Some of the proposed tests apply only to Wafer Sort test. For example, some I/O tests need to be performed with rated load currents, or capacitances, so the test cannot be performed without contacting the pad – these tests can be done at Final test using a low-speed tester channel (PMU) connected to the pin. However, for some ICs (as discussed earlier), only a load capacitance might be connected for final test, and the contactless tests can still be run, with slightly different test times – these tests would also verify the integrity of the bond wire.

The voltages on an on-chip 1149.4 analog bus are typically constrained to be between V_{DD}+100mV and V_{SS}-100mV, and hence testing the electro-static discharge (ESD) protection circuitry at each pin is not normally possible. However, faulty protection circuits often cause excessive pin leakage, and the protection circuit would be tested for the contacted TAP pins.

8. Discussion

The cost of adding 1149.4 to an IC that already has 1149.1 is 0~4 analog pins (depending on whether there are existing analog test pins that can be subsumed), 4 scan bits per pin instead of 1.5 bits (average), and 2 analog bus wires.

A recent paper [2] reported test economics for "low pin-count" testing – the authors predicted minimal benefit from using logic BIST and RPC testing alone, but they predicted significant benefits when also using multi-site probing. The paper predicted that not performing

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parametric test of the I/O circuitry would only decrease Final test yield, and focused on increasing the application rate for scan vectors to the maximum permitted by the I/O pins and 200 MHz ATE.

The scheme presented herein reduces off-chip clock frequency to 10 MHz without reducing test rate, and does not omit I/O parametric tests. High Final test yield is therefore maintained, and any existing ATE can be used for Wafer Sort, especially ATE whose capital cost has been fully depreciated and which needs minimal maintenance (±5 ns edge placement accuracy is sufficient). As a result, higher up-time for these testers can be expected, further increased by being able to test a greater variety of ICs (if designed with embedded test).

Table 1 shows test time benefits of the enhanced boundary scan. It shows an order of magnitude reduction in I/O parametric test time (excluding multi-site testing):

	Standard	MPC access	
Pin leakage	200	2	ms
Output drive	100	2	ms
VIL/VIH	0 *	2	ms
I/O delay	200	2	ms
Pin skew	200	22+	ms
Total	**700**	**30**	**ms**

* VIL/VIH is usually tested concurrently with functional patterns.

\+ The time depends on how many RS flip-flop switching point voltages are measured for the power rail test.

Table 1 Wafer Sort test benefits for a 450 signal-pin IC

Other aspects of test strategy could also be compared, but they are harder to quantify in terms of IC cost benefit. For example:

	Standard	MPC access
Cost of ATE capital:	high	low
Random analog test time:	0.5~2 s	0.1~0.3 s
Test program	Tester-specific	Tester independent
Strategy for 2X volume:	more ATE	multi-site test
Strategy for half volume:	idle high-cost ATE	idle low cost ATE
Strategy for KGD:	high cost probe cards	minimal change
Strategy for burn-in:	ignore I/Os	test I/Os

When combined with embedded test for logic and memory, the cost savings can be greater. Typical functional tests require 2~3 seconds, mostly because of many ATE channel time-set changes and low frequency operation of some core circuitry. Often, a low speed scan test is also performed, incurring another 200~500 ms. Typically, BIST test time for random logic will be about 1 second because, for any target fault coverage, the number of scan chains is increased and their length decreased until predicted test time reaches about 1 second – an arbitrary point of diminishing return.

Total test time for a 2~5M gate IC is typically 6 seconds or more. On a 512-channel, 200 MHz tester and prober, typically costing more than $0.05 per second of test time (see Appendix), this results in a Wafer Sort test cost exceeding $0.30 per IC. Total test time for embedded test of logic, memory, PLL, and I/O, as described in detail earlier in this paper, can be less than 2 seconds. A 32-channel, 20 MHz tester (and the same prober) would cost less than $0.015 per test-second, resulting in a test cost of less than $0.03 per IC – a 10X reduction.

Other benefits of the proposed test access that reduce the cost of I/O testing include the following:

- Probe cards are simpler and cheaper to design and debug because there are no high frequencies or precisely timed edges – this also makes multi-site testing more practical;
- Yield loss due to the number of probes can be improved – for example, 500 signal probes having 99.999% probability of good contact will cause $1\text{-}0.99999^{500}$ = 0.5% yield loss, whereas 20 signal probes will have a yield loss of only $1\text{-}0.99999^{20}$ = 0.02%;
- Pre-burn-in test, that includes I/O tests, can be performed using the burn-in loadboard;
- Faster time-to-volume due to simpler test hardware, easier migration to multi-site testing, and a structural power rail test;
- The IC and board-level interconnect, including passive components such as terminations, can be diagnostically tested before de-soldering suspected ICs for replacement or QA return – this can significantly reduce QA returns and simplifies analysis for ICs that are returned.

The embedded I/O test strategy can be applied to Final test to reduce test costs further. However, as is done for any new test, the quality of the MPC test must be proven first by using it only at Wafer Sort, and then analyzing any devices that subsequently fail Final test for non-packaging related reasons. A few functional tests may continue to be needed at Final test.

Like 1149.1, the value of 1149.4 at the board-level increases as more of the ICs on a board include these test facilities. However, the realities of the marketplace can prevent any new standard from being adopted at the IC level until it makes the IC cheaper to manufacture and test in the first place. Similarly, adding 1149.4 to a mixed-signal IC can appear too expensive if it only addresses analog testing. This paper has presented analysis that shows how 1149.4 can be justified for its digital test capabilities alone – other benefits come at virtually zero additional cost.

9. Conclusions

We presented a new 1149.4-based approach to I/O DC parameter testing that is analogous to analog scan and almost as quick as digital scan. A mostly digital AC parameter test has also been presented that implements a simple at-speed I/O wrap and a new power rail impedance test that responds to the amplitude of sub-nanosecond power rail glitches. Benefits of the new I/O test approach

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include lower cost ATE (fewer channels, lower speed), simpler hardware, and significantly faster test times than conventional FPC access when 1149.4 with a new partial update is used. Many previous papers have anticipated that lower cost testers would result in longer test times.

Analysis shows that Wafer Sort testing costs, and possibly Final testing costs, can be reduced by an order of magnitude for large ICs, while maintaining or increasing defect coverage. The proposed approach facilitates multi-site probing when FPC access might prevent it, so the approach also permits faster ramp-up to high volume and further test time savings.

Complete embedded test of high pin-count ICs, and some SOCs, using the techniques described, allows near-zero cost testing on simpler ATE, and hence approaches the limit, or boundary, of reducing testing costs.

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Appendix

Example calculations for cost per test-second:

	200 MHz, 512 pins	100 MHz, 256 pins	50 MHz, 64 pins
Capital cost for ATE	$2.5M	$1.2M	$0.2M
Capital cost for handler/prober	$0.5M	$0.5M	$0.5M
Amortization period, linear	*3 years*	*3 years*	*3 years*
Depreciation cost/sec	$0.032	$0.018 *	$0.007
Operator + floor space + power	$130K/yr	$100K/yr	$100K/yr
Maintenance (S/W and H/W) @10%	$300K/yr	$170K/yr	$ 70K/yr
Overhead cost/sec	$0.014	$0.009	$0.005
Total cost per elapsed second	$0.046	$0.027	$0.012
Utilization rate	75%	75%	85%
Total cost per active test second	**$0.061**	**$0.035**	**$0.015**

* Comparable to [2] which calculates $0.012/sec (single site) when total capital cost is $1.1M.

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