



US 20040257901A1

(19) **United States**(12) **Patent Application Publication**
Nadeau-Dostie et al.(10) **Pub. No.: US 2004/0257901 A1**(43) **Pub. Date: Dec. 23, 2004**(54) **MEMORY REPAIR CIRCUIT AND METHOD****Publication Classification**(76) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA);
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ABSTRACT(21) Appl. No.: **10/868,208**(22) Filed: **Jun. 16, 2004****Related U.S. Application Data**

(60) Provisional application No. 60/479,229, filed on Jun. 18, 2003.

A self-repair circuit for a semiconductor memory provides input and output test selectors coupled to respective data bit group inputs and outputs, respectively and input and output repair selectors coupled between the input and output test selectors and functional inputs and functional outputs, respectively. This arrangement allows all data bit groups to be tested in one pass and all test and repair selector circuitry to be tested.

