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NADEAU-DOSTIE et al.

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(54) **METHOD AND APPARATUS FOR STORING AND DISTRIBUTING MEMORY REPAIR INFORMATION**

(75) Inventors: **Benoit NADEAU-DOSTIE**, Ottawa (CA); **Jean-Francois Cote**, Chelsea (CA)

Correspondence Address:
RIDOUT & MAYBEE LLP
100 MURRAY STREET, 4TH FLOOR
OTTAWA, ON K1N OA1

(73) Assignee: **LOGICVISION, INC.**, San Jose, CA (US)

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(57) **ABSTRACT**

A system for repairing embedded memories on an integrated circuit is disclosed. The system comprises an external Built-In Self-repair Register (BISR) associated with every reparable memory on the circuit. Each BISR is configured to accept a serial input from a daisy chain connection and to generate a serial output to a daisy chain connection, so that a plurality of BISRs are connected in a daisy chain with a fuse box controller. The fuse box controller has no information as to the number, configuration or size of the embedded memories, but determines, upon power up, the length of the daisy chain. With this information, the fuse box controller may perform a corresponding number of serial shift operations to move repair data to and from the BISRs and into and out of a fuse box associated with the controller. Memories having a parallel repair interface are supported by a parallel address bus and enable control signal on the BISR, while those having a serial repair interface are supported by a parallel daisy chain path that may be selectively cycled to shift the contents of the BISR to an internal serial register in the memory. Preferably, each of the BISRs has an associated repair analysis facility having a parallel address bus and enable control signal by which fuse data may be dumped in parallel into the BISR and from there, either uploaded to the fuse box through the controller or downloaded into the memory to effect repairs. Advantageously, pre-designed circuit blocks may provide daisy chain inputs and access ports to effect the inventive system therealong or to permit the circuit block to be bypassed for testing purposes.