US011430537B2

(12) **United States Patent**
Nadeau-Dostie

(10) **Patent No.: US 11,430,537 B2**
(45) **Date of Patent: Aug. 30, 2022**

(54) **ERROR-CORRECTING CODE-ASSISTED MEMORY REPAIR**

(71) Applicant: **Siemens Industry Software Inc.**, Plano, TX (US)

(72) Inventor: **Benoit Nadeau-Dostie**, Gatineau (CA)

(73) Assignee: **Siemens Industry Software Inc.**, Plano, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/115,894**

(22) Filed: **Dec. 9, 2020**

(65) **Prior Publication Data**

US 2021/0174892 A1 Jun. 10, 2021

Related U.S. Application Data

(60) Provisional application No. 62/945,317, filed on Dec. 9, 2019.

(51) **Int. Cl.**

G11C 29/42	(2006.01)
G11C 11/16	(2006.01)
G11C 29/44	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 29/42*** (2013.01); ***G11C 11/1673*** (2013.01); ***G11C 11/1675*** (2013.01); ***G11C 29/4401*** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

(56) **References Cited**

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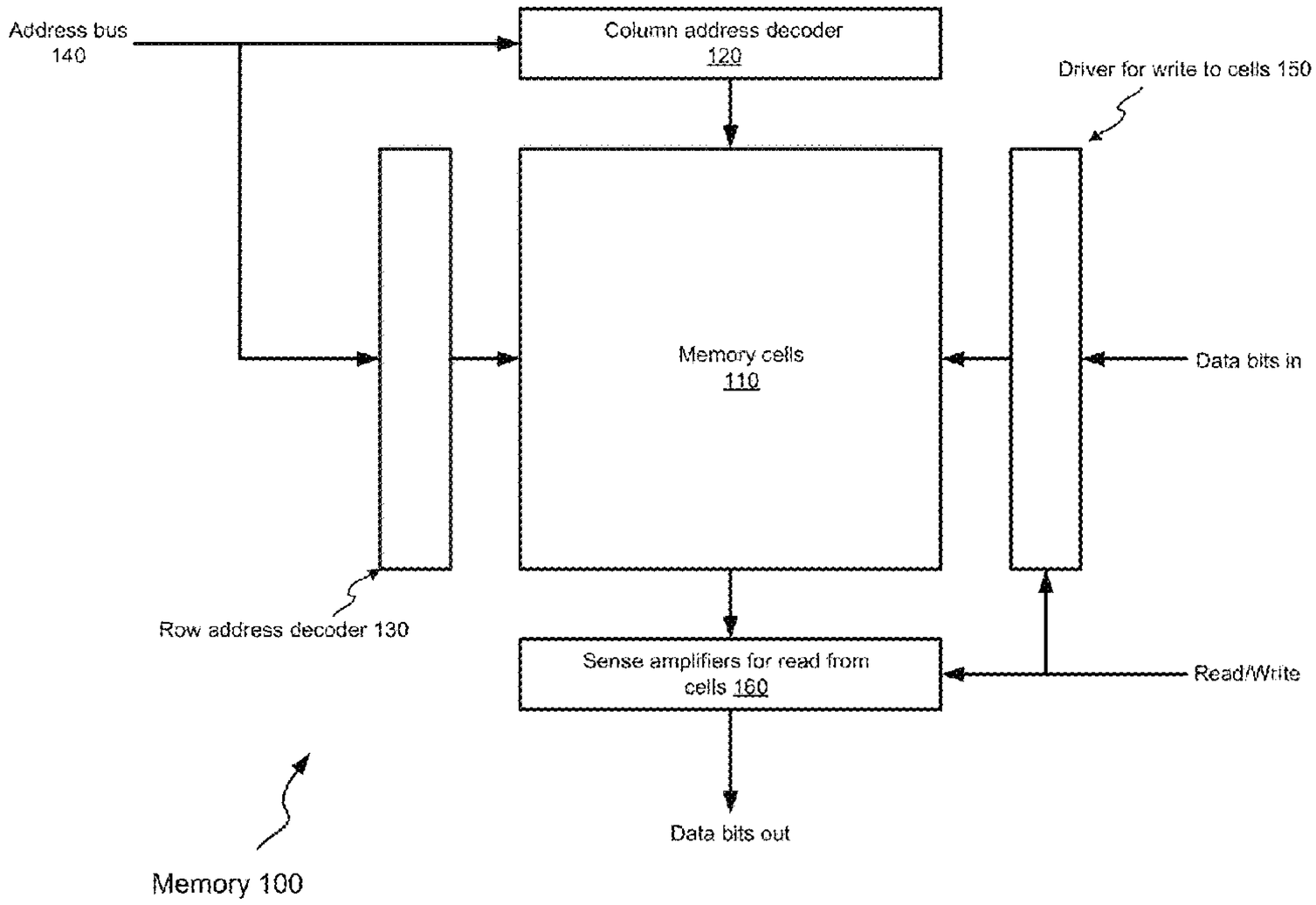
(Continued)

Primary Examiner — Guerrier Merant

(57) **ABSTRACT**

A memory-testing circuit configured to perform a test of a memory comprising error-correcting code circuitry comprises repair circuitry configured to allocate a spare row or row block in the memory for a defective row or row block in the memory, a defective row or row block being a row or row block in which a memory word has a number of error bits greater than a preset number, wherein the test of the memory comprises: disabling the error-correcting code circuitry, performing a pre-repair operation, the pre-repair operation comprising: determining whether the memory has one or more defective rows or row blocks, and allocating one or more spare rows or row blocks for the one or more defective rows or row blocks if the one or more spare rows or row blocks are available, and performing a post-repair operation on the repaired memory.

18 Claims, 10 Drawing Sheets



US011495315B1

(12) **United States Patent**
Zou et al.

(10) **Patent No.: US 11,495,315 B1**
(45) **Date of Patent: Nov. 8, 2022**

(54) **CONFIGURABLE BUILT-IN SELF-REPAIR CHAIN FOR FAST REPAIR DATA LOADING**

(71) Applicant: **Siemens Industry Software Inc.**, Plano, TX (US)

(72) Inventors: **Wei Zou**, Lake Oswego, OR (US); **Benoit Nadeau-Dostie**, Gatineau (CA)

(73) Assignee: **Siemens Industry Software Inc.**, Plano, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/399,104**

(22) Filed: **Aug. 11, 2021**

(51) **Int. Cl.**

G11C 29/00	(2006.01)
G11C 29/10	(2006.01)
G11C 29/32	(2006.01)
G11C 29/12	(2006.01)
G11C 29/44	(2006.01)

(52) **U.S. Cl.**
CPC ***G11C 29/10*** (2013.01); ***G11C 29/12015*** (2013.01); ***G11C 29/32*** (2013.01); ***G11C 29/4401*** (2013.01); ***G11C 29/789*** (2013.01)

(58) **Field of Classification Search**
CPC ... G11C 29/10; G11C 29/12015; G11C 29/32; G11C 29/4401; G11C 29/789
See application file for complete search history.

(56) **References Cited**

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Primary Examiner — Christine T. Tu

(57) **ABSTRACT**

A scan network configured to transport repair information between memories and a controller for a non-volatile storage device comprises: repair registers coupled in parallel to repair information generation circuitry for one of the memories and segment selection devices that divide the repair registers into repair register segments. Each of the segment selection devices comprises: a storage element configured to store a segment selection bit and segment selection bit generation circuitry configured to generate the segment selection bit based on the repair information. Each of the segment selection devices is configurable to include or not include the corresponding repair register segment in a scan path of the scan network in a shift operation based on the segment selection bit.

24 Claims, 14 Drawing Sheets

US011789487B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 11,789,487 B2**
(45) **Date of Patent: Oct. 17, 2023**

(54) **ASYNCHRONOUS INTERFACE FOR TRANSPORTING TEST-RELATED DATA VIA SERIAL CHANNELS**

(71) Applicant: **Siemens Industry Software Inc.**, Plando, TX (US)

(72) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Davie, FL (US)

(73) Assignee: **Siemens Industry Software Inc.**, Plano, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 67 days.

(21) Appl. No.: **17/498,085**

(22) Filed: **Oct. 11, 2021**

(65) **Prior Publication Data**

US 2023/0110161 A1 Apr. 13, 2023

(51) **Int. Cl.**
G06F 1/12 (2006.01)
G06F 1/06 (2006.01)

(52) **U.S. Cl.**
CPC . ***G06F 1/12*** (2013.01); ***G06F 1/06*** (2013.01)

(58) **Field of Classification Search**
CPC G06F 1/10; G06F 1/12
See application file for complete search history.

(56) **References Cited**

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2002/0147951	A1 *	10/2002	Nadeau-Dostie	G01R 31/318552 714/731
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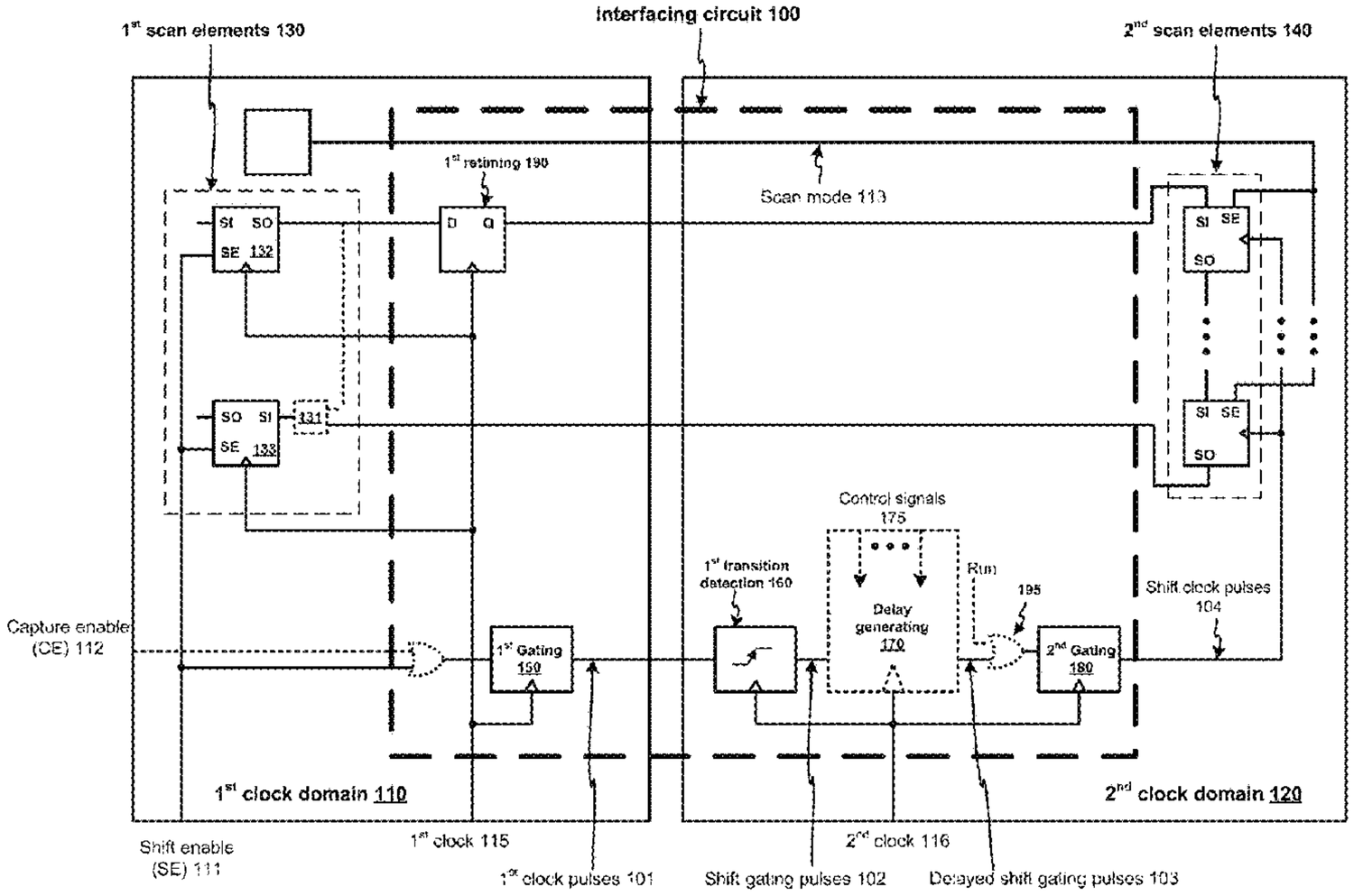
* cited by examiner

Primary Examiner — Phil K Nguyen

(57) **ABSTRACT**

A circuit comprises: a first clock gating device clocked by a first clock signal and configured to generate first clock pulses when a shift enable signal is active, a first transition detecting device clocked by a second clock signal and configured to generate shift gating pulses when detecting active transitions of the first clock pulses, a second clock gating device clocked by the second clock signal and configured to generate shift clock pulses based on the shift gating pulses to clock second scan elements for a shift operation with first scan elements clocked by the first clock signal, and a first retiming device triggered by active pulse edges of the first clock signal and configurable to hold a value for the shift operation. The circuit may further comprise a delay generating device configured to generate delayed shift gating pulses for generating the shift clock pulses.

16 Claims, 14 Drawing Sheets



US011929136B2

(12) **United States Patent**
Yun et al.

(10) **Patent No.: US 11,929,136 B2**
(45) **Date of Patent: Mar. 12, 2024**

(54) **REFERENCE BITS TEST AND REPAIR USING MEMORY BUILT-IN SELF-TEST**

(71) Applicant: **Siemens Industry Software Inc.**, Plano, FL (US)

(72) Inventors: **Jongsin Yun**, Portland, OR (US); **Benoit Nadeau-Dostie**, Gatineau (CA); **Harshitha Kodali**, Wilsonville, OR (US)

(73) Assignee: **Siemens Industry Software Inc.**, Plano, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/906,303**

(22) PCT Filed: **Mar. 18, 2021**

(86) PCT No.: **PCT/US2021/022871**
§ 371 (c)(1),
(2) Date: **Sep. 14, 2022**

(87) PCT Pub. No.: **WO2021/194827**
PCT Pub. Date: **Sep. 30, 2021**

(65) **Prior Publication Data**

US 2023/0178172 A1 Jun. 8, 2023

Related U.S. Application Data

(60) Provisional application No. 63/000,517, filed on Mar. 27, 2020.

(51) **Int. Cl.**
G11C 29/54 (2006.01)
G11C 29/56 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 29/54*** (2013.01); ***G11C 29/56004*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

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2004/0032759 A1 2/2004 Chow et al.
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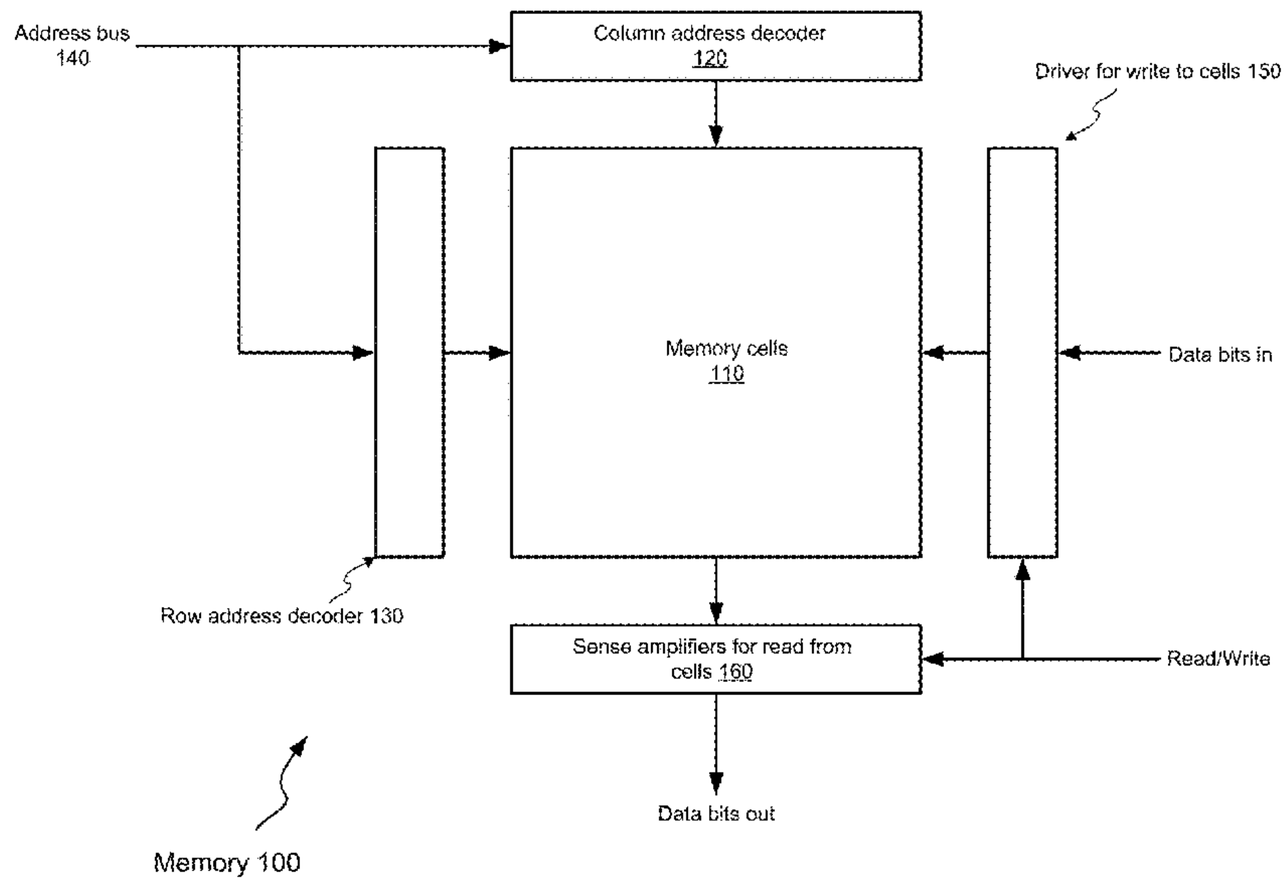
PCT International Search Report and Written Opinion of International Searching Authority dated Jul. 6, 2021 corresponding to PCT International Application No. PCT/US2021/022871 filed Mar. 18, 2021.
(Continued)

Primary Examiner — Guerrier Merant

(57) **ABSTRACT**

A memory-testing circuit configured to perform a test of reference bits in a memory. In a read operation, outputs of data bit columns are compared with one or more reference bit columns. The memory-testing circuit comprises: a test controller and association adjustment circuitry configurable by the test controller to associate another one or more reference bit columns or one or more data bit columns with the data bit columns in the read operation. The test controller can determine whether the original one or more reference bit columns have a defect based on results from the two different association.

10 Claims, 10 Drawing Sheets



US011961576B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 11,961,576 B2**
(45) **Date of Patent: Apr. 16, 2024**

(54) **METHOD AND APPARATUS FOR PROCESSING MEMORY REPAIR INFORMATION**

(71) Applicant: **Siemens Industry Software Inc**, Plano, TX (US)

(72) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Luc Romain**, Gatineau (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 228 days.

(21) Appl. No.: **17/604,805**

(22) PCT Filed: **Aug. 27, 2019**

(86) PCT No.: **PCT/US2019/048223**
§ 371 (c)(1),
(2) Date: **Oct. 19, 2021**

(87) PCT Pub. No.: **WO2020/214195**
PCT Pub. Date: **Oct. 22, 2020**

(65) **Prior Publication Data**

US 2022/0215896 A1 Jul. 7, 2022

Related U.S. Application Data

(60) Provisional application No. 62/836,100, filed on Apr. 19, 2019.

(51) **Int. Cl.**
G11C 29/00 (2006.01)
G11C 29/36 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G11C 29/4401*** (2013.01); ***G11C 29/36*** (2013.01); ***G11C 29/40*** (2013.01); *G11C 2029/3602* (2013.01)

(58) **Field of Classification Search**
CPC G11C 29/4401; G11C 29/36; G11C 29/40; G11C 2029/3602
See application file for complete search history.

(56) **References Cited**

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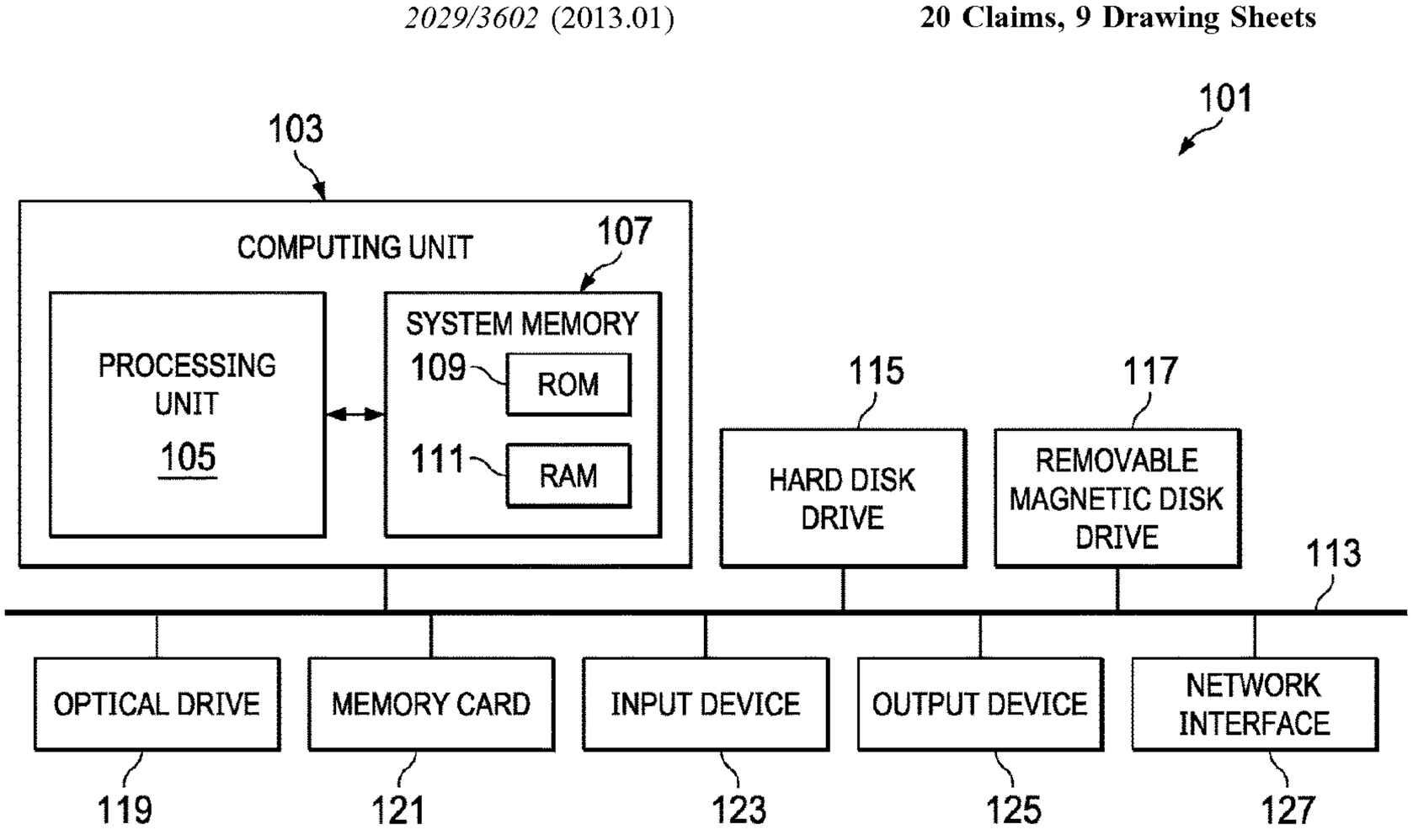
PCT International Search Report and Written Opinion of International Searching Authority dated Dec. 6, 2019 corresponding to PCT International Application No. PCT/US2019/048223 filed Aug. 27, 2019.
(Continued)

Primary Examiner — Min Huang

(57) **ABSTRACT**

Systems and methods for repairing a memory. A method includes performing a repair analysis of the embedded memories to produce repair information. The method includes storing the repair information in the registers, where the registers are organized into groups having chains of identical length. The method includes performing collision detection between the repair information in each of the groups. The method includes merging the repair information in each of the groups. The method includes repairing the embedded memories using the merged repair information.

20 Claims, 9 Drawing Sheets



US012046315B2

(12) **United States Patent**
Yun et al.

(10) **Patent No.: US 12,046,315 B2**
(45) **Date of Patent: Jul. 23, 2024**

(54) **MEMORY BUILT-IN SELF-TEST WITH AUTOMATED REFERENCE TRIM FEEDBACK FOR MEMORY SENSING**

(71) Applicant: **Siemens Industry Software Inc.**, Plano, TX (US)

(72) Inventors: **Jongsin Yun**, Portland, OR (US); **Benoit Nadeau-Dostie**, Gatineau (CA); **Martin Keim**, Sherwood, OR (US)

(73) Assignee: **Siemens Industry Software Inc.**, Plano, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/756,963**

(22) PCT Filed: **May 28, 2020**

(86) PCT No.: **PCT/US2020/034860**
§ 371 (c)(1),
(2) Date: **Jun. 7, 2022**

(87) PCT Pub. No.: **WO2021/118634**
PCT Pub. Date: **Jun. 17, 2021**

(65) **Prior Publication Data**

US 2024/0013846 A1 Jan. 11, 2024

Related U.S. Application Data

(60) Provisional application No. 62/945,335, filed on Dec. 9, 2019.

(51) **Int. Cl.**
G11C 29/14 (2006.01)
G11C 29/12 (2006.01)
G11C 29/46 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 29/14*** (2013.01); ***G11C 29/1201*** (2013.01); ***G11C 29/46*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

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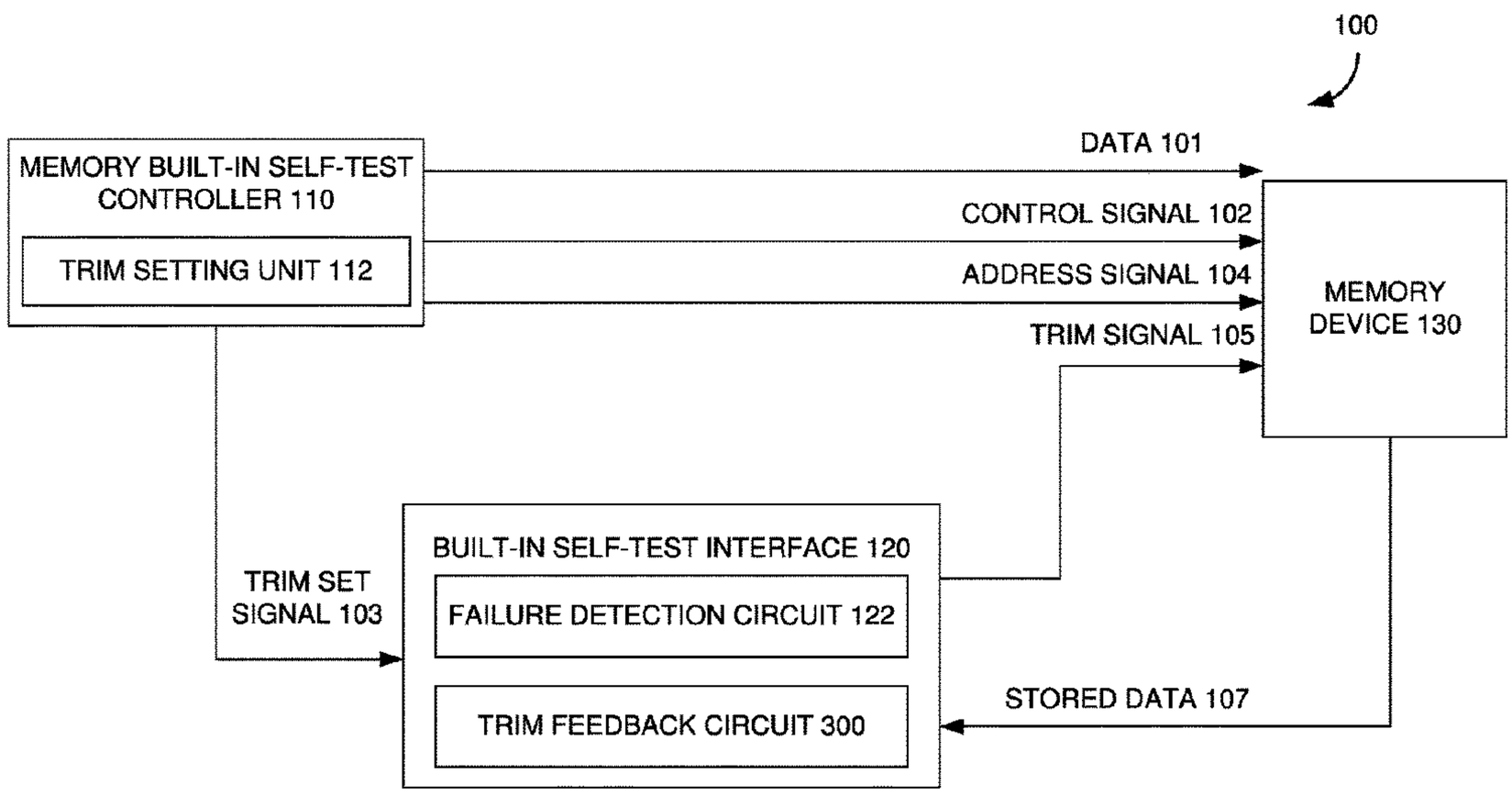
PCT International Search Report and Written Opinion of International Searching Authority mailed Oct. 5, 2020 corresponding to PCT International Application No. PCT/US2020/034860 filed May 28, 2020.

Primary Examiner — Tan T. Nguyen

(57) **ABSTRACT**

This application discloses a memory built-in self-test system to prompt a memory device to sense values of stored data using a reference trim during memory read operations. The memory built-in self-test system can automatically set the reference trim for the memory device. The memory built-in self-test system includes a memory built-in self-test controller to prompt the memory device to perform the memory read operations with different test values for the reference trim. The memory built-in self-test system also includes a trim feedback circuit to determine when the memory device fails to correctly sense the values of the stored data using the test values for the reference trim, and set the reference trim for the memory device based, at least in part, on the failures of the memory device to correctly sense the stored data.

11 Claims, 7 Drawing Sheets



US 20020143515A1

(19) **United States**

(12) **Patent Application Publication**

Nadeau-Dostie et al.

(10) **Pub. No.: US 2002/0143515 A1**

(43) **Pub. Date: Oct. 3, 2002**

(54) **METHOD AND PROGRAM PRODUCT FOR MODELING CIRCUITS WITH LATCH BASED DESIGN**

(76) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Fadi Maamari**, San Jose, CA (US); **Dwayne Burek**, San Jose, CA (US)

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Manager, Intellectual Property
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1525 Carling Avenue, Suite 404
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(21) Appl. No.: **09/817,298**

(22) Filed: **Mar. 27, 2001**

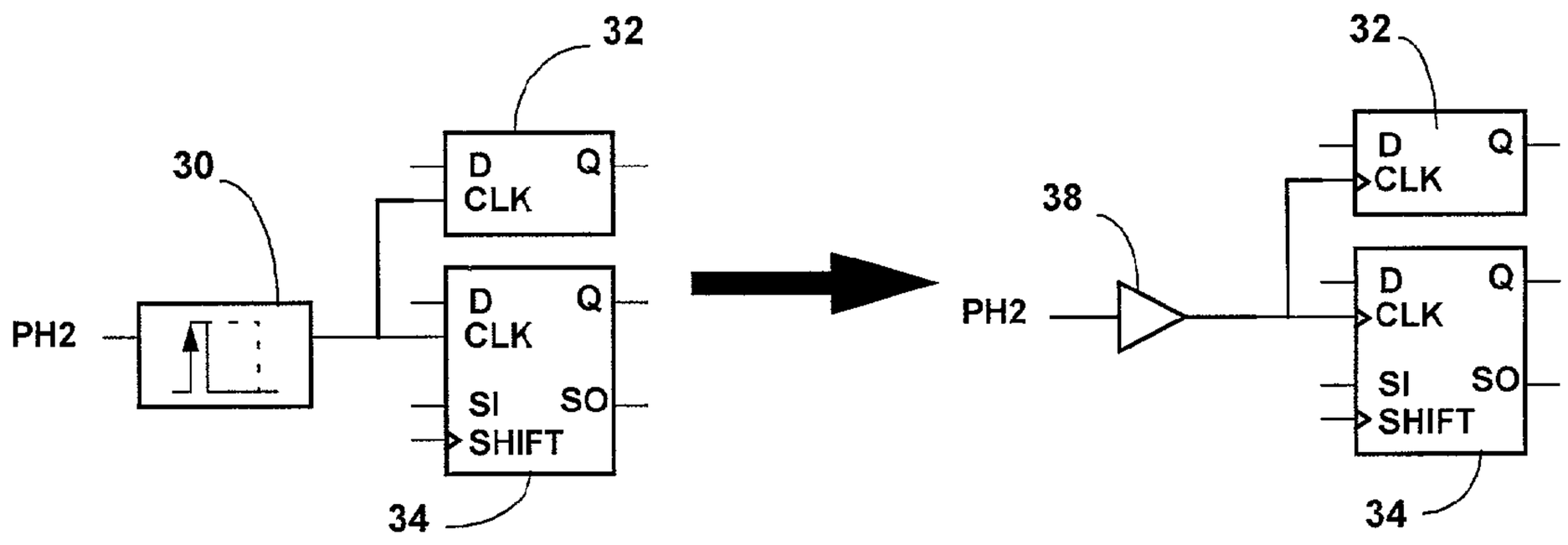
Publication Classification

(51) **Int. Cl.**[7] **G06F 9/45**

(52) **U.S. Cl.** **703/19**

(57) **ABSTRACT**

A method of and computer program product for modeling a logic circuit having combinational logic and latches, in which the latches are clocked by one of a first clock phase, a second clock phase or a pulse derived from the second clock phase, a subset of latches being scannable, comprises, for each latch in the logic circuit, associating the latch with one of the first and second clock phase; and when latch is associated with the first clock phase, modeling the latch as a buffer connected between the data input and output of latch; and when the latch is associated with the second clock phase, modeling the latch as an edge-triggered flip-flop having the same data input, data output and clock input as the latch.



US 20020147951A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2002/0147951 A1**

(43) **Pub. Date: Oct. 10, 2002**

Nadeau-Dostie et al.

(54) **METHOD FOR SCAN TESTING OF DIGITAL CIRCUIT, DIGITAL CIRCUIT FOR USE THEREWITH AND PROGRAM PRODUCT FOR INCORPORATING TEST METHODOLOGY INTO CIRCUIT DESCRIPTION**

(76) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-Francois Cote**, Chelsea (CA)

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(21) Appl. No.: **09/773,541**

(22) Filed: **Feb. 2, 2001**

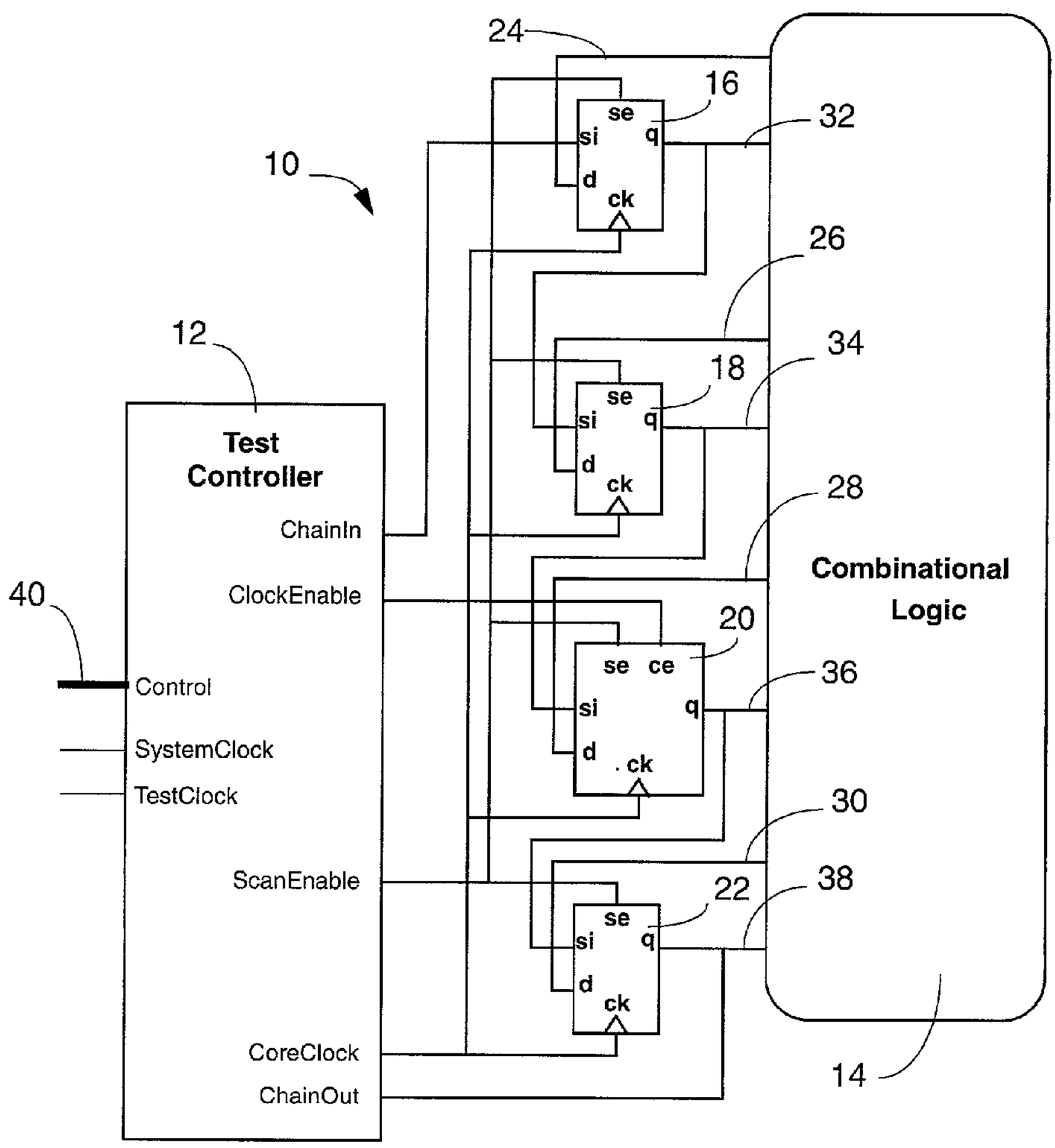
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**; G06F 1/04

(52) **U.S. Cl.** **714/731**; 713/500

(57) **ABSTRACT**

A method for at-speed scan testing of circuits having scannable memory elements which source multi-cycle paths having propagation delays that are longer than the period of a system clock used during normal operation comprises loading a test stimulus into the scannable memory elements; performing a capture operation, including configuring in capture mode throughout the capture operation, non-source memory elements and multi-cycle path source memory elements which have a predetermined maximum capture clock rate which is the same as or higher than the clock rate of the capture clock; and configuring in a hold mode during all but the last cycle of the capture operation and in capture mode for the last cycle, source memory elements which have a predetermined maximum capture clock rate which is lower than the clock rate of the capture clock; applying at least two clock cycles of the capture clock; and unloading test response data captured by said scannable memory elements.



US 20020184562A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2002/0184562 A1**

(43) **Pub. Date: Dec. 5, 2002**

Nadeau-Dostie et al.

(54) **METHOD OF DESIGNING CIRCUIT HAVING MULTIPLE TEST ACCESS PORTS, CIRCUIT PRODUCED THEREBY AND METHOD OF USING SAME**

(76) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-Francois Cote**, Chelsea (CA)

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OTTAWA, ON K1Z 8R9 (CA)

(21) Appl. No.: **09/843,307**

(22) Filed: **Apr. 27, 2001**

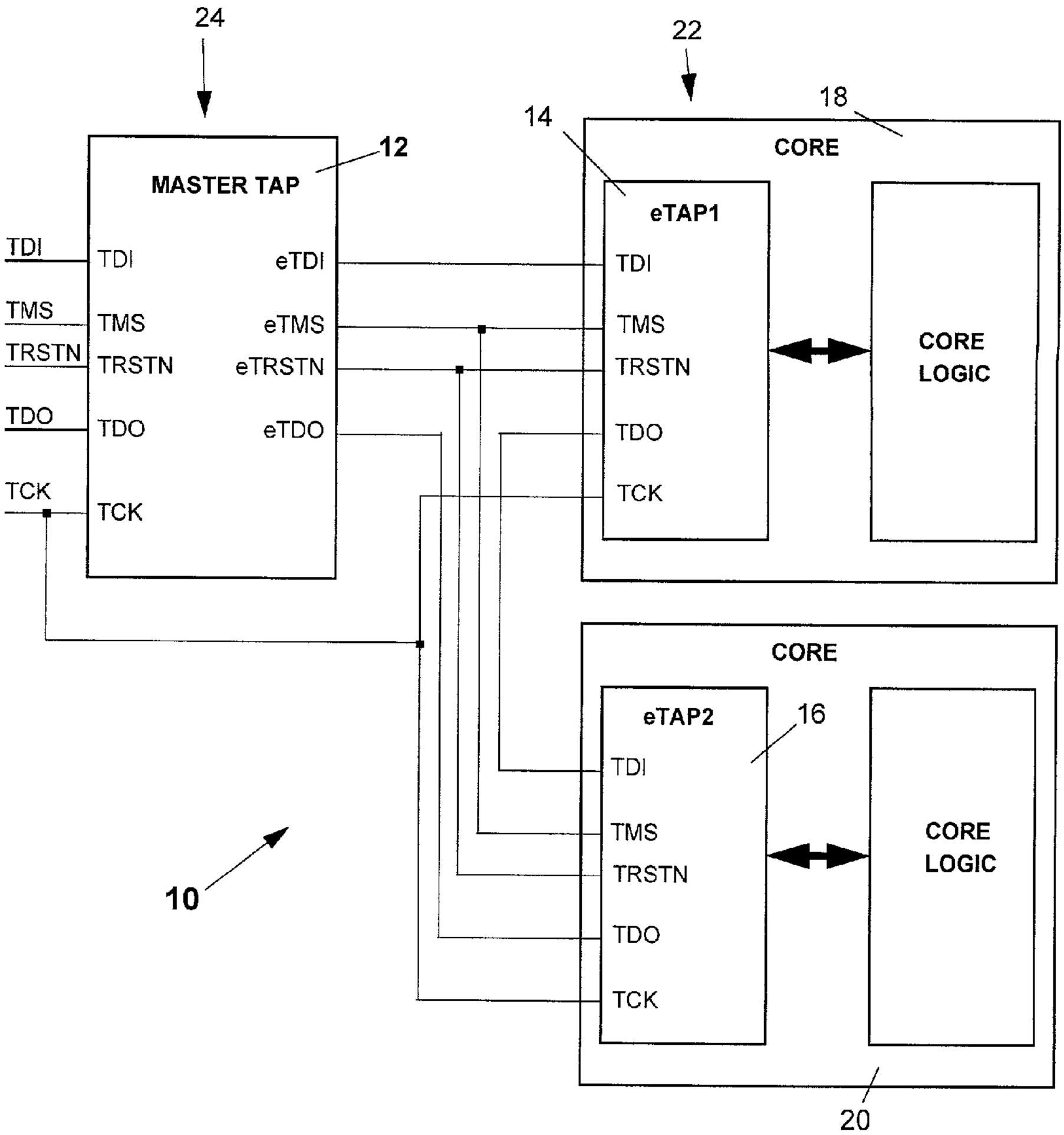
Publication Classification

(51) **Int. Cl.**[7] **H02H 3/05**

(52) **U.S. Cl.** **714/30**

(57) **ABSTRACT**

In a circuit with multiple Test Access Port (TAP) interfaces, the TAPs are arranged into groups, with secondary TAPs in one or more groups and a master TAP in another group, the master TAP having an instruction register with bits for storing a group selection code; a Test Data Output (TDO) circuit responsive to the group selection code connects the group TDO of one of the groups to the circuit TDO; and, for each secondary TAP group, a group Test Data Input (TDI) circuit responsive to a shift state signal for selectively connecting the group TDI to the circuit TDI or to the output of a padding register having its input connected to the circuit TDI, and its output connected to an input of the group TDI circuit; and a group TMS circuit responsive to a predetermined TAP selection code associated with the group for producing a group TMS signal for each TAP in the group.



US 20030110457A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2003/0110457 A1**

(43) **Pub. Date: Jun. 12, 2003**

Nadeau-Dostie et al.

(54) **METHOD AND PROGRAM PRODUCT FOR DESIGNING HIERARCHICAL CIRCUIT FOR QUIESCENT CURRENT TESTING AND CIRCUIT PRODUCED THEREBY**

(76) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-Francois Cote**, Chelsea (CA)

Correspondence Address:
LOGICVISION (CANADA), INC.
1525 CARLING AVENUE, SUITE 404
OTTAWA, ON K1Z 8R9 (CA)

(21) Appl. No.: **10/011,128**

(22) Filed: **Dec. 10, 2001**

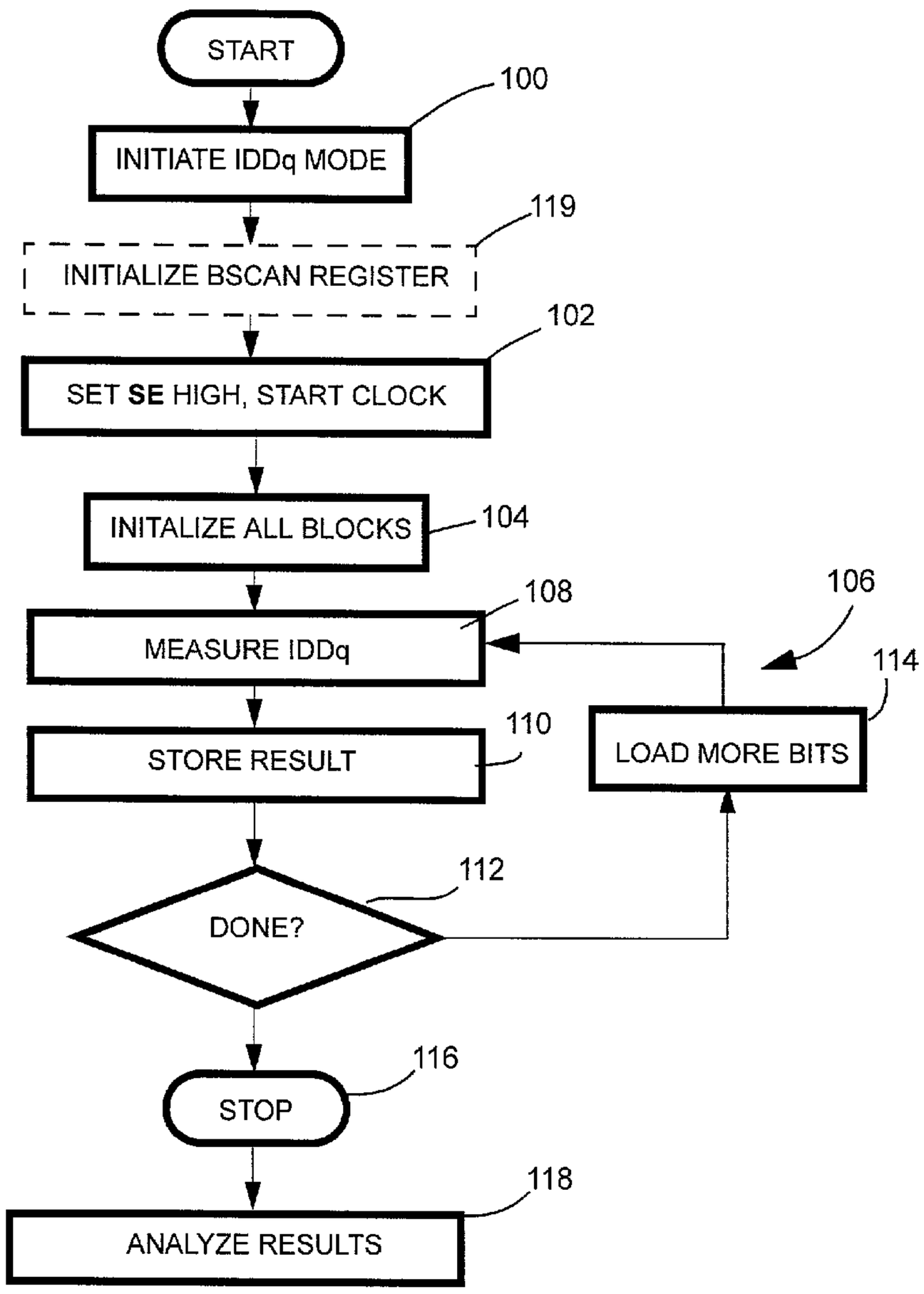
Publication Classification

(51) **Int. Cl.**[7] **G06F 17/50**

(52) **U.S. Cl.** **716/4**

(57) **ABSTRACT**

A method of designing integrated circuits having an hierarchical structure for quiescent current testing, and the circuit which results therefrom is disclosed. The method comprises analyzing each of one or more selected hierarchical blocks independently of other selected blocks identify any circuit states of each block which could result in elevated quiescent current levels during quiescent current testing of the circuit, the analysis beginning with blocks at a lowest level of hierarchy and proceeding in sequence through each level of design hierarchy to a highest level of hierarchy containing a top-level block; and calculating a fault coverage for each selected block.



US 20030115522A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2003/0115522 A1**

(43) **Pub. Date: Jun. 19, 2003**

Nadeau-Dostie et al.

(54) **METHOD AND PROGRAM PRODUCT FOR DESIGNING HIERARCHICAL CIRCUIT FOR QUIESCENT CURRENT TESTING**

(76) Inventors: **Benoit Nadeau-Dostie**, Quebec (CA); **Dwayne Burek**, San Jose, CA (US)

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(21) Appl. No.: **10/015,751**

(22) Filed: **Dec. 17, 2001**

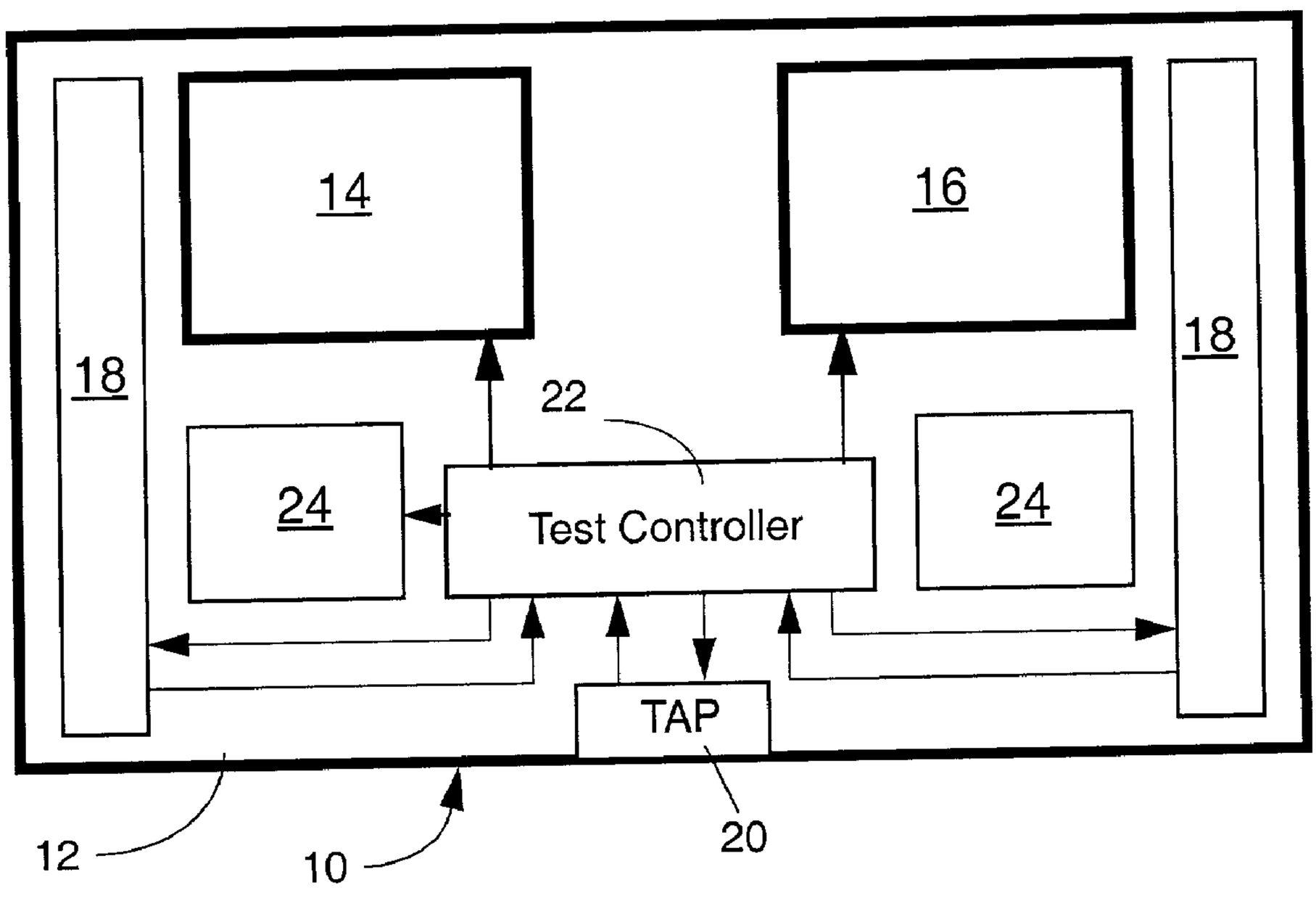
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/726**

(57) **ABSTRACT**

A method of designing a circuit having at least one hierarchical block which requires block specific test patterns to facilitate quiescent current testing of the circuit, comprises, for each block, configuring the block and any embedded blocks located one level down in design hierarchy in quiescent current test mode in which input and output peripheral memory elements are configured in internal test mode and in external test mode, respectively; generating quiescent current test patterns which do not result in elevated quiescent current levels and which include a bit for all memory elements in the block and for any peripheral memory elements in any embedded blocks located one level down in design hierarchy; and, if the block contains embedded blocks, synchronizing the test pattern with a corresponding test pattern generated for embedded blocks so that test patterns loaded in scan chains in the block are consistent with test patterns loaded in scan chains in said embedded blocks.



US 20030146777A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2003/0146777 A1**

(43) **Pub. Date: Aug. 7, 2003**

Nadeau-Dostie et al.

(54) **METHOD AND CIRCUITRY FOR CONTROLLING CLOCKS OF EMBEDDED BLOCKS DURING LOGIC BIST TEST MODE**

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(21) Appl. No.: **10/125,384**

(22) Filed: **Apr. 19, 2002**

Related U.S. Application Data

(60) Provisional application No. 60/353,951, filed on Feb. 5, 2002.

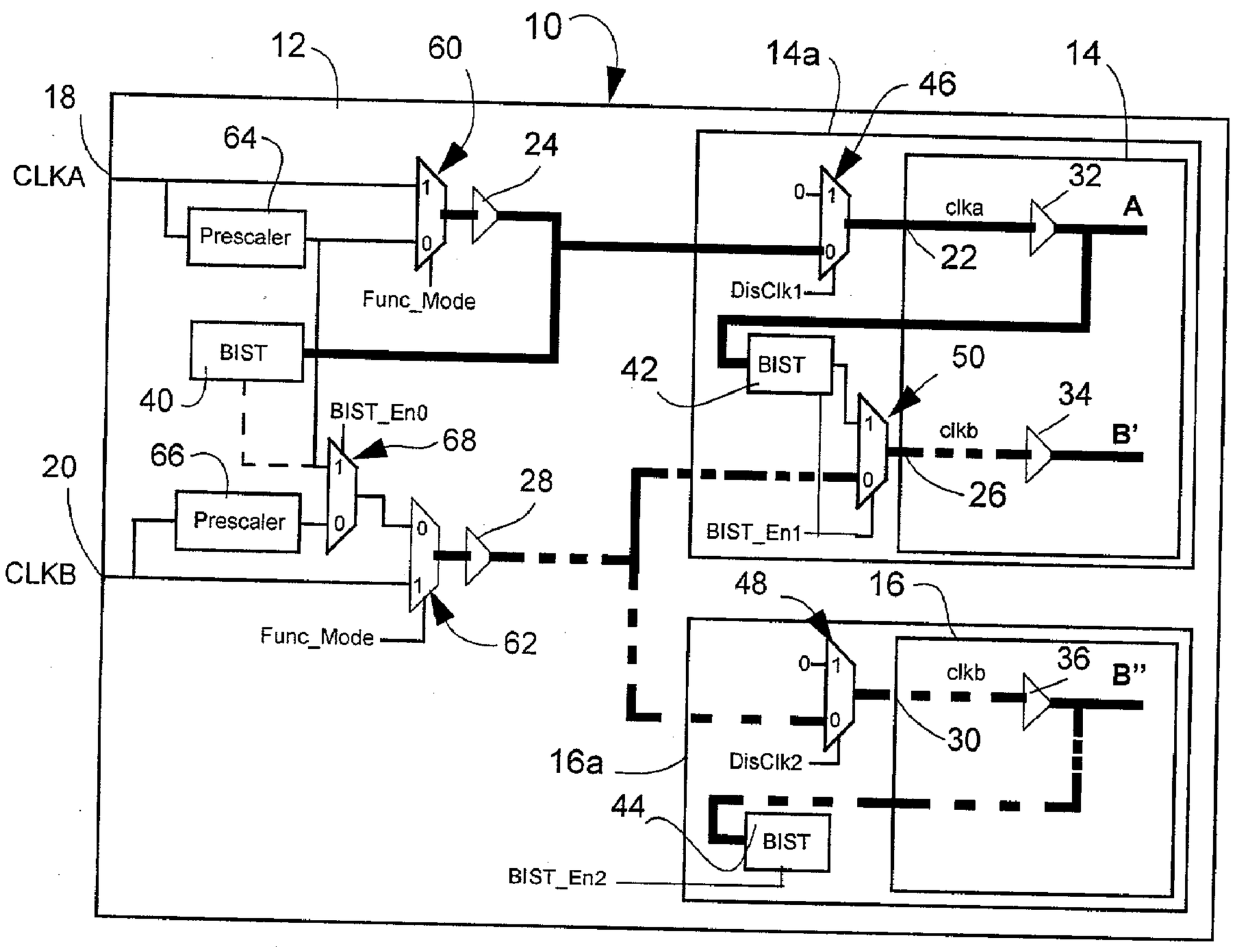
Publication Classification

(51) **Int. Cl.**[7] **H03K 19/00**

(52) **U.S. Cl.** **326/93**

(57) **ABSTRACT**

One aspect of the invention is generally defined as a method of designing an integrated circuit for distributing test clock signals to embedded cores having at least one core functional clock input, the method comprising, for each core, providing a clock gating circuit for selectively disabling a core functional clock signal applied to a core primary clock input; and providing a core clock selection circuit for each secondary core functional clock input for selecting one of a core functional clock signal output by the gating circuit and a core test clock signal and applying a selected signal to the each secondary core functional clock input.



US 20030212524A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2003/0212524 A1**

(43) **Pub. Date: Nov. 13, 2003**

Cote et al.

(54) **TEST ACCESS CIRCUIT AND METHOD OF ACCESSING EMBEDDED TEST CONTROLLERS IN INTEGRATED CIRCUIT MODULES**

(76) Inventors: **Jean-Francois Cote**, Chelsea (CA); **Benoit Nadeau-Dostie**, Aylmer (CA)

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(21) Appl. No.: **10/139,294**

(22) Filed: **May 7, 2002**

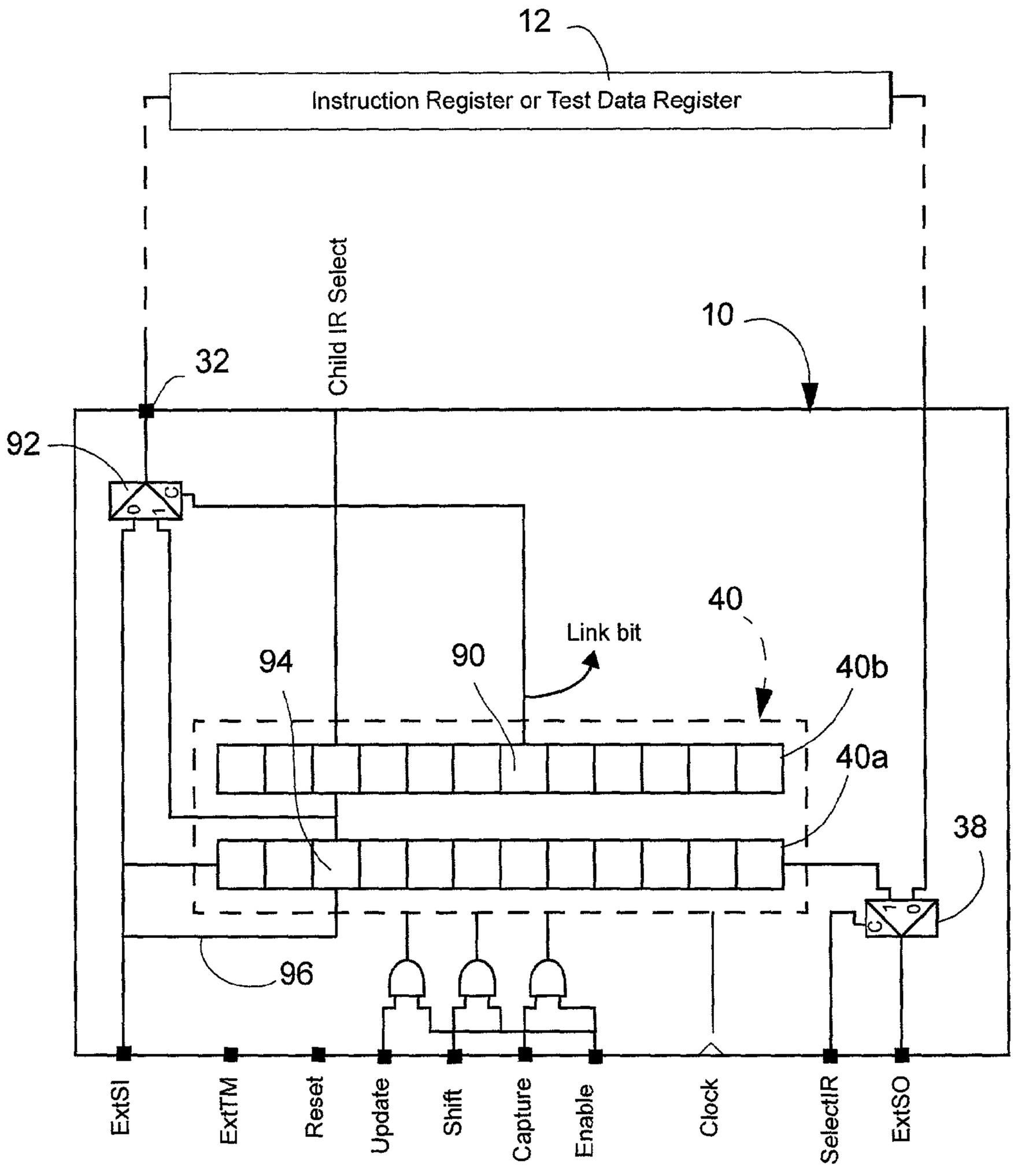
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/14**

(52) **U.S. Cl.** **702/120**

(57) **ABSTRACT**

A test access circuit (TAC) for use in controlling test resources including child test access circuits (TACs) and/or test controllers, in an integrated circuit, comprises an enable input for enabling or disabling access to the test resources, a test port associated with each test resource, each test port including a test port enable output for connection to an enable input of an associated test resource; and an input for receiving a serial output of the associated test resource; and means for selecting a test resource for communication therewith.



US 20030217315A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2003/0217315 A1**

(43) **Pub. Date: Nov. 20, 2003**

Maamari et al.

(54) **METHOD OF AND PROGRAM PRODUCT FOR PERFORMING GATE-LEVEL DIAGNOSIS OF FAILING VECTORS**

(76) Inventors: **Fadi Maamari**, San Jose, CA (US); **Sonny Ngai San Shum**, San Jose, CA (US); **Benoit Nadeau-Dostie**, Aylmer (CA)

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1525 CARLING AVENUE, SUITE 404
OTTAWA, ON K1Z 8R9 (CA)

(21) Appl. No.: **10/435,094**

(22) Filed: **May 12, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/379,732, filed on May 14, 2002.

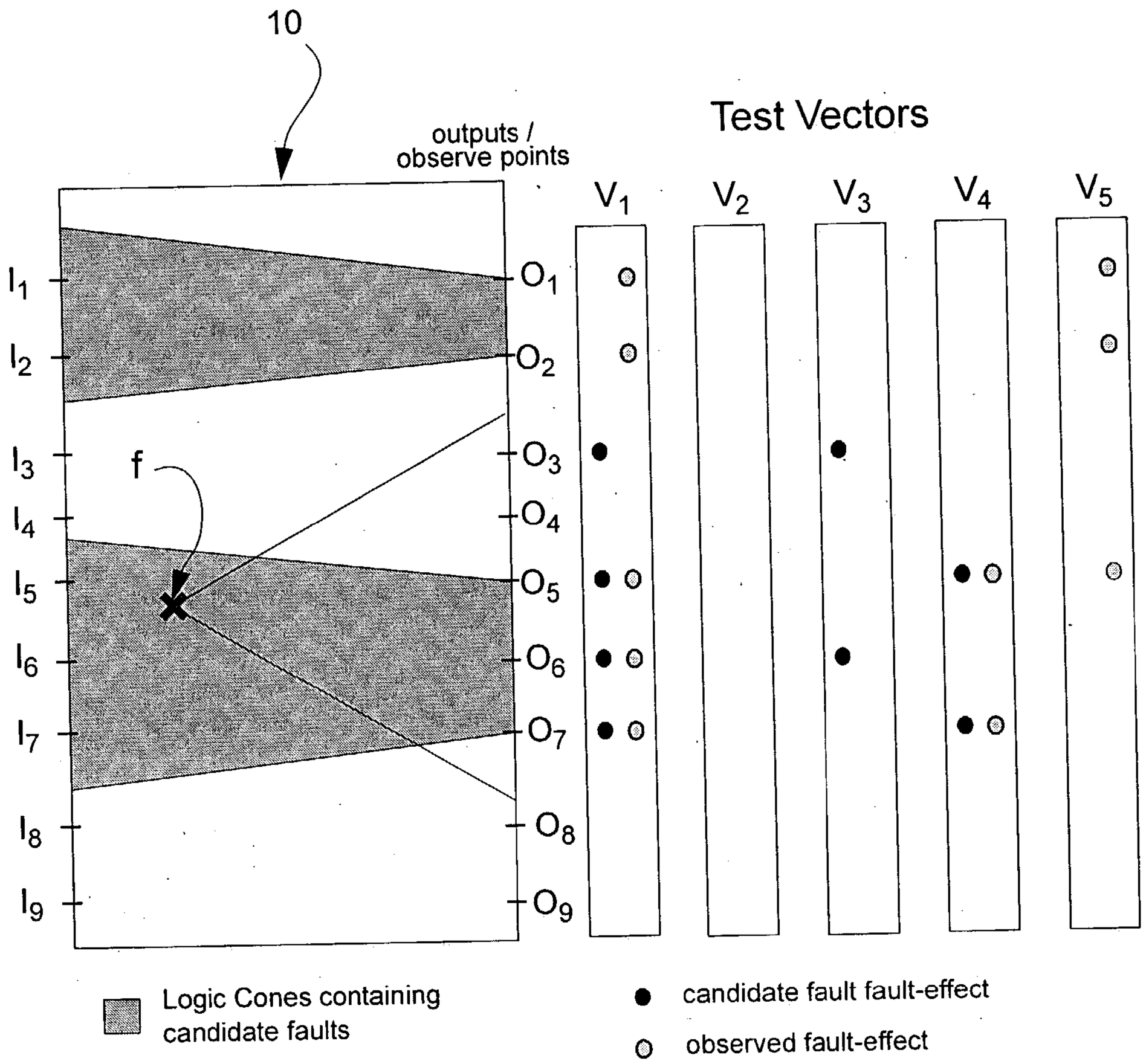
Publication Classification

(51) **Int. Cl.**[7] **G06F 11/00**; G01R 31/28

(52) **U.S. Cl.** **714/741**

(57) **ABSTRACT**

A method of fault diagnosis of integrated circuits having failing test vectors with observed fault effects using fault candidate fault-effects obtained by simulation of a set of test vectors, comprises determining a fault candidate diagnostic measure for each fault candidate, the fault candidate diagnostic measure having a fault candidate match metric, an observed fault effect mismatch metric and a fault candidate excitation metric, ranking fault candidates in decreasing diagnostic measure order; and identifying fault candidate(s) having the highest diagnostic measure as the most likely cause of observed fault effects.



US 20030226073A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2003/0226073 A1**

(43) **Pub. Date: Dec. 4, 2003**

Nadeau-Dostie et al.

(54) **METHOD FOR COLLECTING FAILURE INFORMATION FOR A MEMORY USING AN EMBEDDED TEST CONTROLLER**

(76) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-Francois Cote**, Chelsea (CA)

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(21) Appl. No.: **10/156,117**

(22) Filed: **May 29, 2002**

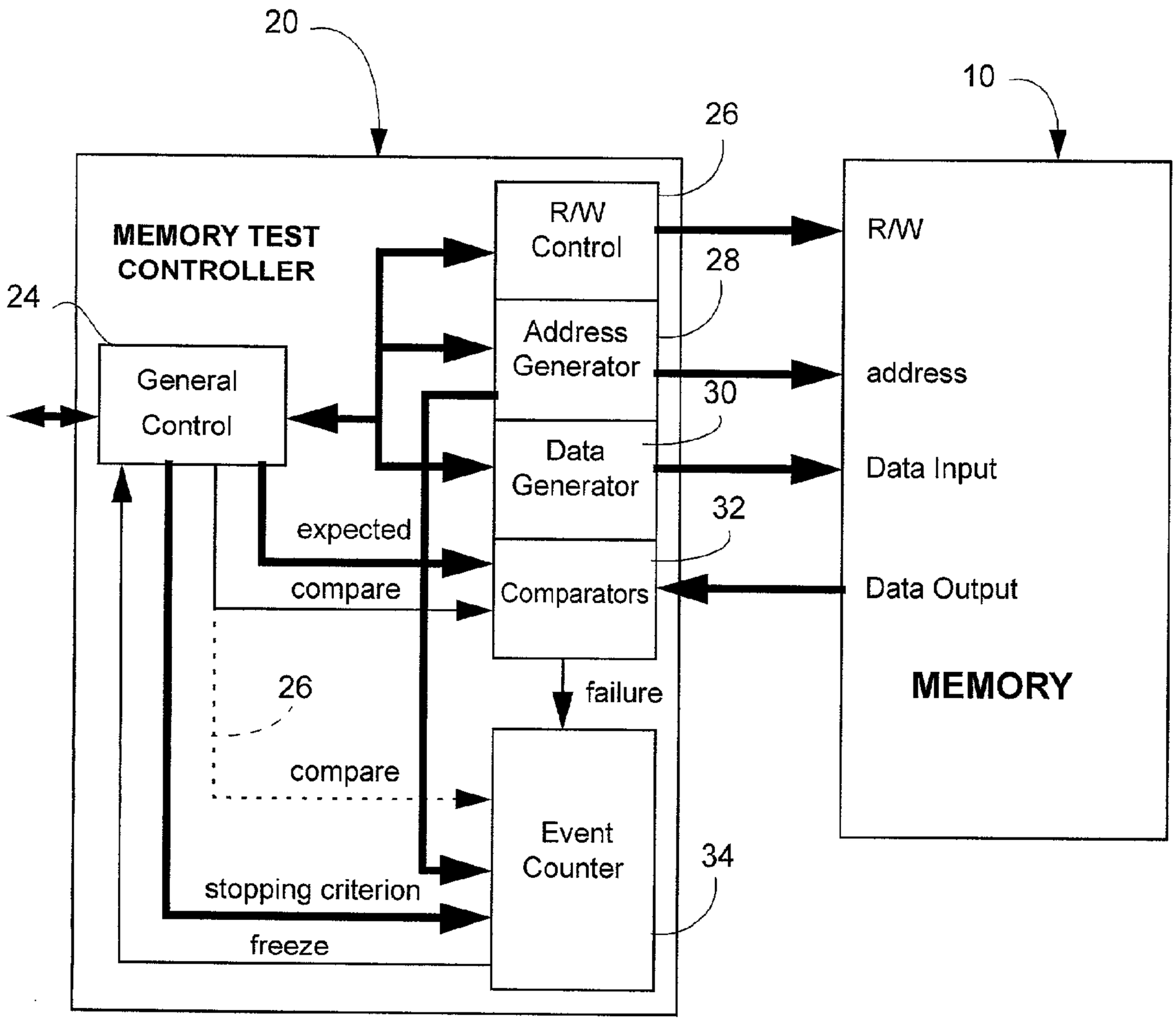
Publication Classification

(51) **Int. Cl.**[7] **G11C 29/00**

(52) **U.S. Cl.** **714/718**

(57) **ABSTRACT**

A method of collecting failure information when testing a memory comprises performing a test of the memory according to a test algorithm, and, while performing the test, counting failure events which occur after a predetermined number of masked events; stopping the test upon occurrence of a stopping criterion which comprises one of occurrence of a first failure event, a change of a test operation; a change of a memory column address; a change of a memory row address; a change of a memory bank address; and a change of a test algorithm phase; and storing failure information.



US 20030229833A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0229833 A1**

Nadeau-Dostie (43) **Pub. Date: Dec. 11, 2003**

(54) **METHOD OF MASKING CORRUPT BITS DURING SIGNATURE ANALYSIS AND CIRCUIT FOR USE THEREWITH**

(76) Inventor: **Benoit Nadeau-Dostie**, Aylmer (CA)

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(21) Appl. No.: **10/162,917**

(22) Filed: **Jun. 6, 2002**

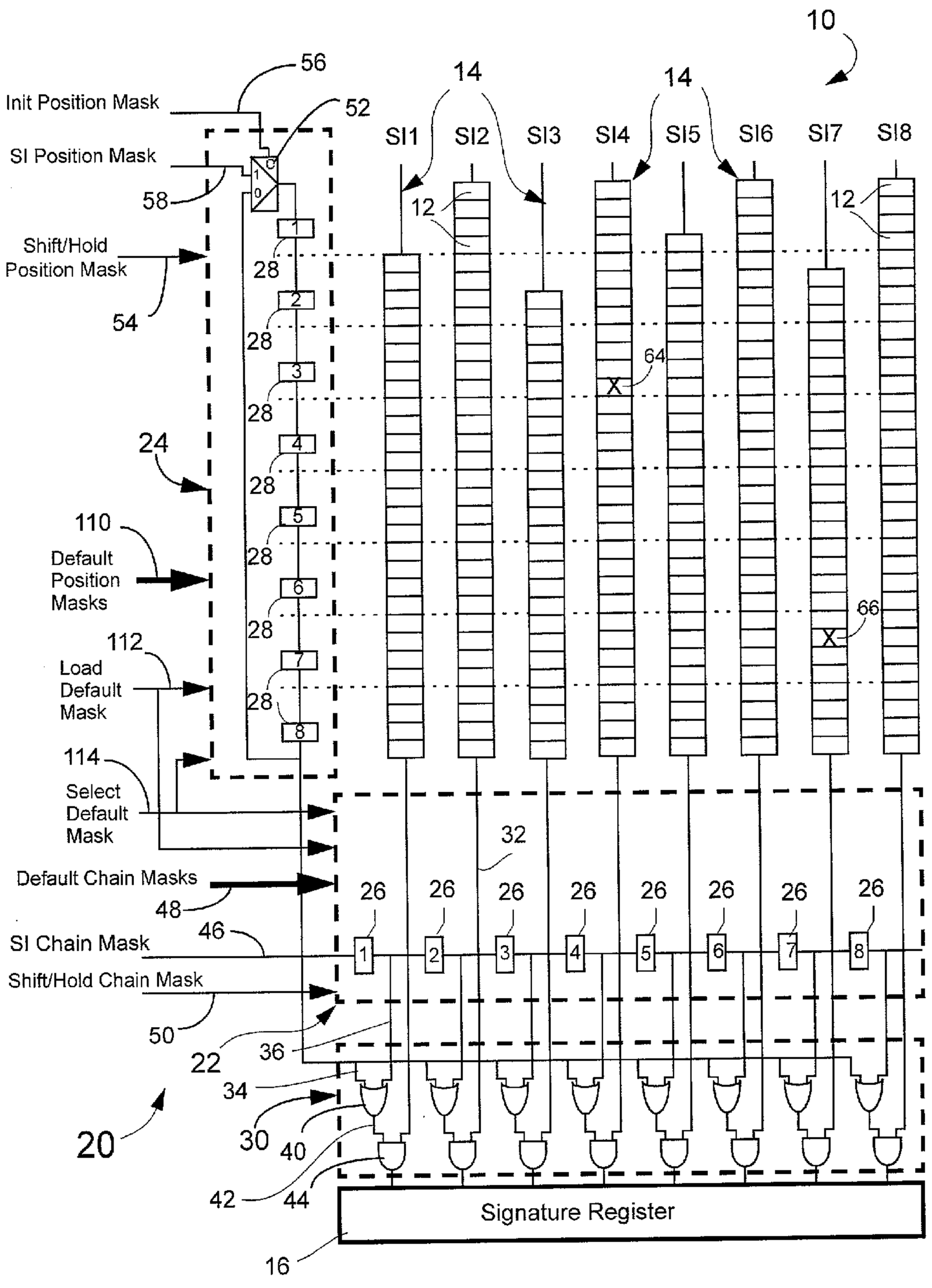
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/726**

(57) **ABSTRACT**

A method of masking corrupt bits in test response pattern scan chains in an integrated circuit, comprising loading and applying a set of test patterns in the scan chains so as to obtain corresponding test response patterns; and masking bits of the test response patterns located in scan chains identified by a chain mask and at a position identified by a position mask.



US 20040003329A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2004/0003329 A1**

(43) **Pub. Date: Jan. 1, 2004**

Cote et al.

(54) **SCAN TEST METHOD FOR PROVIDING REAL TIME IDENTIFICATION OF FAILING TEST PATTERNS AND TEST BIST CONTROLLER FOR USE THEREWITH**

(76) Inventors: **Jean-Francois Cote**, Chelsea (CA); **Benoit Nadeau-Dostie**, Aylmer (CA)

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(21) Appl. No.: **10/180,116**

(22) Filed: **Jun. 27, 2002**

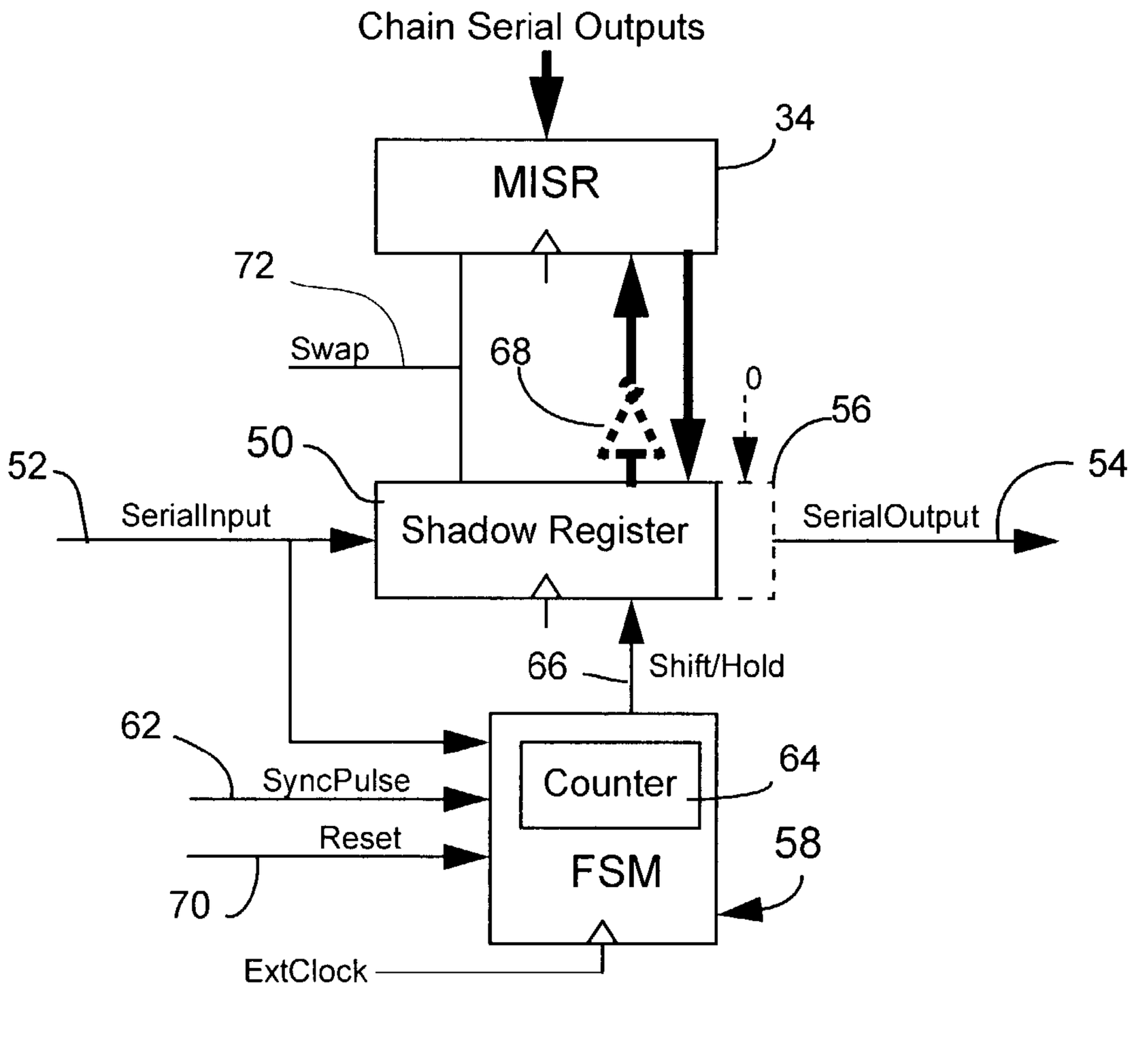
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/726**

(57) **ABSTRACT**

A method of scan testing an integrated circuit to provide real time identification of a block of test patterns having at least one failing test pattern comprises performing a number of test operations and storing a test response signature corresponding to each block of test patterns into a signature register; replacing the test response signature in the signature register with a test block expected signature; identifying the block as a failing test block when the test response signature is different from the test block expected signature; and repeating preceding steps until the test is complete.



US 20040098648A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2004/0098648 A1**

(43) **Pub. Date: May 20, 2004**

Sunter et al.

(54) **BOUNDARY SCAN WITH STROBED PAD DRIVER ENABLE**

(76) Inventors: **Stephen K. Sunter**, Nepean (CA); **Pierre Gauthier**, Gatineau (CA); **Benoit Nadeau-Dostie**, Gatineau (CA)

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(21) Appl. No.: **10/701,479**

(22) Filed: **Nov. 6, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/425,994, filed on Nov. 14, 2002.

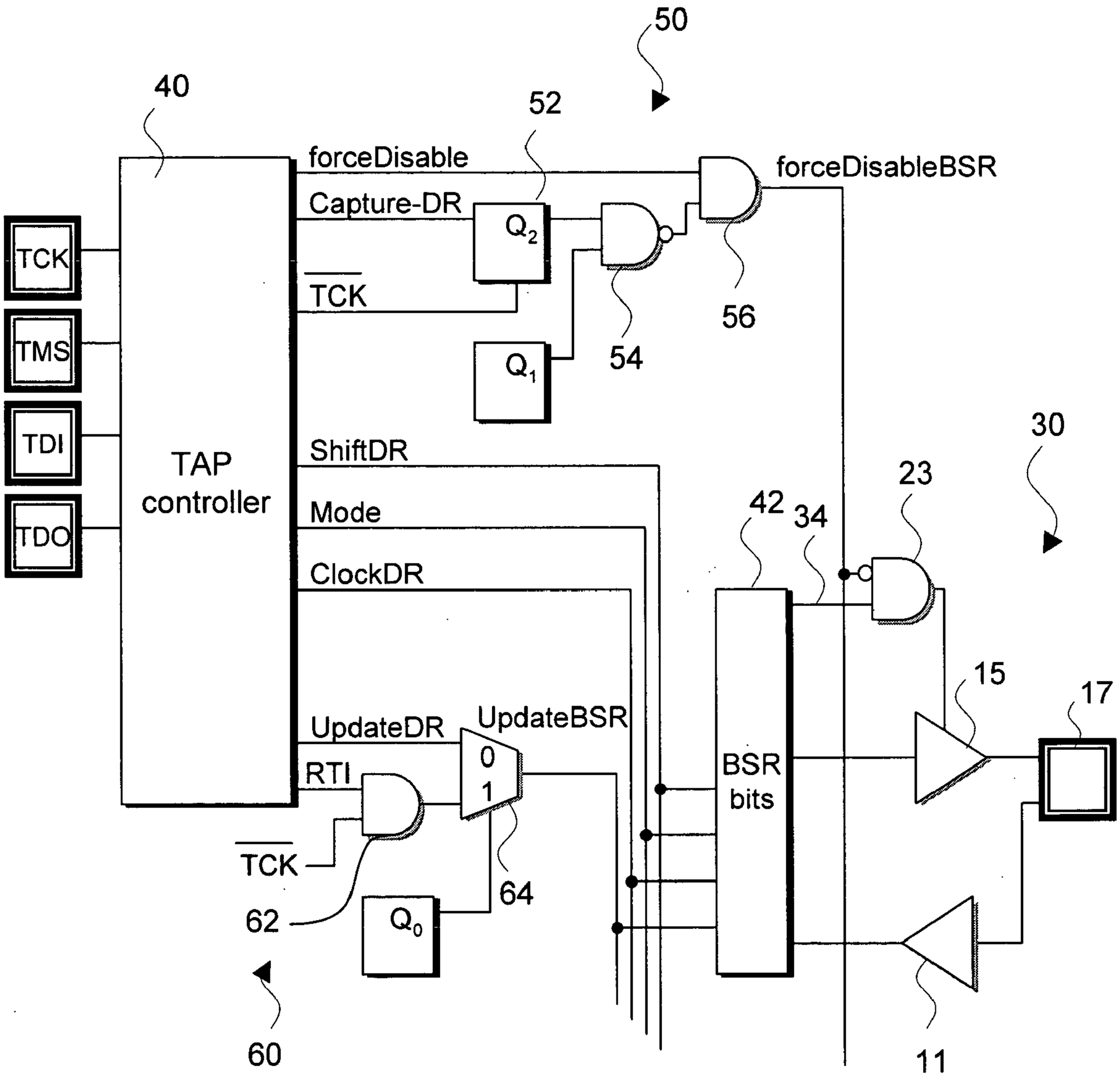
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/727**

(57) **ABSTRACT**

A circuit and a method are provided for testing the enable function of Boundary Scan Register bits that control the driver of unconnected I/O pins of an 1149.1-compliant IC during the IC's reduced pin-count access manufacturing test, and to test the connections to these pins during the test of a circuit board containing the IC, without causing excessive current if a pin is inadvertently short circuited.



US 20040123203A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2004/0123203 A1**

(43) **Pub. Date: Jun. 24, 2004**

Nadeau-Dostie et al.

(54) **METHOD AND TEST CIRCUIT FOR TESTING MEMORY INTERNAL WRITE ENABLE**

(76) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Saman M. I. Adham**, Kanata (CA)

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(21) Appl. No.: **10/638,388**

(22) Filed: **Aug. 12, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/433,987, filed on Dec. 18, 2002.

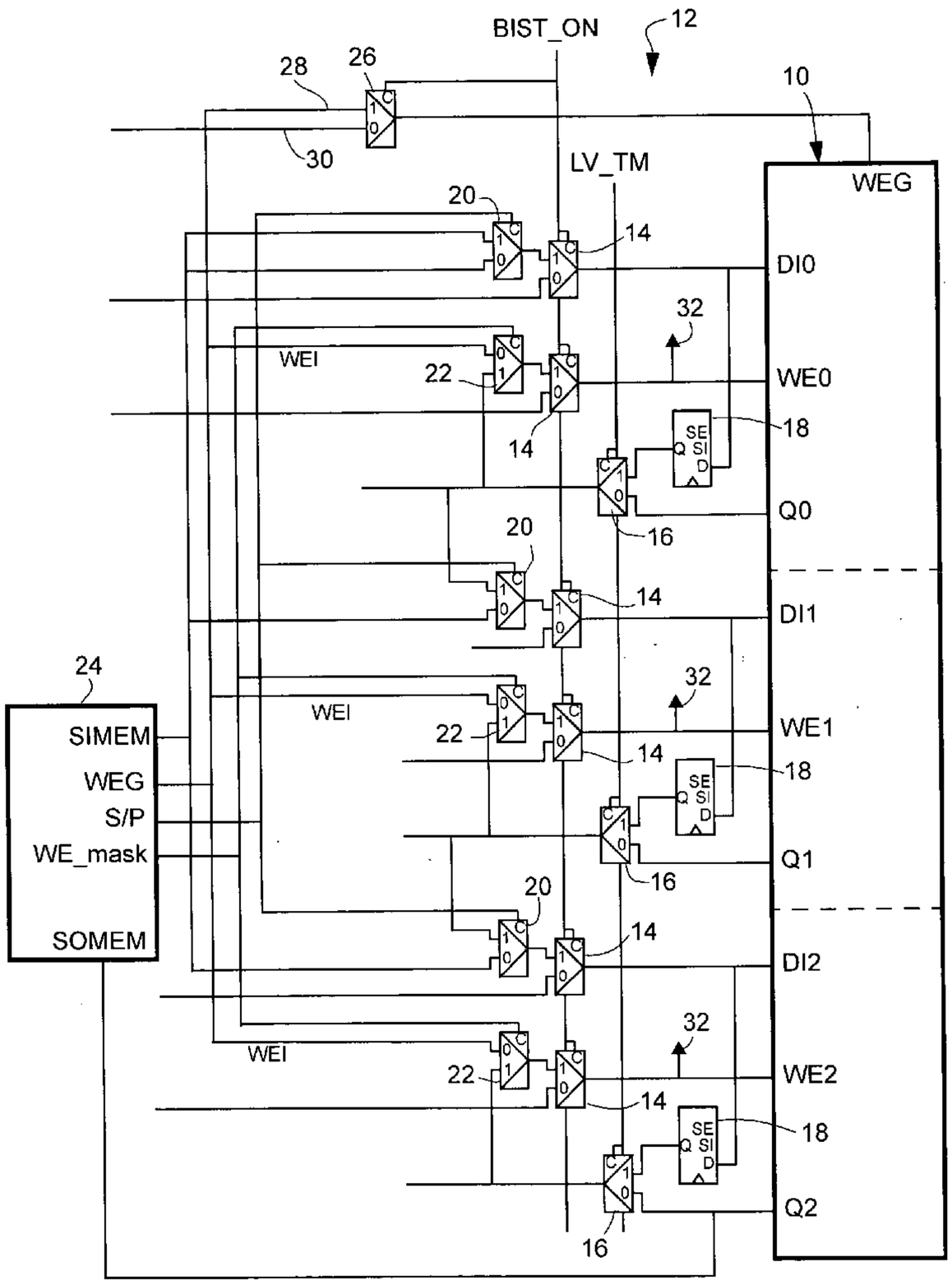
Publication Classification

(51) **Int. Cl.**[7] **G11C 29/00**; G06F 11/00; G01R 31/28

(52) **U.S. Cl.** **714/736**

(57) **ABSTRACT**

A method of testing write enable lines of random access memory having at least one word having one or more write enable inputs for controlling write operations in the word, comprises, for a selected memory address, shifting a series of test bits through an addressed word via a first data input to the word, and for each test bit, performing a write operation to the word using a write enable test input derived from data outputs of the word or from a test write enable signal applied concurrently to each write enable input; and, after each write operation, comparing a last bit of the word against an expected value to determine whether there exists a defect in a write enable line.



US 20040163015A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2004/0163015 A1**

(43) **Pub. Date: Aug. 19, 2004**

Nadeau-Dostie et al.

(54) **MEMORY REPAIR ANALYSIS METHOD AND CIRCUIT**

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(21) Appl. No.: **10/774,512**

(22) Filed: **Feb. 10, 2004**

Related U.S. Application Data

(60) Provisional application No. 60/447,280, filed on Feb. 14, 2003.

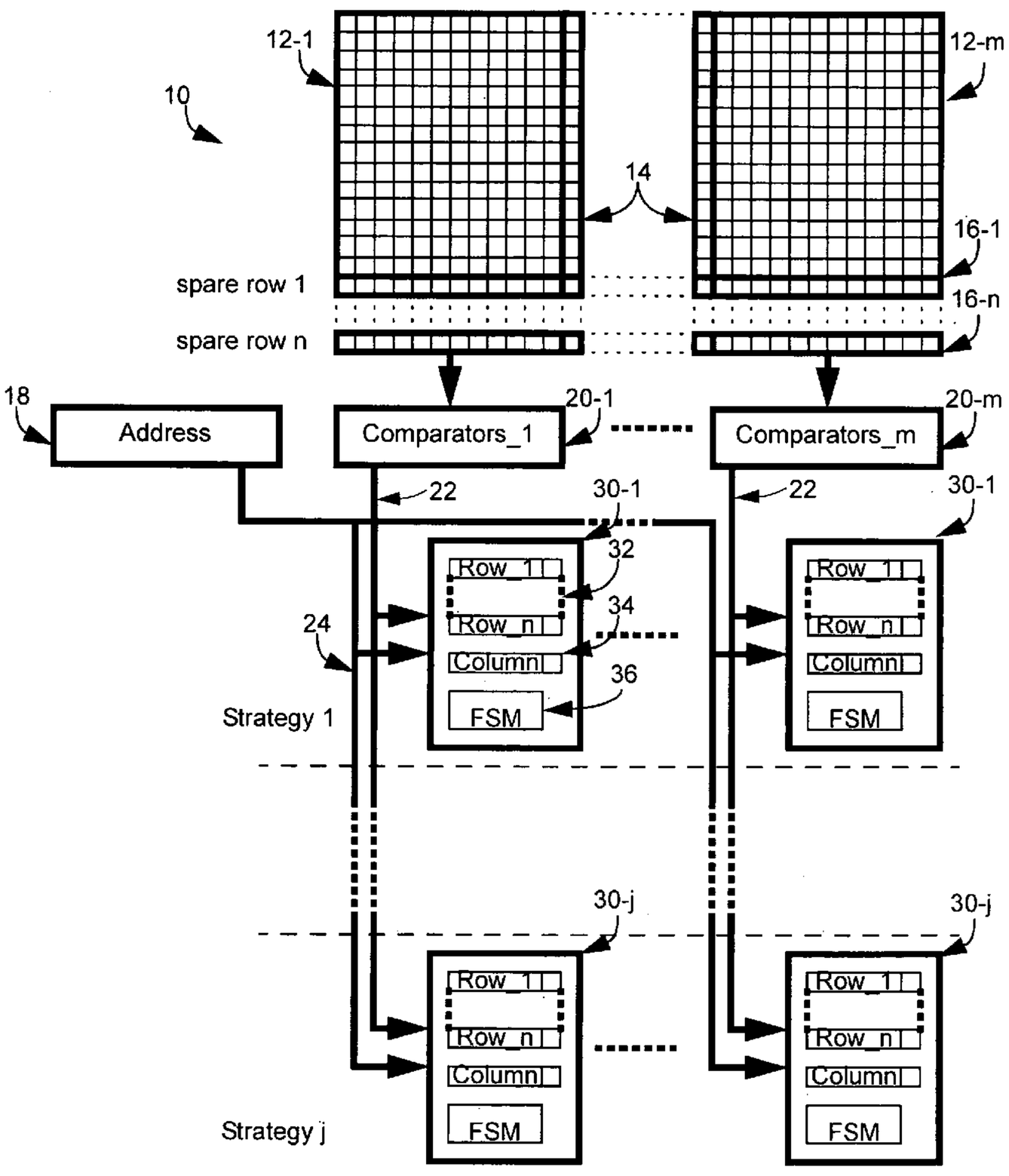
Publication Classification

(51) **Int. Cl.**[7] **H02H 3/05**

(52) **U.S. Cl.** **714/42**

(57) **ABSTRACT**

A method and circuit for repairing a memory array having one or more memory segments each having one spare column and a predetermined number of spare rows common to all segments, the method comprises, while testing the memory array for failures, generating an equal number of unique segment repair solutions for each segment with each segment repair solution including one defective column address, if any, and a number of defective row addresses, if any, corresponding to the predetermined number of spare rows; and, after completing testing, analyzing all segment repair solution combinations consisting of one segment repair solution selected from each segment; and identifying the best segment repair solution combination of combinations having a number of different defective row addresses which is less than or equal to the predetermined number of spare rows.



US 20040163021A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2004/0163021 A1**

(43) **Pub. Date: Aug. 19, 2004**

Nadeau-Dostie

(54) **METHOD AND CIRCUIT FOR AT-SPEED TESTING OF SCAN CIRCUITS**

(76) Inventor: **Benoit Nadeau-Dostie**, Gatineau (CA)

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(21) Appl. No.: **10/739,055**

(22) Filed: **Dec. 19, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/447,279, filed on Feb. 14, 2003.

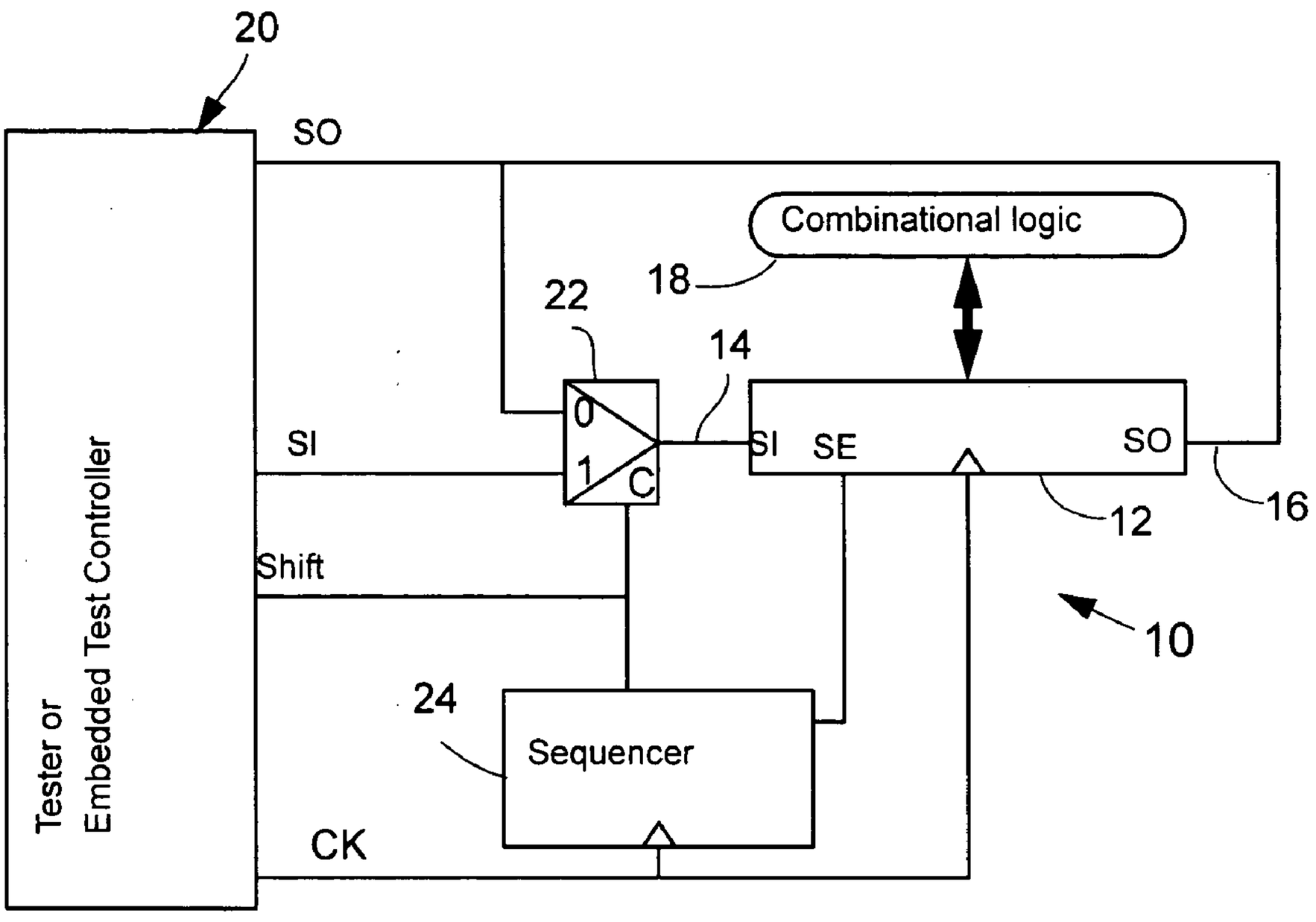
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/726**

(57) **ABSTRACT**

An improvement in a scan testing method for testing a circuit having memory elements arranged into one or more scan chains, the scan testing method having a shift phase for serially loading test patterns into the scan chains and serially unloading test response patterns from the scan chains and a capture phase for capturing the response of the circuit to the test pattern, comprises, during the capture phase, connecting the serial output of each scan chain to its serial input and applying a predetermined number of capture clock cycles with the memory elements configured in a non-capture mode for all but the last capture clock cycle and configured in capture mode for the last capture clock cycle.



US 20040257901A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2004/0257901 A1**

(43) **Pub. Date: Dec. 23, 2004**

Nadeau-Dostie et al.

(54) **MEMORY REPAIR CIRCUIT AND METHOD**

(76) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Saman M.I. Adham**, Kanata (CA)

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(21) Appl. No.: **10/868,208**

(22) Filed: **Jun. 16, 2004**

Related U.S. Application Data

(60) Provisional application No. 60/479,229, filed on Jun. 18, 2003.

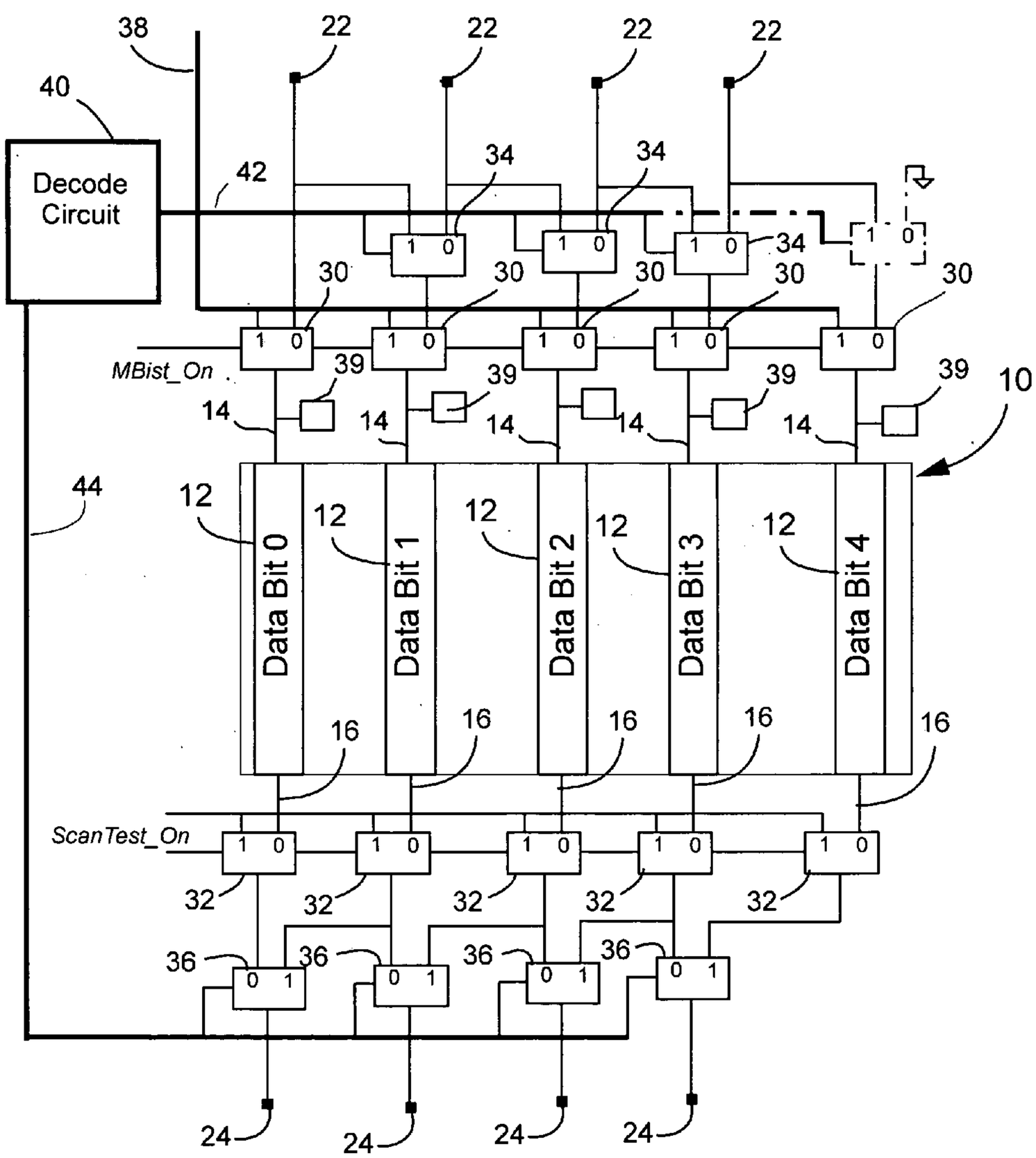
Publication Classification

(51) **Int. Cl.**[7] **G11C 8/00**

(52) **U.S. Cl.** **365/232**

(57) **ABSTRACT**

A self-repair circuit for a semiconductor memory provides input and output test selectors coupled to respective data bit group inputs and outputs, respectively and input and output repair selectors coupled between the input and output test selectors and functional inputs and functional outputs, respectively. This arrangement allows all data bit groups to be tested in one pass and all test and repair selector circuitry to be tested.



US 20050028059A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0028059 A1**

(43) **Pub. Date: Feb. 3, 2005**

Cote et al.

(54) **PROCESSOR INTERFACE FOR TEST ACCESS PORT**

(76) Inventors: **Jean-Francois Cote**, Chelsea (CA); **Benoit Nadeau-Dostie**, Gatineau (CA)

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(21) Appl. No.: **10/892,203**

(22) Filed: **Jul. 16, 2004**

Related U.S. Application Data

(60) Provisional application No. 60/491,558, filed on Aug. 1, 2003.

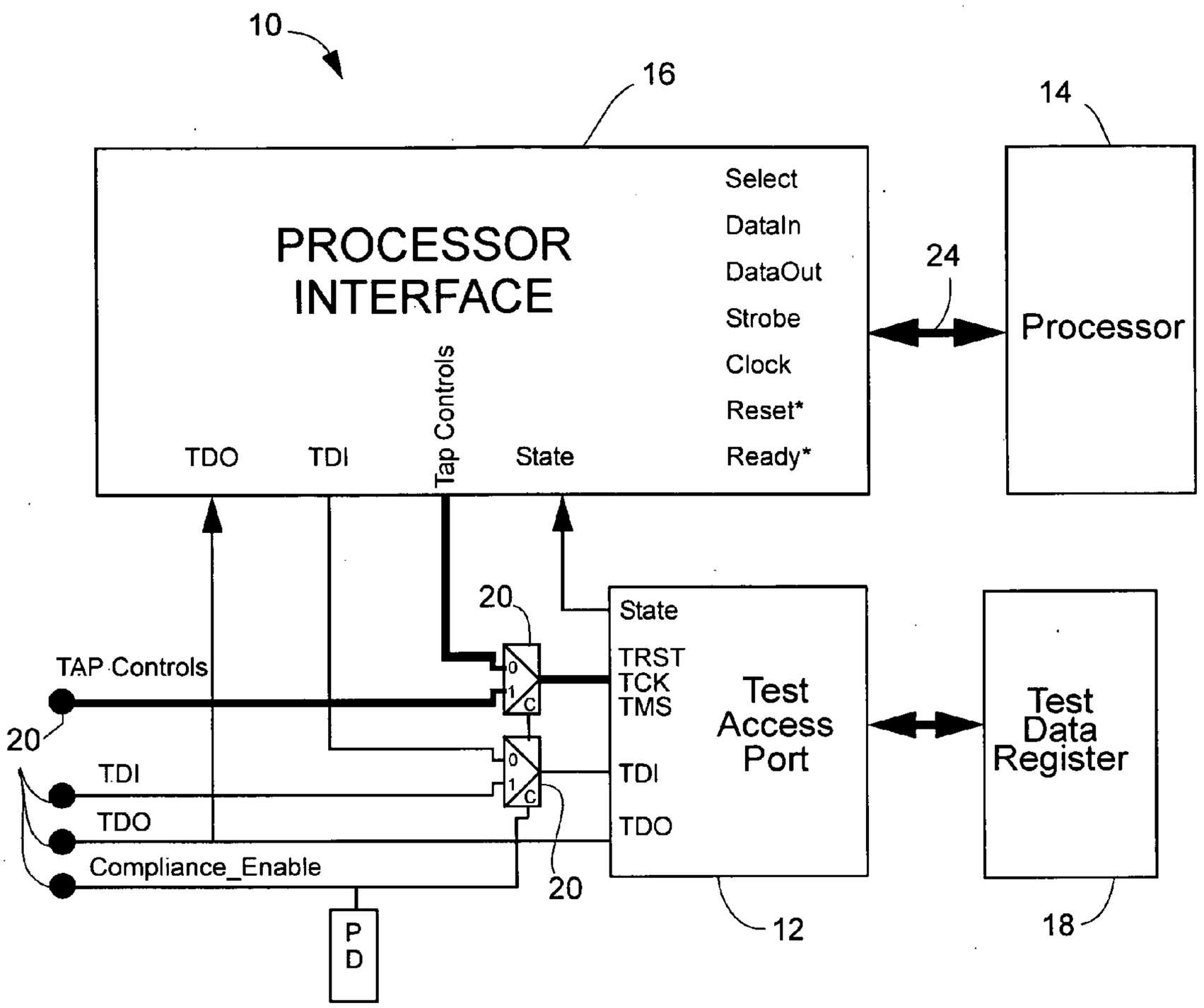
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/724**

(57) **ABSTRACT**

A processor interface for test access port comprises a write buffer for storing data output by a processor and having a command field, a data field, and a serial output connected to a serial input of the test access port, a read buffer for storing data output by the test access port for access by the processor and having a data field, and a serial input connected to a serial output of the test access port; and a control circuit responsive to a command stored in the command field for generating test access port control signals for transferring test data from the write buffer to the test register and from the test register to the read buffer via test access port serial input and serial output.



US 20050047229A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0047229 A1**

(43) **Pub. Date: Mar. 3, 2005**

Nadeau-Dostie et al.

(54) **METHOD AND CIRCUIT FOR COLLECTING MEMORY FAILURE INFORMATION**

(76) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Chelsea (CA)

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(21) Appl. No.: **10/690,594**

(22) Filed: **Oct. 23, 2003**

(30) **Foreign Application Priority Data**

Dec. 18, 2002 (CA) 2,414,632

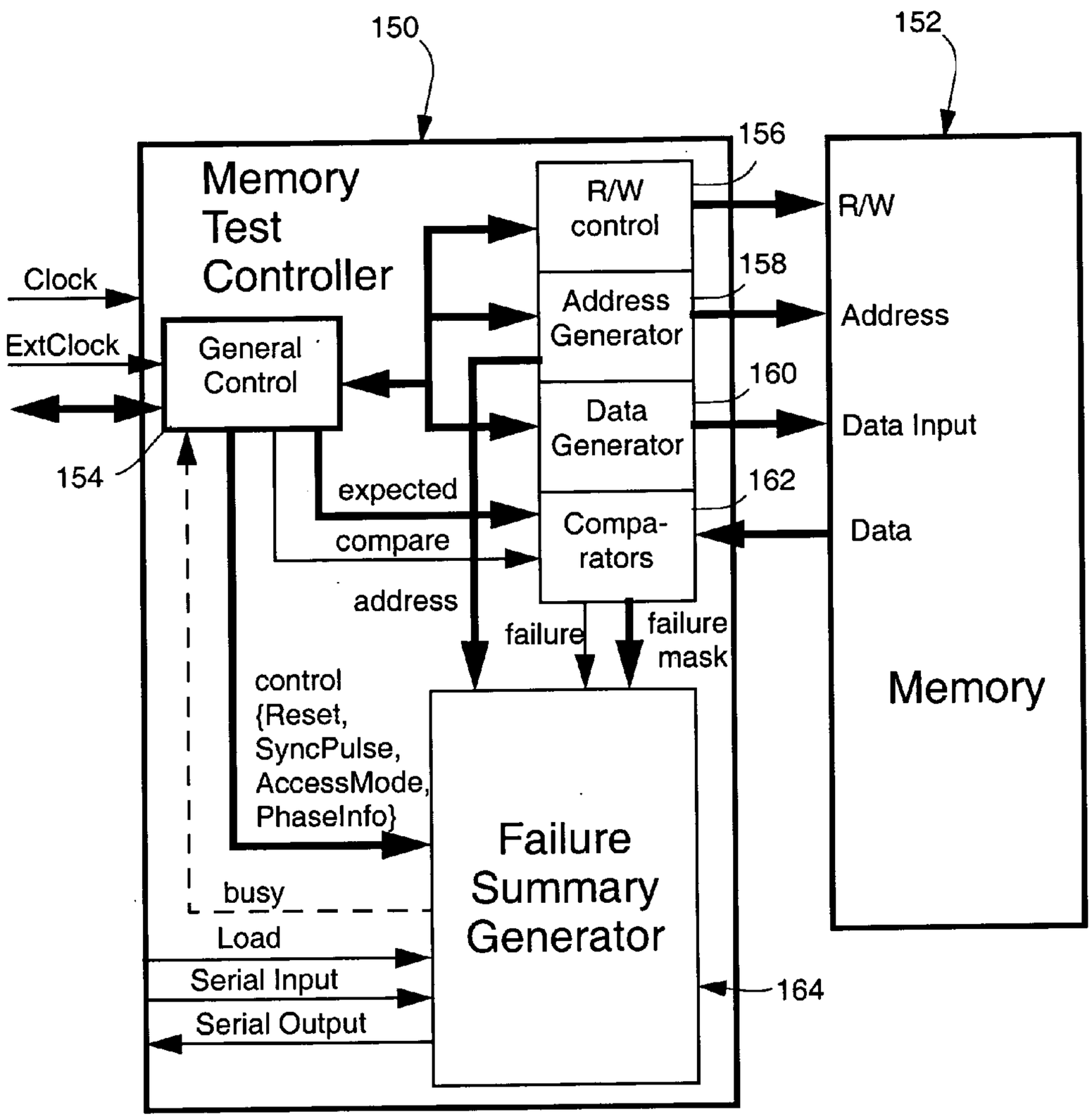
Publication Classification

(51) **Int. Cl.**[7] **G06F 11/00**; G11C 7/00

(52) **U.S. Cl.** **365/201**; 714/25; 714/766

(57) **ABSTRACT**

A method and circuit for collecting memory failure information on-chip and unloading the information in real time while performing a test of memory embedded in a circuit comprises, for each column or row of a memory under test, testing each memory location of the column or row according to a memory test algorithm under control of a first clock, selectively generating a failure summary on-circuit while testing each column or row of the memory; and transferring the failure summary from the circuit under control of a second clock within the time required to test the next column or row, if any, of the memory under test.



US 20050240790A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0240790 A1**

(43) **Pub. Date: Oct. 27, 2005**

Nadeau-Dostie et al.

(54) **CLOCKING METHODOLOGY FOR AT-SPEED TESTING OF SCAN CIRCUITS WITH SYNCHRONOUS CLOCKS**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Chelsea (CA); **Fadi Maamari**, San Jose, CA (US)

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(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(21) Appl. No.: **11/060,407**

(22) Filed: **Feb. 18, 2005**

Related U.S. Application Data

(60) Provisional application No. 60/564,210, filed on Apr. 22, 2004. Provisional application No. 60/579,649, filed on Jun. 16, 2004.

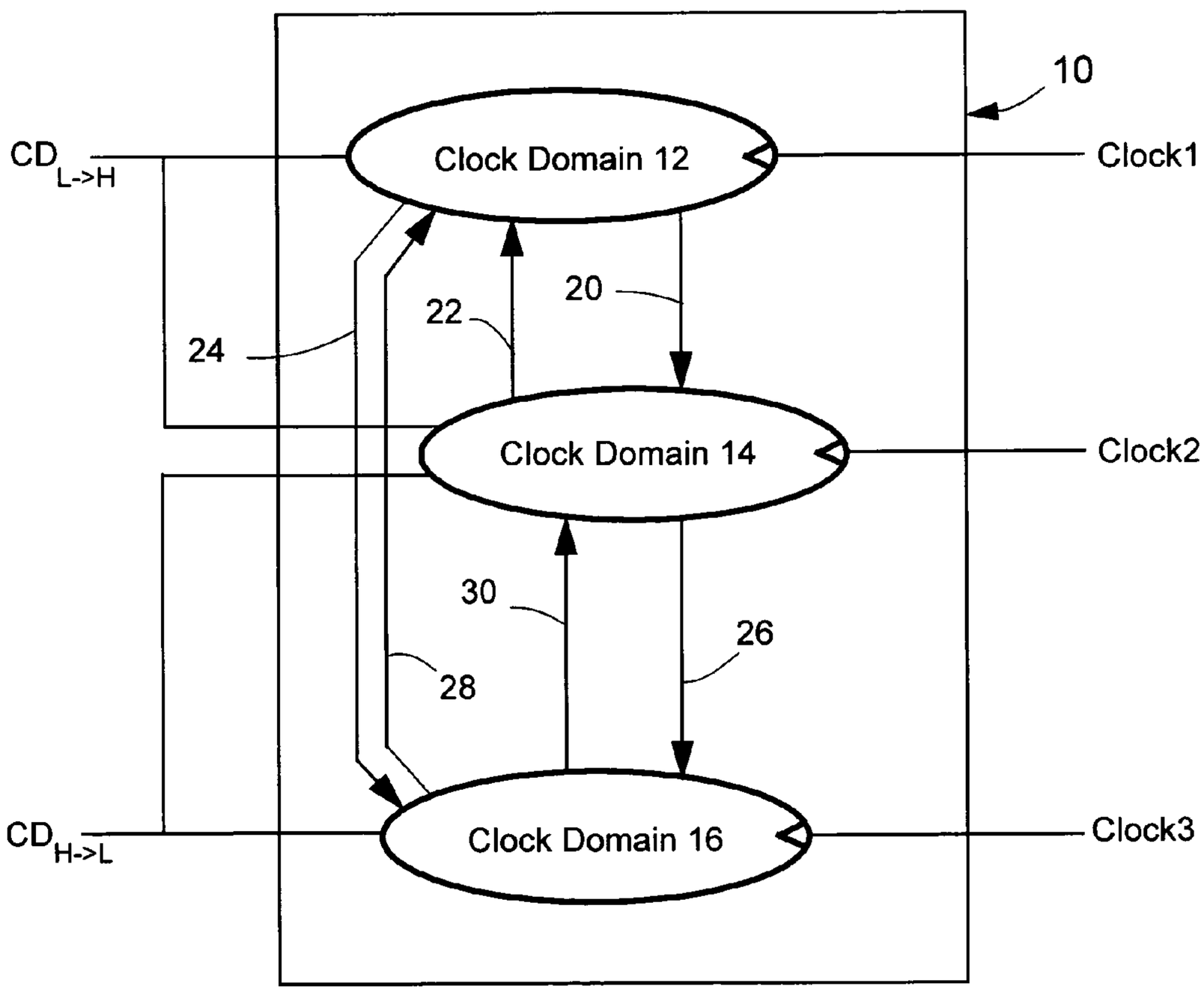
Publication Classification

(51) **Int. Cl.**[7] **G06F 13/42**

(52) **U.S. Cl.** **713/400**

(57) **ABSTRACT**

A clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in a scan circuit, each path originating from a source memory element in one of the domains and terminating at a destination memory element in another of the domains and comprises selectively aligning either a capture edge or a launch edge of the clock of each domain with a corresponding edge of at least one other domain of the interacting synchronous clock domains to determine the cross-domain paths to be tested between a source domain and a destination domain; clocking memory elements in each domain at respective domain clock rates to launch signal transitions from source memory elements in source domains; and for each pair of interacting clock domains under test, capturing, in the destination domain, circuit responses to signal transitions launched along paths originating from the source domain and selectively disabling capturing, in the source domain, of circuit responses to signal transitions launched along paths originating from the destination domain.



US 20050240847A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0240847 A1**

(43) **Pub. Date: Oct. 27, 2005**

Nadeau-Dostie et al.

(54) **CLOCK CONTROLLER FOR AT-SPEED TESTING OF SCAN CIRCUITS**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Chelsea (CA)

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(73) Assignee: **LogicVision, Inc.**, San Jose, CA

(21) Appl. No.: **11/013,319**

(22) Filed: **Dec. 17, 2004**

Related U.S. Application Data

(60) Provisional application No. 60/564,210, filed on Apr. 22, 2004.

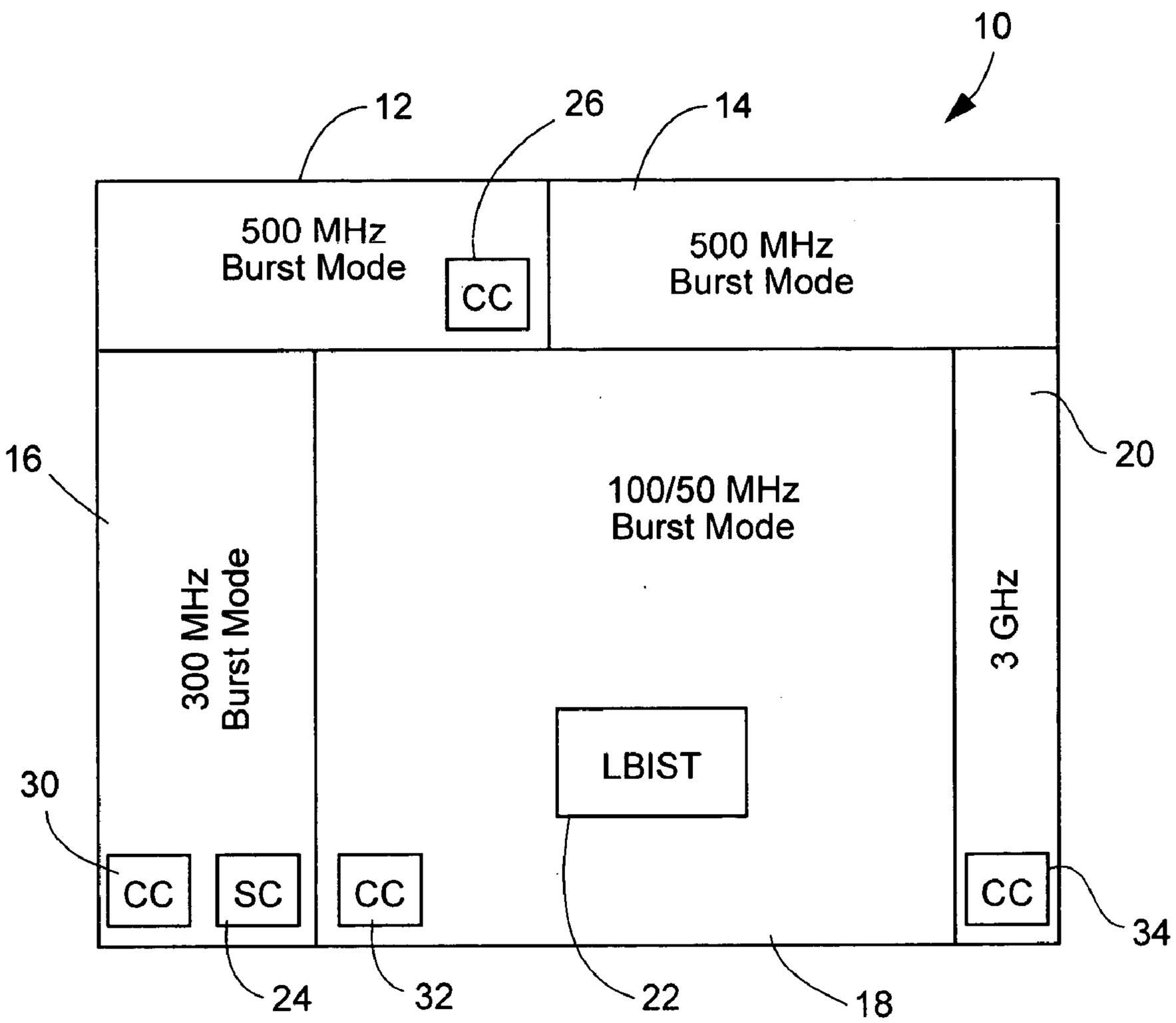
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/726**

(57) **ABSTRACT**

A test clock controller for generating a test clock signal for scan chains in integrated circuits having one or more clock domains, comprises a shift clock controller for generating a shift clock signal for use in loading test patterns into scan chains in the clock domains and for unloading a test response patterns from the scan chains and for generating a burst phase signal after loading a test pattern; and a burst clock controller associated with each of one or more clock domains and responsive to a burst phase signal for generating a burst of clock pulses derived from a respective reference clocks and including a first group of burst clock pulses having a selected reduced frequency relative to the reference clock and a second group of burst clock pulses having a frequency corresponding to that of the reference clock.



US 20050240848A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0240848 A1**

(43) **Pub. Date: Oct. 27, 2005**

Cote et al.

(54) **MASKING CIRCUIT AND METHOD OF MASKING CORRUPTED BITS**

(75) Inventors: **Jean-Francois Cote**, Chelsea (CA); **Paul Price**, Stoughton, MA (US); **Benoit Nadeau-Dostie**, Gatineau (CA)

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(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(21) Appl. No.: **11/109,844**

(22) Filed: **Apr. 20, 2005**

Related U.S. Application Data

(60) Provisional application No. 60/564,211, filed on Apr. 22, 2004.

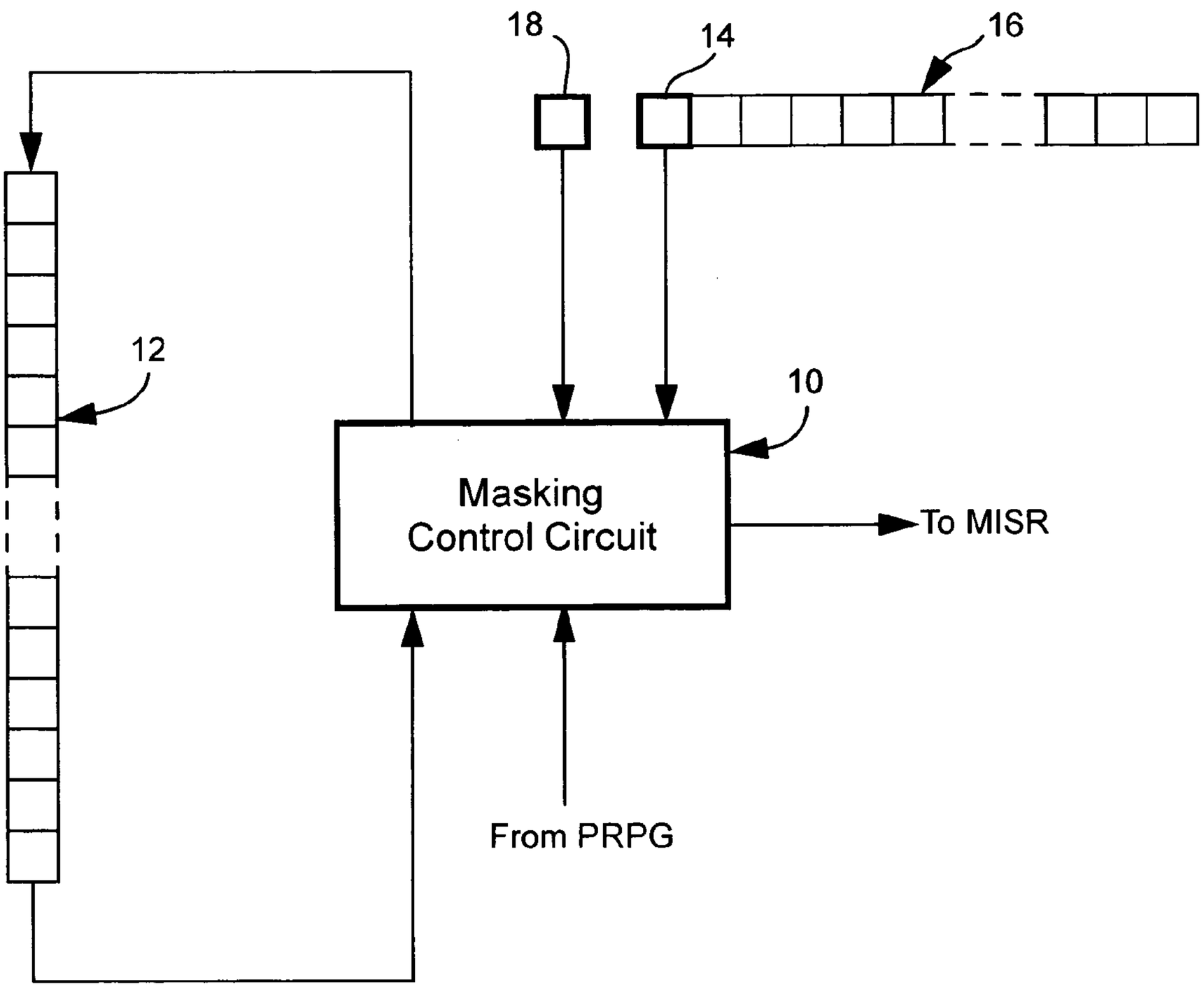
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/726**

(57) **ABSTRACT**

A masking circuit for selectively masking scan chain inputs and/or outputs during scan testing of an integrated circuit, comprises a mask register having at least two mask register elements for each scan chain to provide a plurality of masking modes; and an input and output mask control circuit for each scan chain, each mask control circuit being connected between a test pattern source and a signature register and between a serial input and a serial output of an associated scan chain and being responsive to mask control data stored in the register elements for configuring the associated scan chain in one of the plurality of masking modes during a scan test of the circuit.



US 20050273683A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0273683 A1**

(43) **Pub. Date: Dec. 8, 2005**

Cote et al.

(54) **INSERTION OF EMBEDDED TEST IN RTL TO GDSII FLOW**

(75) Inventors: **Jean-Francois Cote**, Chelsea (CA); **Benoit Nadeau-Dostie**, Gatineau (CA); **Fadi Maamari**, San Jose, CA (US)

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(73) Assignee: **LogicVision, Inc.**, San Jose, CA

(21) Appl. No.: **11/144,764**

(22) Filed: **Jun. 6, 2005**

Related U.S. Application Data

(60) Provisional application No. 60/577,171, filed on Jun. 7, 2004.

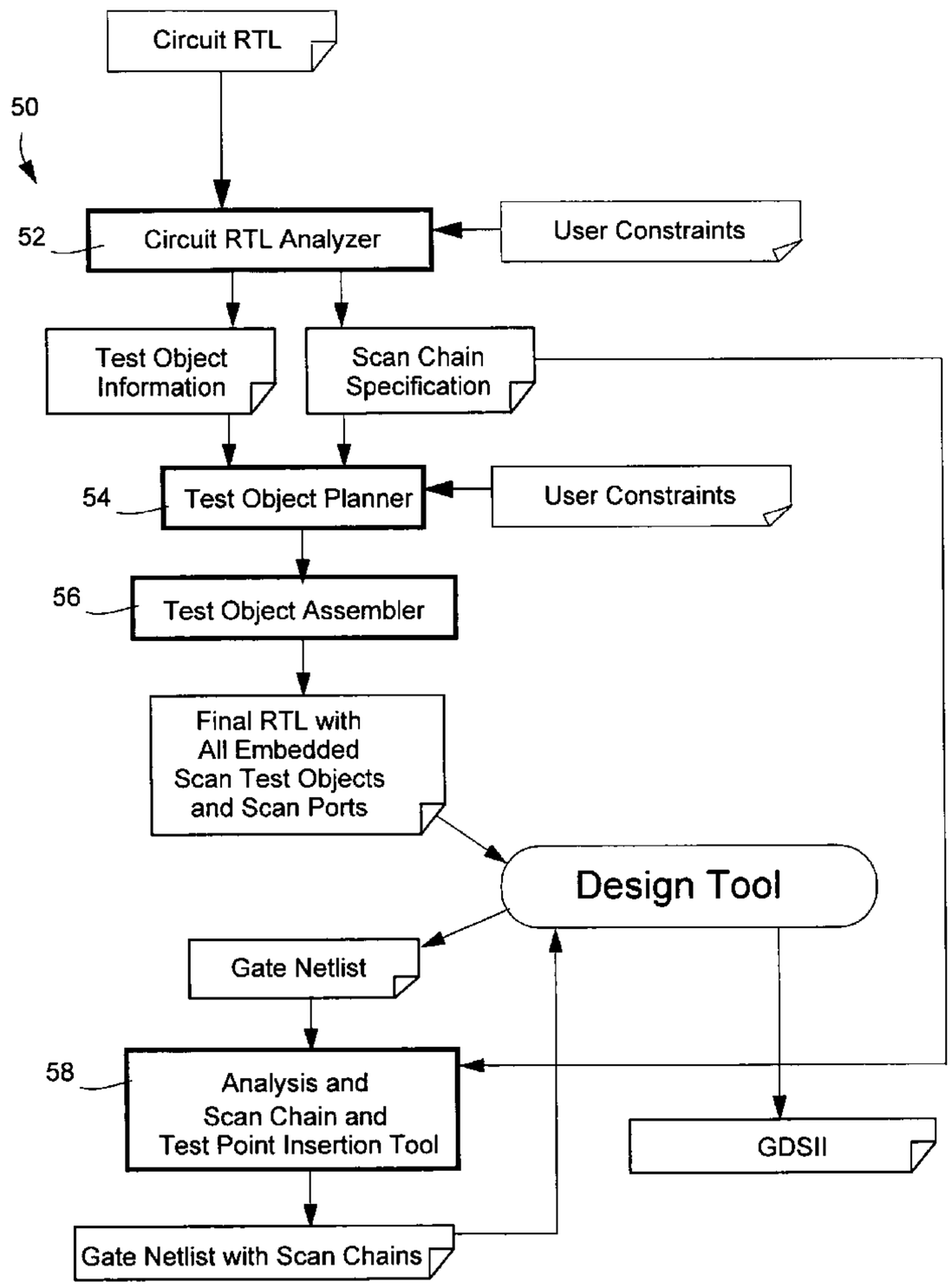
Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**; G06F 17/50

(52) **U.S. Cl.** **714/726**; 716/4; 716/18

(57) **ABSTRACT**

A method of designing a scan testable integrated circuit with embedded test objects for use in scan testing the circuit, comprises compiling a register-transfer level (RTL) circuit description of the circuit into an unmapped circuit description; extracting information from the unmapped circuit description for use in generating and inserting RTL descriptions of test objects into the RTL circuit description and for use in generating and inserting scan chains into the circuit; generating and inserting the RTL descriptions of the test objects into the RTL circuit description to produce a modified RTL circuit description; storing the modified RTL circuit description; synthesizing the modified RTL description into a gate level circuit description of the circuit; and constructing and inserting scan chains into the gate level circuit description according to information extracted from the unmapped circuit description.



US 20070266278A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2007/0266278 A1**

(43) **Pub. Date: Nov. 15, 2007**

Nadeau-Dostie et al.

(54) **METHOD FOR AT-SPEED TESTING OF MEMORY INTERFACE USING SCAN**

(76) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Chelsea (CA)

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(21) Appl. No.: **11/439,497**

(22) Filed: **May 24, 2006**

Related U.S. Application Data

(60) Provisional application No. 60/693,778, filed on Jun. 27, 2005.

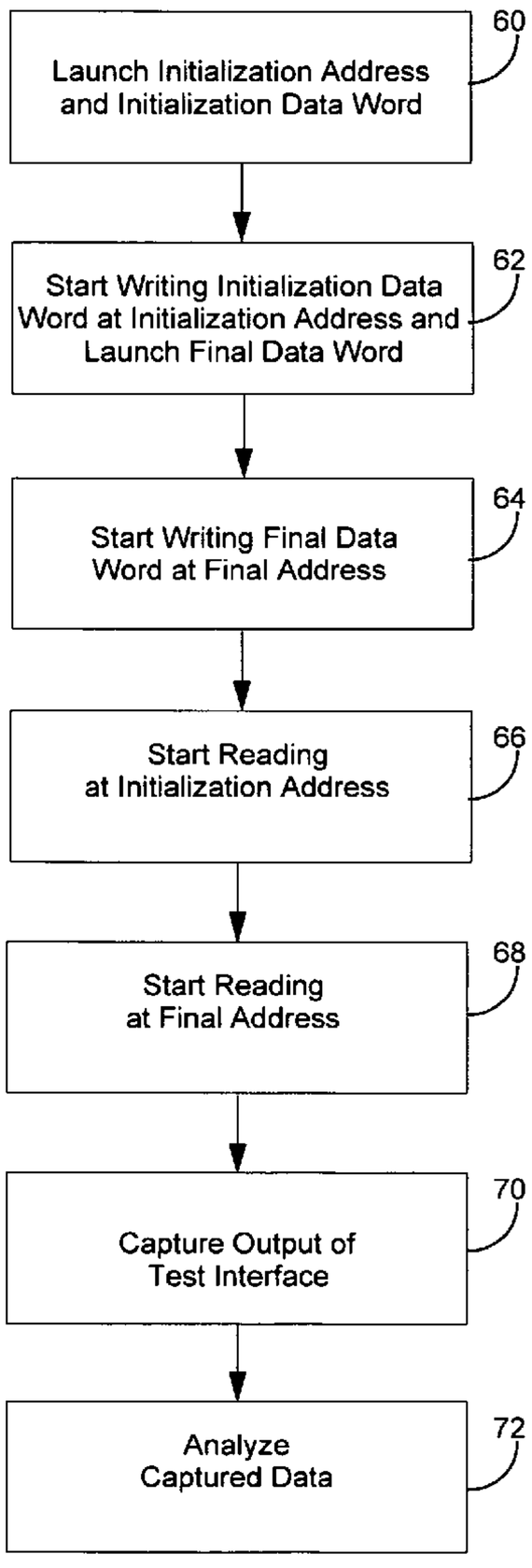
Publication Classification

(51) **Int. Cl.**
G11C 29/00 (2006.01)

(52) **U.S. Cl.** **714/719**

(57) **ABSTRACT**

A method and a circuit of testing of a memory interface associated with an embedded memory in a semiconductor circuit involves writing to two memory locations in succession; reading the two memory locations in succession in the same order in which the two memory locations were written; capturing output data from the memory interface; and analyzing captured output data to determine whether said captured output data corresponds to expected data.



US 20080065929A1

(19) **United States**

(12) **Patent Application Publication**

NADEAU-DOSTIE et al.

(10) **Pub. No.: US 2008/0065929 A1**

(43) **Pub. Date: Mar. 13, 2008**

(54) **METHOD AND APPARATUS FOR STORING AND DISTRIBUTING MEMORY REPAIR INFORMATION**

(75) Inventors: **Benoit NADEAU-DOSTIE**, Ottawa (CA); **Jean-Francois Cote**, Chelsea (CA)

Correspondence Address:
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OTTAWA, ON K1N OA1

(73) Assignee: **LOGICVISION, INC.**, San Jose, CA (US)

(21) Appl. No.: **11/853,383**

(22) Filed: **Sep. 11, 2007**

Related U.S. Application Data

(60) Provisional application No. 60/825,185, filed on Sep. 11, 2006.

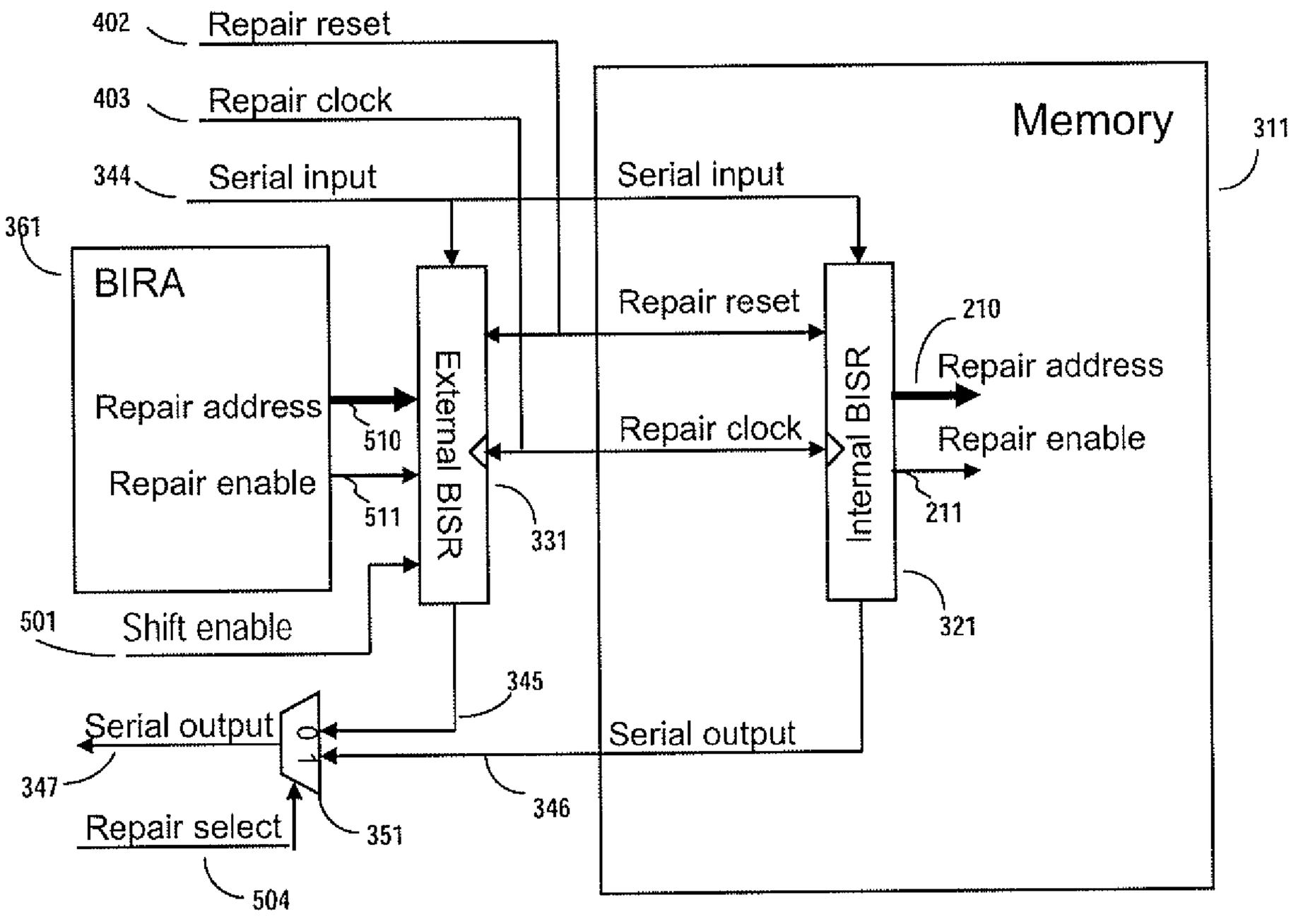
Publication Classification

(51) **Int. Cl.**
G06F 11/16 (2006.01)

(52) **U.S. Cl.** **714/5**; 714/E11.054

(57) **ABSTRACT**

A system for repairing embedded memories on an integrated circuit is disclosed. The system comprises an external Built-In Self-repair Register (BISR) associated with every reparable memory on the circuit. Each BISR is configured to accept a serial input from a daisy chain connection and to generate a serial output to a daisy chain connection, so that a plurality of BISRs are connected in a daisy chain with a fuse box controller. The fuse box controller has no information as to the number, configuration or size of the embedded memories, but determines, upon power up, the length of the daisy chain. With this information, the fuse box controller may perform a corresponding number of serial shift operations to move repair data to and from the BISRs and into and out of a fuse box associated with the controller. Memories having a parallel repair interface are supported by a parallel address bus and enable control signal on the BISR, while those having a serial repair interface are supported by a parallel daisy chain path that may be selectively cycled to shift the contents of the BISR to an internal serial register in the memory. Preferably, each of the BISRs has an associated repair analysis facility having a parallel address bus and enable control signal by which fuse data may be dumped in parallel into the BISR and from there, either uploaded to the fuse box through the controller or downloaded into the memory to effect repairs. Advantageously, pre-designed circuit blocks may provide daisy chain inputs and access ports to effect the inventive system therealong or to permit the circuit block to be bypassed for testing purposes.



US 20100037109A1

(19) **United States**

(12) **Patent Application Publication**

NADEAU-DOSTIE et al.

(10) **Pub. No.: US 2010/0037109 A1**

(43) **Pub. Date: Feb. 11, 2010**

(54) **METHOD FOR AT-SPEED TESTING OF MEMORY INTERFACE USING SCAN**

(75) Inventors: **Benoit NADEAU-DOSTIE**, Gatineau (CA); **Jean-François CÖTÉ**, Chelsea (CA)

Correspondence Address:
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(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(21) Appl. No.: **12/579,572**

(22) Filed: **Oct. 15, 2009**

Related U.S. Application Data

(63) Continuation of application No. 11/439,497, filed on May 24, 2006, now Pat. No. 7,617,425.

(60) Provisional application No. 60/693,778, filed on Jun. 27, 2005.

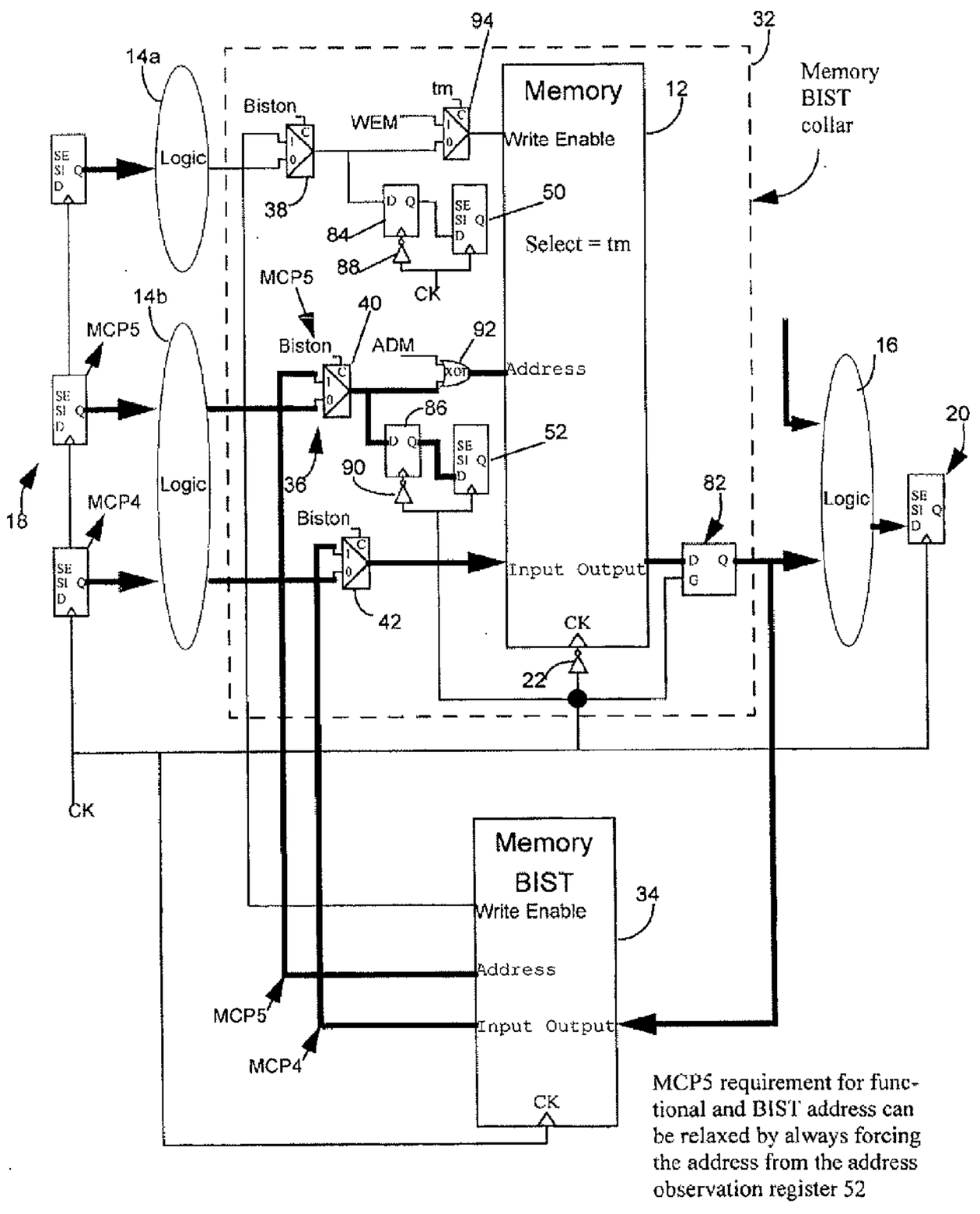
Publication Classification

(51) **Int. Cl.**
G11C 29/10 (2006.01)
G06F 11/263 (2006.01)

(52) **U.S. Cl.** **714/719**; 714/E11.177

(57) **ABSTRACT**

A method and a circuit of testing of a memory interface associated with an embedded memory in a semiconductor circuit involves writing to two memory locations in succession; reading the two memory locations in succession in the same order in which the two memory locations were written; capturing output data from the memory interface; and analyzing captured output data to determine whether said captured output data corresponds to expected data.



MCP5 requirement for functional and BIST address can be relaxed by always forcing the address from the address observation register 52

US 20120198294A1

(19) **United States**

(12) **Patent Application Publication**

Nadeau-Dostie et al.

(10) **Pub. No.: US 2012/0198294 A1**

(43) **Pub. Date: Aug. 2, 2012**

(54) **METHODS FOR AT-SPEED TESTING OF MEMORY INTERFACE**

(76) Inventors: **Benoit Nadeau-Dostie**, (US); **Jean-François Côté**, (US)

(21) Appl. No.: **13/018,279**

(22) Filed: **Jan. 31, 2011**

Publication Classification

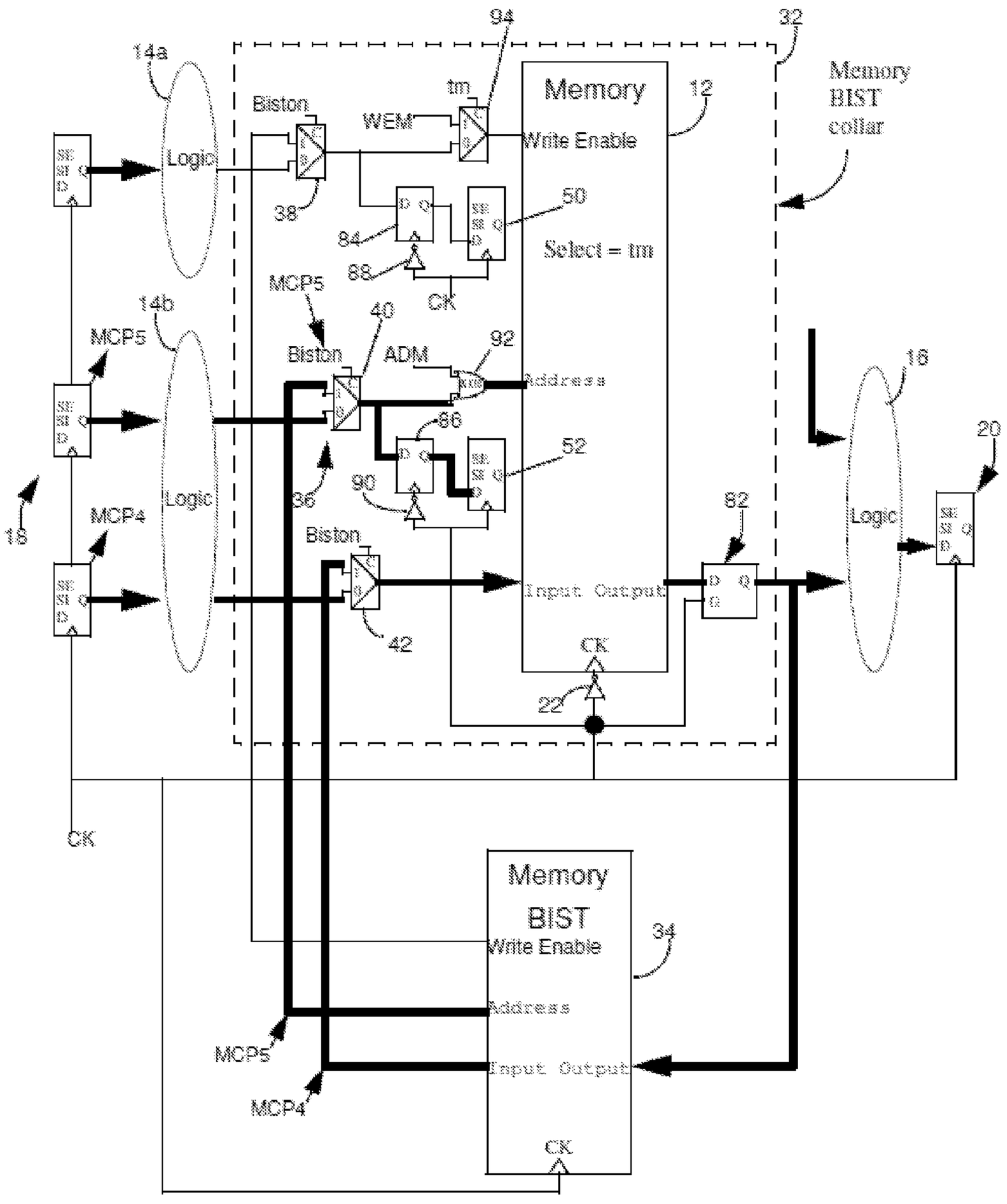
(51) **Int. Cl.**

G11C 29/10	(2006.01)
G06F 11/263	(2006.01)

(52) **U.S. Cl.** **714/719**; 714/E11.177

(57) **ABSTRACT**

Methods for at-speed testing of a memory interface associated with an embedded memory involves in general two write operations in succession, two read operations in succession, and a capture operation using scan cells. The write and read operations may be performed during a single clock burst, two separate clock bursts in a clock signal, or two separate clock bursts in separate clock signals.



US 20120272110A1

(19) **United States**

(12) **Patent Application Publication**

Rajski et al.

(10) **Pub. No.: US 2012/0272110 A1**

(43) **Pub. Date: Oct. 25, 2012**

(54) **TEST GENERATOR FOR LOW POWER BUILT-IN SELF-TEST**

(76) Inventors: **Janusz Rajski**, (US); **Jerzy Tyszer**, (US); **Grzegorz Mrugalski**, (US); **Benoit Nadeau-Dostie**, (US)

(21) Appl. No.: **13/451,527**

(22) Filed: **Apr. 19, 2012**

Related U.S. Application Data

(60) Provisional application No. 61/477,105, filed on Apr. 19, 2011, provisional application No. 61/543,229, filed on Oct. 4, 2011.

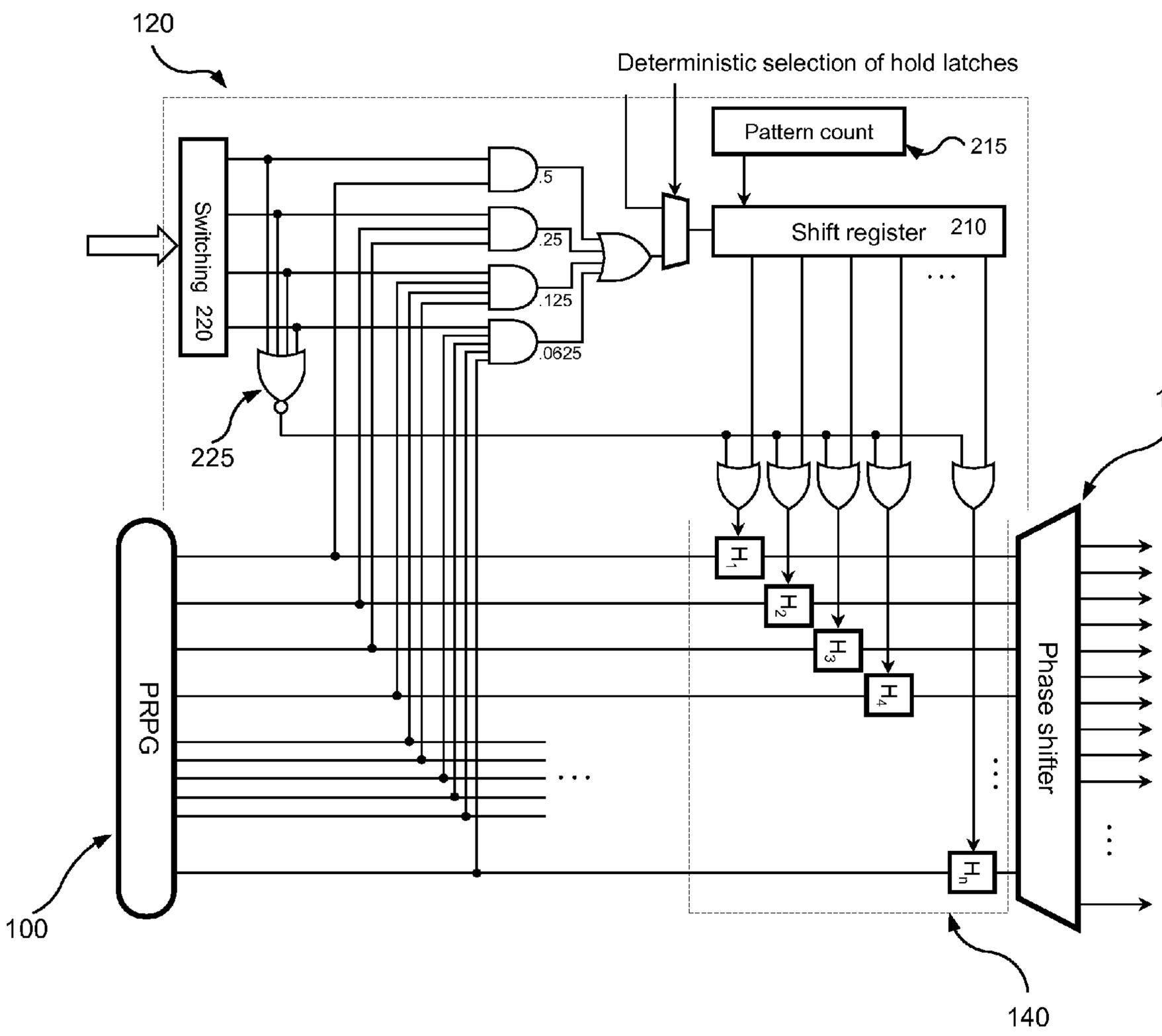
Publication Classification

(51) **Int. Cl.**
G01R 31/3177 (2006.01)
G06F 11/25 (2006.01)

(52) **U.S. Cl.** **714/726**; 714/E11.155

(57) **ABSTRACT**

Aspects of the invention relate to low power BIST-based testing. A low power test generator may comprise a pseudo-random pattern generator unit, a toggle control unit configured to generate toggle control data based on bit sequence data generated by the pseudo-random pattern generator unit, and a hold register unit configured to generate low power test pattern data by replacing, based on the toggle control data received from the toggle control unit, data from some or all of outputs of the pseudo-random pattern generator unit with constant values during various time periods. The low power test generator may further comprise a phase shifter configured to combine bits of the low power test pattern data for driving scan chains.



US 20210174892A1

(19) **United States**

(12) **Patent Application Publication**

Nadeau-Dostie

(10) **Pub. No.: US 2021/0174892 A1**

(43) **Pub. Date: Jun. 10, 2021**

(54) **ERROR-CORRECTING CODE-ASSISTED MEMORY REPAIR**

(71) Applicant: **Mentor Graphics Corporation**, Wilsonville, OR (US)

(72) Inventor: **Benoit Nadeau-Dostie**, Gatineau (CA)

(21) Appl. No.: **17/115,894**

(22) Filed: **Dec. 9, 2020**

Related U.S. Application Data

(60) Provisional application No. 62/945,317, filed on Dec. 9, 2019.

Publication Classification

(51) **Int. Cl.**

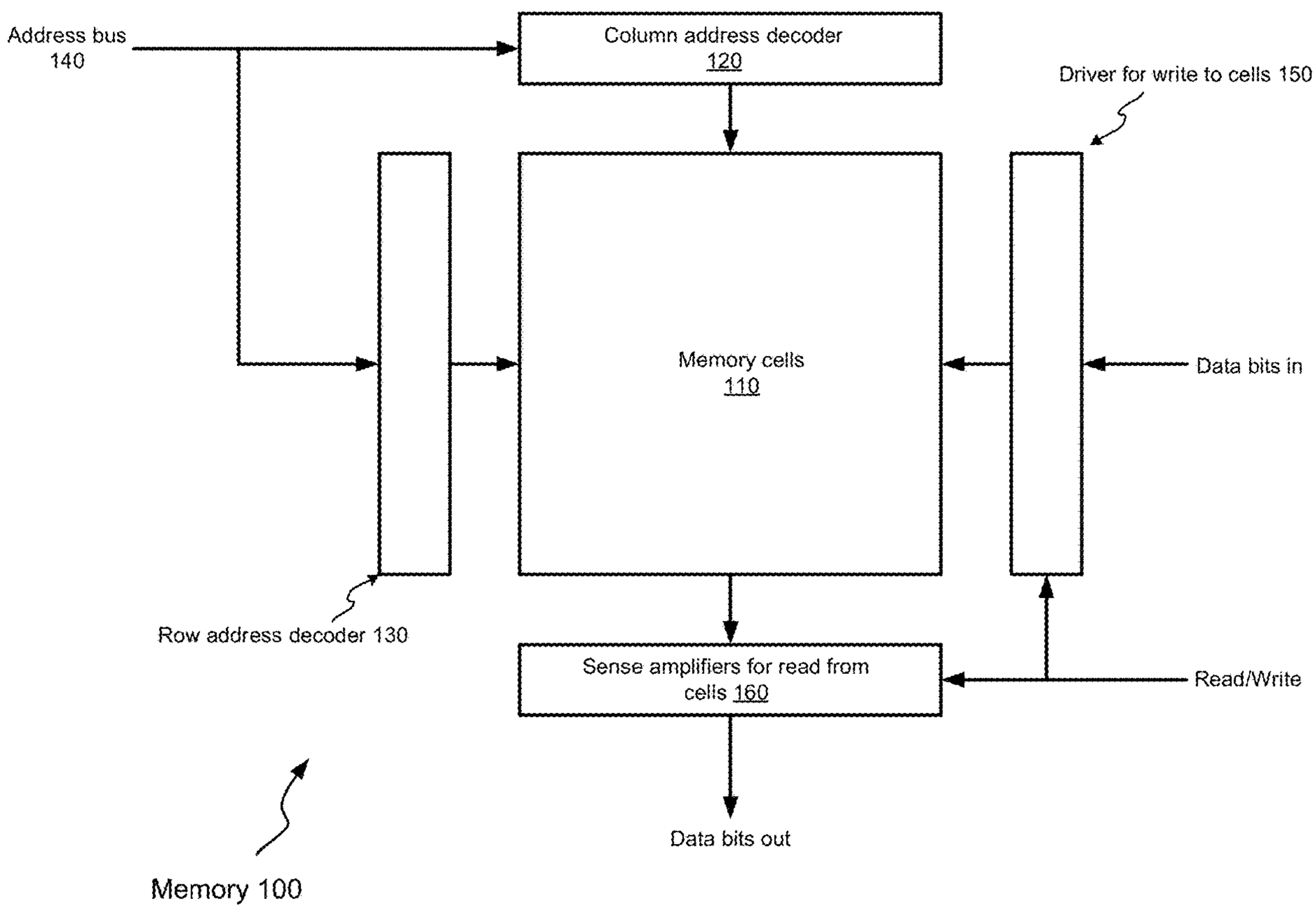
G11C 29/42	(2006.01)
G11C 29/44	(2006.01)
G11C 11/16	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 29/42*** (2013.01); ***G11C 11/1675*** (2013.01); ***G11C 11/1673*** (2013.01); ***G11C 29/4401*** (2013.01)

(57) **ABSTRACT**

A memory-testing circuit configured to perform a test of a memory comprising error-correcting code circuitry comprises repair circuitry configured to allocate a spare row or row block in the memory for a defective row or row block in the memory, a defective row or row block being a row or row block in which a memory word has a number of error bits greater than a preset number, wherein the test of the memory comprises: disabling the error-correcting code circuitry, performing a pre-repair operation, the pre-repair operation comprising: determining whether the memory has one or more defective rows or row blocks, and allocating one or more spare rows or row blocks for the one or more defective rows or row blocks if the one or more spare rows or row blocks are available, and performing a post-repair operation on the repaired memory.



US 20220215896A1

(19) **United States**

(12) **Patent Application Publication**

Nadeau-Dostie et al.

(10) **Pub. No.: US 2022/0215896 A1**

(43) **Pub. Date: Jul. 7, 2022**

(54) **METHOD AND APPARATUS FOR PROCESSING MEMORY REPAIR INFORMATION**

(71) Applicant: **Siemens Industry Software Inc**, Plano, TX (US)

(72) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Luc Romain**, Gatineau (CA)

(21) Appl. No.: **17/604,805**

(22) PCT Filed: **Aug. 27, 2019**

(86) PCT No.: **PCT/US2019/048223**

§ 371 (c)(1),

(2) Date: **Oct. 19, 2021**

Related U.S. Application Data

(60) Provisional application No. 62/836,100, filed on Apr. 19, 2019.

Publication Classification

(51) **Int. Cl.**

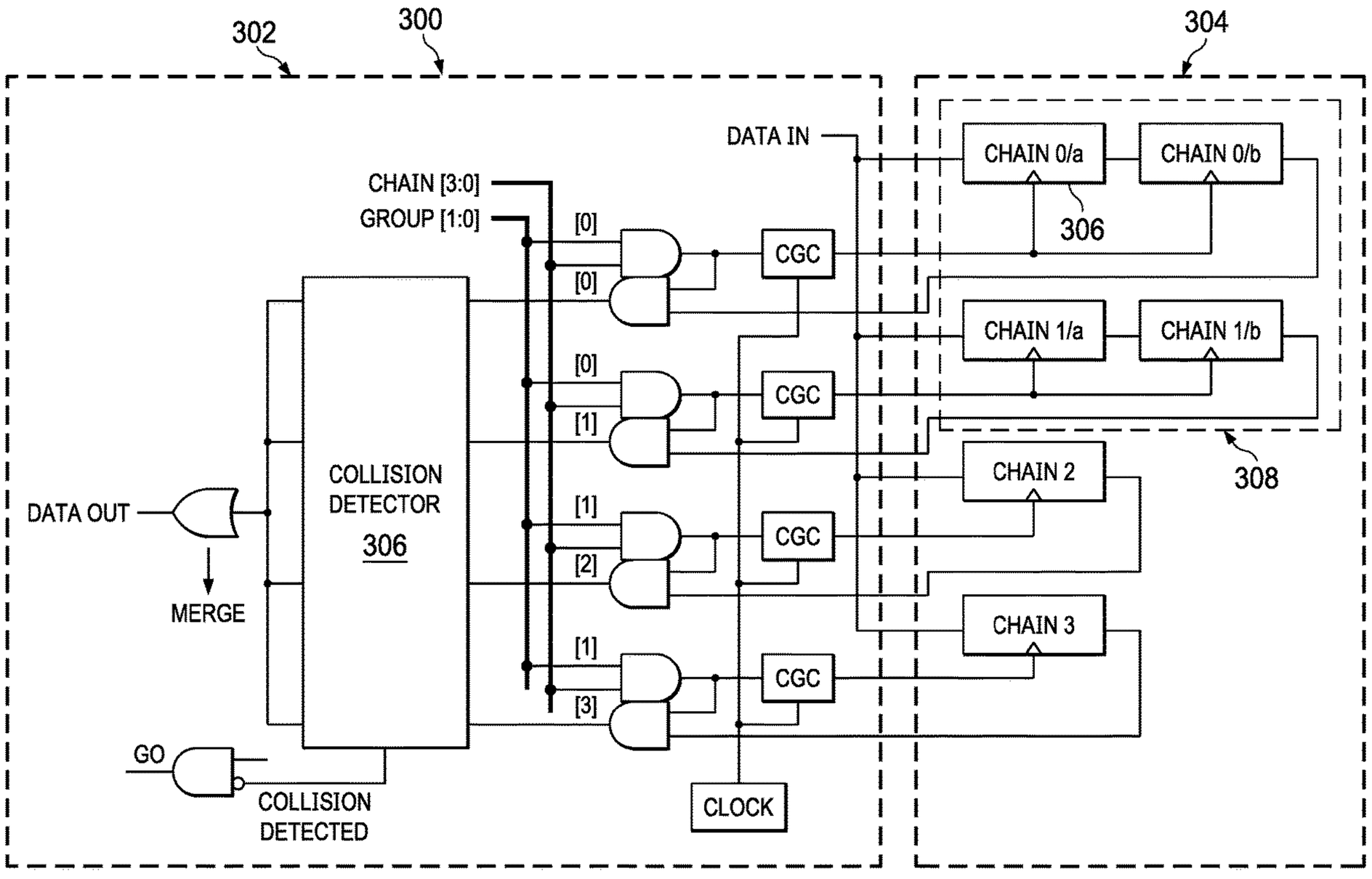
G11C 29/44	(2006.01)
G11C 29/40	(2006.01)
G11C 29/36	(2006.01)

(52) **U.S. Cl.**

CPC .. ***G11C 29/4401*** (2013.01); *G11C 2029/3602* (2013.01); ***G11C 29/36*** (2013.01); ***G11C 29/40*** (2013.01)

(57) **ABSTRACT**

Systems and methods for repairing a memory. A method includes performing a repair analysis of the embedded memories to produce repair information. The method includes storing the repair information in the registers, where the registers are organized into groups having chains of identical length. The method includes performing collision detection between the repair information in each of the groups. The method includes merging the repair information in each of the groups. The method includes repairing the embedded memories using the merged repair information.



US 20230110161A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2023/0110161 A1**

(43) **Pub. Date: Apr. 13, 2023**

Nadeau-Dostie et al.

(54) **ASYNCHRONOUS INTERFACE FOR TRANSPORTING TEST-RELATED DATA VIA SERIAL CHANNELS**

(71) Applicant: **Siemens Industry Software Inc.**, Plando, TX (US)

(72) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Davie, FL (US)

(21) Appl. No.: **17/498,085**

(22) Filed: **Oct. 11, 2021**

Publication Classification

(51) **Int. Cl.**

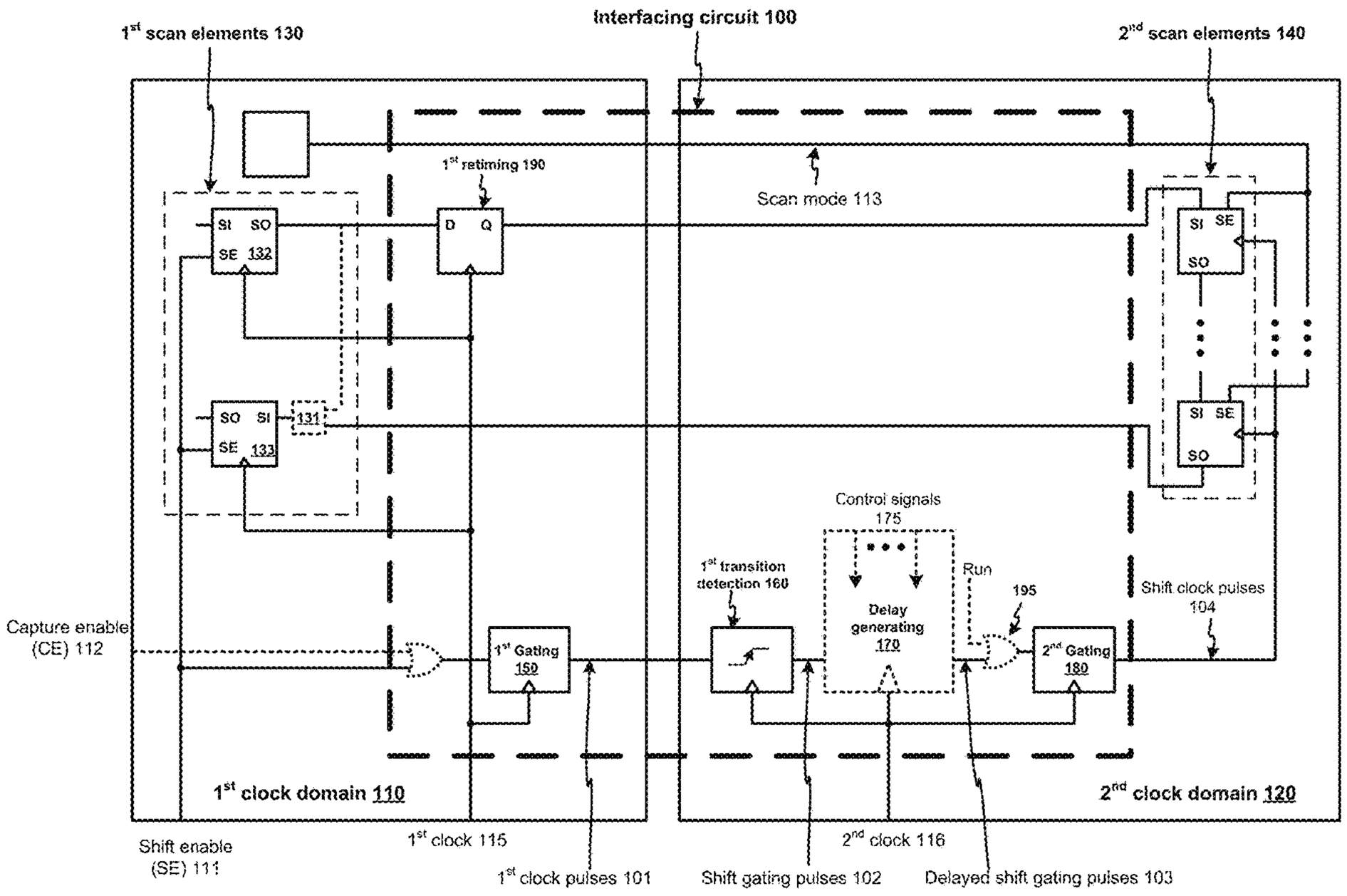
G06F 1/12	(2006.01)
G06F 1/06	(2006.01)

(52) **U.S. Cl.**

CPC . ***G06F 1/12*** (2013.01); ***G06F 1/06*** (2013.01)

(57) **ABSTRACT**

A circuit comprises: a first clock gating device clocked by a first clock signal and configured to generate first clock pulses when a shift enable signal is active, a first transition detecting device clocked by a second clock signal and configured to generate shift gating pulses when detecting active transitions of the first clock pulses, a second clock gating device clocked by the second clock signal and configured to generate shift clock pulses based on the shift gating pulses to clock second scan elements for a shift operation with first scan elements clocked by the first clock signal, and a first retiming device triggered by active pulse edges of the first clock signal and configurable to hold a value for the shift operation. The circuit may further comprise a delay generating device configured to generate delayed shift gating pulses for generating the shift clock pulses.



US 20230178172A1

(19) **United States**

(12) **Patent Application Publication**

Yun et al.

(10) **Pub. No.: US 2023/0178172 A1**

(43) **Pub. Date: Jun. 8, 2023**

(54) **REFERENCE BITS TEST AND REPAIR USING MEMORY BUILT-IN SELF-TEST**

(71) Applicant: **Siemens Industry Software Inc.**, Plano, FL (US)

(72) Inventors: **Jongsin Yun**, Portland, OR (US); **Benoit Nadeau-Dostie**, Gatineau (CA); **Harshitha Kodali**, Wilsonville, OR (US)

(21) Appl. No.: **17/906,303**

(22) PCT Filed: **Mar. 18, 2021**

(86) PCT No.: **PCT/US2021/022871**

§ 371 (c)(1),
(2) Date: **Sep. 14, 2022**

Related U.S. Application Data

(60) Provisional application No. 63/000,517, filed on Mar. 27, 2020.

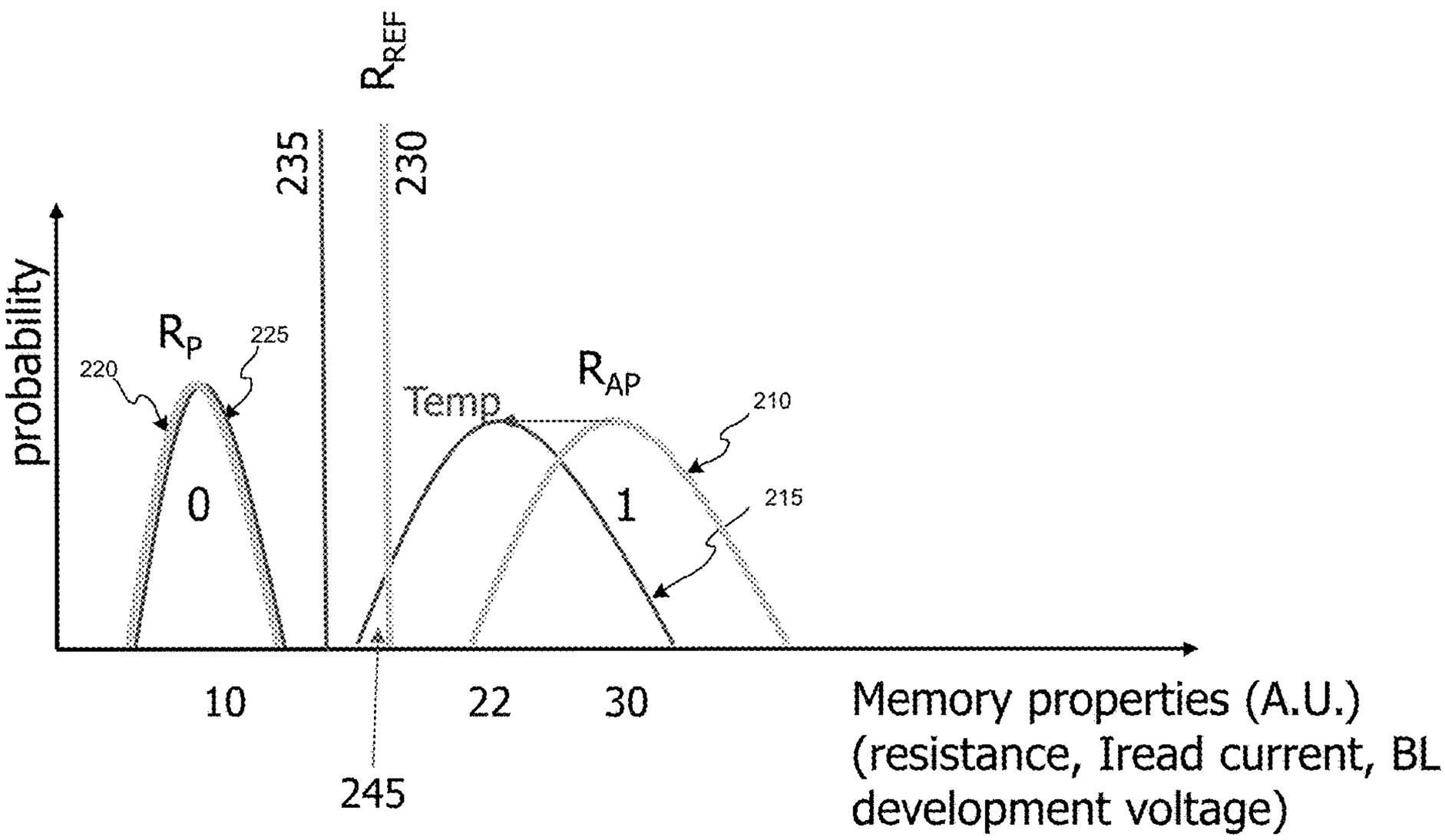
Publication Classification

(51) **Int. Cl.**
G11C 29/54 (2006.01)
G11C 29/56 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 29/54*** (2013.01); ***G11C 29/56004*** (2013.01)

(57) **ABSTRACT**

A memory-testing circuit configured to perform a test of reference bits in a memory. In a read operation, outputs of data bit columns are compared with one or more reference bit columns. The memory-testing circuit comprises: a test controller and association adjustment circuitry configurable by the test controller to associate another one or more reference bit columns or one or more data bit columns with the data bit columns in the read operation. The test controller can determine whether the original one or more reference bit columns have a defect based on results from the two different association.



US 20240013846A1

(19) **United States**

(12) **Patent Application Publication**

Yun et al.

(10) **Pub. No.: US 2024/0013846 A1**

(43) **Pub. Date: Jan. 11, 2024**

(54) **MEMORY BUILT-IN SELF-TEST WITH AUTOMATED REFERENCE TRIM FEEDBACK FOR MEMORY SENSING**

(71) Applicant: **Siemens Industry Software Inc.**, Plano, TX (US)

(72) Inventors: **Jongsin Yun**, Portland, OR (US); **Benoit Nadeau-Dostie**, Gatineau (CA); **Martin Keim**, Sherwood, OR (US)

(21) Appl. No.: **17/756,963**

(22) PCT Filed: **May 28, 2020**

(86) PCT No.: **PCT/US2020/034860**

§ 371 (c)(1),
(2) Date: **Jun. 7, 2022**

Related U.S. Application Data

(60) Provisional application No. 62/945,335, filed on Dec. 9, 2019.

Publication Classification

(51) **Int. Cl.**

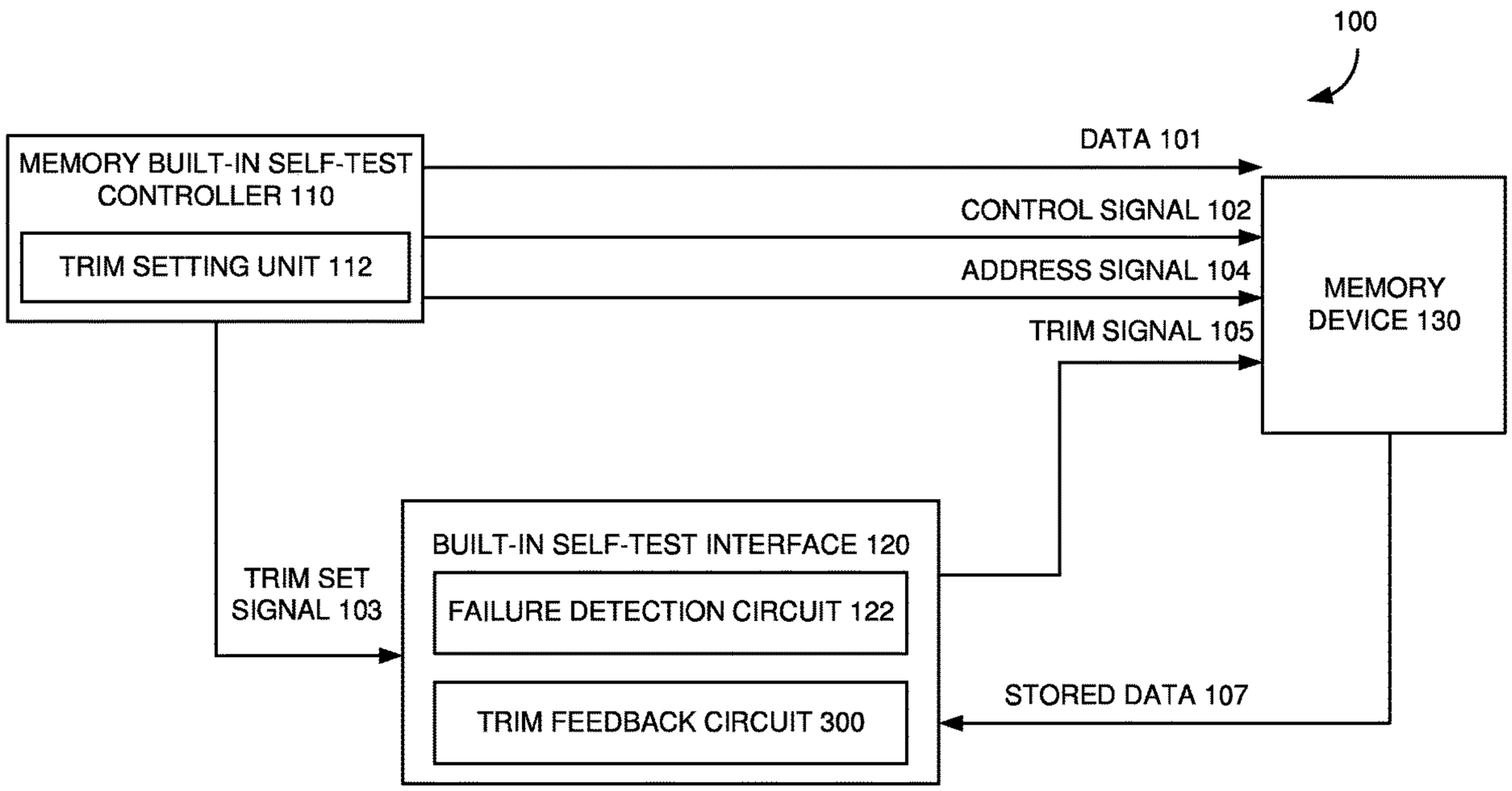
G11C 29/14	(2006.01)
G11C 29/46	(2006.01)
G11C 29/12	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 29/14*** (2013.01); ***G11C 29/46*** (2013.01); ***G11C 29/1201*** (2013.01)

(57) **ABSTRACT**

This application discloses a memory built-in self-test system to prompt a memory device to sense values of stored data using a reference trim during memory read operations. The memory built-in self-test system can automatically set the reference trim for the memory device. The memory built-in self-test system includes a memory built-in self-test controller to prompt the memory device to perform the memory read operations with different test values for the reference trim. The memory built-in self-test system also includes a trim feedback circuit to determine when the memory device fails to correctly sense the values of the stored data using the test values for the reference trim, and set the reference trim for the memory device based, at least in part, on the failures of the memory device to correctly sense the stored data.



US 20240087665A1

(19) **United States**

(12) **Patent Application Publication**

Nadeau-Dostie et al.

(10) **Pub. No.: US 2024/0087665 A1**

(43) **Pub. Date: Mar. 14, 2024**

(54) **READ-ONLY MEMORY DIAGNOSIS AND REPAIR**

(71) Applicant: **Siemens Industry Software Inc.**, Plano, TX (US)

(72) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jongsin Yun**, Portland, OR (US)

(73) Assignee: **Siemens Industry Software Inc.**, Plano, TX (US)

(21) Appl. No.: **18/273,059**

(22) PCT Filed: **Jan. 29, 2021**

(86) PCT No.: **PCT/US2021/015762**

§ 371 (c)(1),
(2) Date: **Jul. 19, 2023**

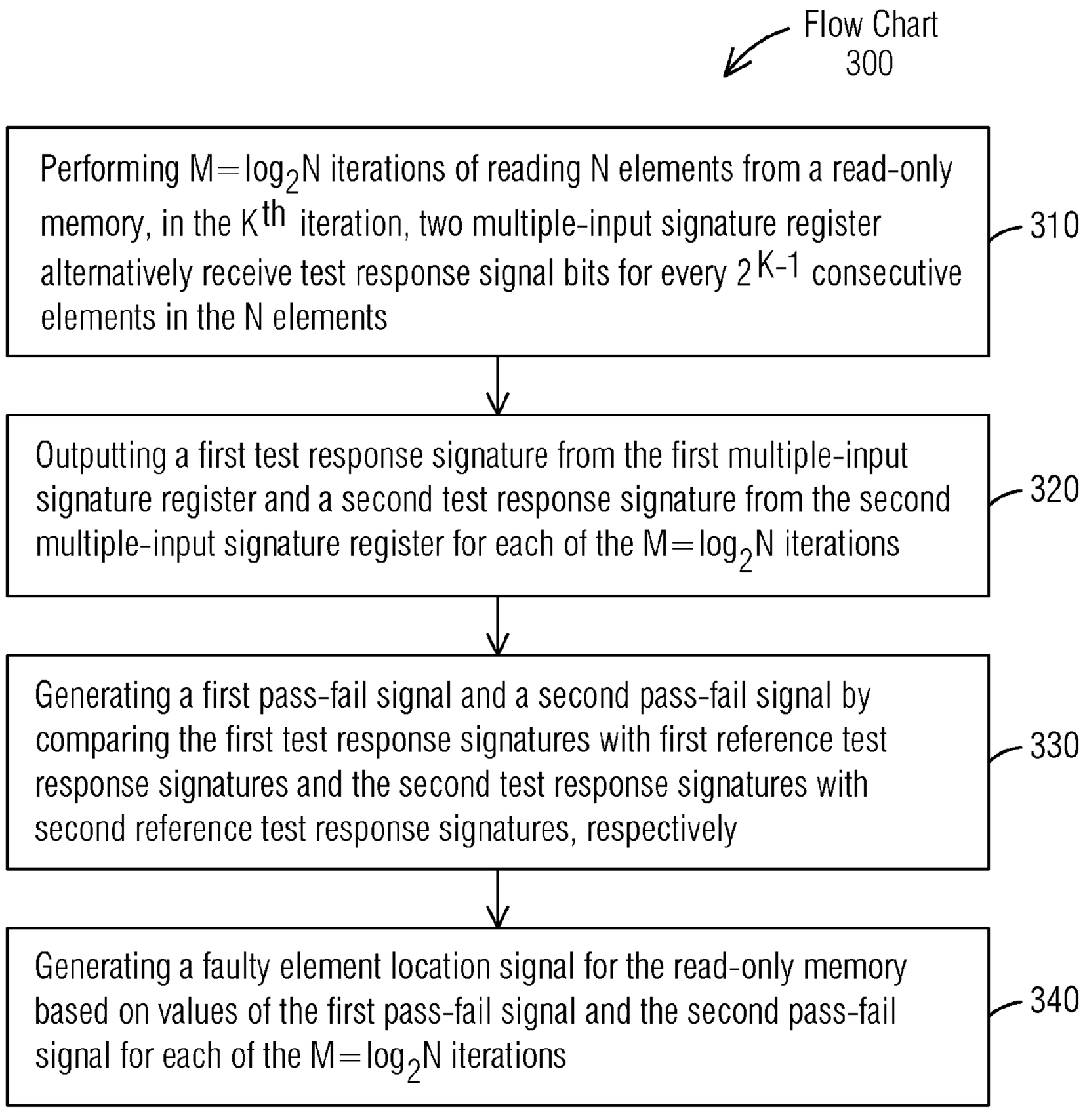
Publication Classification

(51) **Int. Cl.**
G11C 29/38 (2006.01)
G11C 29/44 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 29/38*** (2013.01); ***G11C 29/4401*** (2013.01)

(57) **ABSTRACT**

A testing circuit configured to test and diagnose a read-only memory comprises two multiple-input signature registers configured to generate two sets of signatures for multiple iterations of reading some or all of words stored in the read-only memory, control circuitry configured to control, according to a test algorithm, from which of the outputs of the read-only memory each of the two multiple-input signature registers receives test response signal bits for each of the reading operations during each of the iterations, and a faulty element location determination device configured to generate a faulty element location signal for the read-only memory based on results of comparing the two sets of signatures with reference signatures.



United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 4,969,148**

[45] **Date of Patent: Nov. 6, 1990**

[54] **SERIAL TESTING TECHNIQUE FOR EMBEDDED MEMORIES**

[75] Inventors: **Benoit Nadeau-Dostie,** Aylmer; **Allan Silburt,** Ottawa; **Vinod K. Agarwal,** Brossard, all of Canada

[73] Assignee: **Northern Telecom Limited,** Montreal, Canada

[21] Appl. No.: **319,979**

[22] Filed: **Mar. 7, 1989**

[51] **Int. Cl.**[5] **G06F 11/00**

[52] **U.S. Cl.** **371/21.1;** 371/22.5; 371/27

[58] **Field of Search** 371/21.1, 21.2, 21.3, 371/22.3, 22.2, 22.1, 22.5, 22.6, 25.1, 27; 365/201

[56] **References Cited**

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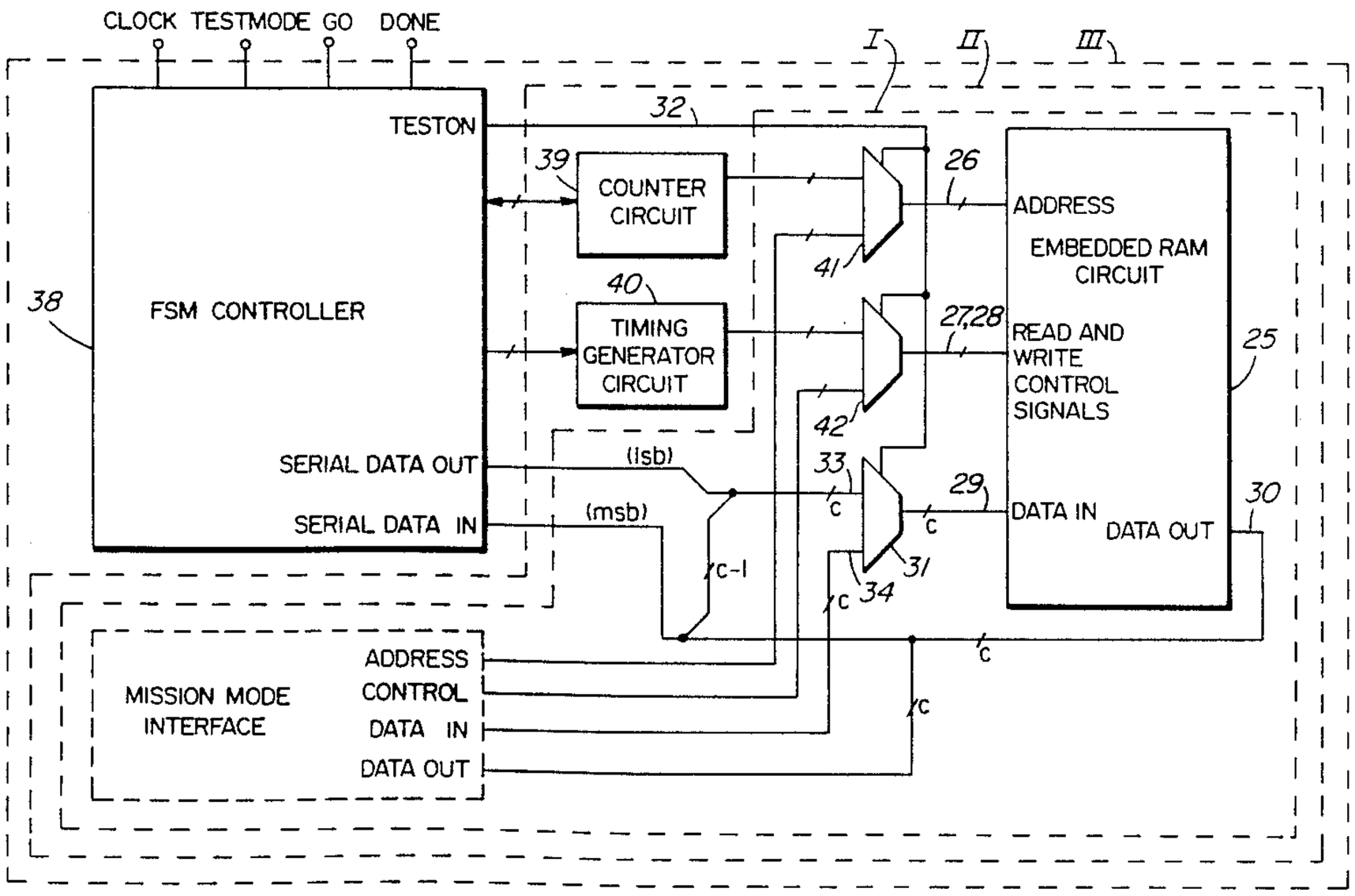
F. P. M. Beenker et al., "IEEE Design & Test", 12/1986, pp. 26–32.

Primary Examiner—Jerry Smith
Assistant Examiner—Robert W. Beausoliel
Attorney, Agent, or Firm—Philip W. Jones

[57] **ABSTRACT**

A testing circuit interfaces serially with the data path of an embedded memory circuit formed from at least one memory unit having separated data input and output lines and tandem addressing. Part of the testing circuit is a series of two-input multiplexer units which are adapted to be embedded on the same chip as the memory circuit. The outputs of the multiplexer units connect to a respective one of the data input lines of the memory circuit. Excepting the first bit position, a first input of each multiplexer unit is adapted to connect to the data output line of the adjacent bit position in the memory circuit. The second inputs of the multiplexer units are adapted to connect to the data bus of the chip. A further part of the testing circuit is a finite state machine which is adapted to connect to the first input of the multiplexer unit at the first bit position and to the data output line at the least bit position. During testing, the finite state machine actuates the multiplexer units to connect the first bits, and for each address outputs a series of test bits, shifts those bits through the addressed word by a series of read and write operations, and examines those bit after their passage through the addressed word for defects in the memory circuit at that address. The finite state machine may or may not be embedded on the same chip as the memory circuit.

9 Claims, 7 Drawing Sheets



United States Patent [19]

Wilcox et al.

[11] **Patent Number: 4,996,691**

[45] **Date of Patent: Feb. 26, 1991**

[54] **INTEGRATED CIRCUIT TESTING METHOD AND APPARATUS AND INTEGRATED CIRCUIT DEVICES FOR USE THEREWITH**

[75] Inventors: **Philip S. Wilcox**, Nepean; **Benoit Nadeau-Dostie**, Aylmer; **Vinod K. Agarwal**, Brossard, all of Canada

[73] Assignee: **Northern Telecom Limited**, Montreal, Canada

[21] Appl. No.: **247,258**

[22] Filed: **Sep. 21, 1988**

[51] **Int. Cl.**[5] **G06F 11/00**

[52] **U.S. Cl.** **371/68.1**; 371/15.1; 371/22.3; 371/24; 371/25.1

[58] **Field of Search** ..... 371/22.3, 68.1, 68.3, 371/71, 67.1, 25.1, 24, 22.1, 22.5, 22.6, 22.4, 15.1; 364/200 MS File, 900 MS File

[56] **References Cited**

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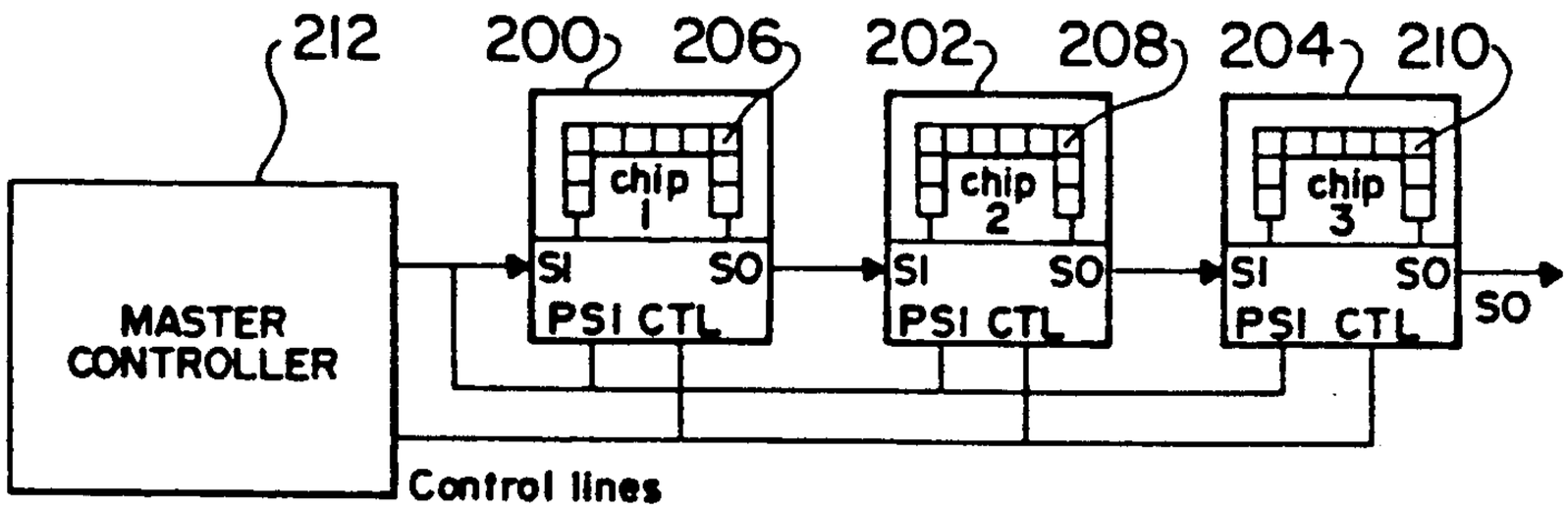
Primary Examiner—Jerry Smith
Assistant Examiner—Robert W. Beausoliel
Attorney, Agent, or Firm—Morrison Law Firm, Thomas Morrison

[57] **ABSTRACT**

In a so-called "scan-design" arrangement for testing integrated circuits, whether at the device level or at system level, problems associated with the storage and handling of vast amounts of data from increasingly complex devices are addressed by testing a pair of identical integrated circuits simultaneously and using the binary vector generated by scanning one of these integrated circuits as the reference against which to compare the binary vector produced by scanning the other integrated circuit. A plurality of "scan-designed" integrated circuits may be connected in series, possibly in a ring, and each compared with its predecessor. Zero-display coupling across each device may be employed to allow each successive integrated circuit to be compared with the same reference circuit in the chain or ring.

11 Claims, 1 Drawing Sheet



US005323400A

United States Patent [19]

Agarwal et al.

[11] **Patent Number: 5,323,400**

[45] **Date of Patent: Jun. 21, 1994**

[54] **SCAN CELL FOR WEIGHTED RANDOM PATTERN GENERATION AND METHOD FOR ITS OPERATION**

[75] Inventors: **Vinod Agarwal**, Brossard; **Benoit Nadeau-Dostie**, Aylmer, both of Canada; **Fidel Muradali**, Tokyo, Japan

[73] Assignee: **Northern Telecom Limited**, Montreal, Canada

[21] Appl. No.: **756,703**

[22] Filed: **Sep. 9, 1991**

[51] **Int. Cl.**[5] **H04B 17/00**

[52] **U.S. Cl.** **371/22.3**; 371/27

[58] **Field of Search** ..... 371/22.3, 27, 15.1, 371/22.1, 22.5, 22.6; 324/73.1, 158 R

[56] **References Cited**

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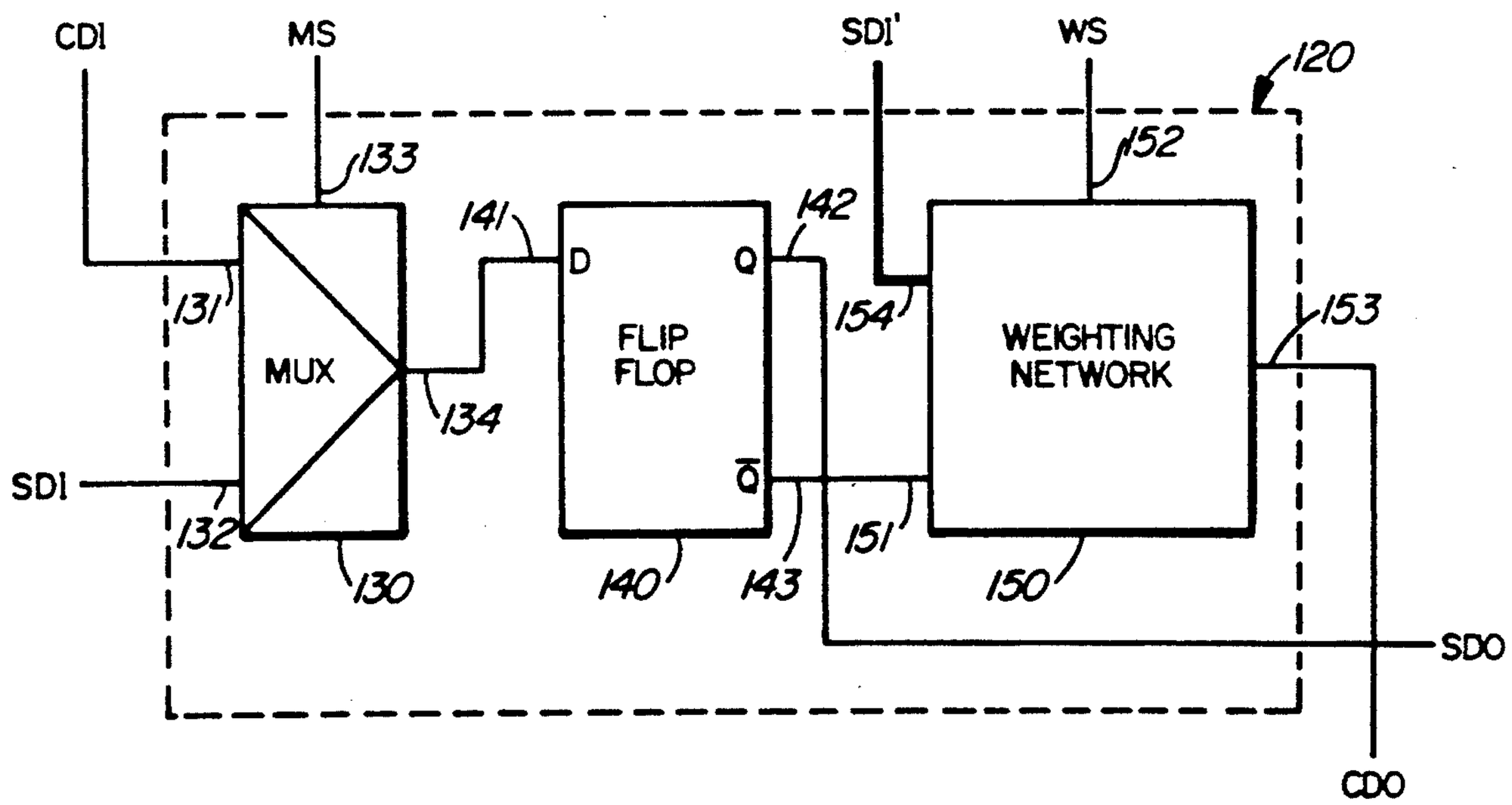
Primary Examiner—Robert W. Beausoliel, Jr.
Assistant Examiner—Phung M. Chung
Attorney, Agent, or Firm—C. W. Junkin

[57] **ABSTRACT**

A scan cell comprises a flip-flop, a mode selector and a weighting network. The mode selector responds to a mode-select signal by selectively applying a circuit data input signal or a scan data input signal to a data input of the flip-flop. The weighting network responds to one logic state of a weight-select signal by applying a circuit data signal substantially identical to a scan data output signal appearing at a scan data output of the flip-flop to a circuit data output. The weighting network responds to another logic state of the weightselect signal by applying a circuit data output signal having a predetermined ratio of occurrences of one logic state to occurrences of another logic state to the circuit data output. The scan cell is used for generating weighted random patterns in scan chains for scan testing digital systems.

15 Claims, 4 Drawing Sheets



US005349587A

United States Patent [19]

Nadeau-Dostie et al.

[11] Patent Number: 5,349,587

[45] Date of Patent: Sep. 20, 1994

[54] **MULTIPLE CLOCK RATE TEST APPARATUS FOR TESTING DIGITAL SYSTEMS**

[75] Inventors: **Benoit Nadeau-Dostie,** Aylmer; **Abu S. M. Hassan,** Nepean; **Dwayne M. Burek,** Nepean; **Stephen K. Sunter,** Nepean, all of Canada

[73] Assignee: **Northern Telecom Limited,** Montreal, Canada

[21] Appl. No.: **858,377**

[22] Filed: **Mar. 26, 1992**

[51] **Int. Cl.**[5] **A04B 17/00;** G01R 31/28

[52] **U.S. Cl.** **371/22.3;** 371/27

[58] **Field of Search** 371/22.3, 22.4, 22.5, 371/22.6, 27

[56] **References Cited**

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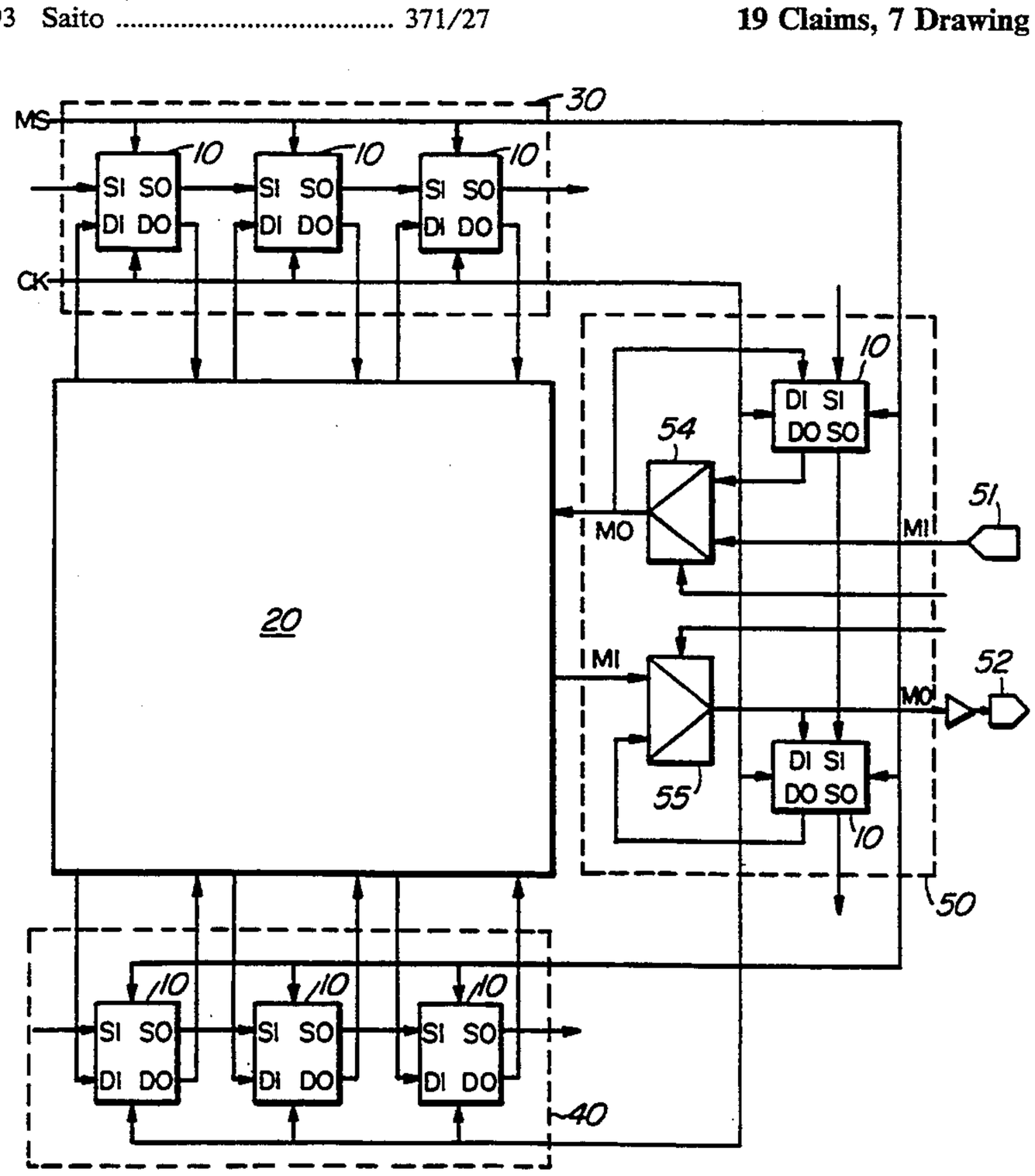
Primary Examiner—Robert W. Beausoliel, Jr.
Assistant Examiner—Joseph E. Palys
Attorney, Agent, or Firm—C. W. Junkin

[57] **ABSTRACT**

In methods and apparatus for testing a digital system, scannable memory elements of the digital system are configured in a scan mode in which the memory elements are connected to define a plurality of scan chains. A test stimulus pattern is clocked into each of the scan chains at a respective clock rate, at least two of the clock rates being different from one another. The memory elements of each scan chain are then configured in a normal operation mode in which the memory elements are interconnected by the combinational network for at least one clock cycle at a highest of the respective clock rates. The memory elements are then reconfigured in the scan mode, and a test response pattern is clocked out of each of the scan chains at its respective clock rate. The methods and apparatus are particularly useful for testing digital systems such as digital integrated circuits in which different memory elements are clocked at different rates during normal operation.

19 Claims, 7 Drawing Sheets



US005812469A

United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 5,812,469**

[45] **Date of Patent: Sep. 22, 1998**

[54] **METHOD AND APPARATUS FOR TESTING MULTI-PORT MEMORY**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-Francois Côté**, both of Aylmer, Canada

[73] Assignee: **Logic Vision, Inc.**, San Jose, Calif.

[21] Appl. No.: **775,856**

[22] Filed: **Dec. 31, 1996**

[51] **Int. Cl.**[6] **G11C 7/00**

[52] **U.S. Cl.** **365/201**; 365/230.05

[58] **Field of Search** 365/201, 230.05, 365/139.04, 220, 221; 371/21.1, 21.2, 25.1, 67.1

[56] **References Cited**

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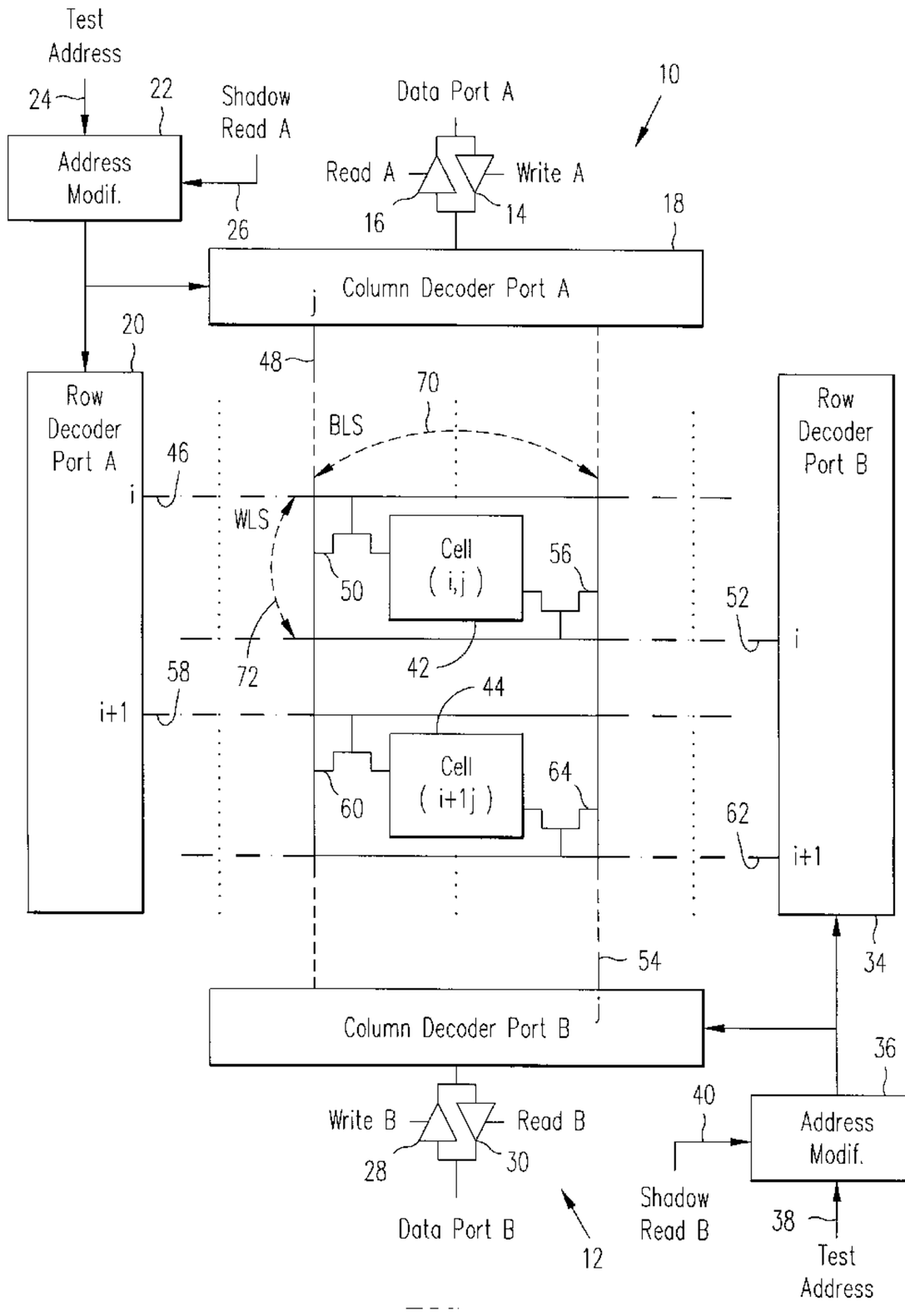
Primary Examiner—A. Zarabian

Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] **ABSTRACT**

A method of and apparatus for testing multi-port memory performs a shadow read to an adjacent memory cell concurrent with a write operation associated with typical read-write testing. In the presence of a bit wire short or a word wire short, the concurrent read of an adjacent memory cell will cause the value of that cell to be corrupted. The corrupted value is then found by the read-write testing. Consequently, the testing takes no longer than read-write testing. In addition, the testing scheme can be modified for memory with read only ports. An embodiment of the apparatus employs an exclusive OR gate on the least significant bit of the test row address line to generate the shadow read address.

4 Claims, 4 Drawing Sheets



US005900753A

United States Patent [19]

Côté et al.

[11] **Patent Number: 5,900,753**

[45] **Date of Patent: May 4, 1999**

[54] **ASYNCHRONOUS INTERFACE**

[75] Inventors: **Jean-Francois Côté** ; **Benoit Nadeau-Dostie**, both of Aylmer, Canada

[73] Assignee: **LogicVision, Inc.**, San Jose, Calif.

[21] Appl. No.: **08/825,446**

[22] Filed: **Mar. 28, 1997**

[51] **Int. Cl.**[6] **H03L 7/00**

[52] **U.S. Cl.** **327/145**; 327/144; 375/359; 371/22.1; 371/22.5; 371/22.36

[58] **Field of Search** 327/144, 145, 327/151, 99, 160; 371/22.1, 55, 22.5, 22.36; 375/354, 355, 359, 362; 395/551

[56] **References Cited**

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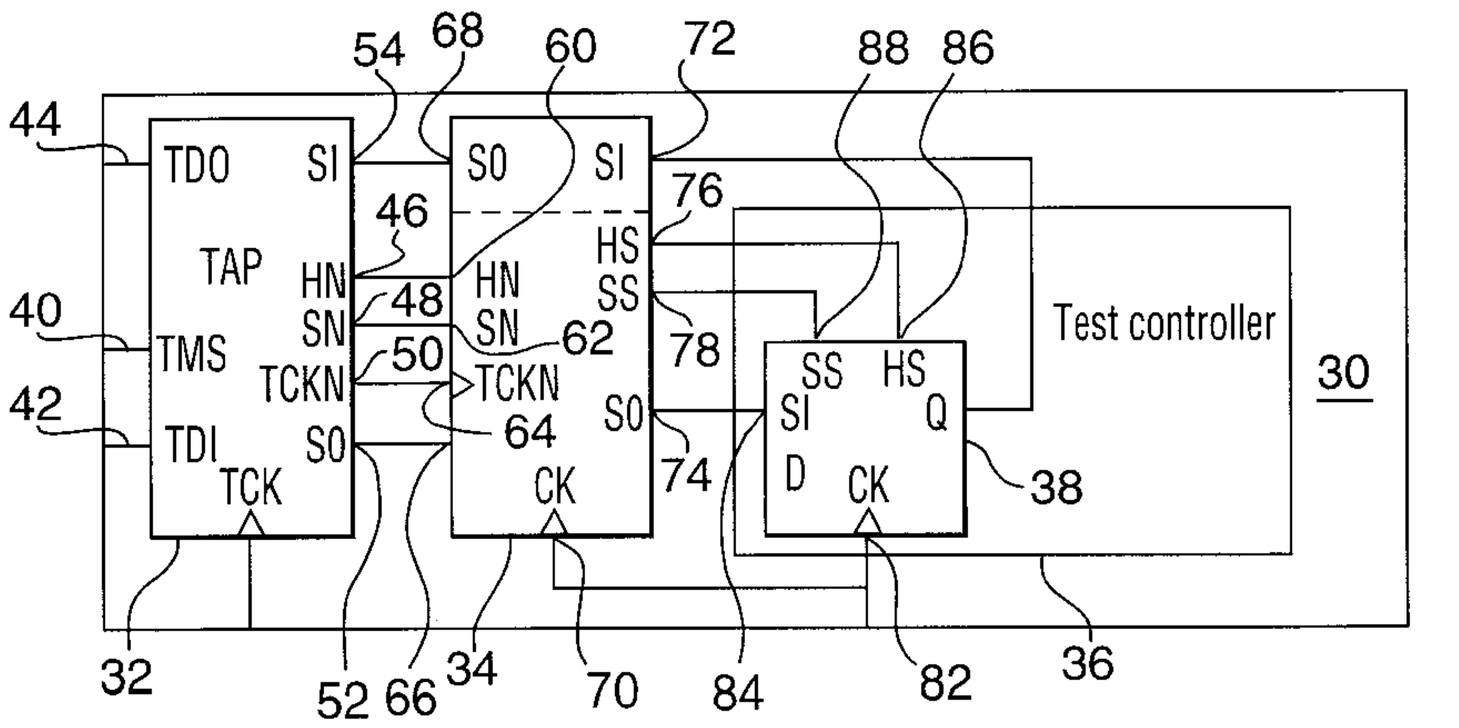
5,717,702	2/1998	Stokes et al.	371/22.35

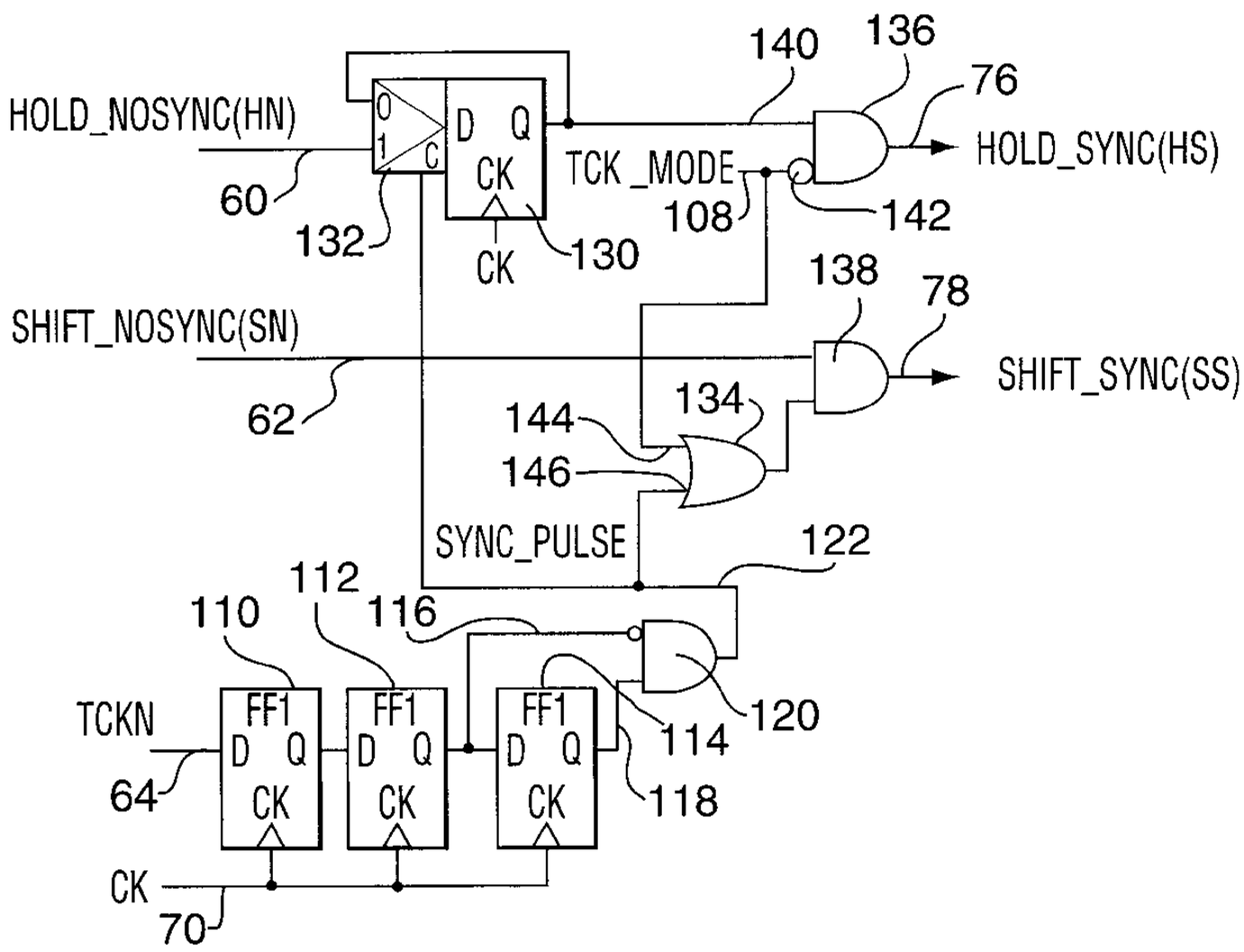
Primary Examiner—Timothy P. Callahan
Assistant Examiner—Jung Ho Kim
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP

[57] **ABSTRACT**

An interface allowing to transfer serial test data from a Test Access Port (TAP) to controllers located in several clock domains is described. The clock frequencies can be different from each other and do not need to be related in phase to each other or with the clock of the TAP. The interface is proven to work reliably as long as the clock frequencies used for the test controllers and registers is 3 times higher than the one of the TAP used to source the serial test data.

67 Claims, 8 Drawing Sheets





US005923676A

United States Patent [19]

Sunter et al.

[11] **Patent Number: 5,923,676**

[45] **Date of Patent: Jul. 13, 1999**

[54] **BIST ARCHITECTURE FOR MEASUREMENT OF INTEGRATED CIRCUIT DELAYS**

[75] Inventors: **Stephen K. Sunter**, Napean; **Benoit Nadeau-Dostie**, Québec, both of Canada

[73] Assignee: **Logic Vision, Inc.**, San Jose, Calif.

[21] Appl. No.: **08/771,302**

[22] Filed: **Dec. 20, 1996**

[51] **Int. Cl.**[6] **G06F 11/00**

[52] **U.S. Cl.** **371/22.5**

[58] **Field of Search** 371/22.5, 22.1, 371/25.1, 27, 28; 364/470; 365/227, 189.09

[56] **References Cited**

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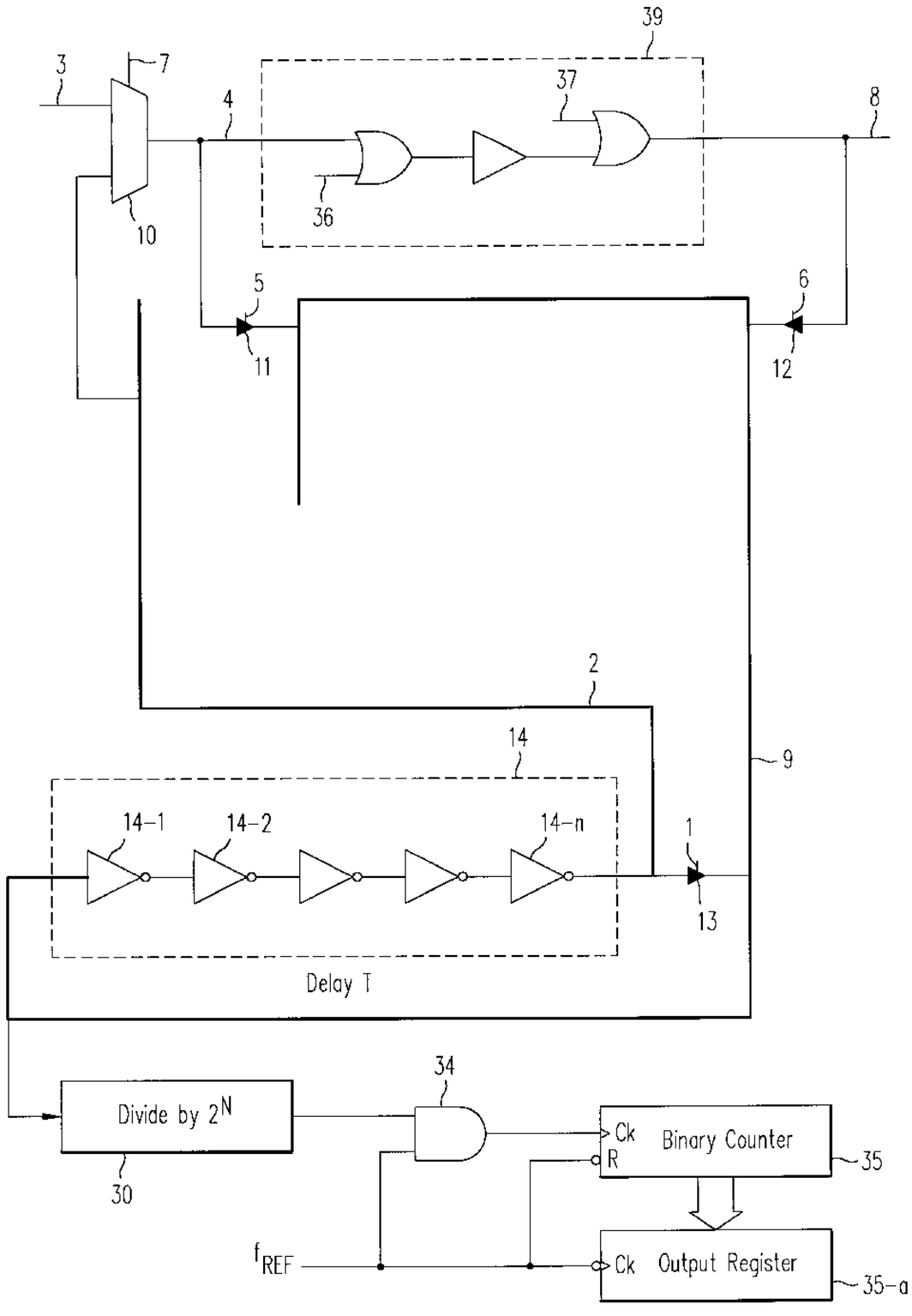
Primary Examiner—Vincent P. Canney

Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP

[57] **ABSTRACT**

A built-in self-test (BIST) method and apparatus for digital integrated circuits (ICs) and for systems including multiple ICs, measures signal propagation delays in combinational and sequential logic, set-up and hold times, and tri-state enable/disable times, from any circuit node to any other circuit node including pin-to-pin and from one IC to another. The IC under test is provided with two test bus conductors passing near every circuit node of interest and connected thereto by switches or buffers. During test, an oscillator is created including the test bus, a constant delay, counters, and a delay path of interest or a reference path. The delay path of interest may include e.g. an analog filter. The oscillation period of the oscillator when the reference path is selected is subtracted from the oscillation period when the oscillator includes a delay path of interest. A circuit automatically accommodates inverting and non-inverting paths. A delay copier copies the delay between any two signal events, without injecting any test signal into the circuit under test (e.g. on-line test), and the delay copy can be measured by selecting it in the oscillator.

31 Claims, 18 Drawing Sheets



US006000051A

United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 6,000,051**

[45] **Date of Patent: Dec. 7, 1999**

[54] **METHOD AND APPARATUS FOR HIGH-SPEED INTERCONNECT TESTING**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-Francois Côté** , both of Aylmer, Canada

[73] Assignee: **Logic Vision, Inc.**, San Jose, Calif.

[21] Appl. No.: **08/948,842**

[22] Filed: **Oct. 10, 1997**

[51] **Int. Cl.**[6] **G01R 31/28**

[52] **U.S. Cl.** **714/727**; 714/731; 327/144

[58] **Field of Search** 714/731, 727, 714/726, 724, 729, 733, 734, 814, 815, 30; 327/144, 141; 377/77, 78, 81

[56] **References Cited**

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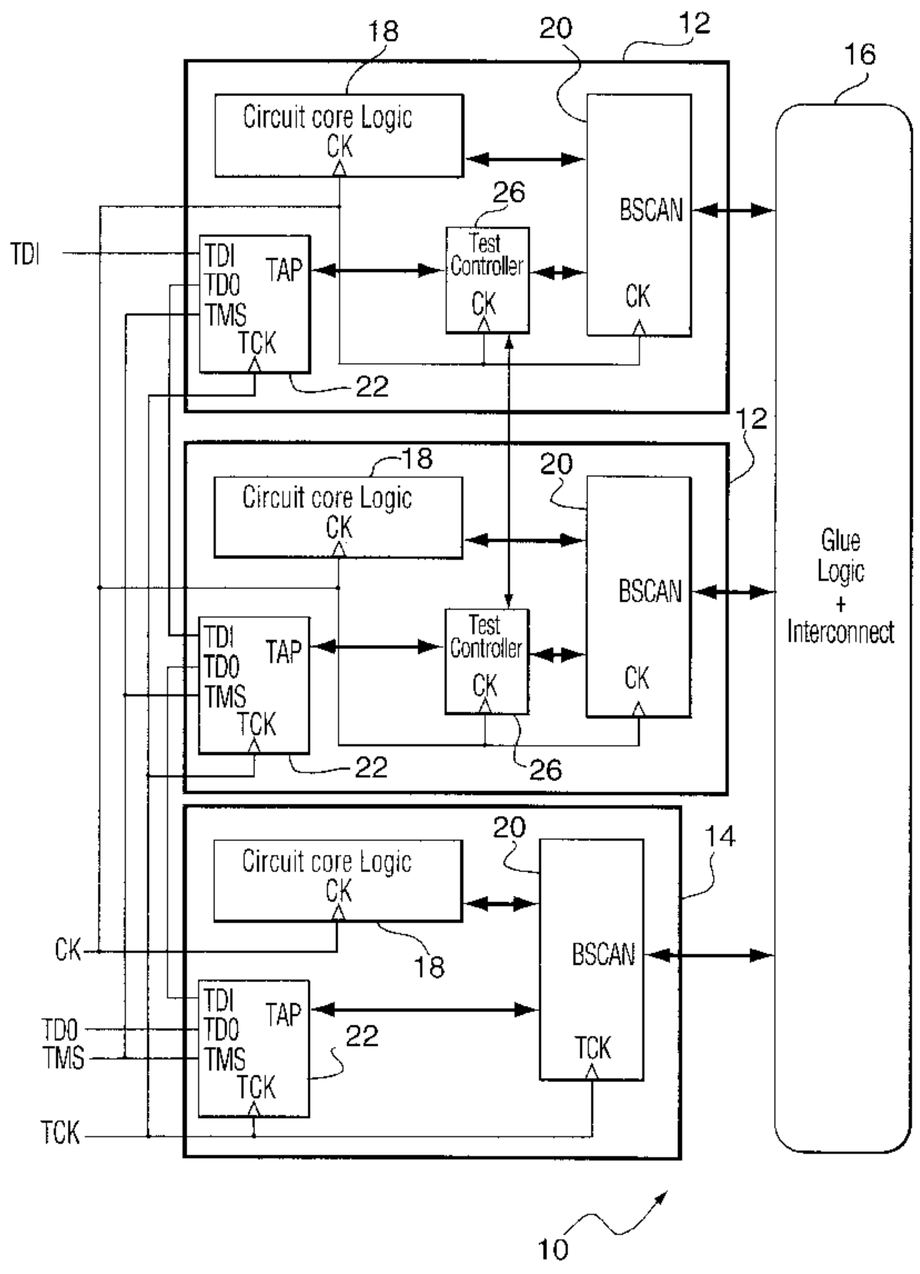
Primary Examiner—Trinh L. Tu

Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] **ABSTRACT**

A method of testing high speed interconnectivity of circuit boards having components operable at a high speed system clock, employing an IEEE 1149.1 standard test method in which test data is shifted into and from the components at the rate of a test clock during Shift_In and Shift_Out operations, and having an Update operation and a Capture operation between the Shift_In and Shift_Out operations, the components including a first group of components capable of performing the Update and Capture operations at the rate of the Test Clock only and a second group of components capable of performing the Update and Capture operations at the rate of the system clock, the method comprising the steps of performing the Shift_In operation in all of the components concurrently at the rate of the Test Clock; performing the Update and Capture Operations in the first group of components at the rate of the Test Clock; and performing the Update and Capture Operations in the second group of components at the rate of the system Clock. The method employs a novel integrated circuit, test controller and boundary scan cells.

43 Claims, 8 Drawing Sheets



US006046946A

United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 6,046,946**

[45] **Date of Patent: Apr. 4, 2000**

[54] **METHOD AND APPARATUS FOR TESTING MULTI-PORT MEMORY USING SHADOW READ**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-François Côté**, both of Aylmer, Canada

[73] Assignee: **Logic Visions, Inc.**, San Jose, Calif.

[21] Appl. No.: **09/047,233**

[22] Filed: **Mar. 25, 1998**

Related U.S. Application Data

[63] Continuation of application No. 08/775,856, Dec. 31, 1996, Pat. No. 5,812,469.

[51] **Int. Cl.**[7] **G11C 7/00**

[52] **U.S. Cl.** **365/201**; 365/230.05

[58] **Field of Search** 365/201, 230.05, 365/189.04, 220, 221; 371/21.1, 21.2

[56] **References Cited**

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B. Nadie–Dostie et al., "Serial Interfacing for Embedded–Memory Testing" IEEE Design and Test of Computers, Apr. 1990, pp. 52–63.

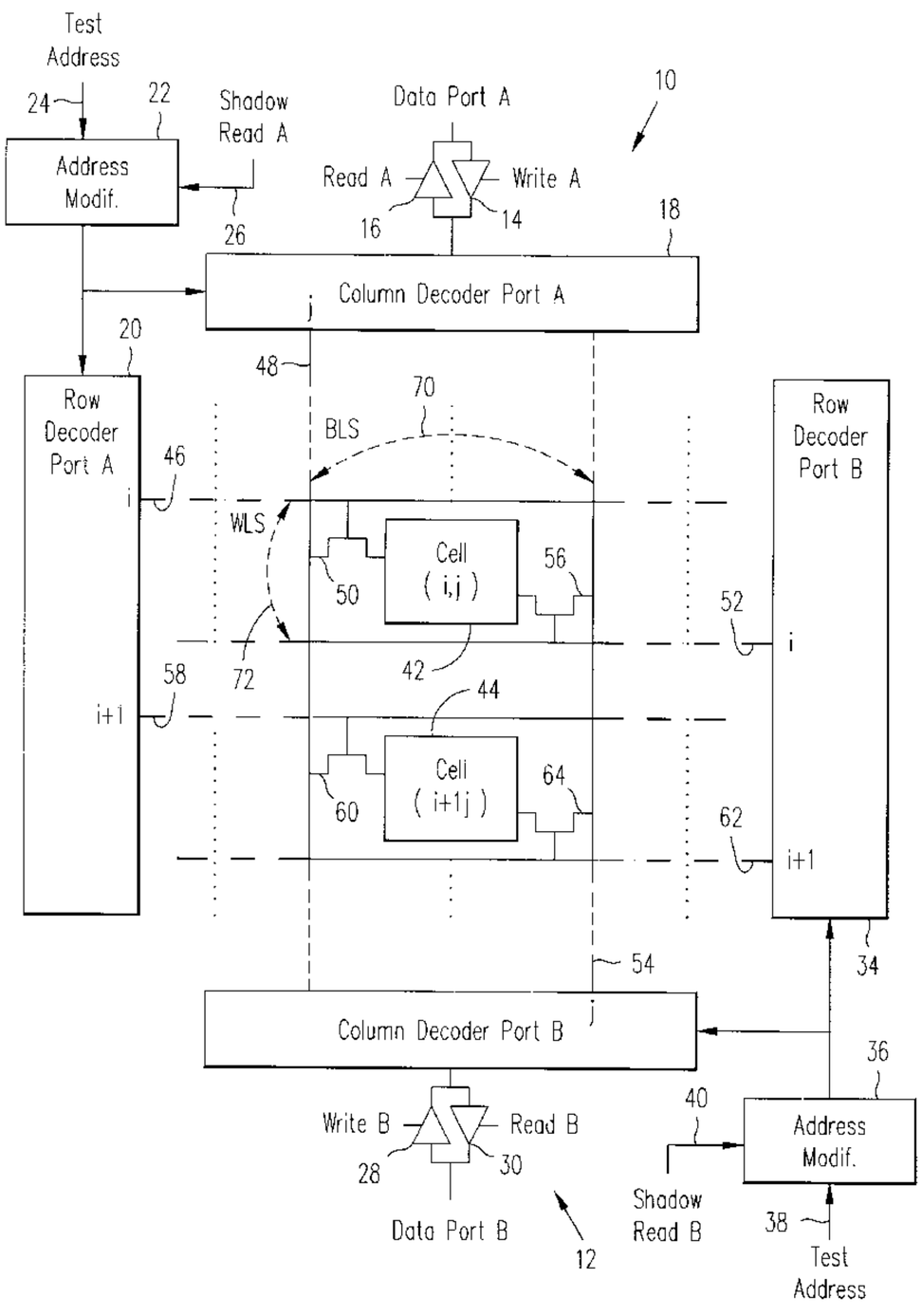
Primary Examiner—A. Zarabian

Attorney, Agent, or Firm—Skjerven, Morrill MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] **ABSTRACT**

A method of and apparatus for testing multi-port memory performs a shadow read to an adjacent memory cell concurrent with a write operation associated with typical read-write testing. In the presence of a bit wire short or a word wired short, the concurrent read of an adjacent memory cell will cause the value of that cell to be corrupted. The corrupted value is then found by the read-write testing. Consequently, the testing takes no longer than read-write testing. In addition, the testing scheme can be modified for memory with read only ports. An embodiment of the apparatus employs and exclusive OR gate on the least significant bit of the test row address line to generate the shadow read address.

21 Claims, 4 Drawing Sheets



US006115827A

United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 6,115,827**

[45] **Date of Patent: Sep. 5, 2000**

[54] **CLOCK SKEW MANAGEMENT METHOD AND APPARATUS**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-François Cote**, both of Aylmer, Canada

[73] Assignee: **LogicVision, Inc.**, San Jose, Calif.

[21] Appl. No.: **09/209,790**

[22] Filed: **Dec. 11, 1998**

[30] **Foreign Application Priority Data**

Dec. 29, 1997 [CA] Canada 2225879

[51] **Int. Cl.**[7] **G06F 1/04**

[52] **U.S. Cl.** **713/503**; 713/502

[58] **Field of Search** 713/500, 501, 713/502, 503

[56] **References Cited**

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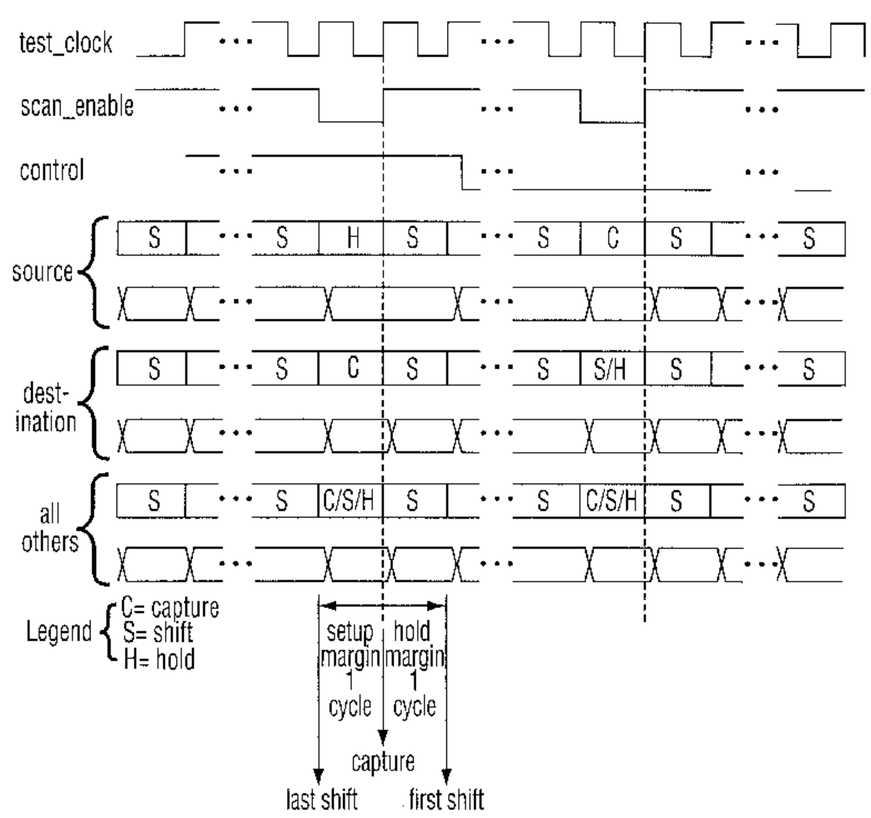
(List continued on next page.)

Primary Examiner—William Grant
Assistant Examiner—Ronald D Hartman, Jr.
Attorney, Agent, or Firm—Fields and Johnson, P.C.

[57] **ABSTRACT**

A method of testing an integrated circuit having core logic with two or more clock domains and at least one signal path originating in one clock domain and terminating in an other clock domain, each signal path having a source control element in the one clock domain and an associated destination control element in the other clock domain, each the control element being a scannable memory element, the method comprising the steps of, for each the control element shifting a test stimulus into all scannable elements in the core logic; placing an associated source control element in a hold mode for a predetermined number of clock cycles prior to a capture operation so that the source control element holds its output constant during the predetermined number of clock cycles; performing a capture operation for capturing the data output in response to the test stimulus by the control element and by all other scannable elements which are not control elements; maintaining an associated source control element in a hold mode for a predetermined number of clock cycles following a capture operation so that the source control element holds its output constant during the predetermined number of clock cycles; shifting out data captured in the capturing step; and analyzing the data captured in the capturing step. An integrated circuit for use with the method comprises a source control element and an associated destination control associated with each signal path for exchanging data between the one and the other of the clock domains, the source control element being located in the one clock domain and the associated destination element being located in the other domain; each control element being a scannable memory element having an input and an output and being configurable a SHIFT mode for shifting data from its input to its output and a CAPTURE mode for capturing data applied its input, each the source control element being further configurable in a HOLD mode for holding its output constant; and the control elements being configurable in the modes in response to predetermined combinations of a Scan Enable signal for enabling or disabling shifting of data therethrough and a Capture Disable signal having a one value to cause a recipient control element to enable the capture mode and another value to cause a recipient control element to suppress the capture mode.

43 Claims, 12 Drawing Sheets



US006145105A

United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 6,145,105**

[45] **Date of Patent: Nov. 7, 2000**

[54] **METHOD AND APPARATUS FOR SCAN TESTING DIGITAL CIRCUITS**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-François Côté** , both of Aylmer; **Dwayne Burek**, Nepean, all of Canada

[73] Assignee: **LogicVision, Inc.**, San Jose, Calif.

[21] Appl. No.: **09/192,839**

[22] Filed: **Nov. 16, 1998**

Related U.S. Application Data

[63] Continuation of application No. 08/752,499, Nov. 20, 1996.

[51] **Int. Cl.**[7] **G01R 31/28**

[52] **U.S. Cl.** **714/726**

[58] **Field of Search** 714/726, 727, 714/728, 733, 736, 30; 324/765

[56] **References Cited**

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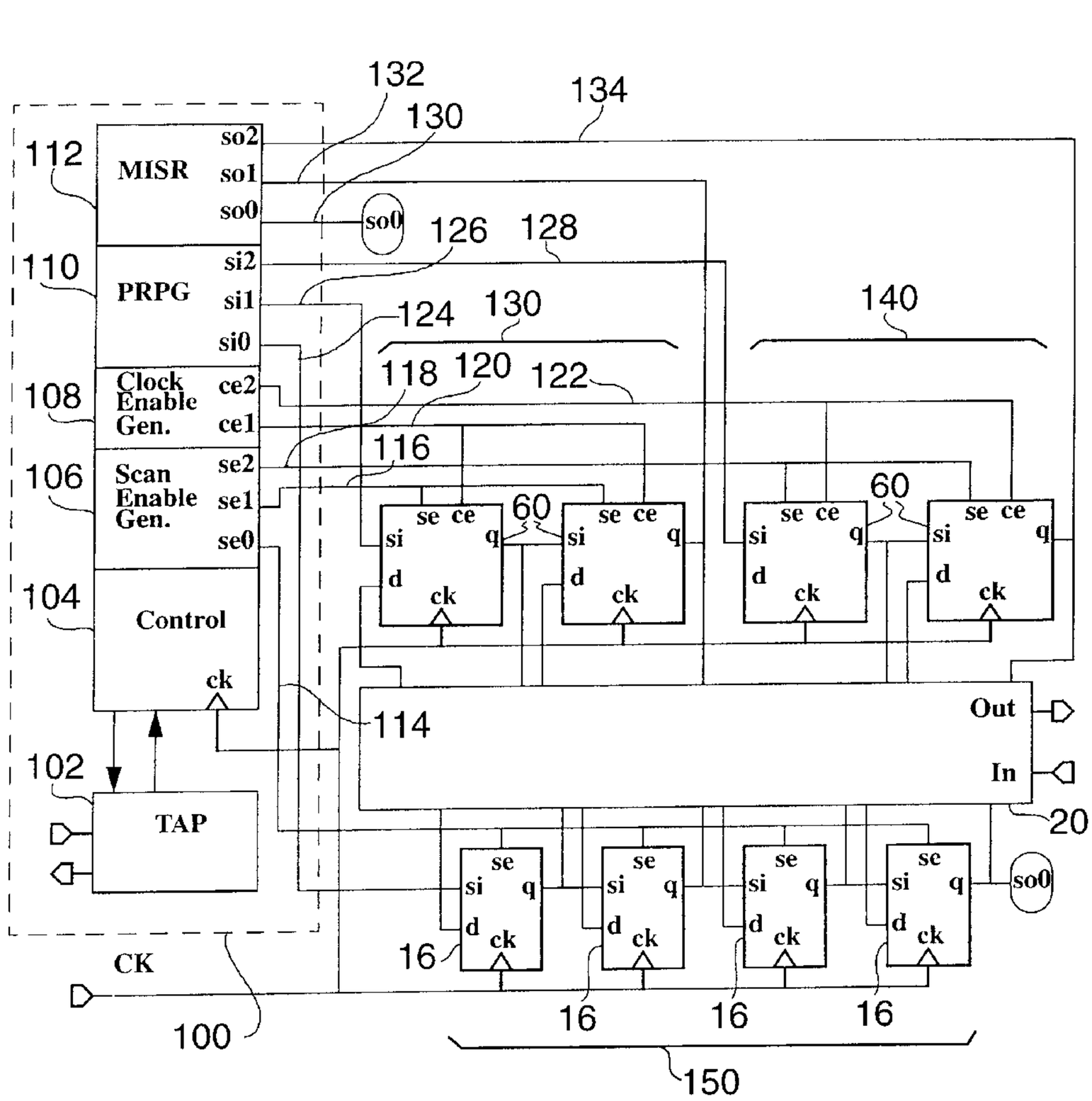
Primary Examiner—Albert De Cady
Assistant Examiner—Jason Greene
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] **ABSTRACT**

A method and digital system for testing scannable memory and combinational networks. The scannable memory is configurable into several scan chains. Each chain may have a different effective clock rate, as determined by respective clock enable signals. The method and digital system allow scan testing of digital circuits that use a single operational clock rate and several functional clock enable signals to effect slower lock operating rates. The digital system includes memory elements having scan enable and clock enable inputs.

28 Claims, 9 Drawing Sheets



US006327684B1

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,327,684 B1**
(45) **Date of Patent: *Dec. 4, 2001**

(54) **METHOD OF TESTING AT-SPEED CIRCUITS HAVING ASYNCHRONOUS CLOCKS AND CONTROLLER FOR USE THEREWITH**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer; **Naader Hasani**, Ottawa; **Jean-François Coté**, Aylmer, all of (CA)

(73) Assignee: **Logicvision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/309,827**

(22) Filed: **May 11, 1999**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/731**
(58) **Field of Search** 714/726, 727, 714/729, 731

(56) **References Cited**

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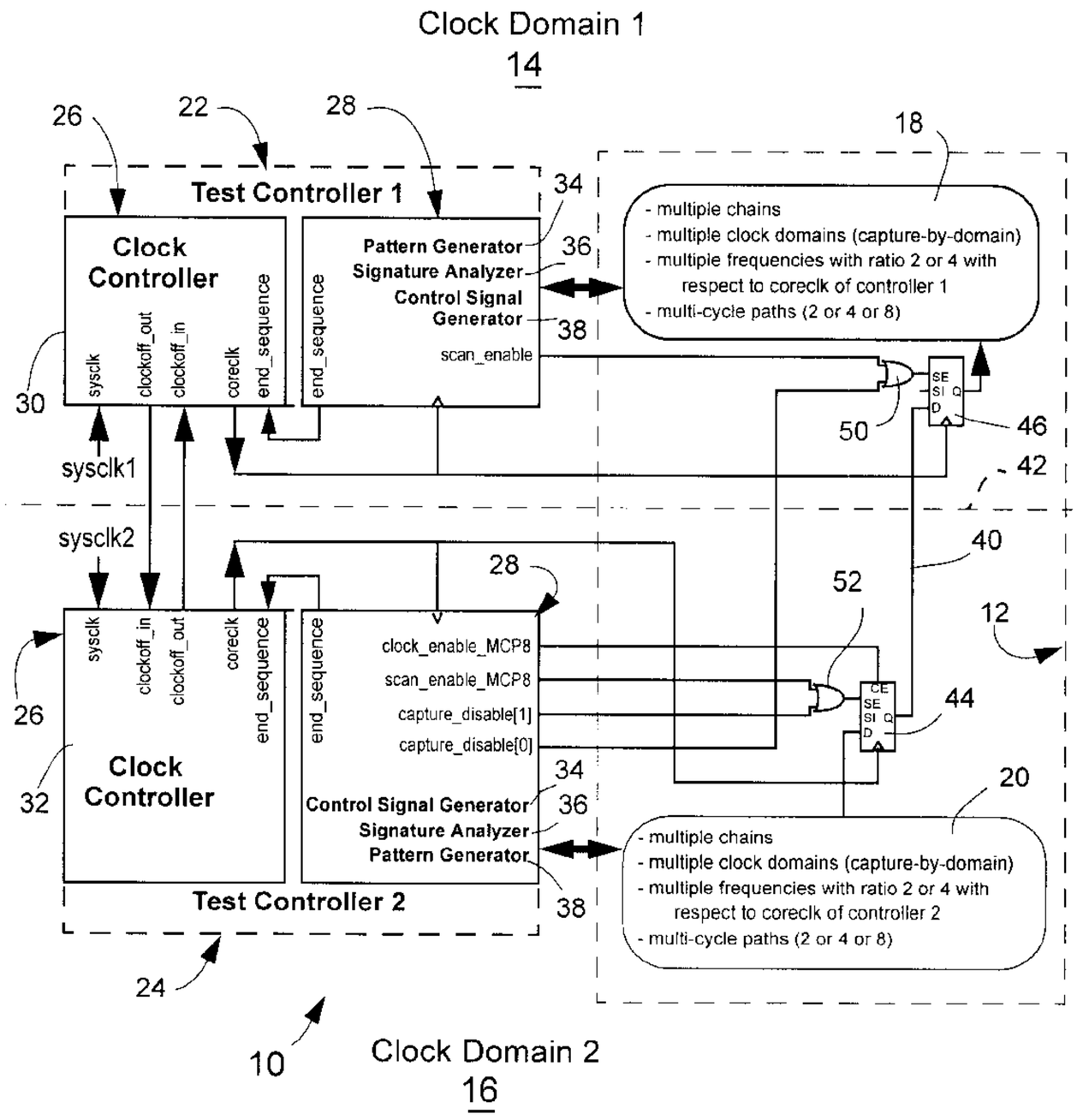
Primary Examiner—Albert Decady
Assistant Examiner—Joseph D. Torres
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A method of testing the core logic in a digital system, the method having a sequence of test operations including a shift-in operation in which a test stimulus is shifted into scanable memory elements in the core logic, a capture operation in which data in the memory elements is captured, and a shift-out operation in which captured data is shifted out of the core logic for analysis, comprises the improvement of, for each the test operation, concurrently enabling the domain clock of each clock domain in the core logic at the beginning of each test operation, performing the test operation in each domain and disabling the domain clock at the end of each test operation in each domain. The method allows all of the clock domains, including signal paths which traverse domain boundaries and/or have multi-cycle paths to be tested concurrently and at their respective functional clock rate of each clock.

31 Claims, 3 Drawing Sheets



US006330681B1

(12) **United States Patent**
Cote et al.

(10) **Patent No.: US 6,330,681 B1**
(45) **Date of Patent: Dec. 11, 2001**

(54) **METHOD AND APPARATUS FOR CONTROLLING POWER LEVEL DURING BIST**

(75) Inventors: **Jean-François Cote**; **Benoit Nadeau-Dostie**; **Pierre Gauthier**, all of Aylmer (CA)

(73) Assignee: **Logicvision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/218,764**

(22) Filed: **Dec. 22, 1998**

(30) **Foreign Application Priority Data**

Dec. 31, 1997 (CA) 2226061

(51) **Int. Cl.**[7] **G06F 1/32**
(52) **U.S. Cl.** **713/322**; 713/601
(58) **Field of Search** 713/322, 501, 713/601; 702/117; 714/718, 719, 724, 733, 735

(56) **References Cited**

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5,614,838		3/1997	Jaber et al.	324/765
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Primary Examiner—Thomas M. Heckler
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

An improvement in a method of testing a digital circuit or system, having a plurality of scannable memory elements, in accordance with conventional BIST methods in which, at a reference clock, a test stimulus is shifted into the memory elements, the response of the elements is captured and the captured data is shifted out of the elements and analyzed, the improvement comprising controlling the average power consumption of the circuit during the test by suppressing clock pulses from the reference clock during phases of the test that do not require the maximum level of activity or in which the performance of the circuit is not to be evaluated; and, suppressing no clock pulses from the reference clock in phases of the test in which the performance of the circuit is to be evaluated, so that the conditions are substantially as those of normal mode of operation of the circuit.

23 Claims, 3 Drawing Sheets

US006363520B1

(12) **United States Patent**
Boubezari et al.

(10) **Patent No.: US 6,363,520 B1**
(45) **Date of Patent: Mar. 26, 2002**

(54) **METHOD FOR TESTABILITY ANALYSIS AND TEST POINT INSERTION AT THE RT-LEVEL OF A HARDWARE DEVELOPMENT LANGUAGE (HDL) SPECIFICATION**

(75) Inventors: **Samir Boubezari**, Mountain View, CA (US); **Eduard Cerny**; **Bozena Kaminska**, both of Montreal (CA); **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/098,555**

(22) Filed: **Jun. 16, 1998**

(51) **Int. Cl.**[7] **G06F 17/50**; G06F 17/10; G06F 7/60

(52) **U.S. Cl.** **716/18**; 716/2; 716/4

(58) **Field of Search** 716/18, 4

(56) **References Cited**

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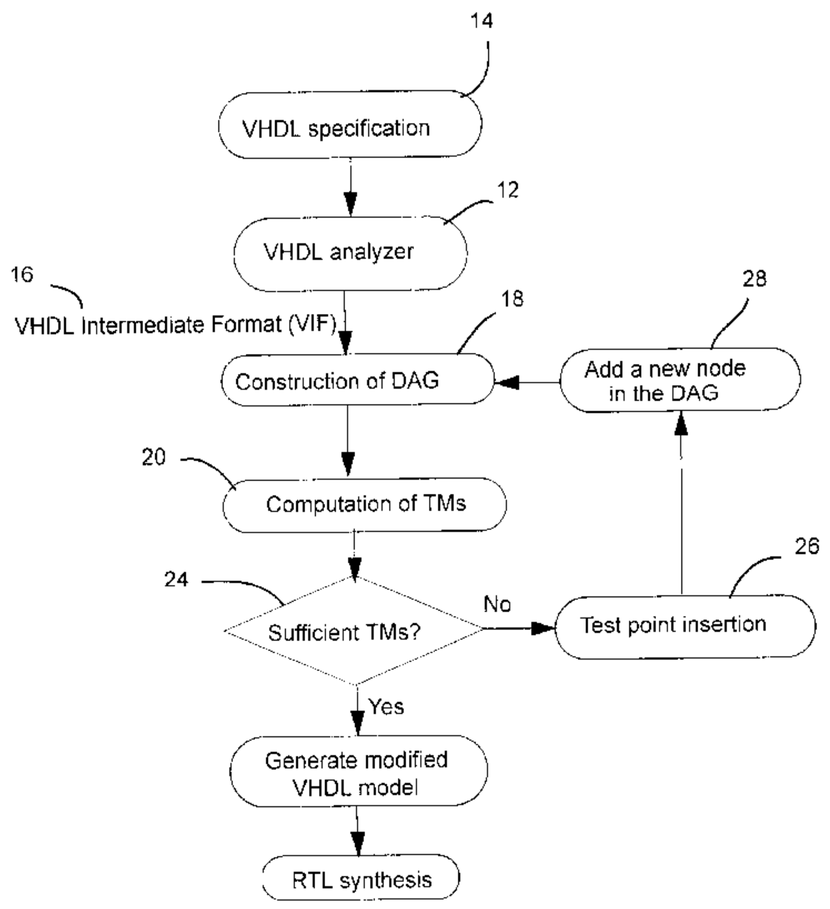
Primary Examiner—Matthew Smith
Assistant Examiner—A. M. Thompson
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A method is provided for producing a synthesizable RT-Level specification, having a testability enhancement from a starting RT-Level specification representative of a circuit to be designed, for input to a synthesis tool to generate a gate-level circuit. The method includes the steps of performing a testability analysis on a Directed Acyclic Graph by computing and propagating Testability Measures forward and backward through VHDL statements, identifying the bits of each signal and/or variable, and adding test point statements into the specification at the RT-Level to improve testability of the circuit to be designed. The computation of Controllability and Observability method is purely functional, and does not subsume the knowledge of a gate-level implementation of the circuit being analyzed.

36 Claims, 7 Drawing Sheets



US006442722B1

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,442,722 B1**
(45) **Date of Patent: Aug. 27, 2002**

(54) **METHOD AND APPARATUS FOR TESTING CIRCUITS WITH MULTIPLE CLOCKS**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **David P. Buck**, San Francisco, CA (US)

(73) Assignee: **Logicvision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/430,686**

(22) Filed: **Oct. 29, 1999**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/731**; 714/729
(58) **Field of Search** 714/726, 729, 714/731

(56) **References Cited**

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(List continued on next page.)

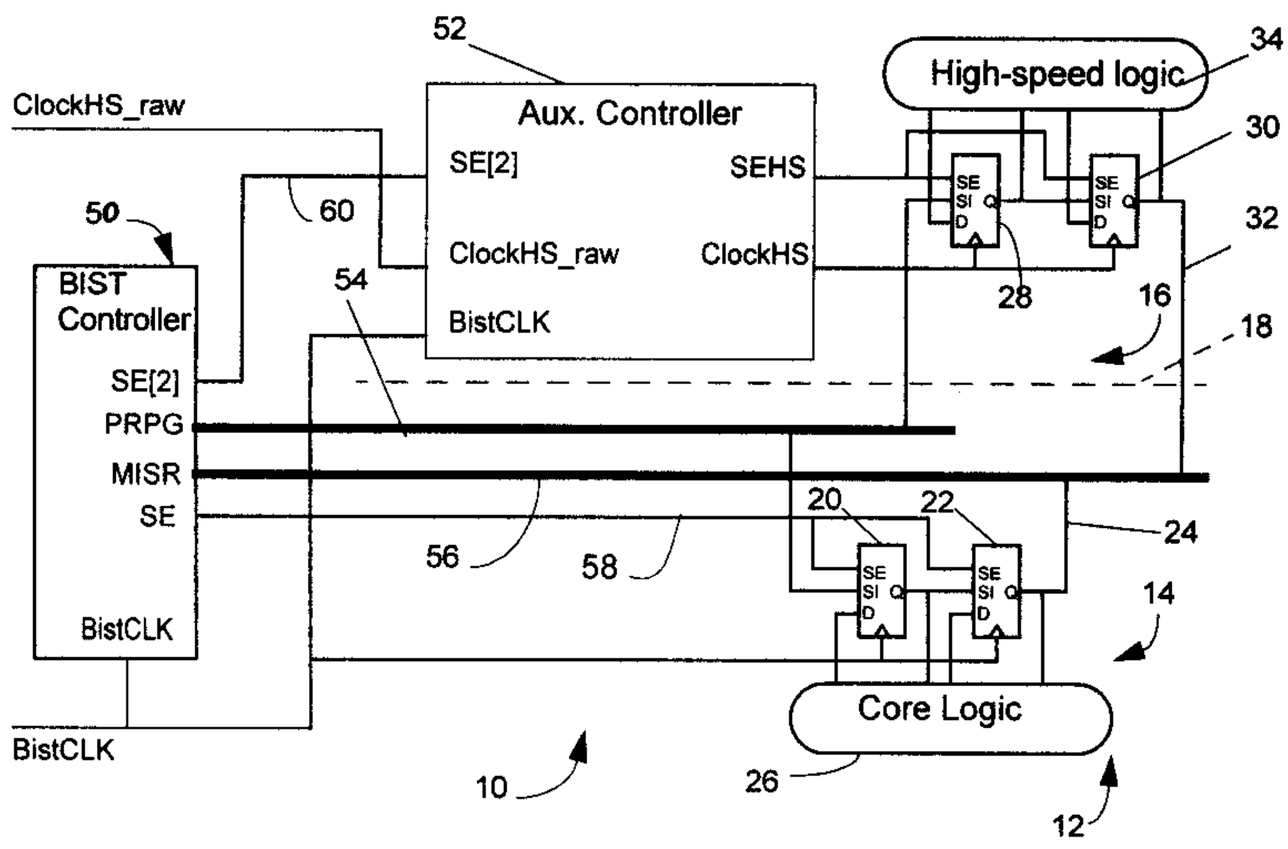
Primary Examiner—Albert Decady
Assistant Examiner—Joseph D. Torres

(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A method of testing a circuit having two or more clock domains at respective domain test clock rates and under control of a main test clock signal, the circuit having core logic, a plurality of scannable memory elements, each having a clock input, an input connected to an output of the core logic and/or an output connected to an input to the core logic, and configurable in scan mode in which the memory elements are connected to define one or more scan chains in each domain and in normal mode in which the memory elements are connected to the core logic in normal operational mode, the method comprising configuring the memory elements in scan mode; concurrently clocking a test stimulus into each scan chain of each clock domain including, for each clock domain having a domain test clock signal which is synchronous with respect to the main test clock signal, clocking the test stimulus at a shift clock rate derived from the main test clock signal and, for each clock domain having a domain test clock signal which is asynchronous with respect to the main test clock signal, clocking all but a predetermined number of bits of the test stimulus at a first domain shift clock rate derived from the main test clock signal followed by clocking the predetermined number of bits of the test stimulus at a second domain shift clock rate corresponding to the domain test clock rate; configuring the memory elements of each scan chain in normal mode in which the memory elements of each scan chain are interconnected by the core logic in the normal operational mode; clocking each memory element in each scan chain at its respective domain test clock rate for at least one clock cycle thereof; configuring the memory elements in scan mode; and clocking a test response pattern out of each of the scan chains at its respective domain shift clock rate during a respective scan-out interval, all respective scan-out intervals overlapping in time for a plurality of clock cycles at the highest of the respective clock rates.

34 Claims, 12 Drawing Sheets



US006457161B1

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,457,161 B1**
(45) **Date of Patent: Sep. 24, 2002**

(54) **METHOD AND PROGRAM PRODUCT FOR MODELING CIRCUITS WITH LATCH BASED DESIGN**

(76) Inventors: **Benoit Nadeau-Dostie**, 17 Croissant de la Paix, Aylmer, Quebec (CA), J9H 3X7; **Fadi Maamari**, 1038 Camino Ricardo, San Jose, CA (US) 95125; **Dwayne Burek**, 5649 Le Fevre Dr., San Jose, CA (US) 95118

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 64 days.

(21) Appl. No.: **09/817,298**

(22) Filed: **Mar. 27, 2001**

(51) **Int. Cl.**[7] **G06F 17/50**
(52) **U.S. Cl.** **716/6**; 716/3
(58) **Field of Search** 716/6, 3, 5, 21

(56) **References Cited**

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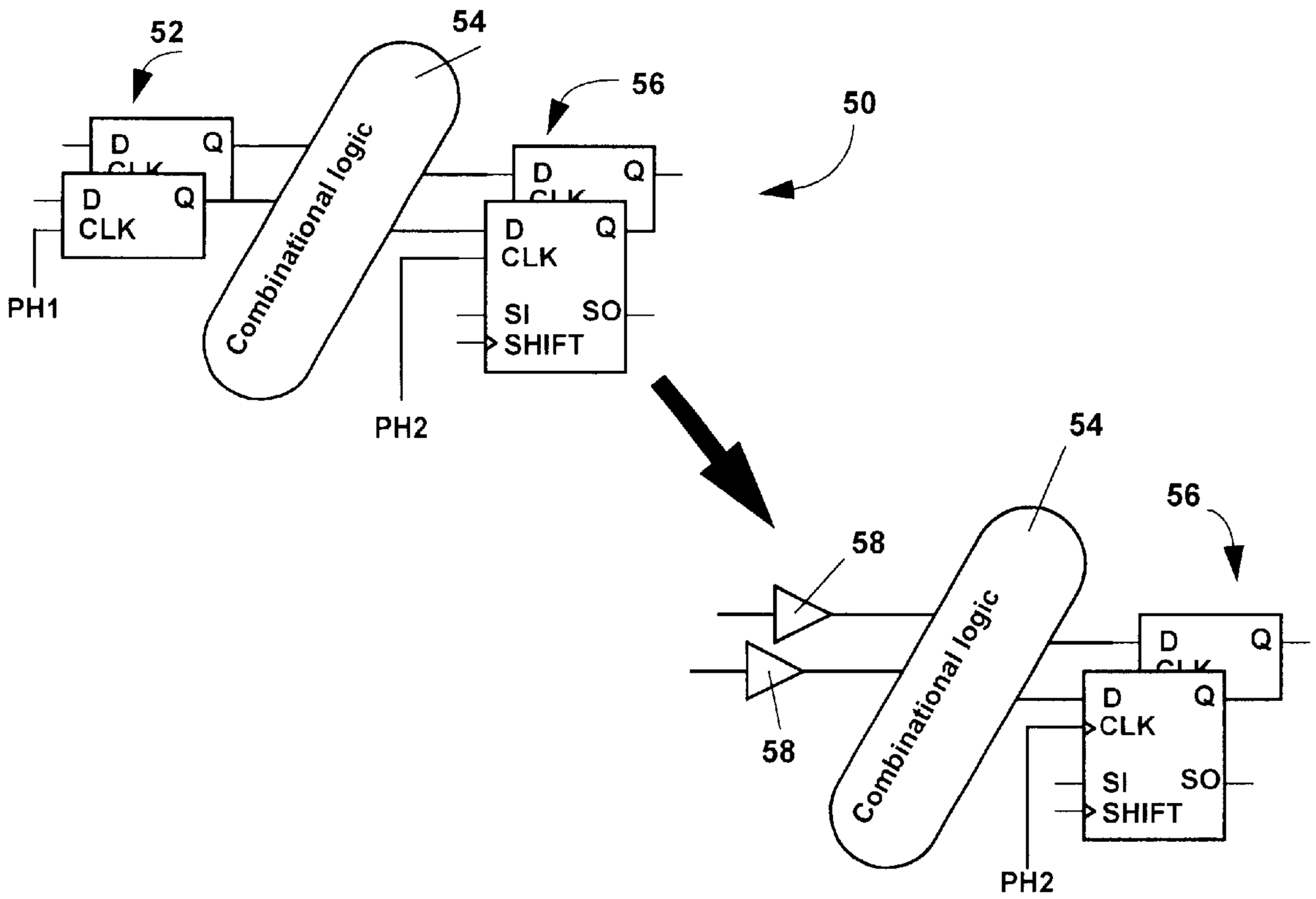
Primary Examiner—Timothy P. Callahan
Assistant Examiner—Cassandra Cox
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method of and computer program product for modeling a logic circuit having combinational logic and latches, in which the latches are clocked by one of a first clock phase, a second clock phase or a pulse derived from the second clock phase, a subset of latches being scannable, comprises, for each latch in the logic circuit, associating the latch with one of the first and second clock phase; and when latch is associated with the first clock phase, modeling the latch as a buffer connected between the data input and output of latch; and when the latch is associated with the second clock phase, modeling the latch as an edge-triggered flip-flop having the same data input, data output and clock input as the latch.

25 Claims, 4 Drawing Sheets



US006487688B1

(12) **United States Patent**
Nadeau-Dostie

(10) **Patent No.: US 6,487,688 B1**
(45) **Date of Patent: Nov. 26, 2002**

(54) **METHOD FOR TESTING CIRCUITS WITH TRI-STATE DRIVERS AND CIRCUIT FOR USE THEREWITH**

(75) Inventor: **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: **Logicvision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/472,386**

(22) Filed: **Dec. 23, 1999**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/726**; 714/727
(58) **Field of Search** 379/106.06; 714/222, 714/726, 724, 727, 729, 730, 743

(56) **References Cited**

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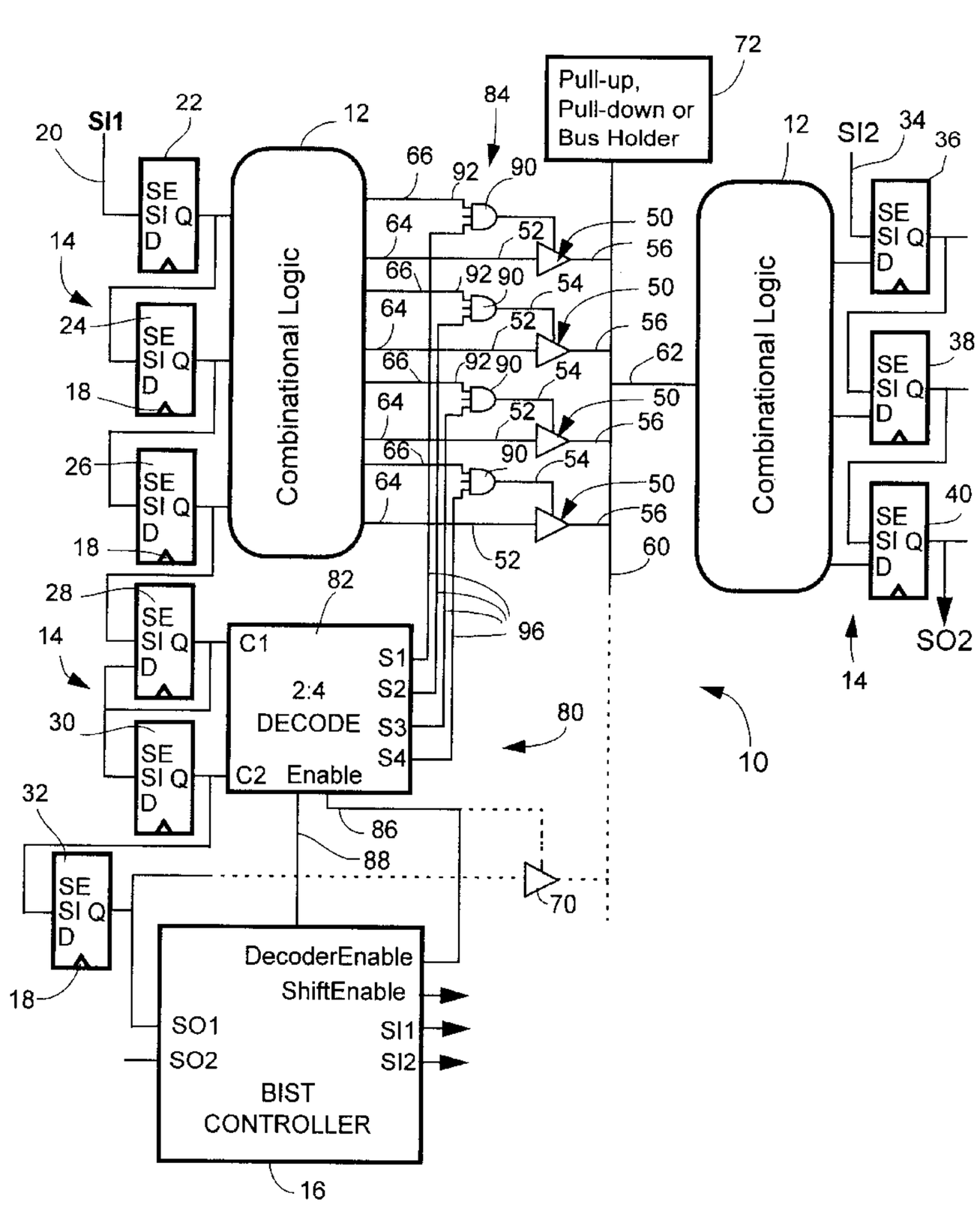
Primary Examiner—David Ton
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A scan-testing method for circuits having tri-state bus drivers disables all drivers during scan intervals and enables at most one of the bus drivers during the capture interval. A driver select signal is generated for each bus driver and gated with a corresponding circuit functional enable signal to generate a driver enable signal. A driver is selected by loading a driver select code into memory elements during the scan-in sequence and decoding the driver select code to produce the driver select signals.

30 Claims, 4 Drawing Sheets



US006510534B1

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,510,534 B1**
(45) **Date of Patent: Jan. 21, 2003**

(54) **METHOD AND APPARATUS FOR TESTING HIGH PERFORMANCE CIRCUITS**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Fadi Maamari**, San Jose, CA (US); **Dwayne Burek**, San Jose, CA (US); **Jean-Francois Cote**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 361 days.

(21) Appl. No.: **09/607,128**

(22) Filed: **Jun. 29, 2000**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/724**; 714/726; 714/729; 714/731
(58) **Field of Search** 714/724, 726, 714/727, 728, 731, 733, 736, 30, 735, 729; 327/765; 365/201

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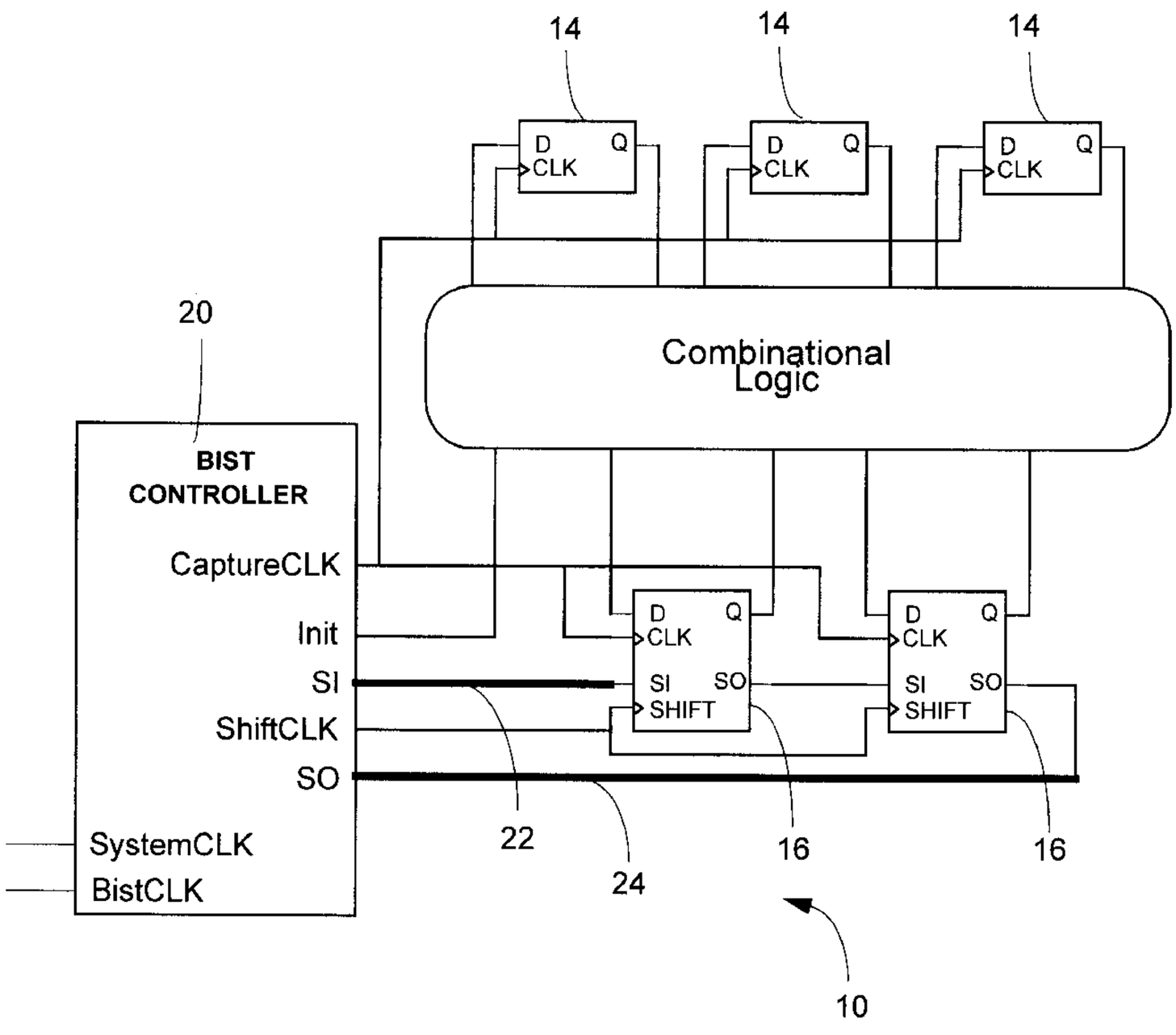
Primary Examiner—Emmanuel L. Moise
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A method for at-speed testing high-performance digital systems and circuits having combinational logic and memory elements that may be both scannable and non-scannable is performed by enabling at least two clock pulses during a capture sequence following a shift sequence. The method provides for initialization of any non-scannable memory elements via the scannable memory elements at the beginning of the test before an at-speed test is performed. During initialization, control logic generates a signal to disable the generation of system clock pulses for capture. Instead, only one clock cycle derived from the test clock or a system clock is generated to initialize the non-scannable elements. The number of shift sequences required depends on the maximum number of non-scannable elements that must be traversed between two scannable memory elements. During the same initialization period, the output response analyzer is disabled since unknown data values will present in the stream of data shifted out. A test controller is clocked a test clock and includes a clock generation module for generating shift and capture clocks. The test clock can be an independent and asynchronous clock or derived from the system clock. The test can also be performed by using only the test clock in the case only the test clock is available or for diagnostic and debug purposes.

44 Claims, 4 Drawing Sheets



US006536008B1

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,536,008 B1**
(45) **Date of Patent: Mar. 18, 2003**

(54) **FAULT INSERTION METHOD, BOUNDARY SCAN CELLS, AND INTEGRATED CIRCUIT FOR USE THEREWITH**

(75) Inventors: **Benoit Nadeau-Dostie**, Alymer (CA); **Jean-François Cote**, Alymer (CA); **Pierre Gauthier**, Aylmer (CA)

(73) Assignee: **Logic Vision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/181,077**

(22) Filed: **Oct. 27, 1998**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/726**; 714/727
(58) **Field of Search** ..... 714/703, 726, 714/724, 727, 729, 733, 734; 324/158 R

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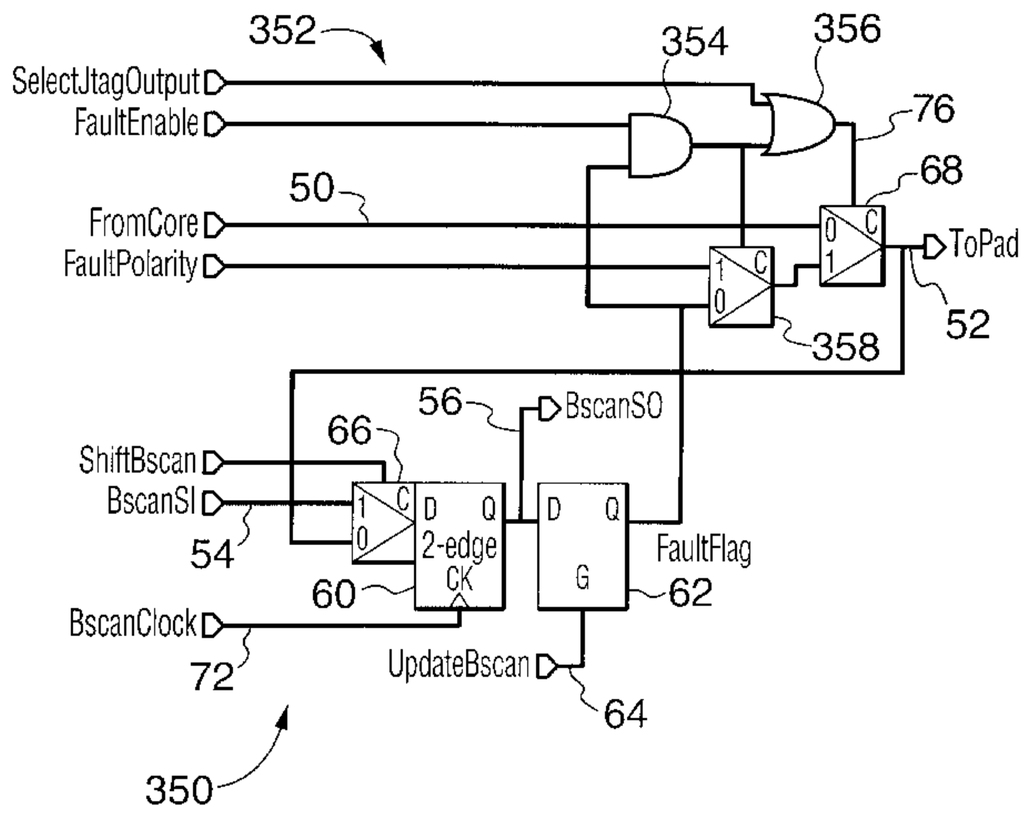
Primary Examiner—David Ton
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A number of fault injection circuits and corresponding methods for injecting correlated, uncorrelated, non-persistent and persisting faults at the primary outputs of boundary scan cells are disclosed. Fault data is loaded in the boundary scan cell update latch of all boundary scan cells at which a fault is to be injected. The fault injection circuits generate a fault inject signal which is applied to the control input of the standard cell output selector, an active signal causing the content of the update latch to be applied to the cell primary output. In order to provide for scan testing of the fault injection circuitry, the boundary scan cell shift and update latches and the fault flag latch (if employed) are provided with hold capability so that the contents of these elements can be controlled and their input captured in accordance with standard scan testing techniques.

76 Claims, 13 Drawing Sheets



US006614263B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,614,263 B2**
(45) **Date of Patent: Sep. 2, 2003**

(54) **METHOD AND CIRCUITRY FOR CONTROLLING CLOCKS OF EMBEDDED BLOCKS DURING LOGIC BIST TEST MODE**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-Francois Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/125,384**

(22) Filed: **Apr. 19, 2002**

(65) **Prior Publication Data**

US 2003/0146777 A1 Aug. 7, 2003

Related U.S. Application Data

(60) Provisional application No. 60/353,951, filed on Feb. 5, 2002.

(51) **Int. Cl.**[7] **H03K 19/00**
(52) **U.S. Cl.** **326/93**; 326/38; 326/16
(58) **Field of Search** 326/37–41, 93–98, 326/16

(56) **References Cited**

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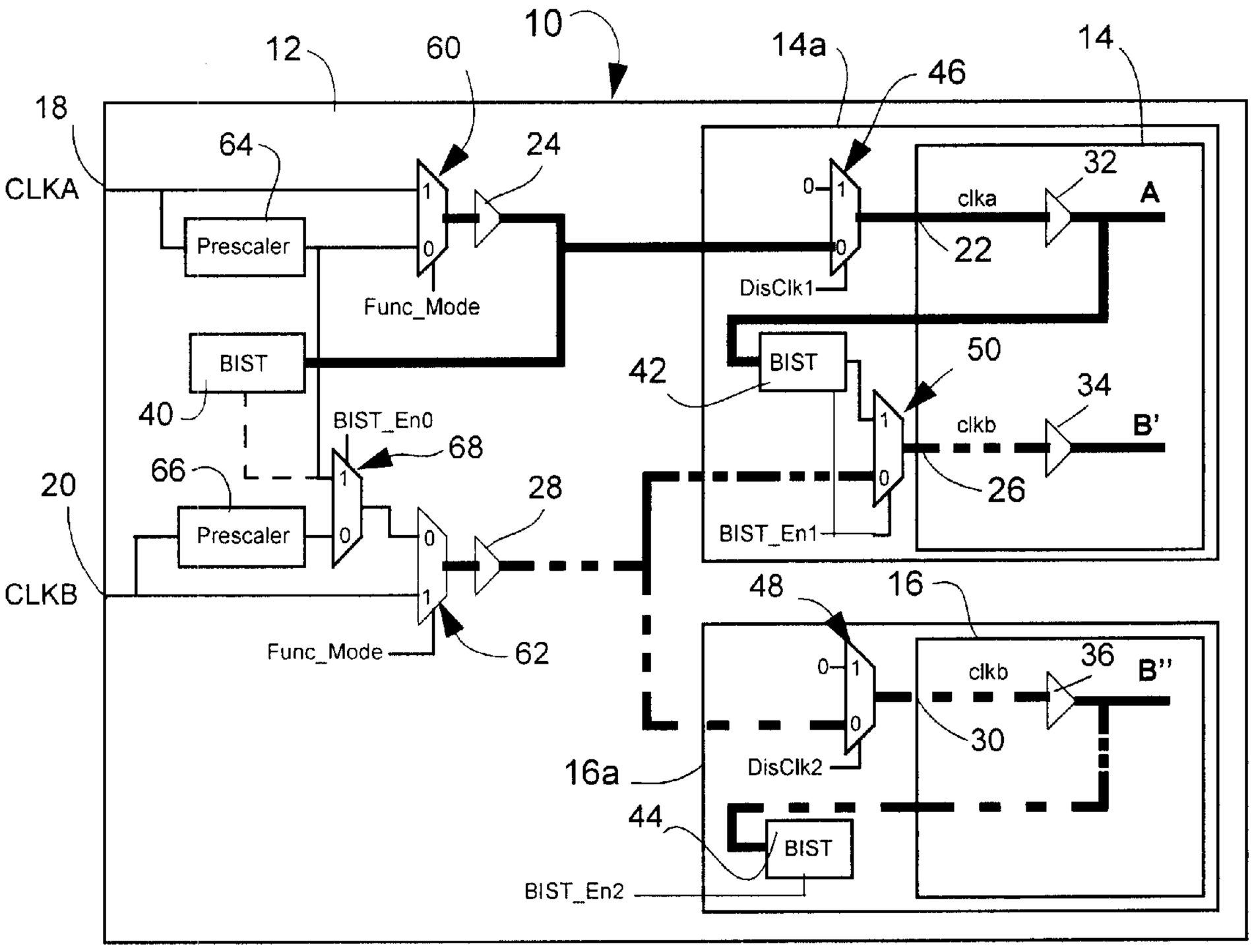
Primary Examiner—Don Le
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

One aspect of the invention is generally defined as a method of designing an integrated circuit for distributing test clock signals to embedded cores having at least one core functional clock input, the method comprising, for each core, providing a clock gating circuit for selectively disabling a core functional clock signal applied to a core primary clock input; and providing a core clock selection circuit for each secondary core functional clock input for selecting one of a core functional clock signal output by the gating circuit and a core test clock signal and applying a selected signal to the each secondary core functional clock input.

54 Claims, 3 Drawing Sheets



US006615392B1

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,615,392 B1**
(45) **Date of Patent: Sep. 2, 2003**

(54) **HIERARCHICAL DESIGN AND TEST METHOD AND SYSTEM, PROGRAM PRODUCT EMBODYING THE METHOD AND INTEGRATED CIRCUIT PRODUCED THEREBY**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Dwayne Burek**, San Jose, CA (US); **Jean-Francois Cote**, Chelsea (CA); **Sonny Ngai San Shum**, San Jose, CA (US); **Pierre Girouard**, San Jose, CA (US); **Pierre Gauther**, Aylmer (CA); **Sai Kennedy Vedantam**, Saratoga, CA (US); **Luc Romain**, Aylmer (CA); **Charles Bernard**, Hollister, CA (US)

(73) Assignee: **Logicvision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 384 days.

(21) Appl. No.: **09/626,877**

(22) Filed: **Jul. 27, 2000**

(51) **Int. Cl.**[7] **G06F 9/45**
(52) **U.S. Cl.** **716/5**; 716/4; 716/18
(58) **Field of Search** 716/5, 6, 7, 8, 716/14, 12; 714/726, 728

(56) **References Cited**

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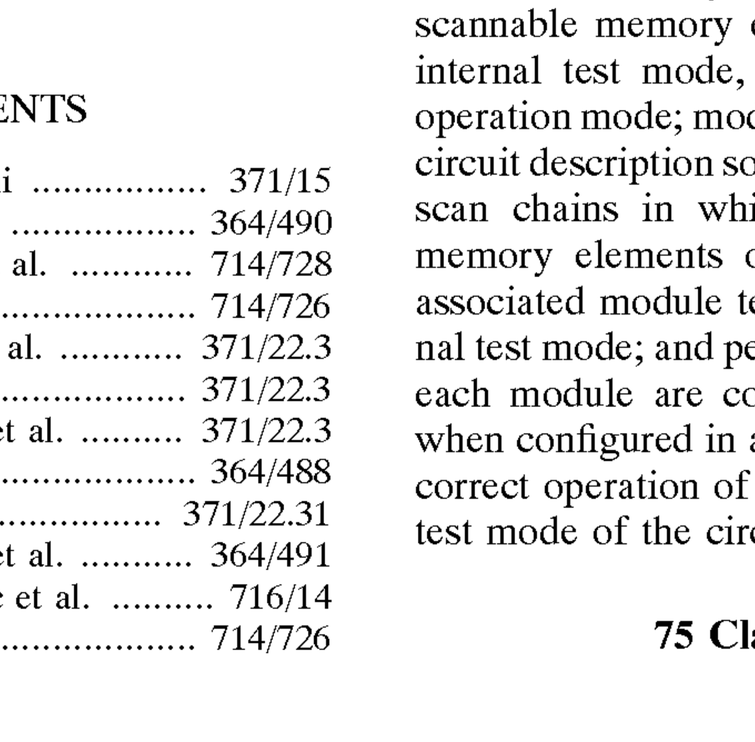
Primary Examiner—Vuthe Siek
Assistant Examiner—Binh Tat
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A method for use in the hierarchical design of integrated circuits having at least one module, each the module having functional memory elements and combinational logic, the method comprising reading in a description of the circuit; replacing the description of each functional memory element of the modules with a description of a scannable memory element configurable in scan mode and capture mode; partitioning each module into an internal partition and a peripheral partition by converting the description of selected scannable memory elements into a description of peripheral scannable memory elements which are configurable in an internal test mode, an external test mode and a normal operation mode; modifying the description of modules in the circuit description so as to arrange the memory elements into scan chains in which peripheral and internal scannable memory elements of each module are controlled by an associated module test controller when configured in internal test mode; and peripheral scannable memory elements of each module are controlled by a top-level test controller when configured in an external test mode; and verifying the correct operation of the internal test mode and the external test mode of the circuit.

75 Claims, 7 Drawing Sheets



US006671839B1

(12) **United States Patent**
Côtéet al.

(10) **Patent No.: US 6,671,839 B1**
(45) **Date of Patent: Dec. 30, 2003**

(54) **SCAN TEST METHOD FOR PROVIDING REAL TIME IDENTIFICATION OF FAILING TEST PATTERNS AND TEST BIST CONTROLLER FOR USE THEREWITH**

(75) Inventors: **Jean-François Côté**, Chelsea (CA); **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/180,116**

(22) Filed: **Jun. 27, 2002**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/726**; 324/16; 324/46
(58) **Field of Search** 714/726–739; 324/765, 46, 16

(56) **References Cited**

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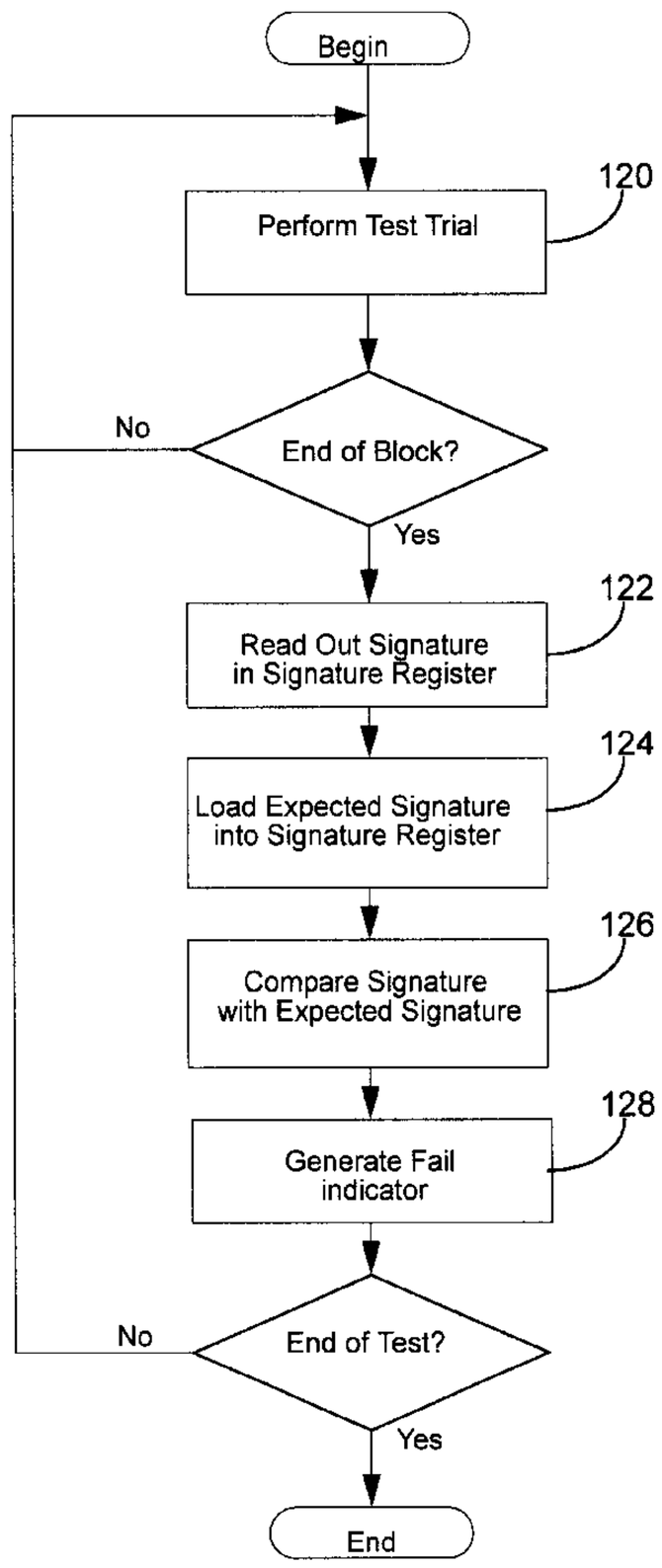
Primary Examiner—Albert Decady
Assistant Examiner—Guy Lamarre
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method of scan testing an integrated circuit to provide real time identification of a block of test patterns having at least one failing test pattern comprises performing a number of test operations and storing a test response signature corresponding to each block of test patterns into a signature register; replacing the test response signature in the signature register with a test block expected signature; identifying the block as a failing test block when the test response signature is different from the test block expected signature; and repeating preceding steps until the test is complete.

70 Claims, 8 Drawing Sheets



US006738938B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,738,938 B2**
(45) **Date of Patent: May 18, 2004**

(54) **METHOD FOR COLLECTING FAILURE INFORMATION FOR A MEMORY USING AN EMBEDDED TEST CONTROLLER**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 8 days.

(21) Appl. No.: **10/156,117**

(22) Filed: **May 29, 2002**

(65) **Prior Publication Data**

US 2003/0226073 A1 Dec. 4, 2003

(51) **Int. Cl.**[7] **G11C 29/00**
(52) **U.S. Cl.** **714/719**; 714/718; 714/704
(58) **Field of Search** 714/718, 719, 714/736, 704

(56) **References Cited**

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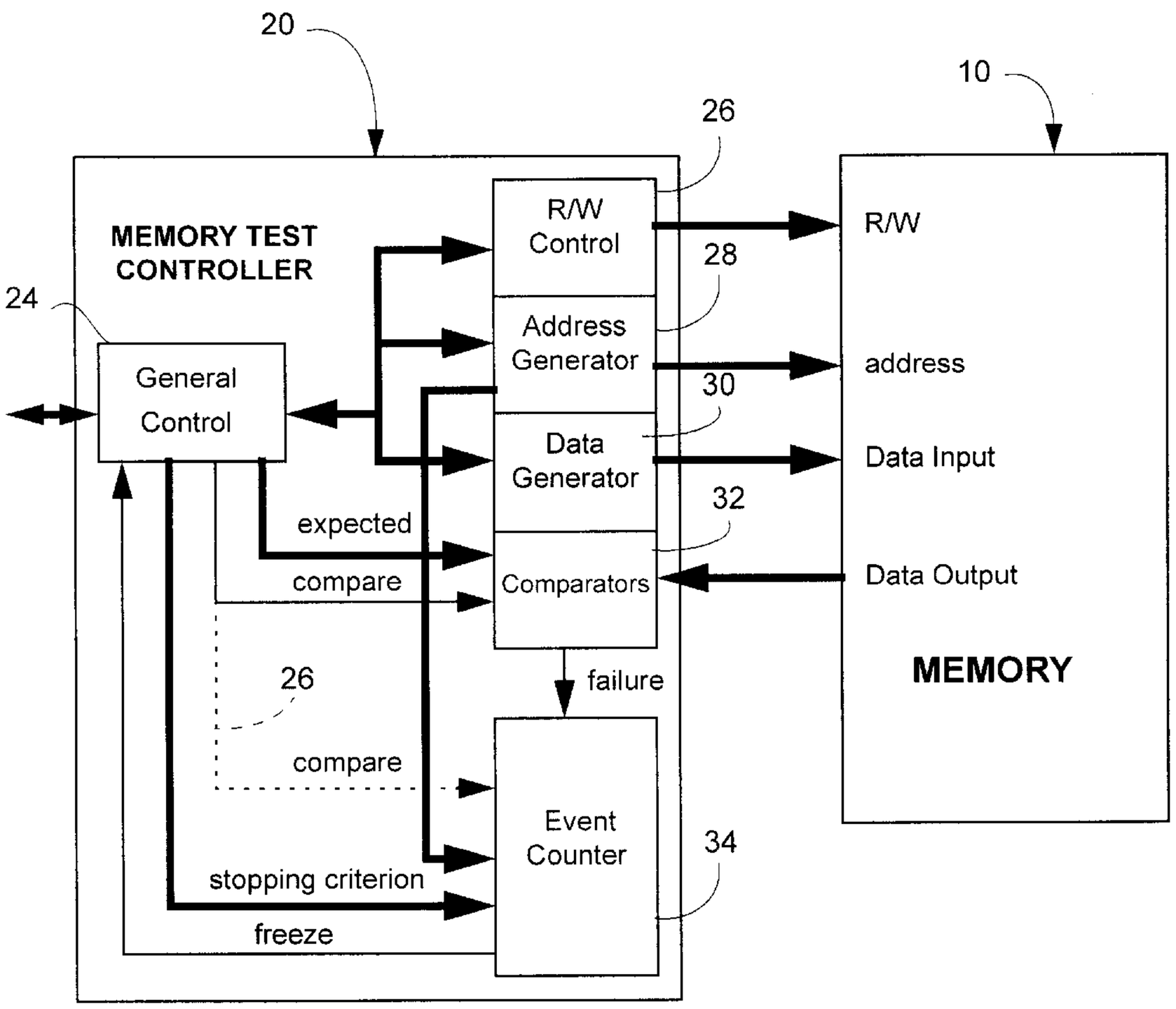
Primary Examiner—Phung M. Chung
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method of collecting failure information when testing a memory comprises performing a test of the memory according to a test algorithm, and, while performing the test, counting failure events which occur after a predetermined number of masked events; stopping the test upon occurrence of a stopping criterion which comprises one of occurrence of a first failure event, a change of a test operation; a change of a memory column address; a change of a memory row address; a change of a memory bank address; and a change of a test algorithm phase; and storing failure information.

52 Claims, 3 Drawing Sheets



US006745359B2

(12) **United States Patent**
Nadeau-Dostie

(10) **Patent No.: US 6,745,359 B2**
(45) **Date of Patent: Jun. 1, 2004**

(54) METHOD OF MASKING CORRUPT BITS DURING SIGNATURE ANALYSIS AND CIRCUIT FOR USE THEREWITH

(75) Inventor: **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 103 days.

(21) Appl. No.: **10/162,917**

(22) Filed: **Jun. 6, 2002**

(65) **Prior Publication Data**

US 2003/0229833 A1 Dec. 11, 2003

(51) **Int. Cl.**[7] **G01R 37/28**
(52) **U.S. Cl.** **714/726**
(58) **Field of Search** 714/732, 724, 714/726, 727; 326/16

(56) **References Cited**

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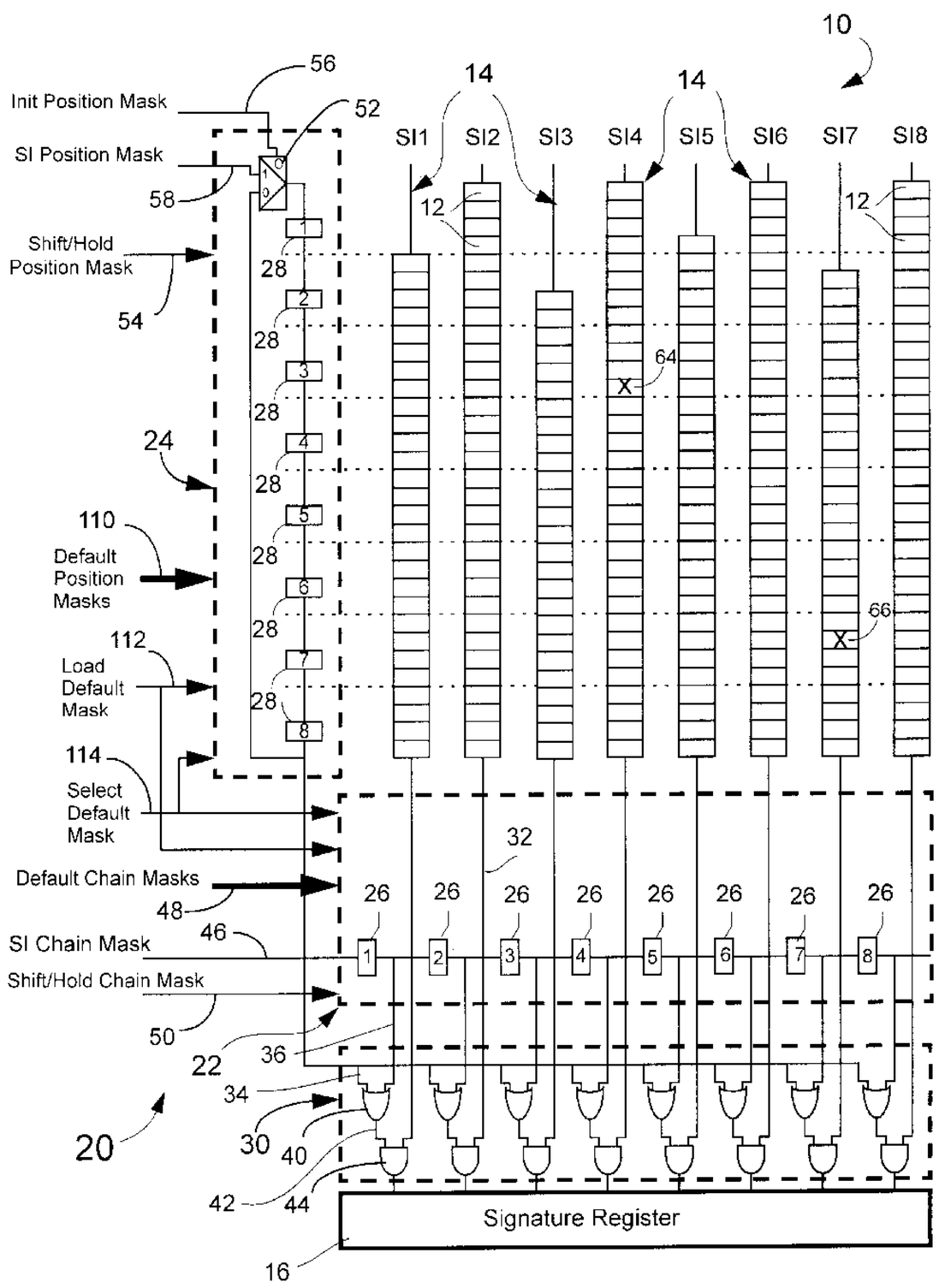
Primary Examiner—Albert Decady
Assistant Examiner—Shelly A Chase
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method of masking corrupt bits in test response pattern scan chains in an integrated circuit, comprising loading and applying a set of test patterns in the scan chains so as to obtain corresponding test response patterns; and masking bits of the test response patterns located in scan chains identified by a chain mask and at a position identified by a position mask.

55 Claims, 3 Drawing Sheets



US006760874B2

(12) **United States Patent**
Côté et al.

(10) **Patent No.: US 6,760,874 B2**
(45) **Date of Patent: Jul. 6, 2004**

(54) **TEST ACCESS CIRCUIT AND METHOD OF ACCESSING EMBEDDED TEST CONTROLLERS IN INTEGRATED CIRCUIT MODULES**

(75) Inventors: **Jean-François Côté**, Chelsea (CA); **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 84 days.

(21) Appl. No.: **10/139,294**

(22) Filed: **May 7, 2002**

(65) **Prior Publication Data**

US 2003/0212524 A1 Nov. 13, 2003

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/724**; 714/729
(58) **Field of Search** 714/724, 729, 714/236; 713/502; 324/73.1; 326/16

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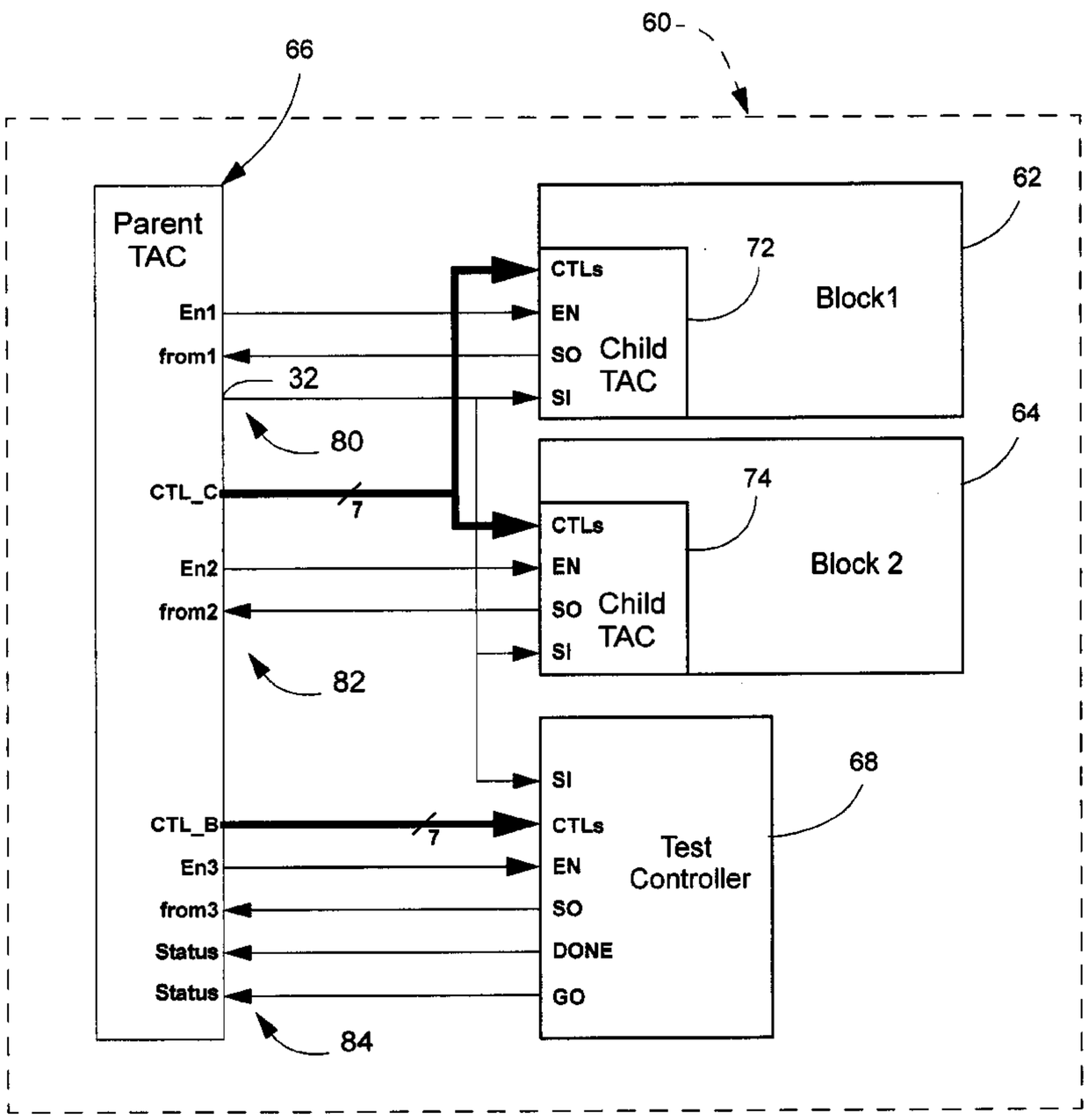
Primary Examiner—Albert Decady
Assistant Examiner—Dipakkumar Gandhi
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A test access circuit (TAC) for use in controlling test resources including child test access circuits (TACs) and/or test controllers, in an integrated circuit, comprises an enable input for enabling or disabling access to the test resources, a test port associated with each test resource, each test port including a test port enable output for connection to an enable input of an associated test resource; and an input for receiving a serial output of the associated test resource; and a selector for selecting a test resource for communication therewith.

53 Claims, 5 Drawing Sheets



US006763489B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,763,489 B2**
(45) **Date of Patent: Jul. 13, 2004**

(54) **METHOD FOR SCAN TESTING OF DIGITAL CIRCUIT, DIGITAL CIRCUIT FOR USE THEREWITH AND PROGRAM PRODUCT FOR INCORPORATING TEST METHODOLOGY INTO CIRCUIT DESCRIPTION**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 661 days.

(21) Appl. No.: **09/773,541**

(22) Filed: **Feb. 2, 2001**

(65) **Prior Publication Data**

US 2002/0147951 A1 Oct. 10, 2002

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/731**; 713/500
(58) **Field of Search** 326/16; 714/726–731; 713/500

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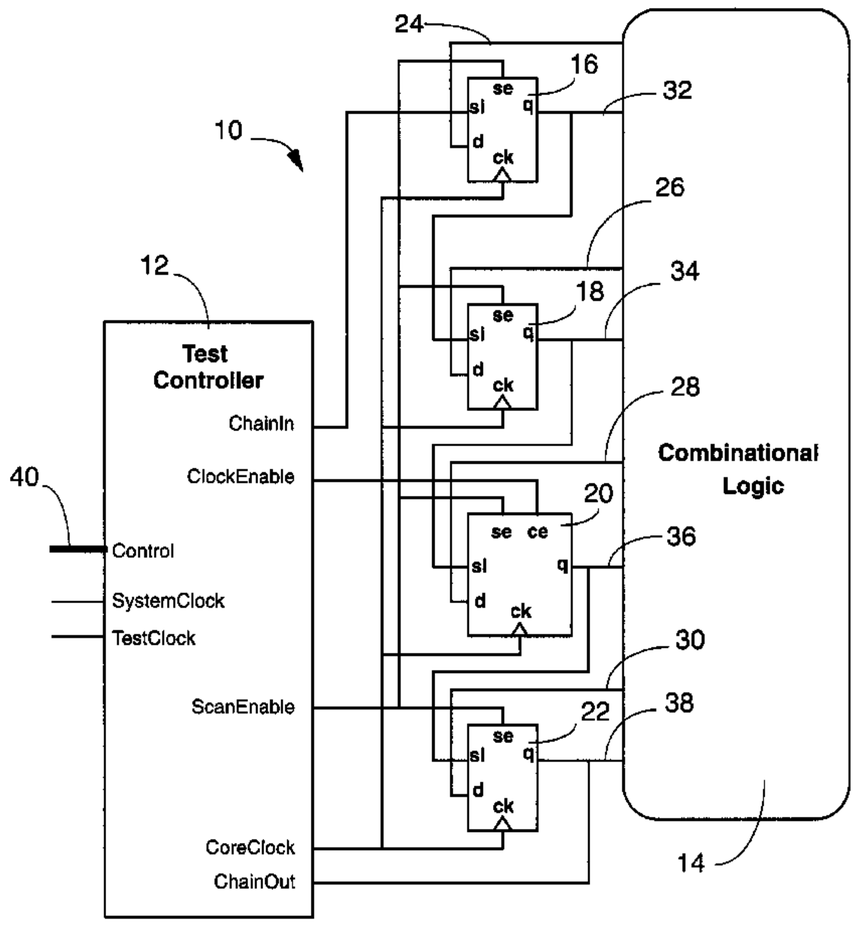
Primary Examiner—Guy J. Lamarre
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method for at-speed scan testing of circuits having scannable memory elements which source multi-cycle paths having propagation delays that are longer than the period of a system clock used during normal operation comprises loading a test stimulus into the scannable memory elements; performing a capture operation, including configuring in capture mode throughout the capture operation, non-source memory elements and multi-cycle path source memory elements which have a predetermined maximum capture clock rate which is the same as or higher than the clock rate of the capture clock; and configuring in a hold mode during all but the last cycle of the capture operation and in capture mode for the last cycle, source memory elements which have a predetermined maximum capture clock rate which is lower than the clock rate of the capture clock; applying at least two clock cycles of the capture clock; and unloading test response data captured by said scannable memory elements.

65 Claims, 7 Drawing Sheets



US006829730B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,829,730 B2**
(45) **Date of Patent: Dec. 7, 2004**

(54) **METHOD OF DESIGNING CIRCUIT HAVING MULTIPLE TEST ACCESS PORTS, CIRCUIT PRODUCED THEREBY AND METHOD OF USING SAME**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 788 days.

(21) Appl. No.: **09/843,307**

(22) Filed: **Apr. 27, 2001**

(65) **Prior Publication Data**

US 2002/0184562 A1 Dec. 5, 2002

(51) **Int. Cl.**[7] **G06F 11/27**
(52) **U.S. Cl.** **714/30**; 714/31; 714/724; 714/729; 714/734; 716/1
(58) **Field of Search** 714/25, 30, 31, 714/37, 38, 724, 727, 729, 733, 734; 703/23, 24, 25, 26, 27, 28; 716/1, 4

(56) **References Cited**

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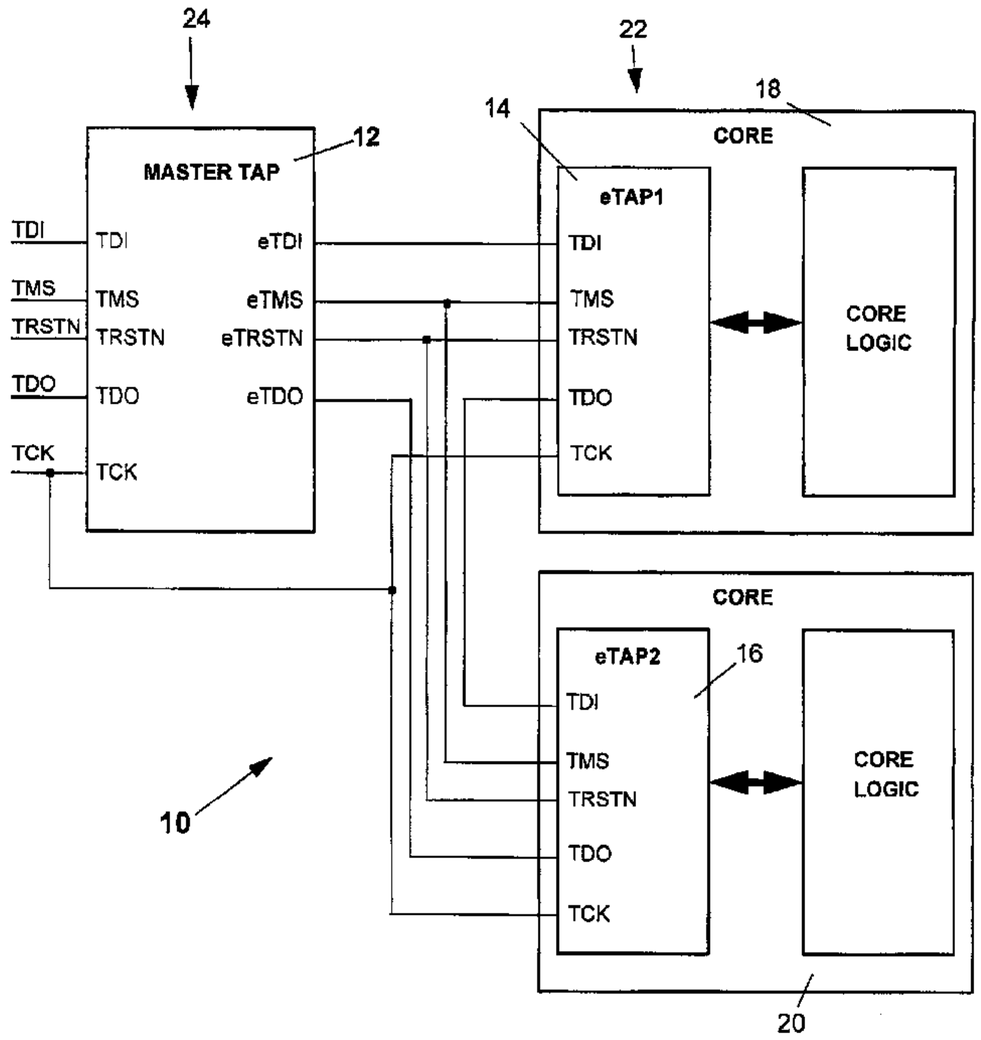
Primary Examiner—Robert Beausoliel
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

In a circuit with multiple Test Access Port (TAP) interfaces, the TAPs are arranged into groups, with secondary TAPs in one or more groups and a master TAP in another group, the master TAP having an instruction register with bits for storing a group selection code; a Test Data Output (TDO) circuit responsive to the group selection code connects the group TDO of one of the groups to the circuit TDO; and, for each secondary TAP group, a group Test Data Input (TDI) circuit responsive to a shift state signal for selectively connecting the group TDI to the circuit TDI or to the output of a padding register having its input connected to the circuit TDI, and its output connected to an input of the group TDI circuit; and a group TMS circuit responsive to a predetermined TAP selection code associated with the group for producing a group TMS signal for each TAP in the group.

51 Claims, 6 Drawing Sheets



US006862717B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,862,717 B2**
(45) **Date of Patent: Mar. 1, 2005**

(54) **METHOD AND PROGRAM PRODUCT FOR DESIGNING HIERARCHICAL CIRCUIT FOR QUIESCENT CURRENT TESTING**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Dwayne Burek**, San Jose, CA (US)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 490 days.

(21) Appl. No.: **10/015,751**

(22) Filed: **Dec. 17, 2001**

(65) **Prior Publication Data**

US 2003/0115522 A1 Jun. 19, 2003

(51) **Int. Cl.**[7] **G06F 17/50**
(52) **U.S. Cl.** **716/4**; 716/2; 716/7; 716/18
(58) **Field of Search** 716/2, 4, 7, 18; 714/30.726

(56) **References Cited**

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2003/0110457	A1	*	6/2003	Cote et al. 716/4

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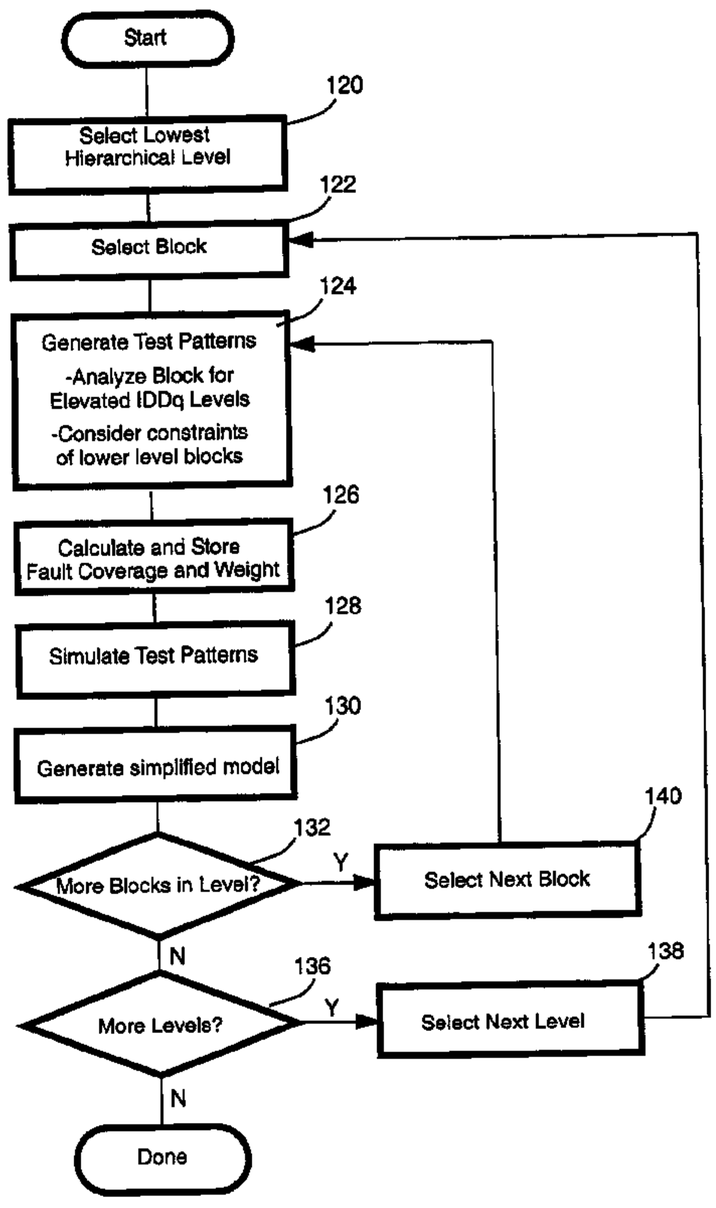
Primary Examiner—Thuan Do
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method of designing a circuit having at least one hierarchical block which requires block specific test patterns to facilitate quiescent current testing of the circuit, comprises, for each block, configuring the block and any embedded blocks located one level down in design hierarchy in quiescent current test mode in which input and output peripheral memory elements are configured in internal test mode and in external test mode, respectively; generating quiescent current test patterns which do not result in elevated quiescent current levels and which include a bit for all memory elements in the block and for any peripheral memory elements in any embedded blocks located one level down in design hierarchy; and, if the block contains embedded blocks, synchronizing the test pattern with a corresponding test pattern generated for embedded blocks so that test patterns loaded in scan chains in the block are consistent with test patterns loaded in scan chains in said embedded blocks.

79 Claims, 11 Drawing Sheets



US006868532B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,868,532 B2**
(45) **Date of Patent: Mar. 15, 2005**

(54) **METHOD AND PROGRAM PRODUCT FOR DESIGNING HIERARCHICAL CIRCUIT FOR QUIESCENT CURRENT TESTING AND CIRCUIT PRODUCED THEREBY**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 284 days.

(21) Appl. No.: **10/011,128**

(22) Filed: **Dec. 10, 2001**

(65) **Prior Publication Data**

US 2003/0110457 A1 Jun. 12, 2003

(51) **Int. Cl.**[7] **G06F 17/50**
(52) **U.S. Cl.** **716/4**; 714/724
(58) **Field of Search** 716/4; 714/724, 714/735, 738–739, 741

(56) **References Cited**

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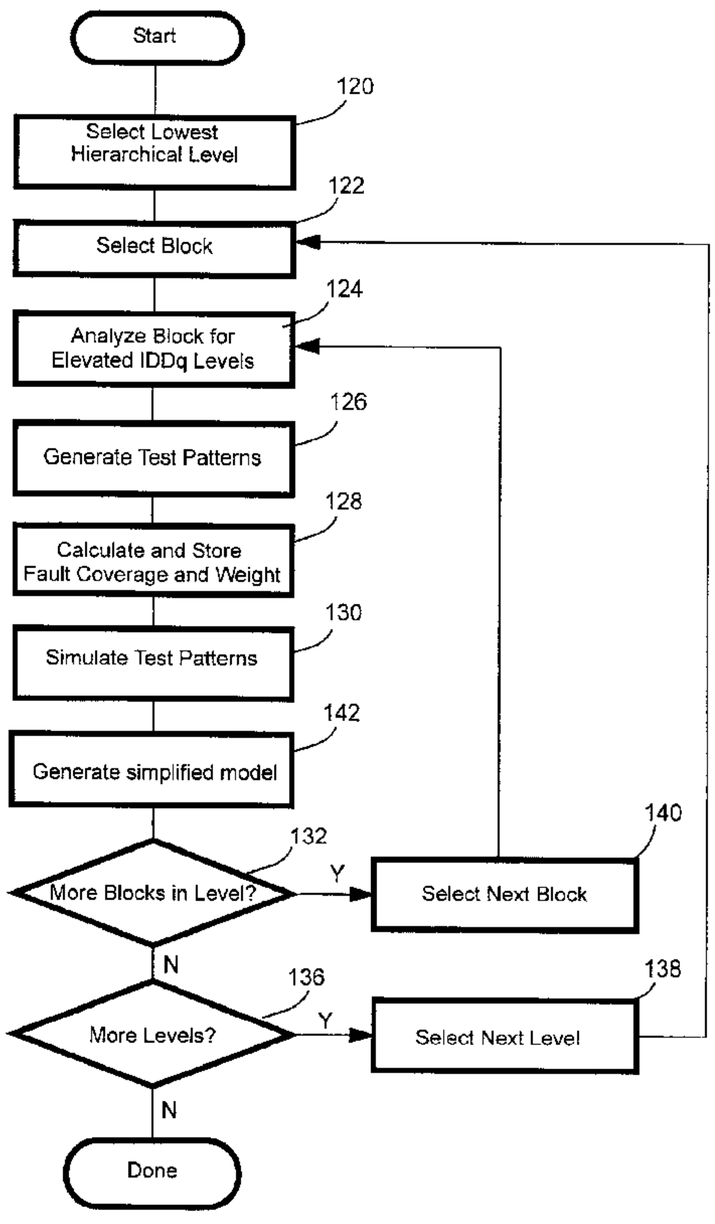
Primary Examiner—Stacy A. Whitmore
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method of designing integrated circuits having an hierarchical structure for quiescent current testing, and the circuit which results therefrom is disclosed. The method comprises analyzing each of one or more selected hierarchical blocks independently of other selected blocks identify any circuit states of each block which could result in elevated quiescent current levels during quiescent current testing of the circuit, the analysis beginning with blocks at a lowest level of hierarchy and proceeding in sequence through each level of design hierarchy to a highest level of hierarchy containing a top-level block; and calculating a fault coverage for each selected block.

78 Claims, 8 Drawing Sheets



US007139946B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,139,946 B2**
(45) **Date of Patent: Nov. 21, 2006**

(54) **METHOD AND TEST CIRCUIT FOR TESTING MEMORY INTERNAL WRITE ENABLE**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Saman M. I. Adham**, Kanata (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 464 days.

(21) Appl. No.: **10/638,388**

(22) Filed: **Aug. 12, 2003**

(65) **Prior Publication Data**

US 2004/0123203 A1 Jun. 24, 2004

Related U.S. Application Data

(60) Provisional application No. 60/433,987, filed on Dec. 18, 2002.

(51) **Int. Cl.**
G11C 29/00 (2006.01)
G11C 7/00 (2006.01)

(52) **U.S. Cl.** **714/720**; 714/719; 365/201

(58) **Field of Classification Search** 714/718–720; 365/200–201
See application file for complete search history.

(56) **References Cited**

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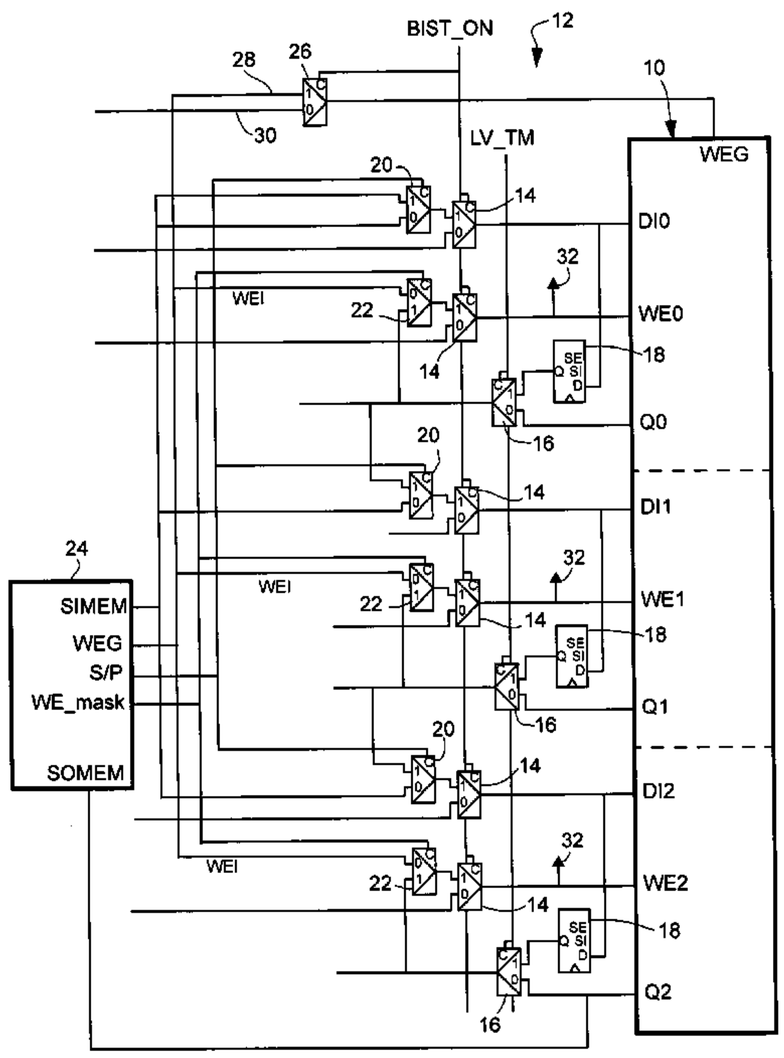
Primary Examiner—Guy Lamarre
Assistant Examiner—Steven D. Radosevich
(74) *Attorney, Agent, or Firm*—Eugene E. Prouix

(57) **ABSTRACT**

A method of testing write enable lines of random access memory having at least one word having one or more write enable inputs for controlling write operations in the word, comprises, for a selected memory address, shifting a series of test bits through an addressed word via a first data input to the word, and for each test bit, performing a write operation to the word using a write enable test input derived from data outputs of the word or from a test write enable signal applied concurrently to each write enable input; and, after each write operation, comparing a last bit of the word against an expected value to determine whether there exists a defect in a write enable line.

49 Claims, 8 Drawing Sheets



US007155651B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,155,651 B2**
(45) **Date of Patent: Dec. 26, 2006**

(54) **CLOCK CONTROLLER FOR AT-SPEED TESTING OF SCAN CIRCUITS**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 194 days.

(21) Appl. No.: **11/013,319**

(22) Filed: **Dec. 17, 2004**

(65) **Prior Publication Data**

US 2005/0240847 A1 Oct. 27, 2005

Related U.S. Application Data

(60) Provisional application No. 60/564,210, filed on Apr. 22, 2004.

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/731**; 714/729

(58) **Field of Classification Search** 375/376; 713/322; 714/30, 731, 729, 726
See application file for complete search history.

(56) **References Cited**

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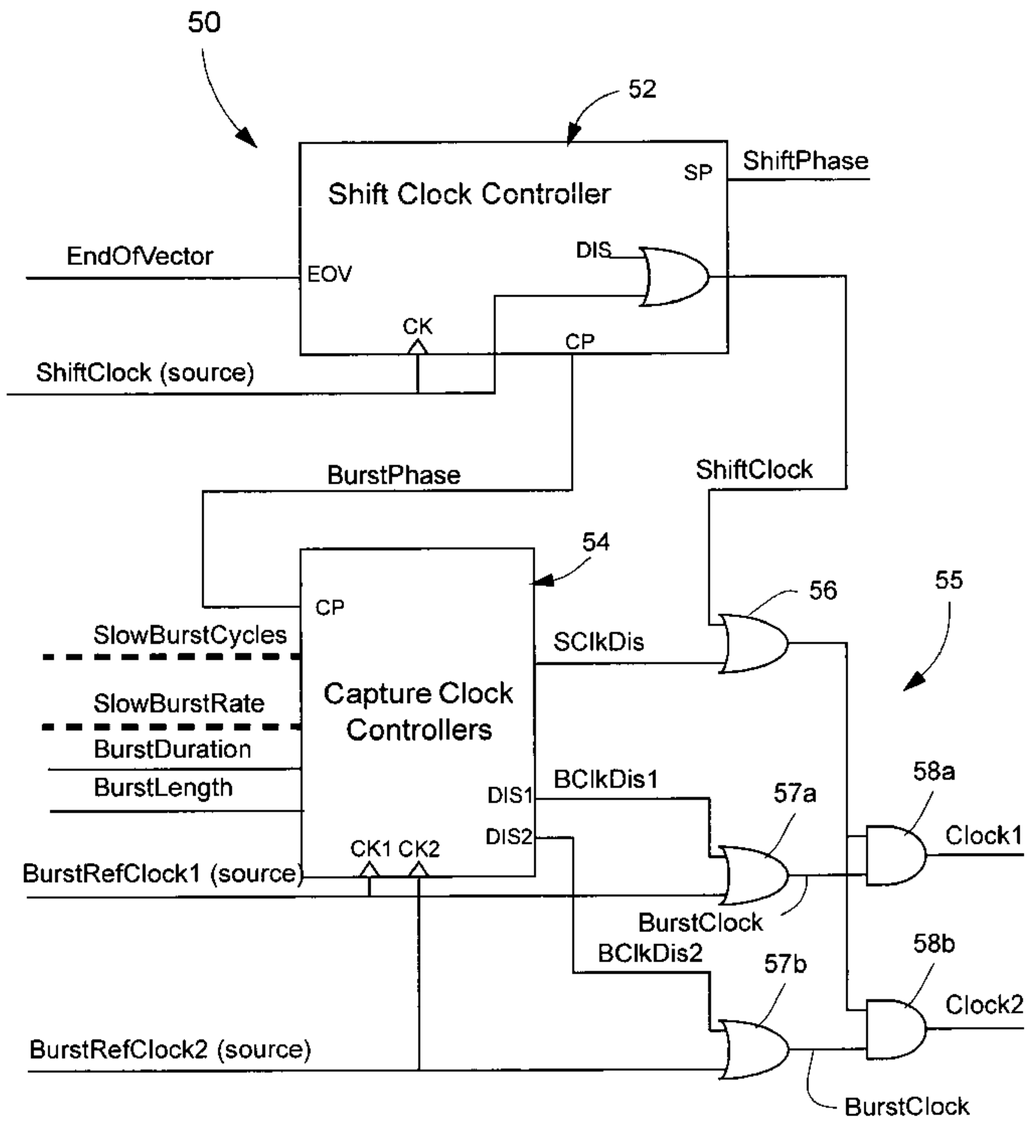
Primary Examiner—David Ton
(74) *Attorney, Agent, or Firm*—Eugene E. Prouix

(57) **ABSTRACT**

A test clock controller for generating a test clock signal for scan chains in integrated circuits having one or more clock domains, comprises a shift clock controller for generating a shift clock signal for use in loading test patterns into scan chains in the clock domains and for unloading a test response patterns from the scan chains and for generating a burst phase signal after loading a test pattern; and a burst clock controller associated with each of one or more clock domains and responsive to a burst phase signal for generating a burst of clock pulses derived from a respective reference clocks and including a first group of burst clock pulses having a selected reduced frequency relative to the reference clock and a second group of burst clock pulses having a frequency corresponding to that of the reference clock.

29 Claims, 7 Drawing Sheets



US007188274B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,188,274 B2**
(45) **Date of Patent: Mar. 6, 2007**

(54) **MEMORY REPAIR ANALYSIS METHOD AND CIRCUIT**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Robert A. Abbott**, Ottawa (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 565 days.

(21) Appl. No.: **10/774,512**

(22) Filed: **Feb. 10, 2004**

(65) **Prior Publication Data**

US 2004/0163015 A1 Aug. 19, 2004

Related U.S. Application Data

(60) Provisional application No. 60/447,280, filed on Feb. 14, 2003.

(51) **Int. Cl.**
G06F 11/00 (2006.01)

(52) **U.S. Cl.** **714/6**; 714/710

(58) **Field of Classification Search** 714/6, 714/7, 710, 711
See application file for complete search history.

(56) **References Cited**

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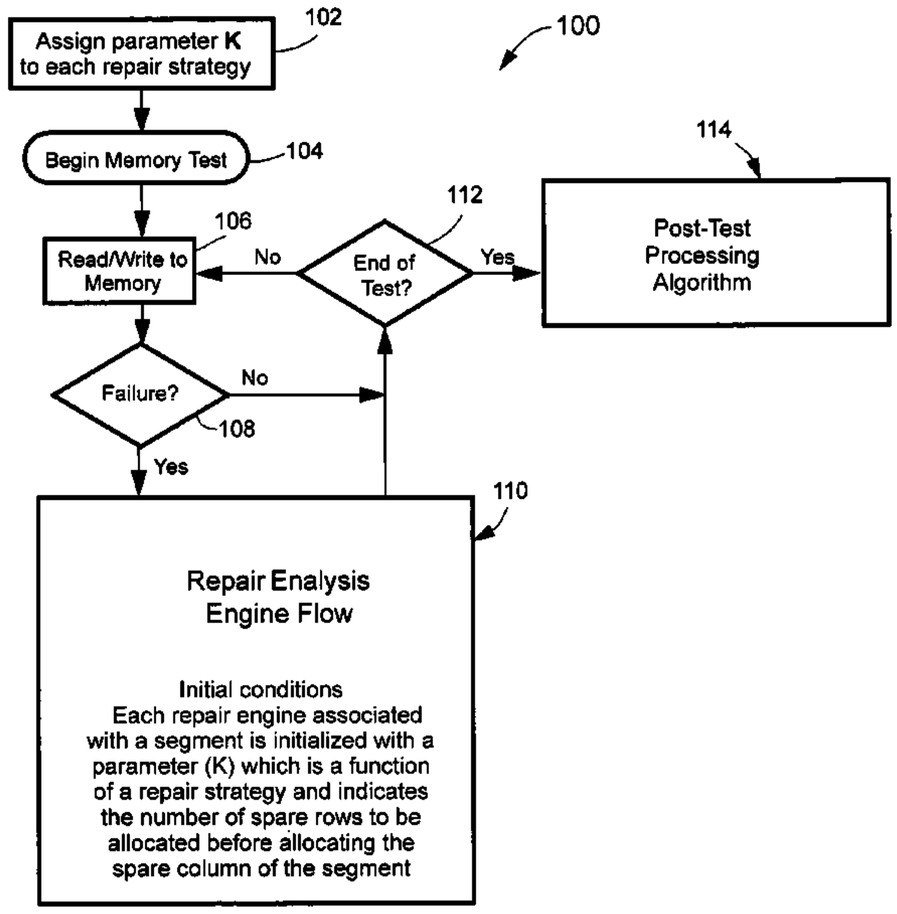
Primary Examiner—Dieu-Minh Le
(74) *Attorney, Agent, or Firm*—Eugene E. Prouix

(57) **ABSTRACT**

A method and circuit for repairing a memory array having one or more memory segments each having one spare column and a predetermined number of spare rows common to all segments, the method comprises, while testing the memory array for failures, generating an equal number of unique segment repair solutions for each segment with each segment repair solution including one defective column address, if any, and a number of defective row addresses, if any, corresponding to the predetermined number of spare rows; and, after completing testing, analyzing all segment repair solution combinations consisting of one segment repair solution selected from each segment; and identifying the best segment repair solution combination of combinations having a number of different defective row addresses which is less than or equal to the predetermined number of spare rows.

46 Claims, 11 Drawing Sheets



US007191374B2

(12) **United States Patent**
Maamari et al.

(10) **Patent No.: US 7,191,374 B2**
(45) **Date of Patent: Mar. 13, 2007**

(54) **METHOD OF AND PROGRAM PRODUCT FOR PERFORMING GATE-LEVEL DIAGNOSIS OF FAILING VECTORS**

(75) Inventors: **Fadi Maamari**, San Jose, CA (US); **Sonny Ngai San Shum**, San Jose, CA (US); **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 634 days.

(21) Appl. No.: **10/435,094**

(22) Filed: **May 12, 2003**

(65) **Prior Publication Data**

US 2003/0217315 A1 Nov. 20, 2003

Related U.S. Application Data

(60) Provisional application No. 60/379,732, filed on May 14, 2002.

(51) **Int. Cl.**
G01R 31/28 (2006.01)
G06F 17/50 (2006.01)

(52) **U.S. Cl.** **714/738**; 716/4

(58) **Field of Classification Search** 714/724, 714/738, 741; 716/4
See application file for complete search history.

(56) **References Cited**

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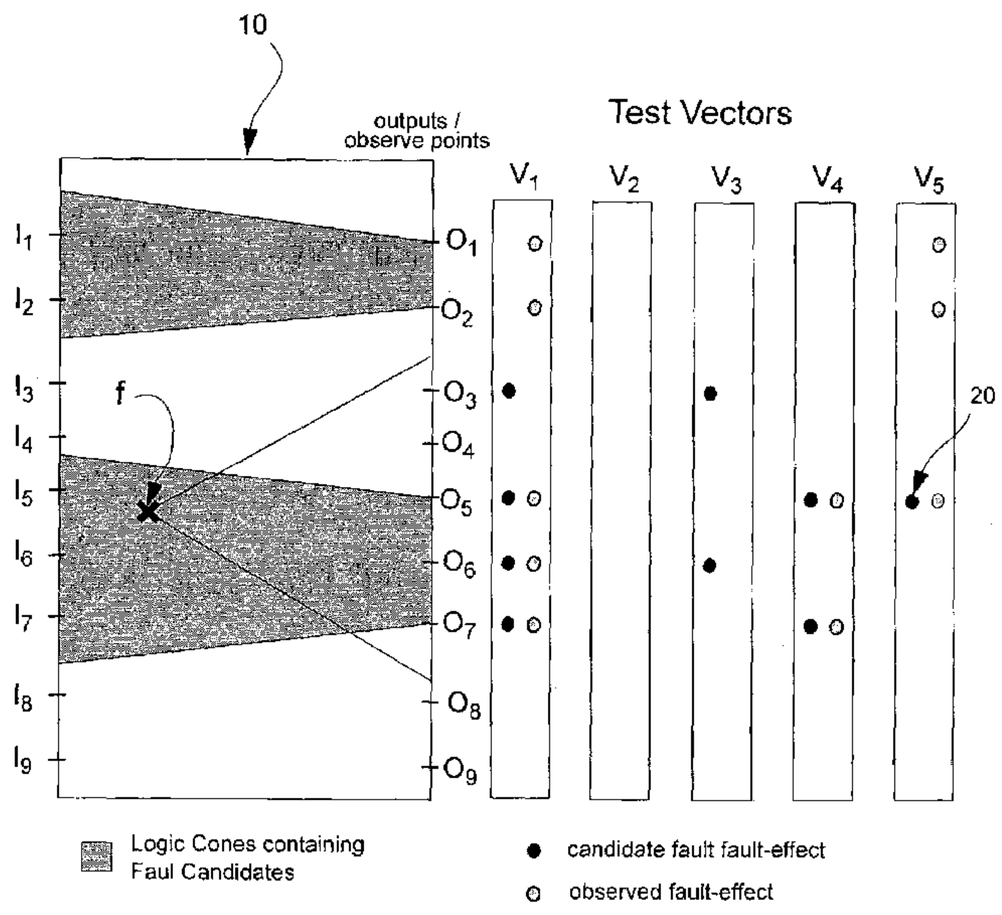
Primary Examiner—Guy Lamarre
Assistant Examiner—Cynthia Britt
(74) *Attorney, Agent, or Firm*—Eugene E. Prouix

(57) **ABSTRACT**

A method of fault diagnosis of integrated circuits having failing test vectors with observed fault effects using fault candidate fault-effects obtained by simulation of a set of test vectors, comprises determining a fault candidate diagnostic measure for each fault candidate, the fault candidate diagnostic measure having a fault candidate match metric, an observed fault effect mismatch metric and a fault candidate excitation metric, ranking fault candidates in decreasing diagnostic measure order; and identifying fault candidate(s) having the highest diagnostic measure as the most likely cause of observed fault effects.

35 Claims, 4 Drawing Sheets



US007194669B2

(12) **United States Patent**
Nadeau-Dostie

(10) **Patent No.: US 7,194,669 B2**
(45) **Date of Patent: Mar. 20, 2007**

(54) **METHOD AND CIRCUIT FOR AT-SPEED TESTING OF SCAN CIRCUITS**

(75) Inventor: **Benoit Nadeau-Dostie**, Gatineau (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 413 days.

(21) Appl. No.: **10/739,055**

(22) Filed: **Dec. 19, 2003**

(65) **Prior Publication Data**

US 2004/0163021 A1 Aug. 19, 2004

Related U.S. Application Data

(60) Provisional application No. 60/447,279, filed on Feb. 14, 2003.

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/726**

(58) **Field of Classification Search** 714/724, 714/726, 727, 729, 731, 732
See application file for complete search history.

(56) **References Cited**

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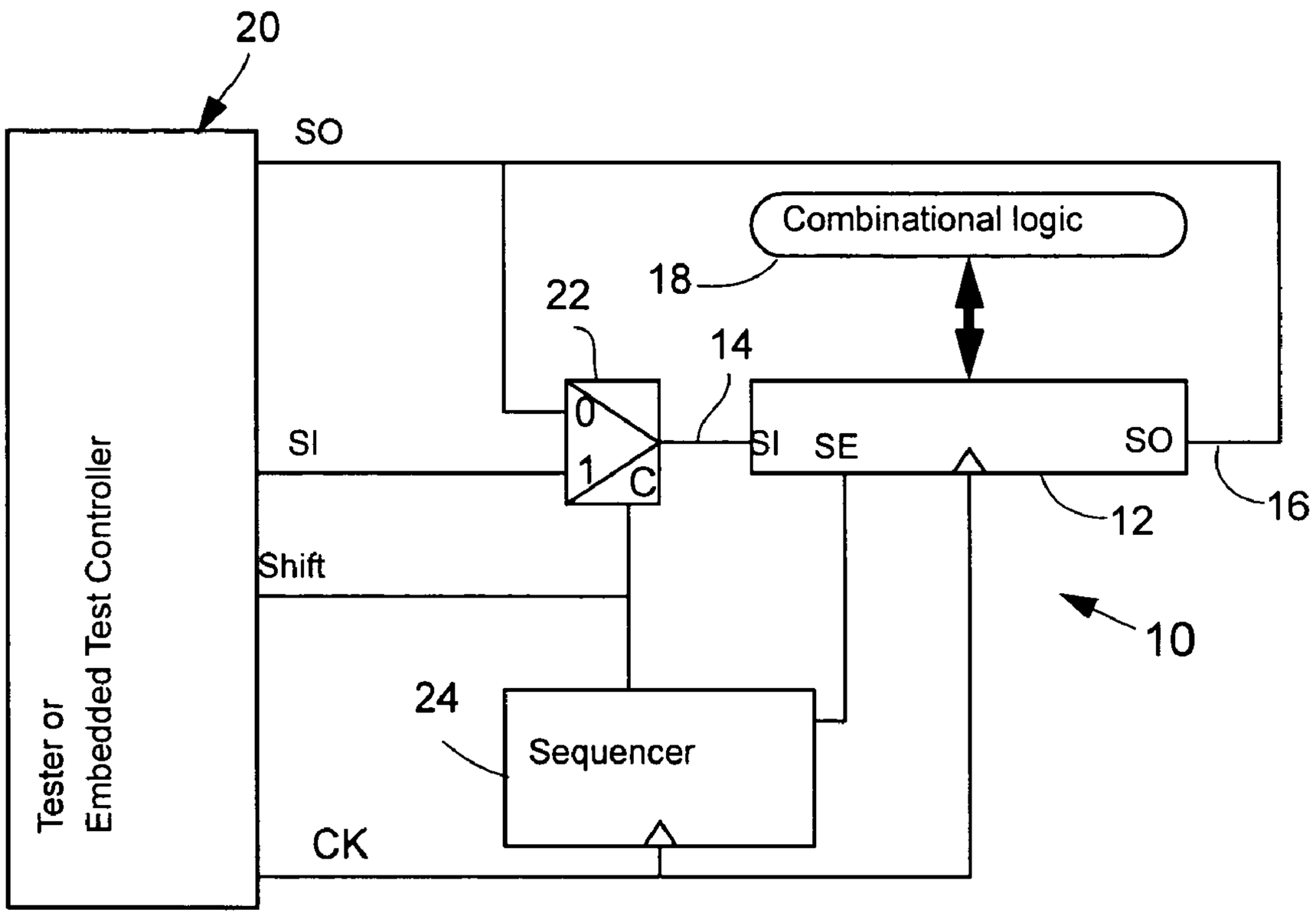
Primary Examiner—James C. Kerveros
(74) *Attorney, Agent, or Firm*—Eugene E Prouix

(57) **ABSTRACT**

An improvement in a scan testing method for testing a circuit having memory elements arranged into one or more scan chains, the scan testing method having a shift phase for serially loading test patterns into the scan chains and serially unloading test response patterns from the scan chains and a capture phase for capturing the response of the circuit to the test pattern, includes, during the capture phase, connecting the serial output of each scan chain to its serial input and applying a predetermined number of capture clock cycles with the memory elements configured in a non-capture mode for all but the last capture clock cycle and configured in capture mode for the last capture clock cycle.

45 Claims, 9 Drawing Sheets



US007219282B2

(12) **United States Patent**
Sunter et al.

(10) **Patent No.: US 7,219,282 B2**
(45) **Date of Patent: May 15, 2007**

(54) **BOUNDARY SCAN WITH STROBED PAD DRIVER ENABLE**

(75) Inventors: **Stephen K. Sunter**, Nepean (CA); **Pièrre Gauthier**, Gatineau (CA); **Benoit Nadeau-Dostie**, Gatineau (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 494 days.

(21) Appl. No.: **10/701,479**

(22) Filed: **Nov. 6, 2003**

(65) **Prior Publication Data**

US 2004/0098648 A1 May 20, 2004

Related U.S. Application Data

(60) Provisional application No. 60/425,994, filed on Nov. 14, 2002.

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/727**; 714/726

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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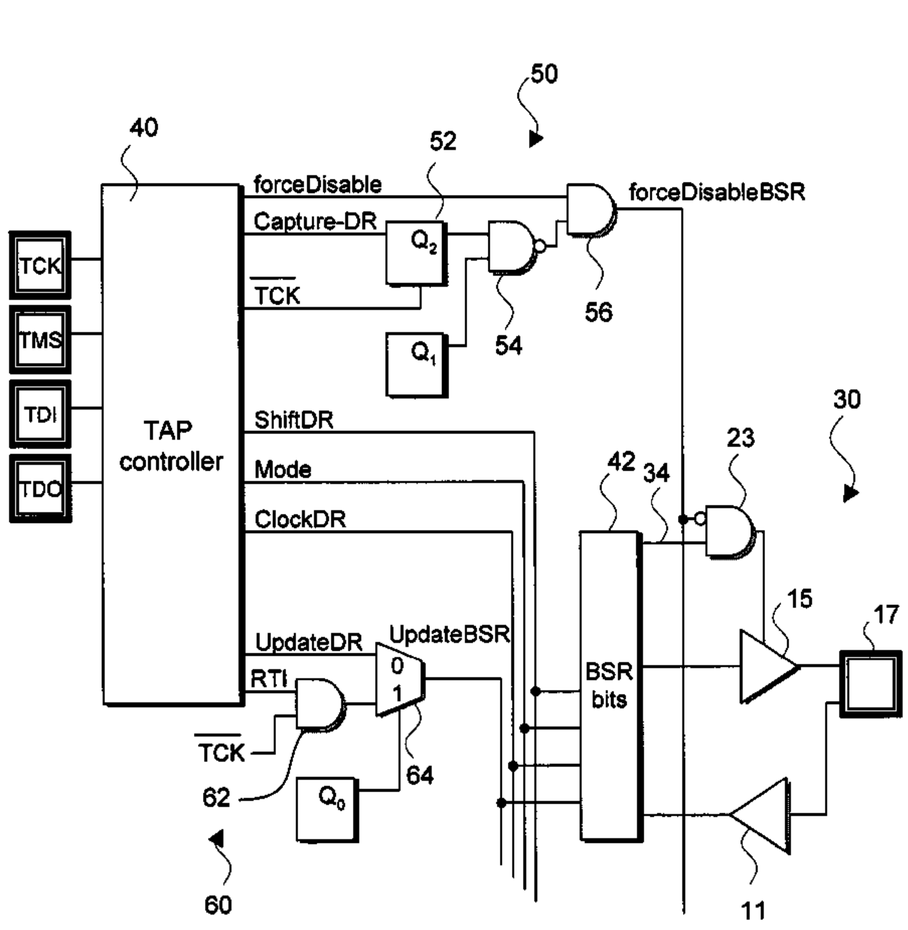
Primary Examiner—Albert Decady
Assistant Examiner—Steve Nguyen
(74) *Attorney, Agent, or Firm*—Eugene E. Prouix

(57) **ABSTRACT**

A circuit and a method are provided for testing the enable function of Boundary Scan Register bits that control the driver of unconnected I/O pins of an 1149.1-compliant IC during the IC's reduced pin-count access manufacturing test, and to test the connections to these pins during the test of a circuit board containing the IC, without causing excessive current if a pin is inadvertently short circuited.

7 Claims, 10 Drawing Sheets



US007257733B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,257,733 B2**
(45) **Date of Patent: Aug. 14, 2007**

(54) **MEMORY REPAIR CIRCUIT AND METHOD**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Saman M. I. Adham**, Kanata (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 513 days.

(21) Appl. No.: **10/868,208**

(22) Filed: **Jun. 16, 2004**

(65) **Prior Publication Data**

US 2004/0257901 A1 Dec. 23, 2004

Related U.S. Application Data

(60) Provisional application No. 60/479,229, filed on Jun. 18, 2003.

(51) **Int. Cl.**
G06F 11/00 (2006.01)

(52) **U.S. Cl.** **714/8**; 714/710; 714/711

(58) **Field of Classification Search** 714/8, 714/710, 711
See application file for complete search history.

(56) **References Cited**

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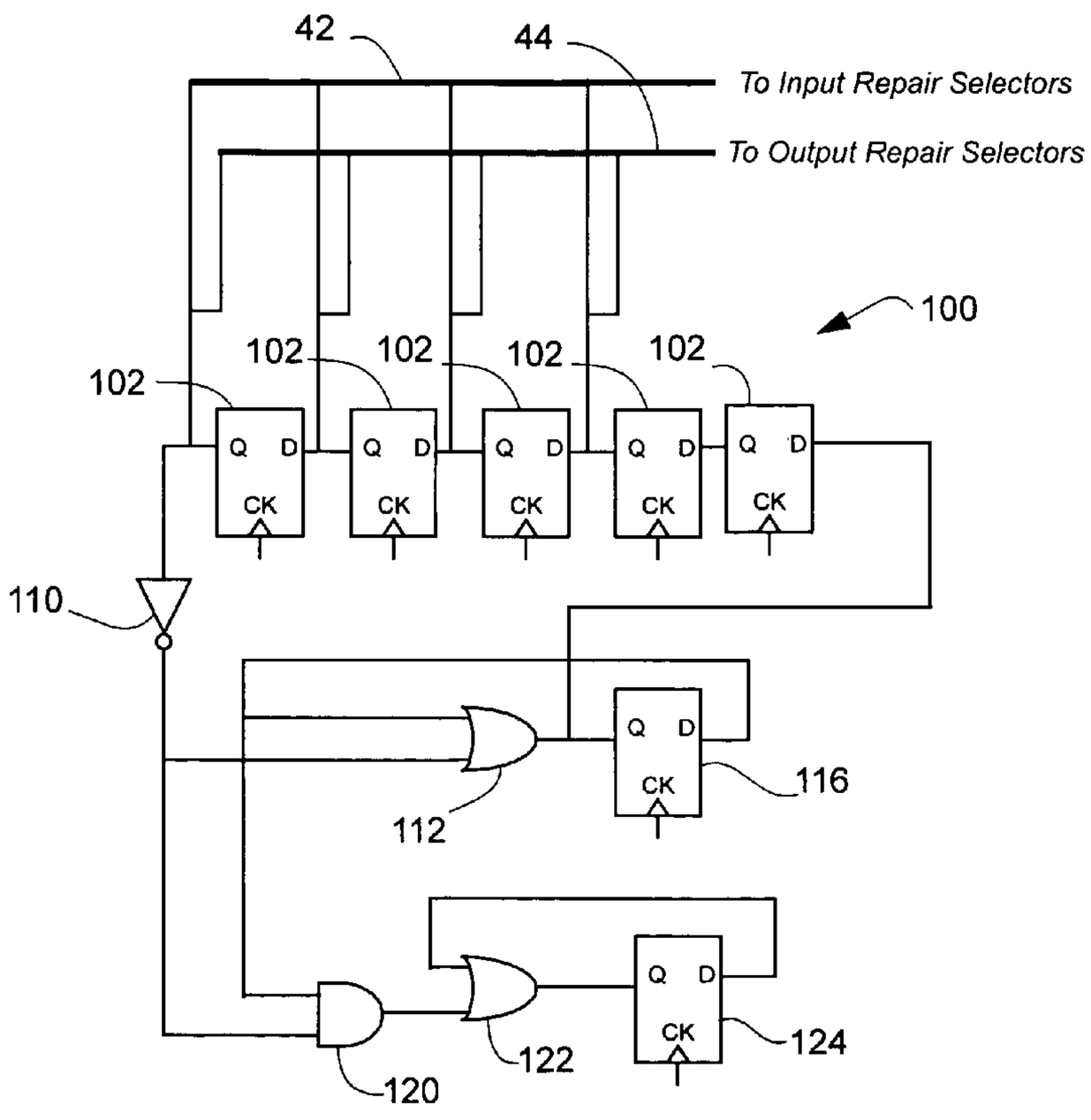
Primary Examiner—Michael Maskulinski
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A self-repair circuit for a semiconductor memory provides input and output test selectors coupled to respective data bit group inputs and outputs, respectively and input and output repair selectors coupled between the input and output test selectors and functional inputs and functional outputs, respectively. This arrangement allows all data bit groups to be tested in one pass and all test and repair selector circuitry to be tested.

18 Claims, 5 Drawing Sheets



US007370251B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,370,251 B2**
(45) **Date of Patent: May 6, 2008**

(54) **METHOD AND CIRCUIT FOR COLLECTING MEMORY FAILURE INFORMATION**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 804 days.

(21) Appl. No.: **10/690,594**

(22) Filed: **Oct. 23, 2003**

(65) **Prior Publication Data**

US 2005/0047229 A1 Mar. 3, 2005

(30) **Foreign Application Priority Data**

Dec. 18, 2002 (CA) 2414632

(51) **Int. Cl.**
G11C 29/00 (2006.01)

(52) **U.S. Cl.** **714/723**

(58) **Field of Classification Search** 714/723
See application file for complete search history.

(56) **References Cited**

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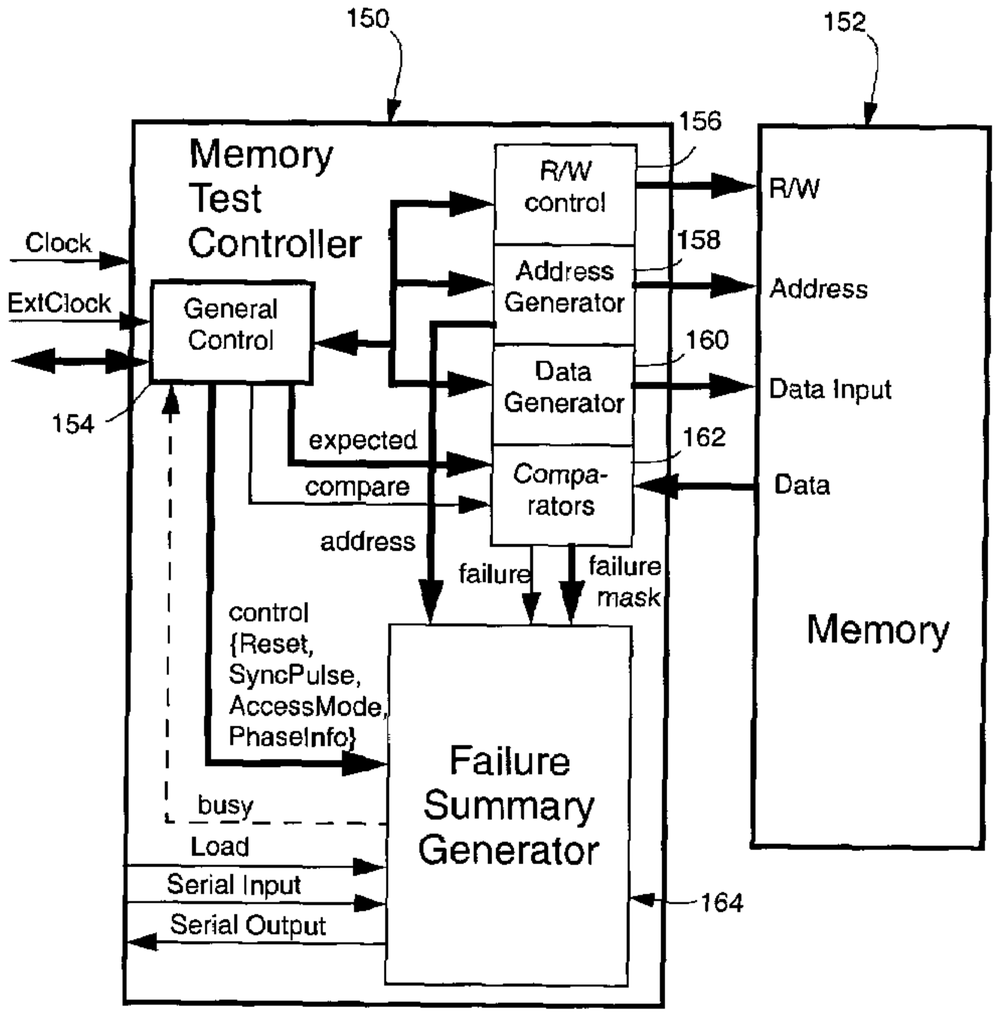
Primary Examiner—James C. Kerveros
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx; Dennis S. K. Leung

(57) **ABSTRACT**

A method and circuit for collecting memory failure information on-chip and unloading the information in real time while performing a test of memory embedded in a circuit comprises, for each column or row of a memory under test, testing each memory location of the column or row according to a memory test algorithm under control of a first clock, selectively generating a failure summary on-circuit while testing each column or row of the memory; and transferring the failure summary from the circuit under control of a second clock within the time required to test the next column or row, if any, of the memory under test.

54 Claims, 15 Drawing Sheets



US007424656B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,424,656 B2**
(45) **Date of Patent: Sep. 9, 2008**

(54) **CLOCKING METHODOLOGY FOR AT-SPEED TESTING OF SCAN CIRCUITS WITH SYNCHRONOUS CLOCKS**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-François Côté**, Chelsea (CA); **Fadi Maamari**, San Jose, CA (US)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 688 days.

(21) Appl. No.: **11/060,407**

(22) Filed: **Feb. 18, 2005**

(65) **Prior Publication Data**

US 2005/0240790 A1 Oct. 27, 2005

Related U.S. Application Data

(60) Provisional application No. 60/579,649, filed on Jun. 16, 2004, provisional application No. 60/564,210, filed on Apr. 22, 2004.

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/731**; 714/25; 714/709; 714/724; 714/726; 714/729; 714/744; 714/30

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

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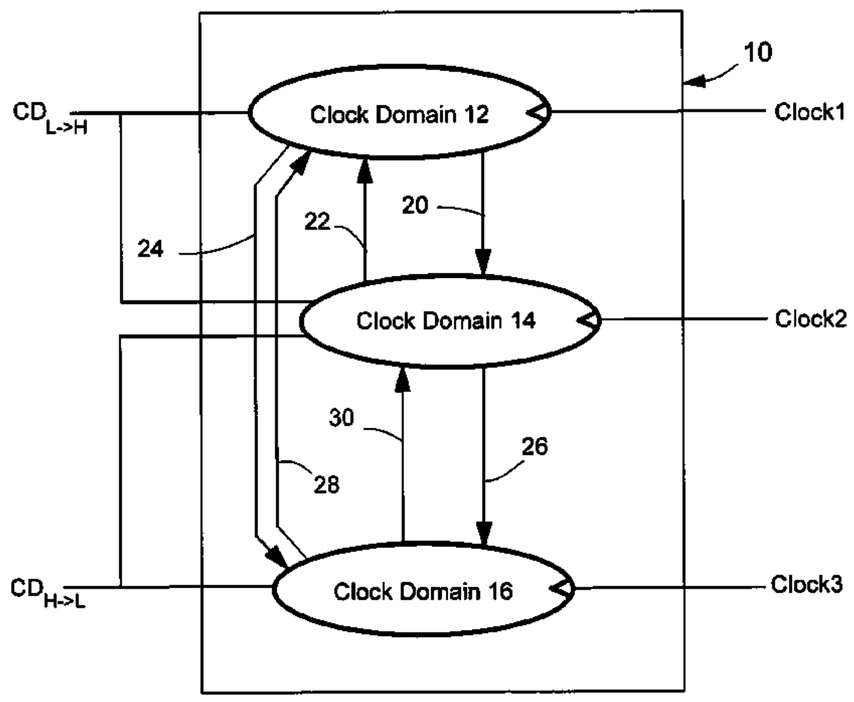
Primary Examiner—John P Trimmings
(74) *Attorney, Agent, or Firm*—Eugene E. Prouix; Dennis S.K. Leung

(57) **ABSTRACT**

A clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in a scan circuit, each path originating from a source memory element in one of the domains and terminating at a destination memory element in another of the domains and comprises selectively aligning either a capture edge or a launch edge of the clock of each domain with a corresponding edge of at least one other domain of the interacting synchronous clock domains to determine the cross-domain paths to be tested between a source domain and a destination domain; clocking memory elements in each domain at respective domain clock rates to launch signal transitions from source memory elements in source domains; and for each pair of interacting clock domains under test, capturing, in the destination domain, circuit responses to signal transitions launched along paths originating from the source domain and selectively disabling capturing, in the source domain, of circuit responses to signal transitions launched along paths originating from the destination domain.

21 Claims, 3 Drawing Sheets



US007617425B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,617,425 B2**
(45) **Date of Patent: Nov. 10, 2009**

(54) **METHOD FOR AT-SPEED TESTING OF MEMORY INTERFACE USING SCAN**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 188 days.

(21) Appl. No.: **11/439,497**

(22) Filed: **May 24, 2006**

(65) **Prior Publication Data**

US 2007/0266278 A1 Nov. 15, 2007

Related U.S. Application Data

(60) Provisional application No. 60/693,778, filed on Jun. 27, 2005.

(51) **Int. Cl.**
G11C 29/00 (2006.01)

(52) **U.S. Cl.** **714/719**; 714/5; 714/25; 714/30; 714/718; 714/723; 714/720; 714/726; 714/727; 714/729; 714/730; 714/732; 714/733; 714/734; 714/736; 714/742; 714/743; 365/201

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

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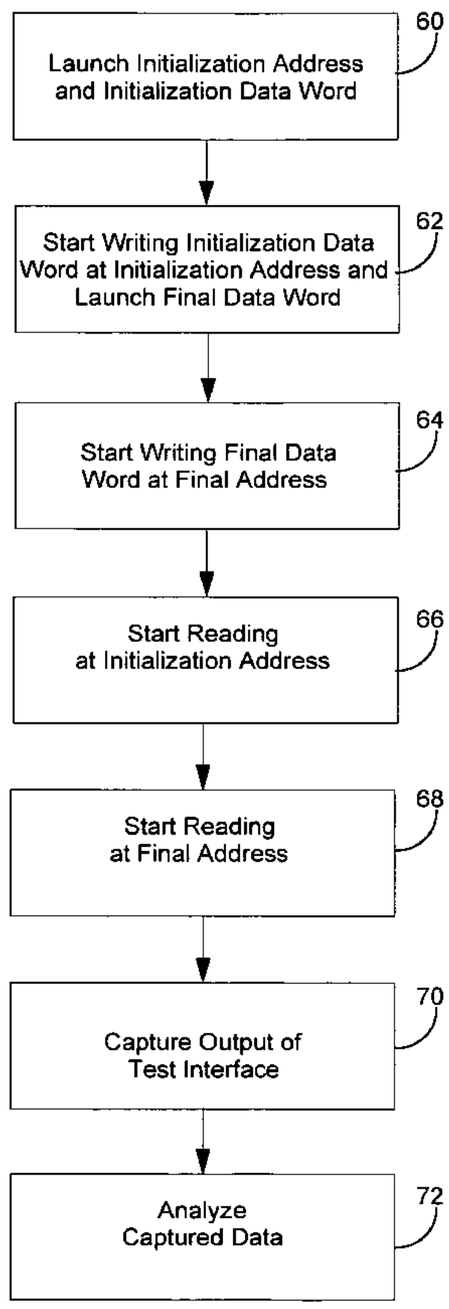
Primary Examiner—John P Trimmings
(74) *Attorney, Agent, or Firm*—Ridout & Maybee LLP

(57) **ABSTRACT**

A method and a circuit of testing of a memory interface associated with an embedded memory in a semiconductor circuit involves writing to two memory locations in succession; reading the two memory locations in succession in the same order in which the two memory locations were written; capturing output data from the memory interface; and analyzing captured output data to determine whether said captured output data corresponds to expected data.

27 Claims, 9 Drawing Sheets



US007757135B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,757,135 B2**
(45) **Date of Patent: Jul. 13, 2010**

(54) **METHOD AND APPARATUS FOR STORING AND DISTRIBUTING MEMORY REPAIR INFORMATION**

(75) Inventors: **Benoit Nadeau-Dostie**, Ottawa (CA); **Jean-François Coté**, Chelsea (CA)

(73) Assignee: **Mentor Graphics Corporation**, Wilsonville, OR (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 166 days.

(21) Appl. No.: **11/853,383**

(22) Filed: **Sep. 11, 2007**

(65) **Prior Publication Data**

US 2008/0065929 A1 Mar. 13, 2008

Related U.S. Application Data

(60) Provisional application No. 60/825,185, filed on Sep. 11, 2006.

(51) **Int. Cl.**
G11C 29/00 (2006.01)
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/723**; 714/711; 714/733

(58) **Field of Classification Search** 714/710, 714/711, 718, 723, 733
See application file for complete search history.

(56) **References Cited**

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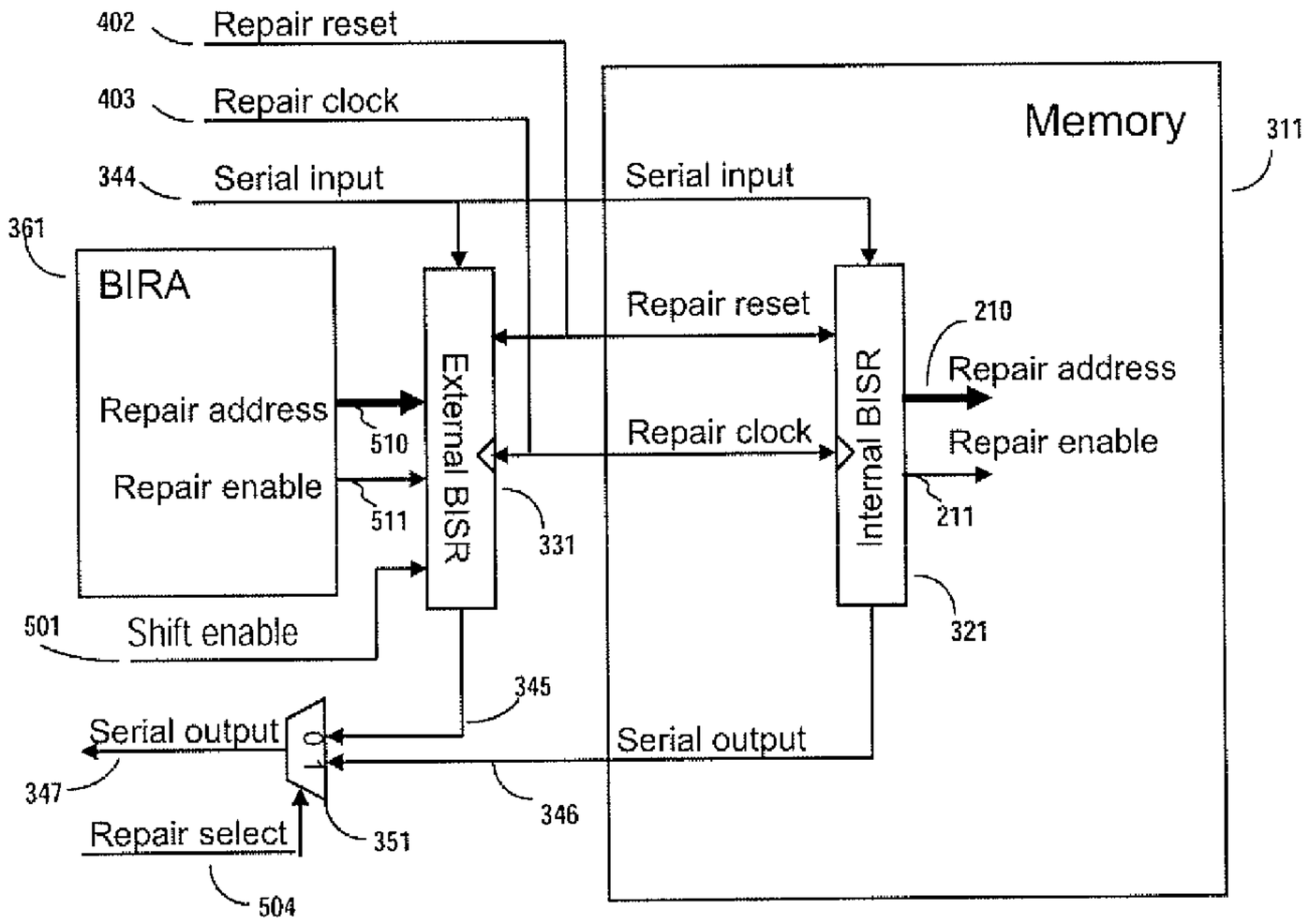
Primary Examiner—James C Kerveros
(74) *Attorney, Agent, or Firm*—Ridout & Maybee LLP

(57) **ABSTRACT**

A system for repairing embedded memories on an integrated circuit includes an external Built-In Self-repair Register (BISR) associated with every reparable memory. Each BISR is serially configured in a daisy chain with a fuse box controller. The controller determines the daisy chain length upon power up. The controller may perform a corresponding number of shift operations to move repair data between BISRs and a fuse box. Memories can have a parallel or serial repair interface. The BISRs may have a repair analysis facility into which fuse data may be dumped and uploaded to the fuse box or downloaded to repair the memory. Pre-designed circuit blocks provide daisy chain inputs and access ports to effect the system or to bypass the circuit block.

23 Claims, 9 Drawing Sheets



US008516317B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 8,516,317 B2**
(45) **Date of Patent: Aug. 20, 2013**

(54) **METHODS FOR AT-SPEED TESTING OF MEMORY INTERFACE**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-François Côté**, Gatineau (CA)

(73) Assignee: **Mentor Graphics Corporation**, Wilsonville, OR (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 290 days.

(21) Appl. No.: **13/018,279**

(22) Filed: **Jan. 31, 2011**

(65) **Prior Publication Data**

US 2012/0198294 A1 Aug. 2, 2012

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.**
USPC **714/726**; 714/733; 714/742

(58) **Field of Classification Search**
USPC 714/726, 733, 742
See application file for complete search history.

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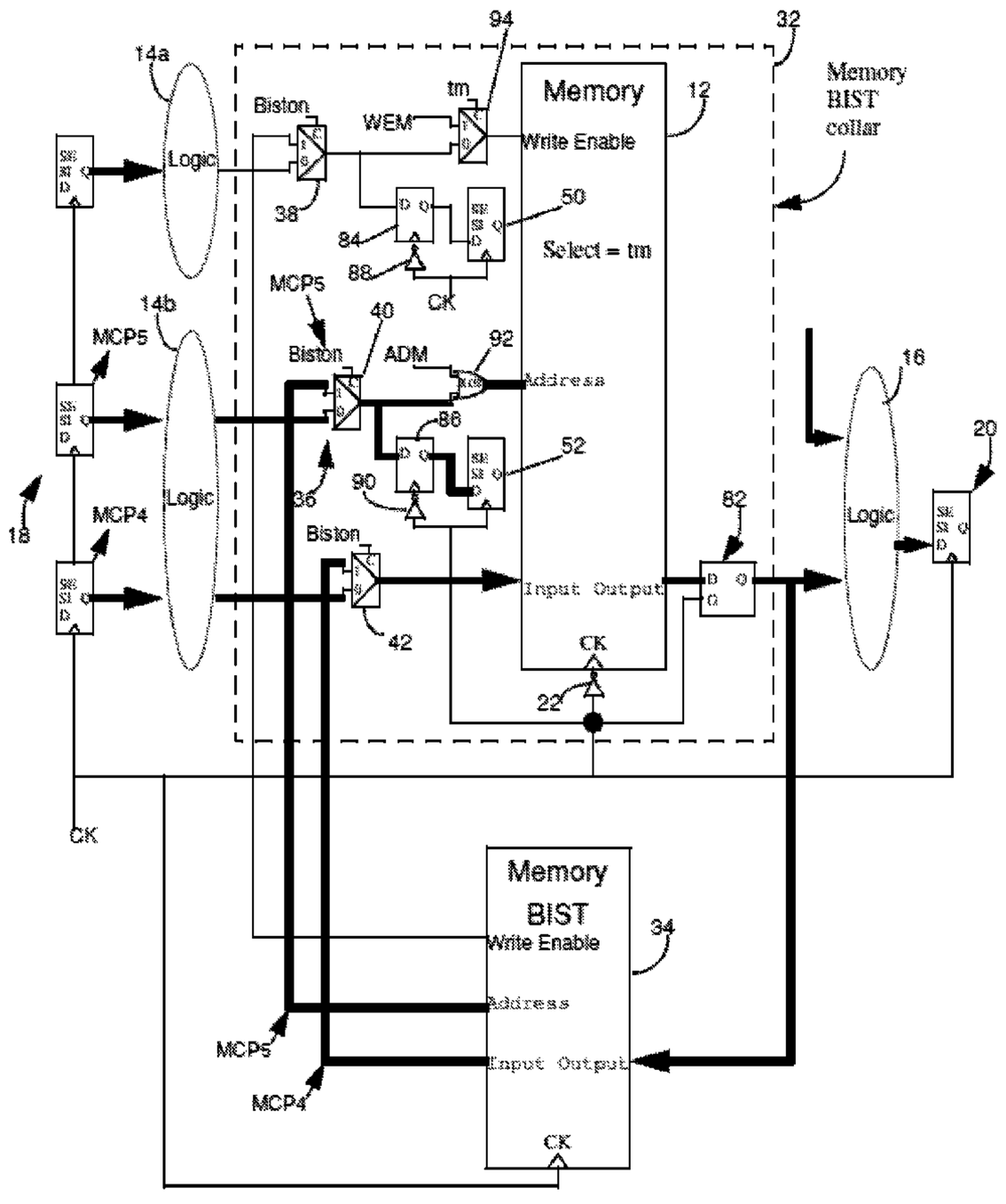
(57) **ABSTRACT**

Methods for at-speed testing of a memory interface associated with an embedded memory comprise two write operations in succession, two read operations in succession, and a capture operation using scan cells. The write and read operations are performed during a single clock burst, two separate clock bursts in a clock signal, or two separate clock bursts in separate clock signals.

31 Claims, 17 Drawing Sheets



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(12) **United States Patent**
Rajski et al.

(10) **Patent No.: US 8,683,280 B2**
(45) **Date of Patent: Mar. 25, 2014**

(54) **TEST GENERATOR FOR LOW POWER BUILT-IN SELF-TEST**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 141 days.

(21) Appl. No.: **13/451,527**

(22) Filed: **Apr. 19, 2012**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**
G01R 31/28 (2006.01)
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(52) **U.S. Cl.**
USPC **714/729**; 714/724; 714/726; 714/727; 714/728; 714/734; 714/736; 714/738; 714/739; 714/30

(58) **Field of Classification Search**
USPC 714/724, 726, 727, 728, 729, 738, 739, 714/734, 736, 30
See application file for complete search history.

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Primary Examiner — John J Tabone, Jr.

(57) **ABSTRACT**

Aspects of the invention relate to low power BIST-based testing. A low power test generator may comprise a pseudo-random pattern generator unit, a toggle control unit configured to generate toggle control data based on bit sequence data generated by the pseudo-random pattern generator unit, and a hold register unit configured to generate low power test pattern data by replacing, based on the toggle control data received from the toggle control unit, data from some or all of outputs of the pseudo-random pattern generator unit with constant values during various time periods. The low power test generator may further comprise a phase shifter configured to combine bits of the low power test pattern data for driving scan chains.

20 Claims, 15 Drawing Sheets