Structural test with functional characteristics

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Abstract

A novel structural test clocking architecture is proposed to reproduce characteristics of the functional mode of operation that are essential to a high-quality test. Bursts of functional mode clocks are controlled to provide accurate timing tests taking into account functional timing constraints such as multi-cycle paths and false paths. Any mix of asynchronous and synchronous clocks is supported. Long term (Idd, temperature) and short term (IR-drop) power characteristics related to circuit activity are independently controlled.

I. Introduction

Defects that affect circuit speed are becoming more prevalent and it is important to provide a thorough at-speed test. Another trend is the replacement of functional test by structural test methods to implement all tests. However, it is not trivial to implement an at-speed structural test. Circuits have several characteristics that complicate the task. Functional clocks can cover a wide frequency range. These clocks can be asynchronous (ie non-integer frequency ratio and/or unknown relative phase) or synchronous (ie their frequency ratio is fixed as well as their relative phase) to each other. Cross-domain paths must be correctly handled to prevent false timing violations caused by false paths while providing proper test of the interface logic. Within each domain, multi-cycle paths are sometimes used, instead of pipelining, to implement functions at a lesser cost. Gated clocks are used for low power designs. PLLs are used to control groups of synchronous clocks and/or multiply external reference clocks. Other aspects of the design affect the implementation of an at-speed test. The circuit is designed to perform at a certain temperature and supply voltage. The circuit activity has a direct influence on the local temperature and reduction of supply voltage (IR-drop) which in turn influence the timing. An at-speed structural test should be implemented such that the supply current, temperature and supply voltage drops can be controlled in a way that physical limits are not exceeded and, preferably, approach the conditions of the functional operation. An at-speed test method must be such that a minimum number of test-specific timing constraints are added to the design. These constraints must be easy to meet so that timing closure is not impacted.

II. Clocking scheme

The clocking scheme proposed in this paper addresses these issues. Clock bursts are applied to the circuit to reproduce characteristics of the functional mode of operation. The burst length is programmable. Burst lengths longer than 2 are needed to test multi-cycle paths [1] and deal with issues related to IR-drop. In [2], it was reported that the results of at-speed tests were different when using a burst of length of 2 as opposed to a free-running clock (ie “infinite” burst length). It is our experience as well that modifying the burst length will cause variations of the supply voltage and change the circuit timing. Some timing defects can only be identified if the burst length is sufficiently long to cause a supply variation that is comparable to the one observed during functional operation. The burst is modifiable at run-time to adjust the number of at-speed clock pulses applied.