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(54) **ASYNCHRONOUS INTERFACE FOR TRANSPORTING TEST-RELATED DATA VIA SERIAL CHANNELS**

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(57) **ABSTRACT**

A circuit comprises: a first clock gating device clocked by a first clock signal and configured to generate first clock pulses when a shift enable signal is active, a first transition detecting device clocked by a second clock signal and configured to generate shift gating pulses when detecting active transitions of the first clock pulses, a second clock gating device clocked by the second clock signal and configured to generate shift clock pulses based on the shift gating pulses to clock second scan elements for a shift operation with first scan elements clocked by the first clock signal, and a first retiming device triggered by active pulse edges of the first clock signal and configurable to hold a value for the shift operation. The circuit may further comprise a delay generating device configured to generate delayed shift gating pulses for generating the shift clock pulses.