US 20020143515A1

(19) **United States**

(12) **Patent Application Publication**

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(10) **Pub. No.: US 2002/0143515 A1**

(43) **Pub. Date: Oct. 3, 2002**

(54) **METHOD AND PROGRAM PRODUCT FOR MODELING CIRCUITS WITH LATCH BASED DESIGN**

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(21) Appl. No.: **09/817,298**

(22) Filed: **Mar. 27, 2001**

Publication Classification

(51) **Int. Cl.**[7] **G06F 9/45**

(52) **U.S. Cl.** **703/19**

(57) **ABSTRACT**

A method of and computer program product for modeling a logic circuit having combinational logic and latches, in which the latches are clocked by one of a first clock phase, a second clock phase or a pulse derived from the second clock phase, a subset of latches being scannable, comprises, for each latch in the logic circuit, associating the latch with one of the first and second clock phase; and when latch is associated with the first clock phase, modeling the latch as a buffer connected between the data input and output of latch; and when the latch is associated with the second clock phase, modeling the latch as an edge-triggered flip-flop having the same data input, data output and clock input as the latch.