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(54) **METHOD AND APPARATUS FOR TESTING CIRCUITS WITH MULTIPLE CLOCKS**

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(57) **ABSTRACT**

A method of testing a circuit having two or more clock domains at respective domain test clock rates and under control of a main test clock signal, the circuit having core logic, a plurality of scannable memory elements, each having a clock input, an input connected to an output of the core logic and/or an output connected to an input to the core logic, and configurable in scan mode in which the memory elements are connected to define one or more scan chains in each domain and in normal mode in which the memory elements are connected to the core logic in normal operational mode, the method comprising configuring the memory elements in scan mode; concurrently clocking a test stimulus into each scan chain of each clock domain including, for each clock domain having a domain test clock signal which is synchronous with respect to the main test clock signal, clocking the test stimulus at a shift clock rate derived from the main test clock signal and, for each clock domain having a domain test clock signal which is asynchronous with respect to the main test clock signal, clocking all but a predetermined number of bits of the test stimulus at a first domain shift clock rate derived from the main test clock signal followed by clocking the predetermined number of bits of the test stimulus at a second domain shift clock rate corresponding to the domain test clock rate; configuring the memory elements of each scan chain in normal mode in which the memory elements of each scan chain are interconnected by the core logic in the normal operational mode; clocking each memory element in each scan chain at its respective domain test clock rate for at least one clock cycle thereof; configuring the memory elements in scan mode; and clocking a test response pattern out of each of the scan chains at its respective domain shift clock rate during a respective scan-out interval, all respective scan-out intervals overlapping in time for a plurality of clock cycles at the highest of the respective clock rates.

34 Claims, 12 Drawing Sheets