

US 20120272110A1

(19) United States

(12) Patent Application Publication Rajski et al.

(10) Pub. No.: US 2012/0272110 A1 (43) Pub. Date: Oct. 25, 2012

54) TEST GENERATOR FOR LOW POWER BUILT-IN SELF-TEST

(76) Inventors: Janusz Rajski, (US); Jerzy Tyszer,

(US); Grzegorz Mrugalski, (US); Benoit Nadeau-Dostie, (US)

(21) Appl. No.: 13/451,527

(22) Filed: Apr. 19, 2012

Related U.S. Application Data

(60) Provisional application No. 61/477,105, filed on Apr. 19, 2011, provisional application No. 61/543,229, filed on Oct. 4, 2011.

Publication Classification

(51) **Int. Cl.**

G01R 31/3177 (2006.01) G06F 11/25 (2006.01)

(57) ABSTRACT

Aspects of the invention relate to low power BIST-based testing. A low power test generator may comprise a pseudorandom pattern generator unit, a toggle control unit configured to generate toggle control data based on bit sequence data generated by the pseudo-random pattern generator unit, and a hold register unit configured to generate low power test pattern data by replacing, based on the toggle control data received from the toggle control unit, data from some or all of outputs of the pseudo-random pattern generator unit with constant values during various time periods. The low power test generator may further comprise a phase shifter configured to combine bits of the low power test pattern data for driving scan chains.

