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Nadeau-Dostie et al.

(54) **METHOD AND CIRCUITRY FOR CONTROLLING CLOCKS OF EMBEDDED BLOCKS DURING LOGIC BIST TEST MODE**

(76) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-Francois Cote**, Chelsea (CA)

Correspondence Address:
LOGICVISION (CANADA), INC.
1525 CARLING AVENUE, SUITE 404
OTTAWA, ON K1Z 8R9 (CA)

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(57) **ABSTRACT**

One aspect of the invention is generally defined as a method of designing an integrated circuit for distributing test clock signals to embedded cores having at least one core functional clock input, the method comprising, for each core, providing a clock gating circuit for selectively disabling a core functional clock signal applied to a core primary clock input; and providing a core clock selection circuit for each secondary core functional clock input for selecting one of a core functional clock signal output by the gating circuit and a core test clock signal and applying a selected signal to the each secondary core functional clock input.