SCAN TESTING OF LATCH ARRAYS

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Abstract

A novel scan-based test method that allows latch-based arrays to be fully tested using conventional scan software tools is described. Very little support circuitry and simple modeling are required. Several useful applications of the method are described. The method was used on several production chips.

Introduction

A digital integrated circuit designed to be tested using scan design techniques must be decomposable into a set of registers and combinational blocks [1,2]. A popular style of scan, known as the Stanford style, requires the use of D-type flip-flops as the only valid storage element for registers. The registers are connected such that they operate as shift registers in a special mode of operation of the circuit called scan mode. In scan mode, the state of the registers can be controlled (observed) from a serial test input (output) pin. Figure 1 shows an example of such a circuit. Only one shift register (or scan chain) is shown for simplicity. The main advantage of this test method is that only the combinational part of the circuit needs to be considered during the test generation step. It is well known that the complexity of test generation for combinational circuits is significantly less than for sequential circuits.

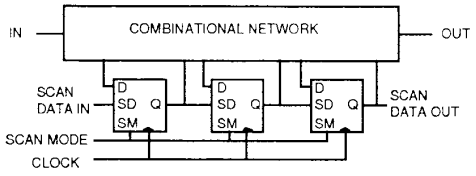

Figure 1

This test method can become expensive for register intensive designs. It would be nice to relax the requirement that imposes the use of full "scannable" D-type flip-flops for every storage element of the circuit under certain circumstances and yet be able to fully test these "illegal" storage elements using the same software tools. For example, small FIFOs, addressable control/status registers and other storage blocks are commonly found in digital circuits. Although these circuit structures can be built using arrays of "scannable" D-type flip-flops, it is more attractive to use transparent latches from a silicon area point of view (3 to 1 ratio on average). Embedded memories could also be used in some cases but they would require different test generation tools because of their specific failure modes [3-5]. Also, embedded memories might not be available for a particular technology, especially when gate-arrays are used.

We have devised a scan-based test method that allows latch-based arrays to be fully tested using conventional scan software tools. With the addition of support circuitry and some restrictions on how the latches may be connected, each latch may be modeled as a combinational gate to the pattern generation software.

This paper is divided as follows. The method is introduced in section II. Applications of the method are described in section III. Results are presented in section IV followed by the conclusion.

Method

The principle of the method is to make the transparent latches used to build the various registers and arrays look like combinational gates. This principle was used in [6]. In this paper, it was proposed to force all latches into their transparent mode for the whole duration of the scan test to verify the interface between the array and the rest of the circuit. However, this method can not test the ability for the latch to hold any data.

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