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Nadeau-Dostie et al.

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[54] **SERIAL TESTING TECHNIQUE FOR EMBEDDED MEMORIES**

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[58] **Field of Search** 371/21.1, 21.2, 21.3, 371/22.3, 22.2, 22.1, 22.5, 22.6, 25.1, 27; 365/201

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[57] **ABSTRACT**

A testing circuit interfaces serially with the data path of an embedded memory circuit formed from at least one memory unit having separated data input and output lines and tandem addressing. Part of the testing circuit is a series of two-input multiplexer units which are adapted to be embedded on the same chip as the memory circuit. The outputs of the multiplexer units connect to a respective one of the data input lines of the memory circuit. Excepting the first bit position, a first input of each multiplexer unit is adapted to connect to the data output line of the adjacent bit position in the memory circuit. The second inputs of the multiplexer units are adapted to connect to the data bus of the chip. A further part of the testing circuit is a finite state machine which is adapted to connect to the first input of the multiplexer unit at the first bit position and to the data output line at the least bit position. During testing, the finite state machine actuates the multiplexer units to connect the first bits, and for each address outputs a series of test bits, shifts those bits through the addressed word by a series of read and write operations, and examines those bit after their passage through the addressed word for defects in the memory circuit at that address. The finite state machine may or may not be embedded on the same chip as the memory circuit.

9 Claims, 7 Drawing Sheets