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(54) **METHOD OF MASKING CORRUPT BITS DURING SIGNATURE ANALYSIS AND CIRCUIT FOR USE THEREWITH**

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(57) **ABSTRACT**

A method of masking corrupt bits in test response pattern scan chains in an integrated circuit, comprising loading and applying a set of test patterns in the scan chains so as to obtain corresponding test response patterns; and masking bits of the test response patterns located in scan chains identified by a chain mask and at a position identified by a position mask.