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(54) **METHOD AND PROGRAM PRODUCT FOR DESIGNING HIERARCHICAL CIRCUIT FOR QUIESCENT CURRENT TESTING AND CIRCUIT PRODUCED THEREBY**

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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,067,091	A	*	11/1991	Nakazawa	716/3
5,459,737	A	*	10/1995	Andrews	714/733
5,592,493	A		1/1997	Crouch et al.	
5,796,990	A	*	8/1998	Erle et al.	716/4
5,939,897	A		8/1999	Ayers et al.	
5,949,692	A	*	9/1999	Beausang et al.	716/18
5,987,636	A	*	11/1999	Bommu et al.	714/738
6,061,284	A		5/2000	Dingemanse et al.	
6,093,212	A		7/2000	Takahashi et al.	
6,098,187	A		8/2000	Takahashi	
6,151,694	A	*	11/2000	Nozuyama	714/724
6,173,426	B1		1/2001	Sanada	
6,175,244	B1		1/2001	Gattiker et al.	
6,487,688	B1	*	11/2002	Nadeau-Dostie	714/726
6,516,432	B1	*	2/2003	Motika et al.	714/732
6,718,524	B1	*	4/2004	Mbouombouo	716/4
2001/0018756	A1		8/2001	Chang et al.	

* cited by examiner

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(57) **ABSTRACT**

A method of designing integrated circuits having an hierarchical structure for quiescent current testing, and the circuit which results therefrom is disclosed. The method comprises analyzing each of one or more selected hierarchical blocks independently of other selected blocks identify any circuit states of each block which could result in elevated quiescent current levels during quiescent current testing of the circuit, the analysis beginning with blocks at a lowest level of hierarchy and proceeding in sequence through each level of design hierarchy to a highest level of hierarchy containing a top-level block; and calculating a fault coverage for each selected block.

78 Claims, 8 Drawing Sheets