A High Speed Embedded Cache Design with Non-Intrusive BIST

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Abstract

This paper describes a 155 MHz wide-word cache design and its test integration features. Design techniques for high speed CAM with single ended match line sensing and highly integrated RAM are described. A new cache BIST algorithm based on the SMARCH [1] algorithm is presented. New techniques are described for the insertion of cache BIST access points into a high speed data path without compromising mission mode performance. Performance results of cache memory used for telecommunications microprocessor applications with 1Kb of CAM referencing a 5 Kb RAM are presented.

I. Introduction

With device gate counts and pin counts increasing and the cost of external functional testing rising, increases in hardware speed and functional complexity must be complemented by robust and complete self-test capability. The requirement to integrate special function macros into high speed data paths combined with the need to insert BIST for these components presents a potential conflict between performance and testability. One such macro, the cache design described here, provides high speed prefetched instruction storage and retrieval for a telecommunications processing application.

From its inception, the memory and BIST circuits were developed with the following objectives:

1) Accommodate the system cycle rate of 60 Mhz and various I/O overheads by completing the system address look-up compare cycle and the prefetched instruction RAM read within 12 ns, worst case (4.5V, 105°C).

2) Minimize active cycle power.

3) Incorporate into the cache's CAM and RAM blocks an interface that facilitates the connection of a cache BIST and is easily testable with functional vectors.

4) Design a BIST that has maximum memory fault coverage for both CAM and RAM blocks of the cache.

5) Insert the BIST circuitry into the high speed memory data path without incurring additional mission mode delay.

The memory performance and power objectives have been achieved by using a new self-timed CAM internal timing loop integrated tightly with the accompanying RAM read circuitry control signals. The self-timed nature of the cache give reasonable and predictable power consumption which increases linearly with frequency of operation. BiCMOS driver circuits used in the memories allow easy expansion from 4 to 256 rows and from 4 to 128 CAM compare data bits with no architectural change.

To achieve an easily testable cache interface, match line outputs are provided to the user to assist with on-chip diagnostics and cache BIST testing.

Cache BIST coverage is maximized by executing a complete SMARCH on the CAM read/write port while simultaneously running compare cycles on the compare port. Priority encoding of match line outputs ensures the correct hit/miss sequence. The CAM SMARCH sequence ends with a preload of the CAM with known states to

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