US007757135B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,757,135 B2**
(45) **Date of Patent: Jul. 13, 2010**

(54) **METHOD AND APPARATUS FOR STORING AND DISTRIBUTING MEMORY REPAIR INFORMATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 166 days.

(21) Appl. No.: **11/853,383**

(22) Filed: **Sep. 11, 2007**

(65) **Prior Publication Data**

US 2008/0065929 A1 Mar. 13, 2008

Related U.S. Application Data

(60) Provisional application No. 60/825,185, filed on Sep. 11, 2006.

(51) **Int. Cl.**
G11C 29/00 (2006.01)
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/723**; 714/711; 714/733

(58) **Field of Classification Search** 714/710, 714/711, 718, 723, 733
See application file for complete search history.

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(57) **ABSTRACT**

A system for repairing embedded memories on an integrated circuit includes an external Built-In Self-repair Register (BISR) associated with every reparable memory. Each BISR is serially configured in a daisy chain with a fuse box controller. The controller determines the daisy chain length upon power up. The controller may perform a corresponding number of shift operations to move repair data between BISRs and a fuse box. Memories can have a parallel or serial repair interface. The BISRs may have a repair analysis facility into which fuse data may be dumped and uploaded to the fuse box or downloaded to repair the memory. Pre-designed circuit blocks provide daisy chain inputs and access ports to effect the system or to bypass the circuit block.

23 Claims, 9 Drawing Sheets