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Nadeau-Dostie et al.

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(54) MEMORY REPAIR CIRCUIT AND METHOD

- (75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Saman M. I. Adham**, Kanata (CA)
- (73) Assignee: LogicVision, Inc., San Jose, CA (US)
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(56) References Cited

U.S. PATENT DOCUMENTS

6,052,798	A *	4/2000	Jeddeloh 714/8
6,065,134	A *	5/2000	Bair et al 714/7
6,246,618	B1 *	6/2001	Yamamoto et al 365/200
6,366,508	B1	4/2002	Agrawal et al.
6,374,370	B1 *	4/2002	Bockhaus et al 714/39
6,462,995	B2	10/2002	Urakawa
6,507,524	B1	1/2003	Agrawal et al.
6,667,918	B2	12/2003	Leader et al.
6,728,910	B1 *	4/2004	Huang 714/711
6,928,591	B2 *	8/2005	Grinchuk et al 714/710
2004/0117694	A1*	6/2004	Howlett 714/710
2004/0205427	A1*	10/2004	Ichikawa 714/710
2004/0237009	A1*	11/2004	Tester 714/710

^{*} cited by examiner

Primary Examiner—Michael Maskulinski (74) Attorney, Agent, or Firm—Eugene E. Proulx

(57) ABSTRACT

A self-repair circuit for a semiconductor memory provides input and output test selectors coupled to respective data bit group inputs and outputs, respectively and input and output repair selectors coupled between the input and output test selectors and functional inputs and functional outputs, respectively. This arrangement allows all data bit groups to be tested in one pass and all test and repair selector circuitry to be tested.

18 Claims, 5 Drawing Sheets

