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Nadeau-Dostie et al.

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(54) **METHOD FOR AT-SPEED TESTING OF
MEMORY INTERFACE USING SCAN**

(58) **Field of Classification Search** None
See application file for complete search history.

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(65) **Prior Publication Data**

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(57) **ABSTRACT**

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714/30; 714/718; 714/723; 714/720; 714/726;
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A method and a circuit of testing of a memory interface
associated with an embedded memory in a semiconductor
circuit involves writing to two memory locations in succes-
sion; reading the two memory locations in succession in the
same order in which the two memory locations were written;
capturing output data from the memory interface; and ana-
lyzing captured output data to determine whether said cap-
tured output data corresponds to expected data.

27 Claims, 9 Drawing Sheets

