A Scan-Based BIST Technique Using Pair-Wise Compare of Identical Components

Benoit Nadeau-Dostie *, Philip S. Wilcox *, Vinod K. Agarwal **

* Bell-Northern Research Ltd.,
P.O. Box 3511 Station C
Ottawa, Ontario, Canada K1Y 4H7

** Department of Electrical Engineering
McGill University, 3480 University Street
Montréal, Québec, Canada H3A 2A7

Abstract

This paper addresses the problem of efficiently testing scannable ASICs in a board-level and system-level environment. The method makes use of a serial testability bus (ETM or IEEE 1149.1) and takes advantage of the presence of identical components on the boards. The main benefits of the method are a significant reduction in test time and test data to be stored. Results obtained for an actual system show a reduction in test time of about 20 times for a module with 50 ASICs. The extra board area required was less than 2% for all boards of the module.

Introduction

This paper addresses the problem of efficiently testing scannable Application Specific Integrated Circuits (ASICs) in a board-level and system-level environment. A new Scan-based BIST technique is described and the results of its application to an actual system are presented. The method makes use of a serial testability bus (IEEE 1149.1 or ETM) and takes advantage of the presence of identical components on the boards.

The paper is organized as follows. The first section describes the system used as the test vehicle for the new testing method and its main test features. The second section presents a possible test procedure and highlights the issues associated with conventional scan testing at the board and system level. The third section describes the key components of the proposed test and diagnosis procedure (Pair-Wise Compare or PWC method) which is detailed in section 4. The fifth section discusses the costs and benefits of the procedure in general and for the particular system described in the first section. Conclusions are drawn from that experience in the last section.

1) System and test features

The system module to be discussed is composed of 4, or optionally 5, Printed Circuit Boards (PCBs), backplane and a processor card (see figure 1). A complete system consists of dozens of such system modules. The Port boards perform the Input/Output operations of the system. The module contains of order 50 ASICs but with less than 10 unique types. On figure 1, each fill pattern can be associated to an ASIC type (the number of instances is not necessarily exact). The main boards have 15 to 20 ASICs each.

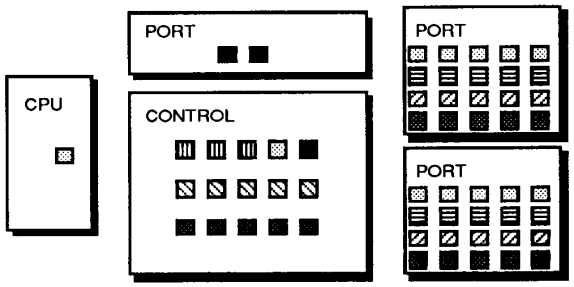

Figure 1 Schematic view of the module showing the ASIC distribution

The ASICs are scan-testable designs, with boundary scan as an integral component. Memories are tested using specialized self-test methods described in [1]. A standard serial slave interface on each chip is used for test access and control. The five-pin testability bus is similar to the Element Test and Maintenance

(ETM) bus developed for the U.S. DOD VHSIC program [2]. The module-level test bus connects the Test Access Ports (TAP) of each ASIC to form a serial scan chain (ring configuration). This test bus can be accessed at the edge connector of each PCB, or through the test bus 'master' located on the CPU board when the boards are connected to the module (see figure 2). The test bus was extended to improve the efficiency of the test procedure. This extension of the bus is described in section 3.

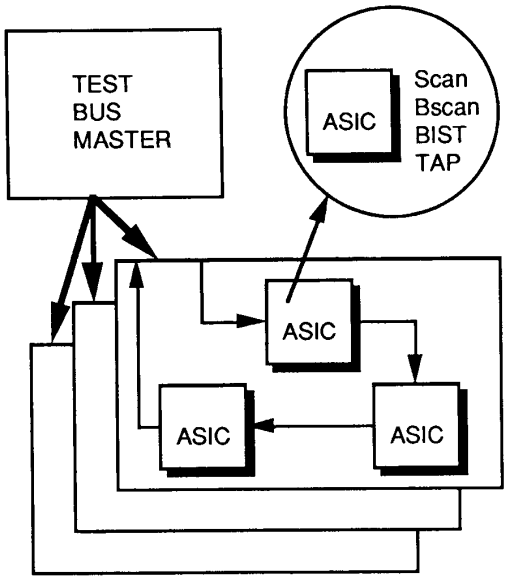

Figure 2 Test hierarchy of the module

The processor board contains a CPU (Motorola 68030), ROM, RAM and an ASIC to perform various memory management and timer functions. As well, this device contains the test bus master function (see figure 3). The test bus master provides an interface to the CPU and memory for deterministic test/instruction sequences and also contains Linear Feedback Shift Registers (LFSRs) configured for random pattern test generation and signature analysis (SA), making the board self-testable to some extent [5]. The 32-bit registers can be loaded with an appropriate seed but the polynomial used is not programmable [6]. The other parameter that needs to be specified is the length of the scan chain of each ASIC under test. The processor card ASIC is scannable and the master interface can be forced into slave mode for external scan test of the chip by Automated Test Equipment (ATE).

This module architecture provides test flexibility in that, not only can the module be self-tested with its own CPU acting as master, or ATE scan tested from an edge connector (with test bus master forced into slave mode), but each Printed Circuit Board (PCB) can be scan tested by ATE via the edge connector.

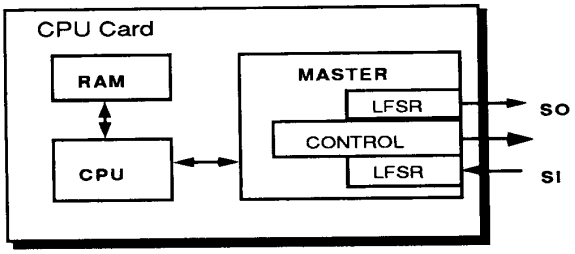

Figure 3 Processor board and test bus master

2) Conventional test procedure and associated issues

The first step of any ASIC test procedure at the module level is a sanity test of the testability bus itself and the Test Access Port (TAP) of each ASIC. On synchronous (or optionally asynchronous) reset of the TAPs, the instruction registers are loaded with a specific sequence that can be shifted out for examination at the test bus master. When a break in the sequence is detected, a simple diagnostic routine indicates which connection of the board or which ASIC is faulty. During the second step, one ASIC is programmed to perform a scan test and all others are put in the bypass mode. Note that this bypass mode involves a one-bit delay in the scan path. This is true for both the ETM and IEEE 1149.1 standards [3]. Finally, the test patterns to each selected ASIC can be applied from the test bus master and the output response can be collected at the test bus master. The second and third steps of the procedure are repeated for each chip.

The main problems with this test procedure are test time and pattern storage. With the serial access method, we are restricted to testing one ASIC at a time, using either stored deterministic vectors or random vectors, and using either stored responses or Signature Analysis (SA). The pattern storage

problem is not a major issue for ATE-based manufacturing test, however pattern storage becomes a problem for module self-test or field self-test because of two factors: limited memory capacity for permanent pattern storage in the CPU card and a limited bandwidth for access to external storage.

For the module under consideration, the number of flip-flops in an ASIC scan chain varies between 700 and 1500. The average is close to 1000. The number of patterns applied is also around 1000 for stored patterns and about 100000 for random patterns. So, for the 50 chips of the module, the test time is approximately 100 seconds for stored patterns applied at 0.5 MHz and about 500 seconds for the random patterns at 10 MHz. For the stored patterns, the requirement is about 2Mbits for each type of ASIC (about 20Mbits total). The random pattern approach was favored mainly because of the small amount of storage required even for individual board testing using an ATE.

Two minor issues related to random pattern testing still needed to be resolved. First, the presence of the bypass registers makes the signature of a chip sensitive to its location on the scan chain. The signatures, and optionally the fault coverage, can either be recomputed for each configuration or "learned" from known good boards. The variation in fault coverage is typically less than 1% for the large number of patterns (100000) applied. The second issue is the aliasing introduced by the signature analysis process [7,8]. All these issues are addressed by the Pair-Wise Compare method described next.

3) Pair-Wise Compare method

The strategy proposed in [4] to minimize both the test time and test storage requirements in a scan-based system like the one described above is to embed both a random pattern source and a signature analyser within each ASIC. This method is applicable in general but adds to the size and the design complexity of the ASICs and is still subject to aliasing. Our method takes advantage of the fact there are multiple copies of most ASICs in the system. The basic method is to apply the same random patterns to all chips at the same time and compare the response of identical chips. It is a form of golden standard testing eliminating the aliasing problem [10]. Also, since the testing proceeds in parallel, a substantial reduction in total test time can be achieved.

To deliver patterns in parallel to the ASICs requires a minor hardware addition to the Test Access Port (TAP). One extra pin per chip is required (PSI on figure 4 and 5). All the PSI pins are connected together and to the regular output of the test bus master and the normal serial input (SI) of the first ASIC, as shown in figure 4. This test bus configuration is a hybrid combining the advantages of the star (direct access to individual chips through PSI without addressing) and the ring configuration (global signals are used except for the serial inputs and outputs).

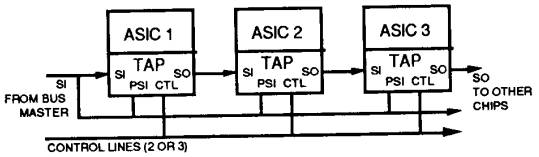

Figure 4 Connection of the parallel input (PSI) to all chips of the board

To enable the most efficient usage of the PWC method, a specific chip connection arrangement must be used on the test serial data bus. All the identical chips must be adjacent on the scan chain since each chip will compare its own serial output with the serial output of its predecessor on the scan chain. Single devices must be at the end of chain to simplify the access to the signature analyser of the test bus master. For the system considered in this paper, there was only one ASIC that was not used more than once. For this ASIC, the output compaction was performed at the test bus master while parallel test proceeded on the other devices. This is an ideal case since both the random pattern generator and the signature analyser are directly connected to the chip. However, this was an exceptional case and we developed two techniques to perform the signature analysis in the case where more than one ASIC with only one instance is present in the system. Both techniques involve the modification of the behavior of the bypass register of the chips located between the chip under test and the signature analyser on the test bus master. These modifications only affect the bypass register during the self-test mode but still comply with the rules of the test bus standard for all the other modes of

operation. One of the techniques is the "zero-delay bypass" feature described in section 4.

The comparator circuitry added to the TAP of each chip consists of one flip-flop, one OR gate, one Exclusive-OR gate and two multiplexers (see figure 5). It can be seen that the regular serial input (SI) is used as the reference to compare against the output of the chip and that the parallel input (PSI) is used to provide the random data to the scan chain. The first error detected will cause the flip-flop to latch a value of one. The flip-flop will remain in this state until it is reset at the end of the self-test. The multiplexer driving the serial output (SO) pin is used to implement the "zero-delay bypass" mode (see section 4).

4) Test procedure and diagnostic

The test bus sanity test is performed as described in section 2. The PWC circuitry is then tested and the actual self-test begins. The test procedure is as follows.

1) Put all chips in scan mode via an instruction sequence
2) Flush the scan chains on all chips with zeroes
3) Initialize the PWC circuitry (reset flip-flop (FF) and select PSI as serial input data)
4) Scan in a random test pattern
5) Enter mission mode for one clock cycle
6) Scan in the next random pattern while comparing the output responses from the previous pattern
7) Repeat 5 and 6 as many times as required
8) Scan out the status register of each ASIC in which the compare results have been captured.

The interpretation of the results is relatively simple given that each type of ASIC has at least 3 instances on the board and if we can assume that no more than a single failure is likely to happen in each ASIC type. For example, consider the case where exactly 3 identical chips are compared to each other. Table 1 shows all possible results that can be obtained. Chip 1 will always indicate a "fail" condition since it is comparing its output with random data coming from the test bus controller or the output of a chip of a different type. So, the first possibility in the table indicates that all chips are good. In the second case, the "fail" condition returned by chip 3 suggests that either chip 2 or 3 is faulty but since chip 2 passed the comparison with chip 1, chip 3 is definitely the bad one. The third case is resolved using a similar reasoning. Finally, in the last case, chip 2 is the faulty one.

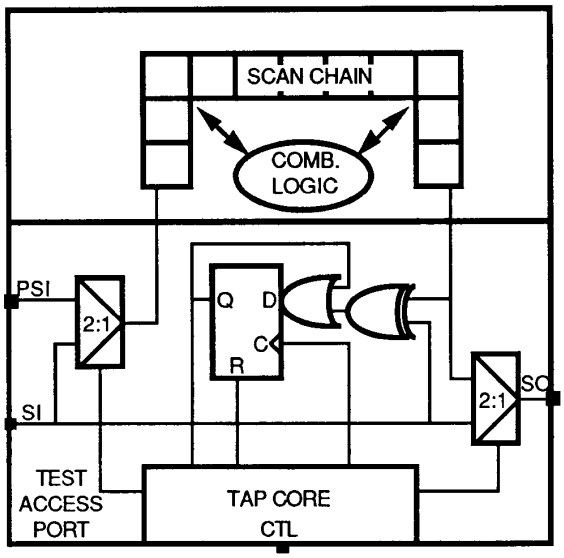

Figure 5 Detail of a single chip showing the modification to the Test Access Port (TAP)

In the multiple fault scenario, the situation is slightly more complex and provides only detection but no diagnosis in some cases. In our example, if any two or three chips are faulty, the status is FFF (case 4 in table 1). Under the single fault assumption, we concluded that chip 2 was the faulty one. However, 4 different possibilities exist under the multiple fault assumption.

Status			Diagnostic		
Chip #			Chip #		
1	2	3	1	2	3
F	P	P	G	G	G
F	P	F	G	G	B
F	F	P	B	G	G
F	F	F	G	B	G
F=Fail P=Pass			B=Bad G=Good		

Table 1 Diagnostic based on chips status

The diagnostic resolution is increased by repeating the test but programming the multiplexer driving the serial output of chip 2 so that the output of chip 1 is presented to chip 3 to use as the reference data. Chip 2 is then said to be in the "zero-delay bypass" mode. If chip 3 returns a "pass" condition after the test, it means that only chip 2 is faulty. If it still returns a "fail" condition, more than one chip is faulty and the signature analyser must be used to identify the ones to be replaced. The need to use signature analysis decreases rapidly when a large number of identical chips is present. This is because each chip can be compared to more than two neighbours using the "zero-delay bypass" feature. The number of consecutive chips programmed to use the "zero-delay bypass" might limit the frequency of the test. This is not an issue since our test board controller has a programmable test clock and the frequency on an ATE can be adjusted at will.

When only two instances of a chip are consecutive on the scan chain, the signature analyser is required if both chips report a "fail" condition. For that reason, they are put close to the signature analyser, just before the chips having a single instance. The "zero-delay bypass" feature can be used to connect the output of each such chip to the signature analyser.

5) Costs and benefits

The main costs of implementation of this method are:

1) An extra pin on each ASIC (PSI)
2) An extra track on each circuit board
3) Additional area on the board due to the constrained ordering of the scan chain
4) A few gates added to the TAP of each ASIC
5) Slightly more complex programming for the diagnostic program

For ASICs of more than 100 pins, it is rare that the extra pin can not be accomodated. The extra board area in the system described in section 1 was limited to less than 2% for all boards of the particular system presented in this paper despite the fact that the chain ordering was not very compatible with the physical arrangement of the different chips on the control board. Instead of having all identical chips grouped together, the chips were arranged in identical clusters composed of several types of ASICs. So, the scan chain had to travel from cluster to cluster all around the board.

Significant reduction in test length and pattern storage requirements are the main benefits of this method. When random patterns are used, the test length is determined by the product of the longest scan chain and the largest number of patterns to be applied for any of the chips. The results are optimum when the chips with the longer scan chain are also the ones that require the more scan patterns to be applied to them. If this is not the case, it might be advisable to test the chips with the longest scan chain(s) in the first pass and the other chips in a second pass. In all cases, it is advisable to insert test points to make the chips more susceptible to random patterns. When deterministic patterns are used, one test set unique to each device type is required and they are applied sequentially. When one type of device is tested, the other ASICs can still compare their output to their neighbour to potentially increase the coverage of unmodeled faults [9].

For the system described here, we exclusively used random patterns and reduced the test time of the random logic section of the ASICS by a factor of about 20 (i.e. a little less than 10 seconds as opposed to a little more than 3 minutes) by using the Pair-Wise Compare method. This time is comparable to the time it takes to run the self-test on the embedded memories. In terms of data pattern storage, only a few hundred bytes are necessary to perform the complete test procedure. In a ring configuration, all instruction registers are concatenated when entering the instruction mode. The TAP bits used to control the self-test modes have been standardized such that the same instruction can be sent to all chips. Otherwise, each instruction to be sent would require 16 times the number of ASICs of storage in RAM because the length of the instruction registers is standardized to 16.

Conclusions

A new method of testing scannable ASICs in a board-level and system-level environment was presented. The method makes use of a serial testability bus (ETM or IEEE 1149.1) and takes advantage of the presence of identical components. The test bus controller provides random data to all chips which compare their output to the output of their predecessor on the scan chain. The main benefit of the method is a potential reduction in test time proportional to the number of chips (random

pattern case) or to the ratio of the total number of chips over the number of unique types of chips (deterministic pattern case). The amount of test data to be stored is very small in the random pattern case. The comparison of chips eliminates the uncertainty associated with aliasing when signature analysis methods are used . Results obtained for an actual system show a reduction in test time of about 20 times for a system with 50 ASICs of 10 different types. The extra board area required was less than 2% for all boards of the system.

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