SERIAL INTERFACING FOR EMBEDDED-MEMORY TESTING

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The authors present a serial interfacing scheme in which several embedded memories share the built-in, self-test circuit. For external testing, this approach requires only two serial pins for access to the data path. There is considerable savings in routing area and fewer external pins are needed to test RAMs with wide words, such as those in telecommunication ASICs. Even though the method uses serial access to the memory, a test pattern is applied every clock cycle because the memory itself shifts the test data. The authors have adapted this method to four common test algorithms. In their implementations of the BIST circuitry on several product chips, they found the area overhead acceptable.

Application-specific digital ICs have become increasingly memory intensive in recent years. The design flexibility and performance offered by module generators for single-port and multiport SRAMs and content-addressable memories are opening up new possibilities in system design as the constraint of standard memory dimensions and operating modes is relaxed. However, these new possibilities in design are posing several new challenges for test. For example, today's telecommunication ICs often have a variety of multiport memories on one chip, some with very wide words. External testing becomes complex because it is difficult to bring all the signals to the pins. Tester hardware and design-automation tools also impose limitations on external testing because usually neither can support the large algorithmic pattern sequences in simulation or high-level test generation. Moreover, even if an algorithmic memory test was expanded into individual vectors, they still must be stored and loaded. These requirements could easily exceed a tester's maximum pattern depth, particularly if the patterns had to be multiplexed.

It is these challenges to external testing that are making built-in self-test more attractive to chip designers and manufacturers. Additional incentives for BIST are the ability to provide full-speed tests with minimal test hardware and the reuse of these tests for diagnostics at the board and system levels.

Various BIST algorithms and techniques have been proposed,[1-8] most of which evaluate all the bits of a memory word in parallel as it is read. Some[1,4,6,7] require modification of the RAM circuitry, which may not be practical or even possible in many ASIC design environments. Others[4,6,7] perform signature analysis and then compress the data. These techniques must then consider aliasing uncertainties when calculating fault coverage.[9] We can encounter significant problems when applying these BIST schemes to chips that have multiple embedded RAMs of varying sizes and port configurations. If each memory required a dedicated BIST circuit, the chip area devoted to testing would be unacceptably high. A better approach is to share BIST circuitry among several RAM blocks. We would also want to reuse as much test circuitry as possible in the normal operation of the chip, called the mission mode. With existing BIST schemes, sharing the circuitry between BIST and mission mode can be quite difficult.

Our solution is a serial interfacing technique for embedded RAMs that allows the BIST circuit to control a single bit of a RAM's (or group of RAMs') input data path. Only one bit of the output data path is available to the BIST circuit for observation while the test algorithms are executed.

0740-7475/90/0004-52$1.00©1990 IEEE