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(54) **HIERARCHICAL DESIGN AND TEST METHOD AND SYSTEM, PROGRAM PRODUCT EMBODYING THE METHOD AND INTEGRATED CIRCUIT PRODUCED THEREBY**

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(57) **ABSTRACT**

A method for use in the hierarchical design of integrated circuits having at least one module, each the module having functional memory elements and combinational logic, the method comprising reading in a description of the circuit; replacing the description of each functional memory element of the modules with a description of a scannable memory element configurable in scan mode and capture mode; partitioning each module into an internal partition and a peripheral partition by converting the description of selected scannable memory elements into a description of peripheral scannable memory elements which are configurable in an internal test mode, an external test mode and a normal operation mode; modifying the description of modules in the circuit description so as to arrange the memory elements into scan chains in which peripheral and internal scannable memory elements of each module are controlled by an associated module test controller when configured in internal test mode; and peripheral scannable memory elements of each module are controlled by a top-level test controller when configured in an external test mode; and verifying the correct operation of the internal test mode and the external test mode of the circuit.

75 Claims, 7 Drawing Sheets