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(54) **METHOD AND CIRCUIT FOR COLLECTING MEMORY FAILURE INFORMATION**

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(57) **ABSTRACT**

A method and circuit for collecting memory failure information on-chip and unloading the information in real time while performing a test of memory embedded in a circuit comprises, for each column or row of a memory under test, testing each memory location of the column or row according to a memory test algorithm under control of a first clock, selectively generating a failure summary on-circuit while testing each column or row of the memory; and transferring the failure summary from the circuit under control of a second clock within the time required to test the next column or row, if any, of the memory under test.