MBIST Supported Multi Step Trim for Reliable eMRAM Sensing

Jongsin Yun
Mentor, A Siemens Business
Wilsonville, USA
jongsin_yun@mentor.com

Benoit Nadeau-Dostie
Mentor, A Siemens Business
Ottawa, Canada
benoit_nadeau-dostie@mentor.com

Martin Keim
Mentor, A Siemens Business
Wilsonville, USA
martin_keim@mentor.com

Lori Schramm
Mentor, A Siemens Business
Atlanta, USA
lori_schramm@mentor.com

Cyrille Dray
ARM
Sophia Antipolis, France
cyrille.dray@arm.com

Mehdi Boujamaa
ARM
Sophia Antipolis, France
mehdi.boujamaa@arm.com

Khushal Gelda
ARM
Bangalore, India
khushal.gelda@arm.com

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***Abstract*—eMRAM (embedded Magnetoresistive Random Access Memory) has many attractive properties such as small size, fast operation speed, and good endurance. However, MRAM has a relatively small TMR (Tunneling Magnetoresistance) ratio, which means a small on-off state separation. It is a challenge to set an optimal reference resistance to reliably differentiate "1" and "0" states. Several trimming circuits were suggested in the literature to adjust a reference value and its search range. The trim setting can be controlled manually by user input; however, it consumes huge test time and requires off-chip engineering analysis to search and apply a trim setting for an individual memory array. In this paper, we will discuss the recent silicon results of fully automated trim process leveraging existing MBIST (Memory Built-in Self-Test) resources and new features to accommodate more complicated multi-step reference setting implementation through minor update of an existing MBIST circuit. The proposed MBIST solution uses a minimal number of tests to analyze massive array properties and automatically set complicated multi-step trim settings within a chip without the need for an external tester or manual adjustments.**

Keywords—MRAM, BIST, yield, reference trim, read operation.

I. Introduction

STT (Spin- Transfer Torque)-MRAM is a type of memory that encodes data as a spin polarity of magnets in its ferromagnetic metal layer. The electron spin polarity of the layer switches based on the write-current direction. As a result, the MRAM cell can be switched to either a high resistance state (anti-parallel, R_{AP}) or a low resistance state (parallel, R_P) [1, 2]. During the Read operation, a sense amplifier latches a differential between the developed voltage or current level of the selected BL (bit line) relative to that of a reference BL. Therefore, the reference level (either resistance, voltage, or current) is one of the most important settings for reliable data sensing.

Due to process variations, On state and Off state memory has a certain range of resistance distribution similar to a normal distribution. An example of On and Off state resistance distribution of an MRAM array is illustrated in Fig. 1 (a). To read all memory data correctly, the reference resistance should be set between the distribution tails of the highest R_P and lowest R_{AP} values. The optimum reference setting is especially challenging in MRAM because the On and Off state resistance separation is relatively narrow compared to other types of resistive memories by an order of magnitude. The small separation of the on/off resistance makes reference setting even more sensitive to variations of resistances, which inevitably happen due to process shift, array configuration, total array size, temperature use case, etc. For that reason, using a fixed hardware preset R_{REF} for the entire array is quite risky to make large array applications. An incorrect reference setting leads to incorrectly interpreting the data, and it also limits the speed of read operation until a suitable differential level is achieved. The silicon measurement results summarized in section IV, allow you to visualize different optimum trim settings required for each individual array segment in the tested chips. To mitigate the reference setting issue, several trimming circuits were suggested in recent MRAM applications which allow post-process reference value control [3, 4]. The reference trim process allows for the update of reference values relative to accessed array properties and improve read margin for reliable sensing; thus ultimately improving yield.

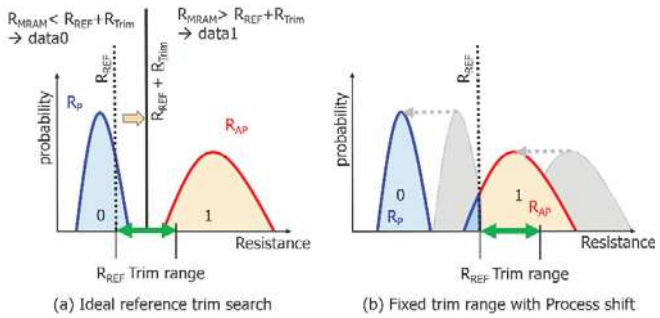

Fig. 1. Distribution of MRAM resistance for value "1" and "0" with sensing reference resistance setting

A trim search function is very efficient when it is executed as a part of MBIST. MBIST can test a chip without using expensive ATE (Automatic Test Equipment), and it is able to automatically evaluate the individual trim setting for each array based on a real-time measured test result. Although a trim search can be accomplished through external IO, collecting and analyzing the full set of memory data for each trim setting is a painful challenge. It requires an impractically large amount of