A Serial Interfacing Technique for Built-In and External Testing of Embedded Memories

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ABSTRACT

This paper describes the design and implementation of a test access method and built-in self-test scheme for embedded static RAMs based on a new serial interfacing technique.

INTRODUCTION

Various BIST algorithms and techniques have been proposed [1-6,9,11] to test RAMs. All of the techniques cited evaluate all the bits of each memory word in parallel as it is read. A comparator or compressor module is then usually used for each bit of the output data path. This may be costly in terms of area for wide data paths. Some of the BIST schemes [1,4-6,9] require modifications of the RAM circuitry which may not be possible or practical in many ASIC design environments. When signature compression of the data is used [4,6,9], it adds the problem of aliasing uncertainties to the calculation of fault coverage [8]. There is also a significant problem in applying all schemes cited above when multiple embedded RAMs of varying sizes and port configurations are used on one chip. If each memory requires its own dedicated BIST circuit, the chip area devoted to testing can be unacceptably high. Therefore, it is advantageous to share the BIST circuit among several RAM blocks. It is also desirable to re-use as much of the test circuitry as possible in the normal operation of the chip. It can be quite difficult or inefficient to achieve this sharing of circuitry with the existing schemes.

This paper describes a serial interfacing technique for embedded RAMs which has been successfully applied to static single port and dual port memories in custom integrated circuits. A single bit of the input data path of a RAM (or a group of RAMs) is controlled by the BIST circuit and a single bit of the output data path is observed during the execution of the algorithms. The other bits are controlled and observed indirectly through the serial data path.

Automatically generated BIST circuits have been developed around this serial technique which embed an algorithm suited for the application with the RAM. The serial data path interface has also been used to provide external access to memories on cost sensitive chips which could not justify the full BIST overhead. This provides a simple external test access mode which uses a minimal number of pins yet exercises the memory at full speed.

SERIAL ACCESS TECHNIQUE

Figure 1 shows a block diagram of a static RAM memory (inside box with dotted outline) and the additional external connections required to implement the shifting capability. The address bus is not latched and applied directly to the X (row) and Y (column) decoders. The input and output data paths are separate. When the READ strobe is high, a word is read and transfered to the output of the memory. When the strobe goes back low, the data is maintained by the transparent latches located at the output of the sense amplifier until the next read operation. When the WRITE strobe is high, a word is written into memory at the location determined by the address.

The shifting capability is provided by the multiplexers connected along the I/O data path. The multiplexers select either the normal inputs or the test inputs depending on the value of the Testmode signal. The test input applied to input i of the memory is simply output i-1 or a signal controled directly by the BIST circuit in the case of the least significant bit. Suppose that M_i and M_{i+1} are two logically consecutive bits of the same word. They may or may not be physically adjacent in memory depending on the layout. In order to move the contents of M_i to M_{i+1}, a read operation of the word containing these two bits is first performed bringing the bit in M_i to the corresponding output latch. A write operation is then performed at the same location to store the bit in M_{i+1}. Actually, the full word gets shifted by one position. The memory cell storing

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