US007424656B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 7,424,656 B2**
(45) **Date of Patent: Sep. 9, 2008**

(54) **CLOCKING METHODOLOGY FOR AT-SPEED TESTING OF SCAN CIRCUITS WITH SYNCHRONOUS CLOCKS**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-François Côté**, Chelsea (CA); **Fadi Maamari**, San Jose, CA (US)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 688 days.

(21) Appl. No.: **11/060,407**

(22) Filed: **Feb. 18, 2005**

(65) **Prior Publication Data**

US 2005/0240790 A1 Oct. 27, 2005

Related U.S. Application Data

(60) Provisional application No. 60/579,649, filed on Jun. 16, 2004, provisional application No. 60/564,210, filed on Apr. 22, 2004.

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/731**; 714/25; 714/709; 714/724; 714/726; 714/729; 714/744; 714/30

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,349,587	A	9/1994	Nadeau-Dostie et al.	
5,680,543	A *	10/1997	Bhawmik	714/30
6,115,827	A *	9/2000	Nadeau-Dostie et al.	713/503
6,327,684	B1 *	12/2001	Nadeau-Dostie et al.	714/731
6,441,666	B1	8/2002	Swanson et al.	
6,467,044	B1	10/2002	Lackey	
6,954,887	B2 *	10/2005	Wang et al.	714/729
7,007,213	B2 *	2/2006	Wang et al.	714/729
7,124,342	B2 *	10/2006	Wang et al.	714/741

(Continued)

OTHER PUBLICATIONS

Qiu et al., "K Longest Paths Per Gate (KLPG) Test Generation for Scan-Based Sequential Circuits", 2004 International Test Conference, Oct. 26-28, 2004, Charlotte, NC, Charlotte Convention Center, USA.

Primary Examiner—John P Trimmings
(74) *Attorney, Agent, or Firm*—Eugene E. Prouix; Dennis S.K. Leung

(57) **ABSTRACT**

A clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in a scan circuit, each path originating from a source memory element in one of the domains and terminating at a destination memory element in another of the domains and comprises selectively aligning either a capture edge or a launch edge of the clock of each domain with a corresponding edge of at least one other domain of the interacting synchronous clock domains to determine the cross-domain paths to be tested between a source domain and a destination domain; clocking memory elements in each domain at respective domain clock rates to launch signal transitions from source memory elements in source domains; and for each pair of interacting clock domains under test, capturing, in the destination domain, circuit responses to signal transitions launched along paths originating from the source domain and selectively disabling capturing, in the source domain, of circuit responses to signal transitions launched along paths originating from the destination domain.

21 Claims, 3 Drawing Sheets