US 20050240790A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0240790 A1**

(43) **Pub. Date: Oct. 27, 2005**

Nadeau-Dostie et al.

(54) **CLOCKING METHODOLOGY FOR AT-SPEED TESTING OF SCAN CIRCUITS WITH SYNCHRONOUS CLOCKS**

(75) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Chelsea (CA); **Fadi Maamari**, San Jose, CA (US)

Correspondence Address:
LOGICVISION (CANADA), INC.
1565 CARLING AVENUE, SUITE 508
OTTAWA, ON K1Z 8R1 (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(21) Appl. No.: **11/060,407**

(22) Filed: **Feb. 18, 2005**

Related U.S. Application Data

(60) Provisional application No. 60/564,210, filed on Apr. 22, 2004. Provisional application No. 60/579,649, filed on Jun. 16, 2004.

Publication Classification

(51) **Int. Cl.**[7] **G06F 13/42**

(52) **U.S. Cl.** **713/400**

(57) **ABSTRACT**

A clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in a scan circuit, each path originating from a source memory element in one of the domains and terminating at a destination memory element in another of the domains and comprises selectively aligning either a capture edge or a launch edge of the clock of each domain with a corresponding edge of at least one other domain of the interacting synchronous clock domains to determine the cross-domain paths to be tested between a source domain and a destination domain; clocking memory elements in each domain at respective domain clock rates to launch signal transitions from source memory elements in source domains; and for each pair of interacting clock domains under test, capturing, in the destination domain, circuit responses to signal transitions launched along paths originating from the source domain and selectively disabling capturing, in the source domain, of circuit responses to signal transitions launched along paths originating from the destination domain.