US 20040163021A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2004/0163021 A1**

(43) **Pub. Date: Aug. 19, 2004**

Nadeau-Dostie

(54) **METHOD AND CIRCUIT FOR AT-SPEED TESTING OF SCAN CIRCUITS**

(76) Inventor: **Benoit Nadeau-Dostie**, Gatineau (CA)

Correspondence Address:
LOGICVISION (CANADA), INC.
1565 CARLING AVENUE, SUITE 508
OTTAWA, ON K1Z 8R1 (CA)

(21) Appl. No.: **10/739,055**

(22) Filed: **Dec. 19, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/447,279, filed on Feb. 14, 2003.

Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**

(52) **U.S. Cl.** **714/726**

(57) **ABSTRACT**

An improvement in a scan testing method for testing a circuit having memory elements arranged into one or more scan chains, the scan testing method having a shift phase for serially loading test patterns into the scan chains and serially unloading test response patterns from the scan chains and a capture phase for capturing the response of the circuit to the test pattern, comprises, during the capture phase, connecting the serial output of each scan chain to its serial input and applying a predetermined number of capture clock cycles with the memory elements configured in a non-capture mode for all but the last capture clock cycle and configured in capture mode for the last capture clock cycle.