Testability Analysis and Test-Point Insertion in RTL VHDL Specifications for Scan-Based BIST

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***Abstract*— This paper proposes a new testability analysis and test-point insertion method at the register transfer level (RTL), assuming a full scan and a pseudorandom built-in self-test design environment. The method is based on analyzing the RTL synchronous specification in synthesizable very high speed integrated circuit hardware descriptive language (VHDL). A VHDL intermediate form representation is first obtained from the VHDL specification and then converted to a directed acyclic graph (DAG) that represents all data dependencies and flow of control in the VHDL specification. Testability measures (TM's) are computed on this graph. The considered TM's are controllability and observability for each bit of each signal/variable that is declared or may be implied in the VHDL specification. Internal signals of functional modules (FM's) such as adders and comparators are also analyzed to compute their controllability and observability values. The internal signals are obtained by decomposing at the RTL large FM's into smaller ones. The calculation of TM's is carried out at a functional level rather than the gate level, to reduce or eliminate errors introduced by ignoring reconvergent fanouts in the gate network, and to reduce the complexity of the DAG construction. Based on the controllability/observability values, test-point insertion is performed to improve the testability for each bit of each signal/variable. This insertion is carried out in the original VHDL specification and thus becomes a part of it unlike in other existing methods. This allows full application of RTL synthesis optimization on both the functional and the test logic concurrently within the designer constraints such as area and delay. A number of benchmark circuits were used to show the applicability and the effectiveness of our method in terms of the resulting testability, area, and delay.**

***Index Terms*—Built-in self-test, register transfer level, testability analysis, testability measures, test point insertion.**

I. Introduction

NOWADAYS, register transfer level (RTL) synthesis or logic synthesis has become an integral part of a design process of digital circuits. Most industrial digital designs use automated RTL synthesis and we can thus achieve design-for-testability (DFT) by incorporating test and synthesis into a single methodology that is as automated as possible. Indeed, considering testability during design synthesis can reduce the overall design and manufacturing time. Even more important, the testability enhancement at the entry level to a synthesis tool makes it independent of the tool and the implementation technology. It becomes part of the design specification and may be optimized with the other synthesis tasks in terms of area and delay.

The main objective of our method is thus to raise the level of abstraction at which testability analysis and test-point insertion are performed. We propose a new testability analysis and test-point insertion method at the RTL, assuming full scan and pseudorandom built-in self-test (BIST) design environment. Full scan in combination with pseudorandom patterns is widely adopted in the industry due to its ease of implementation and fault diagnostic. Unfortunately, the presence of random pattern resistant faults in many practical circuits poses a serious limitation to its success. The solutions to tackle this limitation can be broadly classified as those that modify the input patterns or those that modify the circuit-under-test. In this paper, we are interested in the second class of solutions, circuit modifications, that introduce test points to improve the random pattern testability of a circuit. Our goal is to analyze and modify the very high speed integrated circuit hardware descriptive language (VHDL) RTL description of the circuit, in order to generate an easily testable gate-level circuit by a pseudorandom sequence under the BIST environment. This is the main advantage and motivation of this work. That is, whatever the complexity of the circuit, our objective is to apply synthesis compilation and optimization technology directly to a testable VHDL description, thus optimizing functional and inserted test logic concurrently, rather than introducing testability after the VHDL has been compiled to gate-level.

The proposed method uses as the starting point a VHDL specification given at the synthesizable synchronous RTL. It is analyzed to produce an intermediate representation, called the VHDL intermediate format (VIF), and transformed into a DAG on which testability analysis is performed by computing and propagating testability measures (TM's) forward and backward through the VHDL statements. The TM's are the controllability and the observability for each bit of each signal/variable. Internal signals of functional modules (FM's) such as adders, comparators, and multiplexers are also analyzed to determine their controllability and observability values. The internal signals are obtained by decomposing at the RTL large FM's into smaller FM blocks, each such

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