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(54) **ERROR-CORRECTING CODE-ASSISTED MEMORY REPAIR**

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(52) **U.S. Cl.**

CPC ***G11C 29/42*** (2013.01); ***G11C 11/1673*** (2013.01); ***G11C 11/1675*** (2013.01); ***G11C 29/4401*** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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(57) **ABSTRACT**

A memory-testing circuit configured to perform a test of a memory comprising error-correcting code circuitry comprises repair circuitry configured to allocate a spare row or row block in the memory for a defective row or row block in the memory, a defective row or row block being a row or row block in which a memory word has a number of error bits greater than a preset number, wherein the test of the memory comprises: disabling the error-correcting code circuitry, performing a pre-repair operation, the pre-repair operation comprising: determining whether the memory has one or more defective rows or row blocks, and allocating one or more spare rows or row blocks for the one or more defective rows or row blocks if the one or more spare rows or row blocks are available, and performing a post-repair operation on the repaired memory.

18 Claims, 10 Drawing Sheets