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Nadeau-Dostie et al.

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(54) **METHOD AND PROGRAM PRODUCT FOR DESIGNING HIERARCHICAL CIRCUIT FOR QUIESCENT CURRENT TESTING**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Dwayne Burek**, San Jose, CA (US)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

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Primary Examiner—Thuan Do
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method of designing a circuit having at least one hierarchical block which requires block specific test patterns to facilitate quiescent current testing of the circuit, comprises, for each block, configuring the block and any embedded blocks located one level down in design hierarchy in quiescent current test mode in which input and output peripheral memory elements are configured in internal test mode and in external test mode, respectively; generating quiescent current test patterns which do not result in elevated quiescent current levels and which include a bit for all memory elements in the block and for any peripheral memory elements in any embedded blocks located one level down in design hierarchy; and, if the block contains embedded blocks, synchronizing the test pattern with a corresponding test pattern generated for embedded blocks so that test patterns loaded in scan chains in the block are consistent with test patterns loaded in scan chains in said embedded blocks.

79 Claims, 11 Drawing Sheets