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(54) **METHODS FOR AT-SPEED TESTING OF MEMORY INTERFACE**

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(57) **ABSTRACT**

Methods for at-speed testing of a memory interface associated with an embedded memory involves in general two write operations in succession, two read operations in succession, and a capture operation using scan cells. The write and read operations may be performed during a single clock burst, two separate clock bursts in a clock signal, or two separate clock bursts in separate clock signals.