A 5 Gb/s 9-Port Application Specific SRAM with Built-In Self Test

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Abstract

This paper describes the architecture of a Time-Slot Interchange (TSI) SRAM for a SONET switching application and its associated BIST architecture. To reduce the number of data RAMs required for full switching, the memory throughput is boosted by providing multiplexed access to the core at twice the system clock rate. The nature of the memory requires a novel BIST architecture to ensure full test coverage and ensure easy access of the BIST function at different levels of system integration.

I. Introduction

This paper describes the architecture of a Time-Slot Interchange (TSI) SRAM for a SONET switching application and its associated BIST architecture. The memory port architecture of eight byte-wide, read-only ports and a single, 128-bit write-only port was designed to provide maximum data throughput with the minimum number of memories and to fit easily into the data flow at the ASIC level. To reduce the number of data RAMs required for full switching, the memory throughput is boosted by providing multiplexed access to the core at twice the system clock rate. Other mission-mode features such as self-contained, sequential write-address generation, application-specific address mapping, no-power mode, and page-synchronization controls provide system-level flexibility and simplified ASIC design. A synchronous memory interface with scan path collar and special test modes is provided to simplify scan application and design while enhancing multiport-BIST coverage. The nature of the memory requires a novel BIST architecture to ensure full test coverage.

II. 9-Port Memory Architecture

The 9-port SRAM, shown in Figure 1, is configured as 384 bytes of memory storage with a single 24×128-bit (16 byte) write port and eight 384×8-bit read ports. It is implemented as a 48 row by 64 column core cell array. The 128-bit write is row interleaved with 64-bits written to each of two selected rows per write cycle to give a more optimum array aspect ratio.

A 5-port core cell with four fully-differential read ports and a single-ended pseudo-differential write port has been designed. Differential read ports were selected for enhanced performance relative to a more compact single-ended architecture. An indirect read-access architecture is used to eliminate multiport cell stability problems associated with multiple simultaneous accesses to a cell. The single-ended write scheme combined with row interleaving saves two write bit lines per column. A local bit line inversion scheme is used to provide a pseudo-differential write capability at the core-cell for equivalent-to-differential write performance.

The 9-port operation is obtained by time multiplexing the four physical read ports in the core array. Two full read accesses to the core are performed on these ports in each clock cycle. The read data is then re-timed and latched into eight output ports for presentation to the user on the rising edge of the system clock. All read port inputs are provided to the 9-port interface at the same rising clock edge and are internally pipelined to perform the read

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