Power-Aware At-Speed Scan Test Methodology for Circuits with Synchronous Clocks

Benoit Nadeau-Dostie*, Kiyoshi Takeshita, Jean-François Côté
LogicVision Inc
* : contact and presenter

Abstract

The BurstMode™ test clocking methodology, first presented in [8]*, is improved to handle circuits with synchronous clocks of different frequencies. An on-chip clock controller allows to select a large number of clock waveforms necessary to test synchronous cross-domain paths at-speed and control supply voltage variations. The methodology is applicable to both ATPG and BIST and only requires combinational analysis tools. The methodology is applied to a large circuit to adjust power supply margins of an at-speed BIST test.*

Topics: Power issues in test, high-speed digital test, case study

I. Introduction

Defects that affect circuit speed are more prevalent in sub-90 nm CMOS ICs making it more important to provide a thorough at-speed test. Another trend is the replacement of functional test by structural test to implement all tests. Functional tests are too difficult to implement and have limited diagnostic capabilities. Diagnosis is especially important in a context of debug and yield learning. Scan-based structural tests automatically achieve high coverage of DC defects and have excellent diagnostic capabilities.

However, implementing an at-speed structural test is more difficult than simply clocking a circuit at functional speed during the capture cycle. Circuits have several characteristics that complicate the task. Functional clocks can cover a wide frequency range, and can be asynchronous (i.e., non-integer frequency ratio and/or unknown relative phase) or synchronous (i.e., their frequency ratio is fixed as well as their relative phase) to each other. Asynchronous cross-domain paths must be correctly handled to prevent false timing violations caused by false paths while providing proper test of the interface logic. Within each domain, paths with multi-cycle delays are sometimes used, instead of pipelining, to implement functions at a lower cost. Gated clocks are often used for low power designs. PLLs are used to control groups of synchronous clocks and/or multiply external reference clock frequencies. Synchronous cross-domain paths must be tested for propagation and hold times.

For circuits with multi-cycle paths and multiple synchronous clocks, it is necessary to have the possibility of testing all paths simultaneously. This is needed to catch defects due to crosstalk or other defects related to local supply variations. Transitions in coupled net pairs must coincide as much as possible over the normal process variations spread [4] to detect these defects. The detection of crosstalk faults requires an excellent coverage of transition faults. Also, the complexity introduced by the simultaneous handling of multi-cycle paths and synchronous clocks makes the fault simulation and ATPG more complex.

An at-speed test method should impose a minimum number of test-specific timing constraints on the design. These constraints should be easy to meet so that timing closure does not become more difficult to achieve. Preferably, the clocking methodology should be applicable to BIST and ATPG, including test compression applications.

Other design aspects affect the implementation of an at-speed test. The circuit is designed to perform at a certain temperature and supply voltage. Circuit activity has a direct influence on the average current, local temperature, and reduction of supply voltage (di/dt, IR-drop) which in turn influence the timing. For example, in [5], the authors show that the clock period varies by more than 15% due to supply variations, as shown in Fig. 1 The supply variations are due to the sudden change in circuit activity (di/dt) occuring during the application of two consecutive clock cycles during the capture phase of a scan test. In [6], the delays of specific paths were measured for different values of don't care bits within the test pattern. The delay varied by 10% to 30%. The two effects are independent so the total imprecision can be even larger. Clearly, the test clocking methodology must

1-4244-4203-0/08/$20.00 ©2008 IEEE