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Nadeau-Dostie et al.

(54) **MEMORY REPAIR ANALYSIS METHOD AND CIRCUIT**

(76) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Robert A. Abbott**, Ottawa (CA)

Correspondence Address:
LOGICVISION (CANADA), INC.
1565 CARLING AVENUE, SUITE 508
OTTAWA, ON K1Z 8R1 (CA)

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(57) **ABSTRACT**

A method and circuit for repairing a memory array having one or more memory segments each having one spare column and a predetermined number of spare rows common to all segments, the method comprises, while testing the memory array for failures, generating an equal number of unique segment repair solutions for each segment with each segment repair solution including one defective column address, if any, and a number of defective row addresses, if any, corresponding to the predetermined number of spare rows; and, after completing testing, analyzing all segment repair solution combinations consisting of one segment repair solution selected from each segment; and identifying the best segment repair solution combination of combinations having a number of different defective row addresses which is less than or equal to the predetermined number of spare rows.