Power-Aware At-Speed Scan Test Methodology for Circuits with Synchronous Clocks

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Abstract

The BurstMode™ test clocking methodology, first presented in [8]*, is improved to handle circuits with synchronous clocks of different frequencies. An on-chip clock controller allows to select a large number of clock waveforms necessary to test synchronous cross-domain paths at-speed and control supply voltage variations. The methodology is applicable to both ATPG and BIST and only requires combinational analysis tools. The methodology is applied to a large circuit to adjust power supply margins of an at-speed BIST test.*

Topics: Power issues in test, high-speed digital test, case study

I. Introduction

Defects that affect circuit speed are more prevalent in sub-90 nm CMOS ICs making it more important to provide a thorough at-speed test. Another trend is the replacement of functional test by structural test to implement all tests. Functional tests are too difficult to implement and have limited diagnostic capabilities. Diagnosis is especially important in a context of debug and yield learning. Scan-based structural tests automatically achieve high coverage of DC defects and have excellent diagnostic capabilities.

However, implementing an at-speed structural test is more difficult than simply clocking a circuit at functional speed during the capture cycle. Circuits have several characteristics that complicate the task. Functional clocks can cover a wide frequency range, and can be asynchronous (i.e., non-integer frequency ratio and/or unknown relative phase) or synchronous (i.e., their frequency ratio is fixed as well as their relative phase) to each other. Asynchronous cross-domain paths must be correctly handled to prevent false timing violations caused by false paths while providing proper test of the interface logic. Within each domain, paths with multi-cycle delays are sometimes used, instead of pipelining, to implement functions at a lower cost. Gated clocks are often used for low power designs. PLLs are used to control groups of synchronous clocks and/or multiply external reference clock frequencies. Synchronous cross-domain paths must be tested for propagation and hold times.

For circuits with multi-cycle paths and multiple synchronous clocks, it is necessary to have the possibility of testing all paths simultaneously. This is needed to catch defects due to crosstalk or other defects related to local supply variations. Transitions in coupled net pairs must coincide as much as possible over the normal process variations spread [4] to detect these defects. The detection of crosstalk faults requires an excellent coverage of transition faults. Also, the complexity introduced by the simultaneous handling of multi-cycle paths and synchronous clocks makes the fault simulation and ATPG more complex.

An at-speed test method should impose a minimum number of test-specific timing constraints on the design. These constraints should be easy to meet so that timing closure does not become more difficult to achieve. Preferably, the clocking methodology should be applicable to BIST and ATPG, including test compression applications.

Other design aspects affect the implementation of an at-speed test. The circuit is designed to perform at a certain temperature and supply voltage. Circuit activity has a direct influence on the average current, local temperature, and reduction of supply voltage (di/dt, IR-drop) which in turn influence the timing. For example, in [5], the authors show that the clock period varies by more than 15% due to supply variations, as shown in Fig. 1 The supply variations are due to the sudden change in circuit activity (di/dt) occuring during the application of two consecutive clock cycles during the capture phase of a scan test. In [6], the delays of specific paths were measured for different values of don't care bits within the test pattern. The delay varied by 10% to 30%. The two effects are independent so the total imprecision can be even larger. Clearly, the test clocking methodology must

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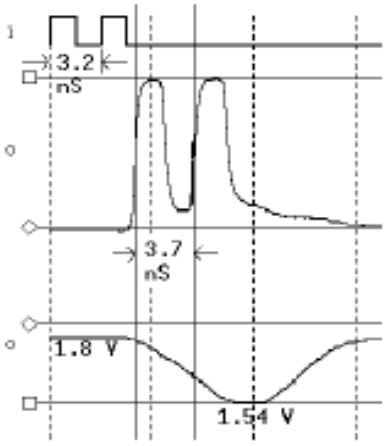
provide some way to control supply variations and circuit activity.

Fig. 1 Clock stretching effect (from [5])



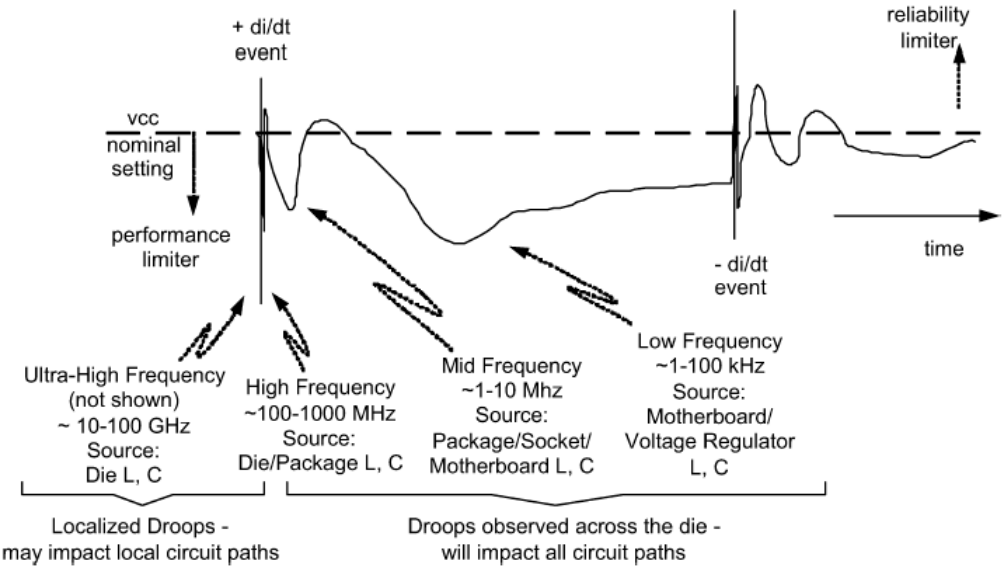
To address the clock stretching effect, it was suggested in [5] that the burst should be longer to allow enough time for the supply to stabilize. In [7], it was shown that the voltage drop due to di/dt effects was reduced by an order of magnitude (56% to 4.5%) when three launch cycles instead of one were used prior to the capture cycle. They could obtain a much closer correlation with the normal mode of operation in terms of the supply voltage profile.

However, applying a burst of four, or even more, system clock cycles during the capture phase makes it difficult to use a launch-off-capture (LOC) approach because of the significant increase in ATPG complexity and fault coverage reduction. In [2] and [12], it was shown that the number of patterns required to test for transition faults is significantly larger using the LOC approach, up to an order of magnitude more patterns for the same coverage achieved using the launch-off-shift (LOS) approach. The increase is even more significant when considering burst lengths longer than two. The main difficulty to implement the LOS approach is the propagation of the scan enable signal within a system clock cycle. In [1] and [12], practical methods of addressing this issue are described.

Supply voltage variations can be quite complex because of contributions from multiple sources. They are documented in [11] and illustrated in Fig. 2. Inductance and capacitance (L, C) characteristics of the power supply regulator, socket, package and chip power grid induce variations with time constants which differ by orders of magnitude. These characteristics vary at the board, package and wafer level testing, and a same at-speed test might pass at the board and package level but fail at the wafer level due to those different characteristics. So, a test clocking methodology should be able to adjust to the characteristics of the different levels at run time and have some form of programmability.

Popular power reduction techniques based on input patterns constraining, such as the ones described in [10], have not been considered as the primary mechanism to control supply variations. They do not address the large transients of the supply voltage resulting from the changes in clock activity. Those transients are responsible for the clock stretching effect and other effects described in [11] and later in this paper (Section V). Also, these techniques are not practical for BIST applications. However, they can be used in ATPG applications as a complement to the techniques described in this paper.

Fig. 2 Supply variation sources (from [11])



A test clocking methodology, called BurstMode, that addresses the requirements listed in this introduction was developed. In [8], we described the basic principle applied to a single clock domain, with or without multi-cycle paths, as well as to interacting asynchronous clock domains of arbitrary frequency ratios. This work is summarized in Section II of this paper. We then describe some improvements made to the handling of timing exceptions like multi-cycle paths (MCPs) in Section III, and a new method of handling interacting synchronous clock domains in Section IV. The methodology is applied to a large product IC to adjust power supply margins of an at-speed BIST test in Section V followed by conclusions.

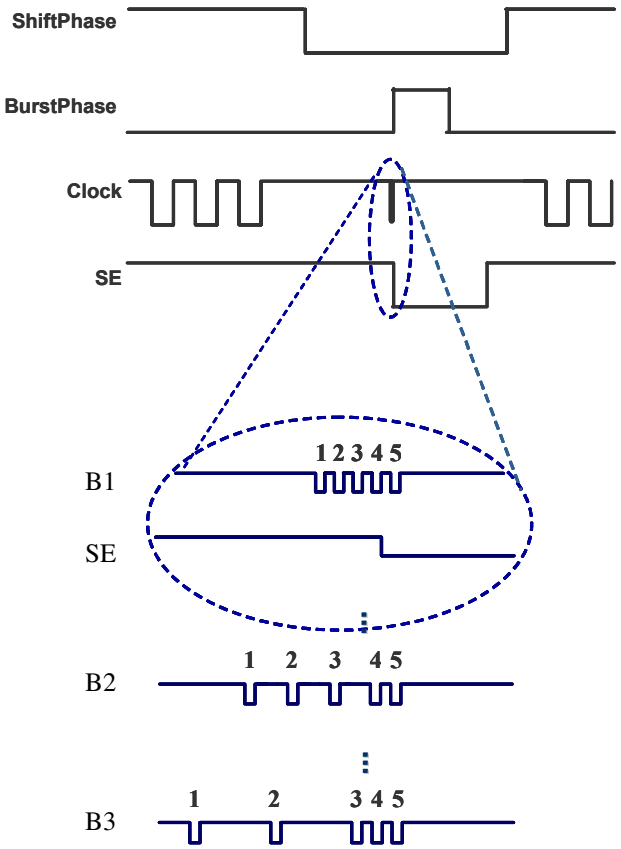
II. BurstMode architecture summary

In our test architecture, clock bursts with programmable frequency and duration are applied to the circuit under test. Fig. 3 shows a few examples of burst waveforms that can be applied. All bursts shown comprise five system clock cycles. The first four cycles are shift cycles and, only the last one is a capture cycle. All combinations are created by gating a free-running system clock with a small finite-state machine, called a burst clock controller (BCC).

In Fig. 3, burst B1 consists of five consecutive at-speed cycles and is the default. Usually, the supply voltage has time to stabilize by the last shift and capture cycles, which are the most critical ones. However, in some cases, di/dt effects induced by the sudden change of circuit activity cause a power droop exceeding the expected IR drop. The BCC can slow down some of the last shift clock cycles to permit a more gradual increase in circuit activity and reduce di/dt effects. Waveforms **B2** and **B3** of Fig. 3 are examples of burst waveforms where shift clock cycles have been slowed down. In **B2,** one out of two system clock cycle is gated so that the effective frequency of the first three shift clock cycles is half of the system clock frequency. In **B3**, the first two shift clock cycles are applied at a quarter of the system clock frequency. The usefulness of such waveforms will be demonstrated in Section V.

Since we are using an LOS approach, the scan enable signal (**SE**) is kept high until the final clock cycle. This signal is generated by a simple shift register, the input of which is the (low speed) **ShiftPhase** signal (See Fig. 6). The shift register has a length of four bits, i.e., burst length minus one. The scan enable signal has one system clock period to propagate from the output of the shift register to all flip-flops controlled by it. Nowadays, it is trivial to do this even in large designs because all major layout tools realize that the shift register can be connected on an "early" branch of the clock tree to increase the setup time margin at the destination flip-flops. Also, the last stages of the shift register are automatically replicated to reduce the fanout whenever needed. A similar method has been used in [1] and [12].

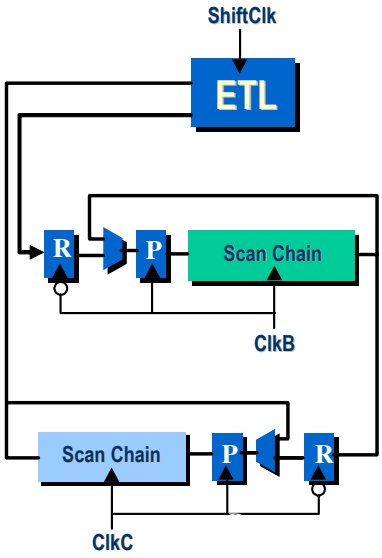
Fig. 3 Example clock burst waveforms



The challenge in our architecture was to find where to connect the serial input and output of the scan chains during the burst without limiting the burst length. The bursts can occur at very high speeds (i.e. hundreds of megahertz, or even gigahertz) and, there could be several asynchronous clock domains in the circuit. So, it is not possible to drive the scan chains from a tester or even a BIST controller. The solution that we use is illustrated in Fig. 4. Scan chains are organized into segments that can be concatenated into longer chains that are connected to an Embedded Test for Logic (**ETL**) controller (for BIST or test compression logic) or to an external tester. The segments can be on the same or different clock domains. If the domains are different, they can be synchronous or asynchronous. In the example of Fig. 4, **ClkB** and **ClkC** are in different asynchronous clock domains. This is why a retiming (**R**) flip-flop is used at the input of the segment controlled by **ClkC**. Another retiming flip-flop is used at the input of the chain controlled by **ClkB** because the **ETL** controller is in its own domain which is asynchronous to the others. Finally, there is a retiming flip-flop at the input of the controller (not shown). During the shift phase, data is shifted into and out of the test

controller through both segments at a low or moderate speed using **ShiftClk** which is injected in all domains.

Fig. 4 Rotating chain segments and controller



A novel aspect is that during the burst phase, the output of each segment is fed back to its own input. Once configured in this rotation mode, the data loaded into the segments during the shift phase are simply rotated at the respective system clock speed for as long as needed for the power supply to stabilize. There are no signal exchanges between the clock domains, or between any of the clock domains and the controller or the tester. The exact timing during the rotation is not critical. Only the final launch and capture clock edges must be placed accurately. This is in contrast with an LOC approach using multiple launch clock cycles where all clock cycles are critical.

In order to facilitate timing closure for the rotation path, a pipeline (**P**) flip-flop is inserted at the beginning of each segment. Since this flip-flop is not connected to anything else in the circuit, the layout tool will automatically place it to ensure that the rotation can be performed at-speed.

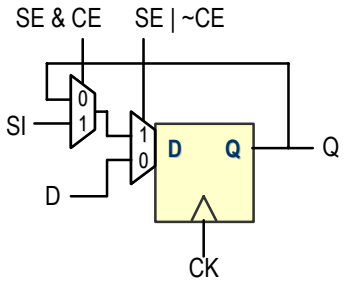
Since the shift phase is relatively (but not completely as will be seen in Section V) independent from the burst phase, there is some flexibility in the selection of the shift clock rate. It is set as high as possible to minimize test time but without imposing undue timing constraints on the scan path timing or exceeding power supply limits (especially at wafer probe) or thermal dissipation limits of the circuit. The shift rate can be higher for implementations using a BIST circuit, or a test compression circuit based on reseeding, compared to an implementation where scan data must be shifted into and out of chip pins at the same rate as the scan chains. This is because the interface between the tester and the chip pins is usually the limiting factor in terms of speed.

Note that there are no critical signals between the scan chains and the tester or embedded test controller. Also, during the burst phase, the **SI** input can be in any state and the activity on **SO** is ignored. This is because the number of clock cycles during the shift phase is sufficient to unload the circuit response of the previous scan pattern. The absence of critical signals coming into and out of a domain is very useful in the handling of multiple clock domains.

III. Timing exceptions

In this section, we review the handling of timing exceptions in the BurstMode architecture and introduce improvements in the handling of multi-cycle paths (MCPs). There are various types of timing exceptions to handle in a typical real circuit. They are primarily related to multi-cycle paths (MCPs) within a domain and in cross-domain paths between asynchronous or synchronous clock domains. Flip-flops that source multi-cycle and/or asynchronous cross-domain paths must be put in separate chain segments because their rotation during the burst phase is subject to conditions. The source flip-flops must sometimes hold while other flip-flops rotate. The hold capability is implemented using a multiplexer inserted on the scan input of the flip-flop so that there is no impact on functional timing. This is illustrated in Fig. 5 for a flip-flop sourcing an MCP. The generation of the control signals for MCP source flip-flops is explained later in this section.

Fig. 5 Flip-flop with holding mux

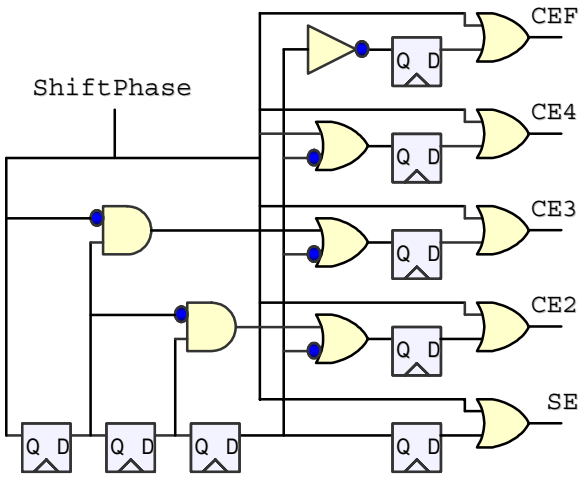


Alternatively, low power designs use clock gating cells to implement the hold capability to eliminate power that would be wasted in the clock branches of flip-flops configured in hold mode. The advantage of clock gating cells is that they can be shared by several flip-flops. Typically, less than 1% of the flops in the design need to be put in separate chain segments. All types of segments, including those without timing exceptions, can be concatenated to form a longer chain because they are all shifting at a single lower rate during the shift phase. This

allows optimal chain balancing. All cross-domain paths between asynchronous clock domains are automatically detected by both the RT-level and gate-level analysis tools supporting our methodology, and the handling of these paths is described in [8].

MCP flip-flops are identified, either explicitly or implicitly through constraints from one clock domain to another, in design constraints files already needed by physical design tools and static timing analysis tools. Their handling has been improved compared to what was described in [8]. During the burst phase, MCP segments now only rotate once before launching an at-speed transition at an appropriate time based on their multiplicity (i.e. 2, 3, 4 or >4). So, the new method no longer requires at-speed rotation within these segments, which simplifies timing constraints for the physical design tools. Note that the multiplicity indicates the number of clock cycles allowed for signal propagation. For false paths (multiplicity >4), the transition is launched from the last shift cycle of the shift phase. We allow at least 8 shift clock cycles for intra-domain false path signal propagation as well as asynchronous cross-domain paths. Since the shift clock is typically slower than the burst clock, there is largely enough time for signal propagation.

Fig. 6 Generation of scan and clock enable signals



MCP segments require one new control signal for each multiplicity that is present in the domain because the flip-flops must be able to hold. A scan enable and clock enable signal generator is shown in Fig. 6. Note that, usually, only one or two clock enable signals are used within a specific clock domain and the unnecessary logic is automatically removed. The clock enable signals are pipelined because they have to switch within a single system clock cycle. However, the fanout on these signals is very small compared to the fanout of the associated **SE** signal so the timing is easy to achieve. Note that the clock enable signals are identified by their multiplicity (i.e. CE2, CE3, CE4). CEF is used for false paths.

One advantage of treating MCPs as described above (i.e. launching transitions at different times and capturing at the same time) is that all paths are tested simultaneously without requiring different clock period settings. Also, no masking needs to be done on the output response of circuits and scan/BIST tests can be signed-off at design time using static timing analysis (STA) scripts automatically generated from functional constraints. Test programs are quickly set up and usually work within hours after first silicon is received.

IV. Synchronous clock domains

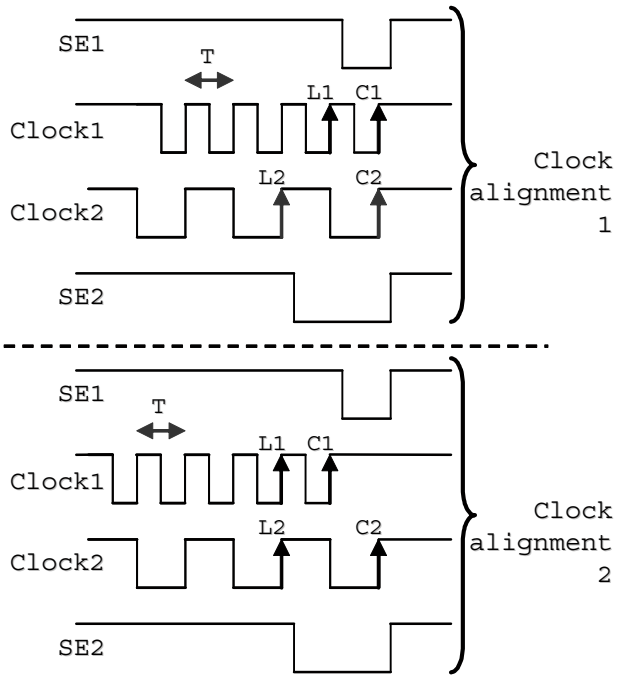
Burst phases for synchronous clock domains must be synchronized very precisely to facilitate testing the various cross-domain timing relationships. The exact skew relationship between these domains must be preserved during test, so functional clocks are used. Two main clock alignments are used to test cross-domain paths. They are illustrated in Fig. 7 Only two clocks are shown for clarity. The first alignment is the same as shown in [1]. The capture operation is performed simultaneously in all synchronous domains. This first alignment is used to test the propagation delay of cross-domain paths according to the clock period of the source flip-flop. For example, paths from Domain 1 to any sub-frequency domain are checked to be less than T (period of the highest frequency domain) and paths from Domain 2 must be less than 2T, etc... Multi-cycle path exceptions to this rule are treated as described earlier in Section III.

This first clock alignment also checks that there are no hold time violations across domains. This hold time verification is often neglected in other clocking architectures, such as [3] and [4], but is a very important aspect of the operation of synchronous clock groups. Skew between the clock trees of two synchronous domains only has a 50% chance of being detected if only the propagation time between the domains is tested.

The second clock alignment shown in Fig. 7 is used to test the propagation delay of cross-domain paths according to the clock period of the destination flip-flop. For example, paths to Domain 1 from any sub-frequency domain are checked to be less than T, paths to Domain 2 from any other domain are checked to be less than 2T, etc.. Again here, multi-cycle path exceptions can be specified. One undesirable effect of the second clock alignment is that the staggered capture operations increase the sequential depth of the circuit to analyze. This is because the values captured in Domain 2 are a function of the values captured in Domain 1. Test generation, fault simulation, and diagnosis are all affected especially when the number of synchronous domains exceeds two. We use a simple and inexpensive DFT

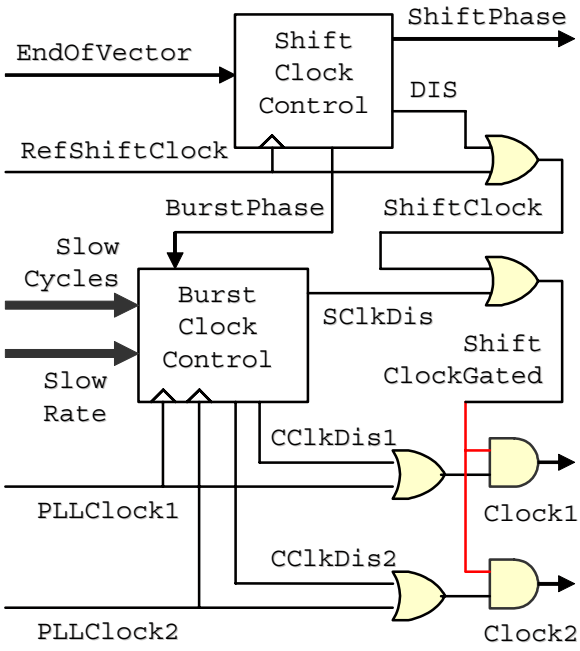
technique to keep the circuit combinational (i.e. the output response is only a function of the values shifted in all flip-flops). When the second clock alignment is used, all paths sourced from a domain to a lower frequency domain are suppressed by keeping the destination flip-flops in shift mode. The circuit analysis required to identify these paths is simpler than the one required for the analysis of cross-domain paths between asynchronous domains because there is only one group of destination flip-flops that have their capture suppressed according to the clock alignment in the LOS approach. Using this technique, the circuit remains combinational. The flip-flop that selects the clock alignment is scannable so that the ATPG has full control. In BIST mode, the clock alignment is randomly selected and reduces the observability of the destination flip-flops by 50% since there are two possible alignments. However, the large majority of faults are observed multiple times and, the effect on BIST coverage was found to be insignificant.

Fig. 7 Dual clock alignment of synchronous clocks



A high level view of the connections of the shift clock and burst clock controllers is shown in Fig. 8 The shift clock controller generates the shift clock as well as the **ShiftPhase** and **BurstPhase** signals shown in Fig. 3 The burst clock controller synchronizes the BurstPhase signal to the clock domains that it is controlling, using the slowest frequency, **PLLClock2**, which is typically generated by a PLL. The clock gating logic (OR-AND gates driving **Clock1** and **Clock2** on Fig. 8) is guaranteed to be glitch-free since the changes on **CClkDis1** and **CClkDis2** are masked by the active level of the reference clock that caused the changes. There are other implementations based on clock-gating cells (CGC) and multiplexers that can be used to replace the OR-AND gates as shown in Fig. 9. Cells used on clock paths are often specially designed to have a balanced rise and fall time. Our automation tools allow the user to identify those cells in the library which are then used to implement the clock controllers. The delay of the clock-gating logic is negligible compared to the clock distribution delay and is comparable to a multiplexer that is typically used to switch in test clocks. There are always sufficiently long pauses between clock bursts and shift clock cycles to avoid any glitches.

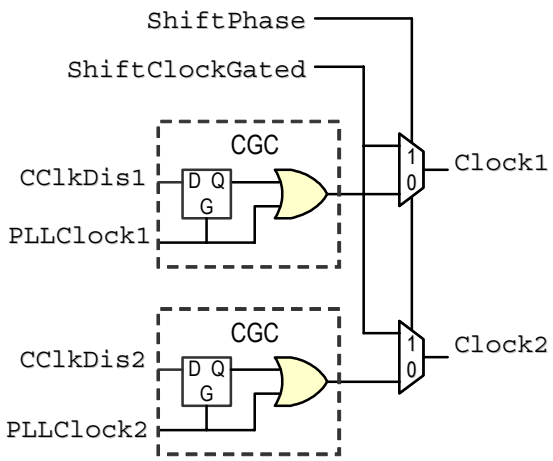
Fig. 8 Clock control



No additional timing constraints are put on the layout of the clock tree if the reference functional clocks can always be used during the burst phase. However, testers can only source a limited number of test frequencies. This means that the at-speed test, BIST or ATPG, must be repeated because only a sub-set of the clock domains will be tested at-speed. Domains which are not tested at-speed in a given pass can still use the tester reference frequency or the shift clock derived from it. For a group of synchronous domains, it is then required that the branches of the shift clock going to the OR-AND gates be balanced with the same limits than the reference clock, which is not difficult to do since a single wire, highlighted in red (Shift Clock Gated) in Fig. 8, is involved. Note that the same frequency will be applied to both clock outputs in this case, but the output response will not be changed despite the fact that some clock edges are not occuring in the same order. This is an additional benefit of the path suppression technique used for the

second clock alignment of Fig. 7. A detailed description of the burst clock controller is given in [9].

Fig. 9 Clock gating alternative



V. Application example

In the last 3 years, the BurstMode clocking methodology has been implemented on tens of circuit designs, several of them including synchronous clock groups handled as described in Section IV. In the large majority of the cases, the default burst of 5 consecutive system clock cycles ending with a single capture cycle, is used for production testing. In circuits with synchronous clocks, the dual alignement shown in Fig. 7 is used. However, sometimes such bursts cause excessive variations of the power supply voltage which, in turn, cause the at-speed test to fail for certain combinations of IC manufacturing process, supply voltage, temperature conditions, and test setup (i.e. wafer, package, board) as described in Section I. The application described next makes use of the run-time programmable waveforms and synchronous clock support described earlier to evaluate the lowest power supply voltage at which a structural test can run for a given frequency for a chip experiencing yield issues using the default test waveforms. Some margin is usually added to the minimum tolerable V_{DD} to establish the supply voltage test limit.

The circuit under test has about two million combinational gates and a hundred thousand flip-flops distributed in 38 clock domains. Table 1 indicates the number of domains for each frequency, the burst length (BL) used for the domain, the synchronous clock group identification when applicable, and the number of flip-flops for that frequency.

There are nine different frequencies which means that nine burst clock controllers (BCCs) were used. Some of the clocks are generated by on-chip PLLs connected to a reference clock. This is the case for synchronous clock group A for which the external reference frequency is 5 MHz. The multiplication factor for this PLL is 40.

Table 1: Clock domains list

freq. (MHz)	domains	group	BL	FFs
400	1	-	5	12
200	1	A	5	830
100	24	A	5	64802
50	3	A	5	23666
50	1	-	2	3944
48	1	-	2	183
24	3	-	2	1351
24	3	B	2	798
12	1	-	2	2187

The flip-flops were organized in 256 chains of approximately 412 flip-flops each. Most chains were organized in a single segment and there is a total of 338 segments. Note that each segment requires one pipeline flip-flop, a rotation multiplexer and, when crossing a clock domain boundary, a retiming flip-flop.

The test used for the measurements is a BIST test with 95% SA fault coverage and 90% transition fault coverage with 32K patterns (scan vectors).

The first measurements were made using the default waveform for all clock domains which corresponds to **B1** in Fig. 3 The test limit for the minimum V_{DD} was set to 1.080 V and several chips failed, which reduced yield. So, additional burst waveforms were selected for the **BCC** controlling synchronous clock group **A** because it is by far the most important group in terms of the number of flip-flops and susceptibility to excessive circuit activity.

The results for one sample are summarized in Table 2 . For each burst waveform, the minimum V_{DD} for which the circuit can run at the nominal frequency is measured. The waveforms are represented with “I” and “.” symbols which represent the presence or absence of a clock pulse respectively. The waveform is applied to all clocks of the synchronous clock group A including 3 different frequencies and the two alignments described earlier in Fig. 7.

Table 2: Supply margin

Waveform	Vdd min (V)	margin (mV)
IIIII	1.100	-20
I...IIII	1.080	0
I...I...III	1.030	50
I...I...I...II	1.000	80

The results in Table 2 show that the burst waveform has a significant effect on the measured supply margin: the margin is improved by 100 mV between the first and fourth waveforms. This is approximately equal to the expected margin. Note that the resolution of the measurements is 10 mV and that results were consistent for the three samples analyzed. Note that all intra- and inter-domain paths are tested at-speed because the launch and capture operations are still using the nominal system clock period; only the first 3 shift cycles of the burst are slowed down.

We observed the supply variations at the chip input when applying the clock waveforms. This is shown in Fig. 10 and Fig. 11. For the first waveform, corresponding to the highest level of activity, it can be seen that the voltage at the chip input goes down by more than 100 mV during the burst. For the second waveform, the voltage drop is about half. The three superimposed color markers indicate the approximate period during which the clocks are active for each frequency of the synchronous clock group. They are in descending frequency order from 200 MHz to 50 MHz. The flip-flops clocked at 100 MHz have the most impact on the behavior of the supply monitored at the pin because they represent the largest group of flip-flops (see Table 1).

Fig. 10 Burst waveform IIIII (50MHz shift)

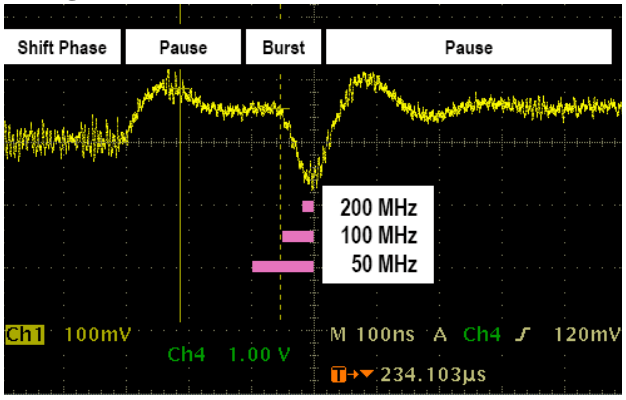
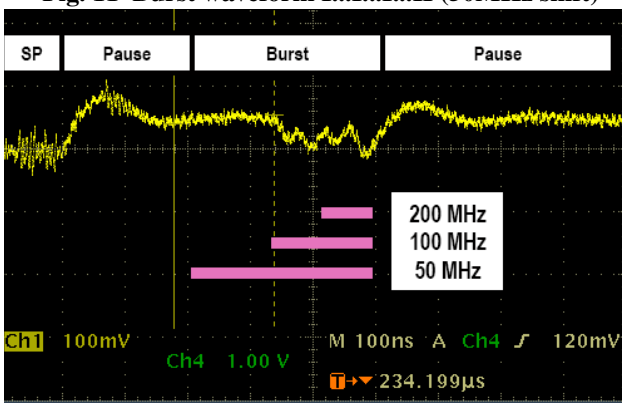


Fig. 11 Burst waveform I...I...I...II (50MHz shift)



The difference in the voltage drop measured at the pin does not seem to correspond to the margin improvement of Table 2. However, there are a few important aspects to consider here. One is that the time at which the capture operation is performed is not necessarily when the supply level is at its minimum since the capture itself will generate additional circuit activity that might cause further decrease of the voltage measured at the pin. Also, the local variations of the supply within the chip can be more significant than the ones measured at the chip input. Finally, the clock stretching effect observed in [5] might affect the circuit differently for each waveform. This is why the pictures only give a qualitative appreciation of what is happening on chip.

Some measurements were also made using functional tests. The results are shown in Table 3 for three samples coming from a slow process batch. Measurements were made at 25°C and 80°C with the chips soldered on the evaluation board and mounted on a socket to facilitate probing. The temperature causes the minimum tolerable V_{DD} to increase by about 20 mV while the socket adds 40 to 50 mV. The reference structural test was only run when the chips were mounted on a socket and at a temperature of 25°C. Therefore, the results obtained at 80°C were adjusted for temperature by subtracting 20 mV to have comparable conditions. The results are shown in Table 4.

Table 3: Minimum V_{DD} for functional tests

Sample number	25°C soldered (V)	80°C soldered (V)	80°C socket (V)
1	1.080	1.097	1.140
2	1.070	1.090	1.140
3	1.077	1.098	1.140

Table 4: Minimum V_{DD}: structural *vs* functional

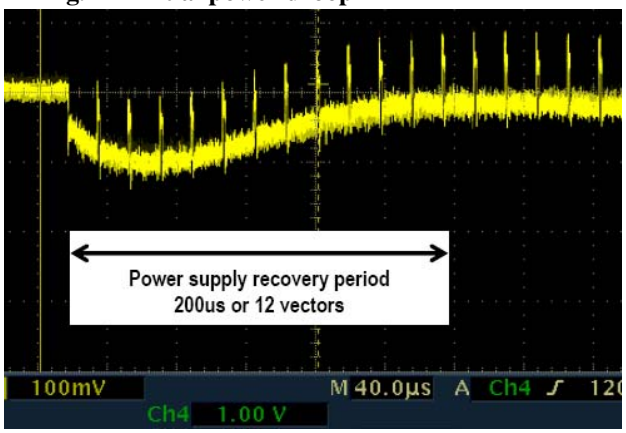
Sample number	Structural 25°C socket (V)	Functional 25°C socket (V) (adjusted)	delta (mV)
1	1.170	1.120	50
2	1.150	1.120	30
3	1.160	1.120	40

It can be seen that there is still a difference of 30 to 50 mV between the structural and the functional tests. It is always difficult to compare the functional and structural test results because the coverage of the functional test is unknown and we do not know precisely which paths are

being exercised. Nevertheless, it was felt that the difference should be smaller.

After some investigation, we found a possible explanation for this difference. It is illustrated in Fig. 12. The figure shows the supply voltage variations at the chip input for the first 18 vectors using a shift-phase frequency of 50 MHz. Each spike corresponds to a burst as shown in Fig. 10. The time required for each vector (distance between spikes) is approximately 17 us. It can be seen that the supply voltage at the chip input goes down by approximately 100 mV at the beginning of the test. This is because of the large current variation (di/dt) occuring at the beginning of the test when switching from functional mode to test mode. It takes about 200 us for the supply to stabilize to its final value. So, the first twelve vectors are more likely to fail as the supply voltage is lower than for all other vectors. We ran our diagnostic tool on some of the chips and effectively found chips which minimum V_{DD} was determined by vector number 4 that corresponds to the lowest supply voltage point as measured at the input. The shift frequency had to be reduced to 5 MHz to eliminate this effect but this was not acceptable in this case because it increased the test time by a factor of ten. It was also not possible to modify the production loadboard to increase the supply decoupling. A simple solution is to mask the output of the first vectors. This solution was not available for this particular design but a run-time programmable option was added to subsequent versions of our test controller. The impact on coverage is insignificant for BIST applications since tens of thousands of vectors are applied.

Fig. 12 Initial power droop

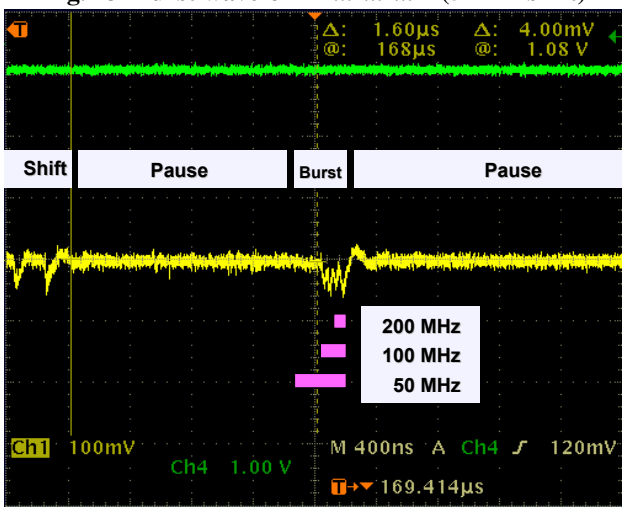


Based on Fig. 2 taken from [11], the source of the initial power droop is due to the power regulator of the tester. Power supplies are adaptive, and time constants of hundreds of microseconds are typically used on testers to avoid oscillations. Faster power supply modules exist but are reserved for specialized tasks.

Another source of supply variations introduces some coupling between the shift phase and the burst phase of a scan load. In Fig. 11, at the end of the shift phase, the supply voltage increases by roughly 40-50mV after clocking is paused due to di/dt effects and the burst starts from a higher voltage, increasing the minimum V_{DD} margin compared to the case where the shift phase frequency is lowered to 5 MHz to make the "pull-up" effect disappear as shown in Fig. 13. The "pull-up" effect is a possible explanation of the correlation in [8] between the maximum frequency of operation of the circuit (Fmax) and the shift phase frequency. This new source of supply variation needs to be taken into account when increasing the shift speed. The "pull-up" effect has a time constant of about 100ns (approximately 10MHz) and would be caused by the inductance and capacitance characteristics of the chip package and/or socket based on Fig. 2.

Obviously, more work is needed to characterize and identify the source(s) of this "pull-up" effect as well as the initial power droop and supply variations during the burst itself which would require to measure supply variations on chip. In any event, the clocking methodology described in this paper allows the test engineer to characterize and work around these issues.

Fig. 13 Burst waveform I...I...I...II (5MHz shift)



VI. Conclusions

The BurstMode methodology allows control of digital circuit activity to reflect the functional mode of operation during the application of at-speed structural tests (BIST or ATPG). It proved to be useful in the diagnosis and characterization of unexpected supply variations, including di/dt effects, that were affecting the yield of a chip using complex clocking including multi-cycle paths and synchronous clocks. The results led to improved margins on the minimum V_{DD} specification of a production test. Those margins were comparable to results obtained with functional tests. More work is required in the modeling of resistance, capacitance,

inductance, and response time in tester setups (e.g. power supply and loadboard) and power grids, to better anticipate yield issues that might result from supply voltage variations, off-chip and on-chip, during production testing. The clocking methodology described in this paper is a useful tool to correlate models with silicon.

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