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# United States Patent [19]

**Côté et al.**

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[54] **ASYNCHRONOUS INTERFACE**

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[58] **Field of Search** ..... 327/144, 145, 327/151, 99, 160; 371/22.1, 55, 22.5, 22.36; 375/354, 355, 359, 362; 395/551

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[57] **ABSTRACT**

An interface allowing to transfer serial test data from a Test Access Port (TAP) to controllers located in several clock domains is described. The clock frequencies can be different from each other and do not need to be related in phase to each other or with the clock of the TAP. The interface is proven to work reliably as long as the clock frequencies used for the test controllers and registers is 3 times higher than the one of the TAP used to source the serial test data.

**67 Claims, 8 Drawing Sheets**