BIST of PCB Interconnects Using Boundary-Scan Architecture

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***Abstract*—This paper addresses the issues of printed circuit board (PCB) interconnect testing in the context of boundary-scan architecture. Boundary-scan architecture is treated here as the framework for a PCB level built-in self-test (BIST). A novel BIST method is developed which utilizes various features of the architecture. Boundary-scan architecture is shown to have the capability to generate time efficient test vector sets. Response compaction within the boundary-scan chain is introduced to reduce shift out time as well as to simplify detection and diagnosis. However, the proposed BIST schemes require some extensions of the standard boundary-scan cells, and schemes can work only if every boundary-scan cell of every IC on the PCB has the proposed extensions.**

I. Introduction

IN RECENT years, structured design-for-testability at the printed circuit board (PCB) level has become an activity of major interest. This is a natural evolution, following a wide acceptance of the structured DFT (i.e., scan and built-in self-test) [21] at the IC level and the realization that the cost associated with implementing scan cannot be justified unless it can be used to simplify the testing efforts at the PCB and higher levels as well. This, combined with the emergence of very high density packaging technology at the PCB level, in particular, that of surface mount interconnects, and the growing interest in multichip modules, made it essential to develop the concept of boundary-scan, as detailed in [15].

The boundary-scan concept allows one to access and control the primary input and output pins on each component of the PCB from its edges. This is done by connecting all the primary inputs and outputs of each component into a shift register which has a boundary-scan input and a boundary-scan output. A simple boundary-scan cell is shown in Fig. 1 [15, fig. 1-1]. The shift registers on all the components of a PCB can be connected together to form a larger shift register with a single scan in edge and a single scan out edge, as shown in Fig. 2 [15, fig. 1-2]. A test clock line and a test mode select line, along with the boundary scan in and scan out lines, form a four-wire testability bus [15]. Thus, in effect, the boundary scan concept provides a type of electronic in-circuit testing facility.

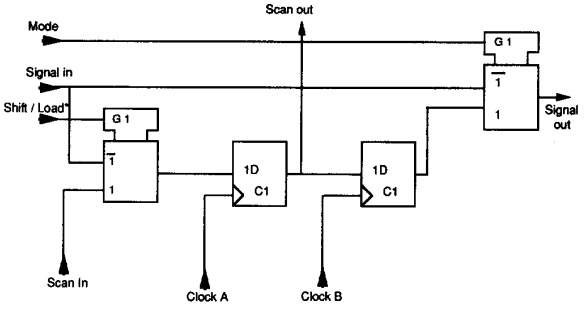

Fig. 1. A Simple boundary-scan cell.

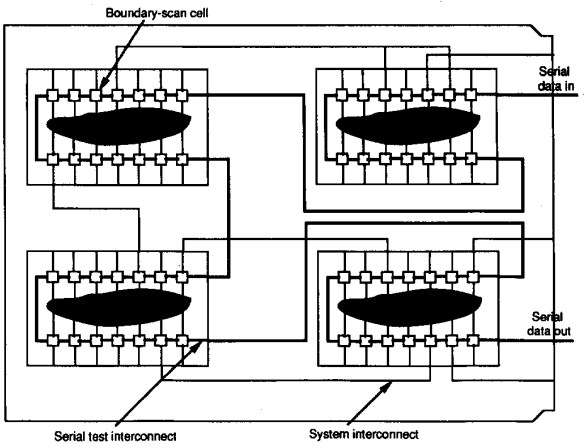

Fig. 2. Boundary-scan chain.

Using this concept at the PCB level, it should be possible to confirm that each component, such as an IC, performs its required function, and that the IC's are interconnected in the correct manner. The problem of interest in this work is that of using this concept to verify that the interconnects connecting these IC's on a PCB are free from structural faults.

The interconnection of IC's and other discrete components on a PCB is a complex maze of multilayer electrical

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