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Nadeau-Dostie

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(54) **METHOD AND CIRCUIT FOR AT-SPEED
TESTING OF SCAN CIRCUITS**

(75) Inventor: **Benoit Nadeau-Dostie**, Gatineau (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

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See application file for complete search history.

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Primary Examiner—James C. Kerveros

(74) *Attorney, Agent, or Firm*—Eugene E Prouix

(57) **ABSTRACT**

An improvement in a scan testing method for testing a circuit having memory elements arranged into one or more scan chains, the scan testing method having a shift phase for serially loading test patterns into the scan chains and serially unloading test response patterns from the scan chains and a capture phase for capturing the response of the circuit to the test pattern, includes, during the capture phase, connecting the serial output of each scan chain to its serial input and applying a predetermined number of capture clock cycles with the memory elements configured in a non-capture mode for all but the last capture clock cycle and configured in capture mode for the last capture clock cycle.

45 Claims, 9 Drawing Sheets

