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[54] BIST ARCHITECTURE FOR MEASUREMENT OF INTEGRATED CIRCUIT DELAYS

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[57] ABSTRACT

A built-in self-test (BIST) method and apparatus for digital integrated circuits (ICs) and for systems including multiple ICs, measures signal propagation delays in combinational and sequential logic, set-up and hold times, and tri-state enable/disable times, from any circuit node to any other circuit node including pin-to-pin and from one IC to another. The IC under test is provided with two test bus conductors passing near every circuit node of interest and connected thereto by switches or buffers. During test, an oscillator is created including the test bus, a constant delay, counters, and a delay path of interest or a reference path. The delay path of interest may include e.g. an analog filter. The oscillation period of the oscillator when the reference path is selected is subtracted from the oscillation period when the oscillator includes a delay path of interest. A circuit automatically accommodates inverting and non-inverting paths. A delay copier copies the delay between any two signal events, without injecting any test signal into the circuit under test (e.g. on-line test), and the delay copy can be measured by selecting it in the oscillator.

31 Claims, 18 Drawing Sheets

