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(54) **METHOD AND PROGRAM PRODUCT FOR DESIGNING HIERARCHICAL CIRCUIT FOR QUIESCENT CURRENT TESTING AND CIRCUIT PRODUCED THEREBY**

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(57) **ABSTRACT**

A method of designing integrated circuits having an hierarchical structure for quiescent current testing, and the circuit which results therefrom is disclosed. The method comprises analyzing each of one or more selected hierarchical blocks independently of other selected blocks identify any circuit states of each block which could result in elevated quiescent current levels during quiescent current testing of the circuit, the analysis beginning with blocks at a lowest level of hierarchy and proceeding in sequence through each level of design hierarchy to a highest level of hierarchy containing a top-level block; and calculating a fault coverage for each selected block.

