# Complete, Contactless I/O Testing – Reaching the Boundary in Minimizing Digital IC Testing Cost

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## Abstract

*Embedded test of memory and random logic can enable very low cost ATE to test large, high speed ICs because high quality at-speed tests can be generated on-chip. However, it is also necessary to test the DC and AC parameters of the input/output (I/O) circuitry. This paper describes how most I/O pin characteristics can be tested cost-effectively with a variety of novel techniques that exploit the 1149.1 and 1149.4 test standards. The techniques measure VOL/IOL, VOH/IOH, VIH, and VIL at DC, perform at-speed I/O wrap, and test on-chip power rail impedance, all via minimum pin-count (MPC) access. The 1149.4 bus is also suitable, of course, for testing mixed-signal functions. The paper then discusses costs and benefits of MPC testing of high pin-count ICs on a low cost tester to show that testing costs can be reduced to insignificance.*

## 1. Introduction

Reduced pin-count (RPC) testing has been proposed [1], [2], [3] to facilitate low-cost probe testing of high pin-count ICs – it can also facilitate multi-site testing. These techniques contact between 10 and 64 digital pins, including at least the four or five IEEE 1149.1 Test Access Port (TAP) pins. Conventional probe cards limit robust digital test frequencies to less than 10 MHz, however, probe cards are available that can handle much higher frequencies for a smaller number of probes or a higher cost. Of course, the tester must be able to accurately deliver these higher frequencies (or more accurate signal edge timing).

Although the reported RPC probe techniques test the logic core and embedded memories via scan or BIST, and test the basic structure of wrap-around input/output (I/O) circuitry, the I/O pin DC and AC parameters are not tested, with the exception of pin leakage current as reported in [3][9]. The resultant yield dropout in the subsequent full pin-count (FPC) Final test, due to insufficient I/O parametric performance, will usually be less than 1% as suggested in [2], so not probe testing I/O parametric performance would appear to have minimal cost impact. However, I/O parametric tests are often regarded as essential at Wafer Sort, for several reasons: Wafer Sort and Final (package) tests are typically performed at different temperatures to improve fault coverage; parametric tests during Wafer Sort provide an early indication of processing quality; some ICs are only ever tested at the wafer level, i.e., those destined for chip scale packaging (CSP) or multi-chip modules (MCM).

BIST is widely used for testing embedded SRAM because the quality of simple scan-access testing is inadequate, the number of memories is too many for direct access, the fault coverage of some BIST algorithms has been demonstrated to be equivalent to direct access, the patterns can be applied at higher speed by BIST, and the number of test patterns is too many for single-site testing by conventional ATE. Programmable BIST for embedded DRAM offers the same benefits, plus new algorithms can be applied if new defect mechanisms are found after silicon fabrication. The test time for memory BIST which applies the patterns at-speed is therefore the minimum possible (or very nearly). For example, a megabit of SRAM, partitioned as four 8Kx32b SRAMs, can be tested sequentially by one BIST controller having a 22N algorithm, and operating at 25 MHz, in 70 ms.

Recent experiments by Prof. McCluskey and his students [22] provide an interesting conclusion regarding BIST for random logic: the only combinational logic test that achieved zero test escapes, relative to an exhaustive test, was pseudo-random patterns applied at-speed until every stuck-at fault had been detected at least fifteen times.

Therefore, one can conclude that random logic and embedded memories could be structurally tested by BIST, and that functional tests for these functions might no longer be necessary to achieve zero test escapes (if the BIST is applied consistent with the above experiment). The test time for BIST of logic can be reduced, almost arbitrarily, by reducing the length of the scan chains and increasing the number of scan chains. In practice, the number of scan chains is limited to several hundred per pseudo-random pattern generator (PRPG) to minimize interconnect. Circuit macro-blocks tend to contain less than 50,000 scan bits, so a hierarchical approach that uses one PRPG per macro block is sufficient to reduce all scan chains to less than 300 bits, and many blocks can be tested in parallel. If each pseudo-random scan pattern is shifted at half-speed (to consume power that is comparable to normal operation) but applied at-speed for a few clock cycles around the mission-mode cycle, then test times can be near minimum (for example: 500 bits × 50K vectors / 50MHz = 500 ms ).

It has previously been reported [20] that BIST for PLLs can be implemented digitally, and that the test time


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