US006000051A

United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 6,000,051**

[45] **Date of Patent: Dec. 7, 1999**

[54] **METHOD AND APPARATUS FOR HIGH-SPEED INTERCONNECT TESTING**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-Francois Côté** , both of Aylmer, Canada

[73] Assignee: **Logic Vision, Inc.**, San Jose, Calif.

[21] Appl. No.: **08/948,842**

[22] Filed: **Oct. 10, 1997**

[51] **Int. Cl.**[6] **G01R 31/28**

[52] **U.S. Cl.** **714/727**; 714/731; 327/144

[58] **Field of Search** 714/731, 727, 714/726, 724, 729, 733, 734, 814, 815, 30; 327/144, 141; 377/77, 78, 81

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,494,066	1/1985	Goel et al.	714/726
5,109,190	4/1992	Sakashita et al.	714/727
5,463,338	10/1995	Yurash	327/202
5,774,476	6/1998	Pressly et al.	714/726

OTHER PUBLICATIONS

Y. Zorian et al., "An Effective Multi–Chip BIST Scheme", Journal of Electronic Testing: Theory and Applications 10, (1997), pp. 87–95.

T.M. Storey et al., "A Test Methodology for High Performance MCMs", Journal of Electronic Testing: Theory and Applications 10, (1977), pp. 109–118.

C. Maunder et al., "Boundary–Scan, A framework for structured design–for–test", IEEE 1987 International Test Conference, Paper 30.1, (1987), pp. 714–723.

IEEE Standard Test Access Port and Boundary–Scan Architecture, IEEE Standard 1149.1–1990 (Includes IEEE Standard 1149.1a–1993) pp. 1–1 to 1–5; 5–1 to 5–16.

Primary Examiner—Trinh L. Tu

Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] **ABSTRACT**

A method of testing high speed interconnectivity of circuit boards having components operable at a high speed system clock, employing an IEEE 1149.1 standard test method in which test data is shifted into and from the components at the rate of a test clock during Shift_In and Shift_Out operations, and having an Update operation and a Capture operation between the Shift_In and Shift_Out operations, the components including a first group of components capable of performing the Update and Capture operations at the rate of the Test Clock only and a second group of components capable of performing the Update and Capture operations at the rate of the system clock, the method comprising the steps of performing the Shift_In operation in all of the components concurrently at the rate of the Test Clock; performing the Update and Capture Operations in the first group of components at the rate of the Test Clock; and performing the Update and Capture Operations in the second group of components at the rate of the system Clock. The method employs a novel integrated circuit, test controller and boundary scan cells.

43 Claims, 8 Drawing Sheets