US 20050273683A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2005/0273683 A1**

(43) **Pub. Date: Dec. 8, 2005**

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(54) **INSERTION OF EMBEDDED TEST IN RTL TO GDSII FLOW**

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(21) Appl. No.: **11/144,764**

(22) Filed: **Jun. 6, 2005**

Related U.S. Application Data

(60) Provisional application No. 60/577,171, filed on Jun. 7, 2004.

Publication Classification

(51) **Int. Cl.**[7] **G01R 31/28**; G06F 17/50

(52) **U.S. Cl.** **714/726**; 716/4; 716/18

(57) **ABSTRACT**

A method of designing a scan testable integrated circuit with embedded test objects for use in scan testing the circuit, comprises compiling a register-transfer level (RTL) circuit description of the circuit into an unmapped circuit description; extracting information from the unmapped circuit description for use in generating and inserting RTL descriptions of test objects into the RTL circuit description and for use in generating and inserting scan chains into the circuit; generating and inserting the RTL descriptions of the test objects into the RTL circuit description to produce a modified RTL circuit description; storing the modified RTL circuit description; synthesizing the modified RTL description into a gate level circuit description of the circuit; and constructing and inserting scan chains into the gate level circuit description according to information extracted from the unmapped circuit description.