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(54) **METHOD OF TESTING AT-SPEED CIRCUITS HAVING ASYNCHRONOUS CLOCKS AND CONTROLLER FOR USE THEREWITH**

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(58) **Field of Search** 714/726, 727, 714/729, 731

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(57) **ABSTRACT**

A method of testing the core logic in a digital system, the method having a sequence of test operations including a shift-in operation in which a test stimulus is shifted into scanable memory elements in the core logic, a capture operation in which data in the memory elements is captured, and a shift-out operation in which captured data is shifted out of the core logic for analysis, comprises the improvement of, for each the test operation, concurrently enabling the domain clock of each clock domain in the core logic at the beginning of each test operation, performing the test operation in each domain and disabling the domain clock at the end of each test operation in each domain. The method allows all of the clock domains, including signal paths which traverse domain boundaries and/or have multi-cycle paths to be tested concurrently and at their respective functional clock rate of each clock.

31 Claims, 3 Drawing Sheets