A 180-MHz 0.8-μm BiCMOS Modular Memory Family of DRAM and Multiport SRAM

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***Abstract*—This paper describes a family of modular memories with a built-in self-test interface designed using a synchronous self-timed architecture. This approach is ideally suited to modular memories embedded within synchronous systems due to its simple boundary specification, excellent speed/power performance, and ease of modeling. The basic port design is self-contained and extensible to any number of ports sharing access to a common-core cell array. The same design has been used to implement modular one-, two-, and four-port SRAM's and a one-port DRAM based on a four-transistor (4-T) cell. The latter provides a 45% core cell density improvement over the one-port SRAM. Nominal access and cycle times of 5.5 ns for 64-kb blocks have been shown for a 0.8-μm BiCMOS process with no memory process enhancements. System operation at 100 MHz has been demonstrated on a broad-band time-switch chip containing 96 kb of two-port SRAM.**

I. Introduction

MODULAR memory is an essential component of any digital IC design library. Telecommunications circuits make extensive use of embedded RAM in a wide variety of applications including processor data and microcode stores, time-switch cores, register files, elastic stores, buffers, finite state machine registers, and caches. The ability to create any memory size and configuration provides system designers with the power and flexibility required to optimize designs for custom applications. The availability of a multiport capability adds an additional dimension of flexibility that can often simplify a system design. Systems are further simplified when embedded memories present a synchronous interface in which a minimum number of timing-critical signals are presented at its boundary.

Thus, in developing the modular RAM family for a mixed-signal 0.8-μm BiCMOS ASIC process technology [1], the following objectives were set out:

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TABLE I
RAM Family Modularity Range

Parameter	Min	Step	Max
Words	16	–	8k
I/O Bits per Word	1	1	64
Total Bits	16	–	64k
Rows	8	2	256
Columns	2	2	256
Columns per I/O Bit	2	2	32
Row Address Bits	3	1	8
Column Address Bits	1	1	5

1) Design an interface which would enable system designers to easily deploy embedded RAM's within a predominantly synchronous design environment in such a way that the system function and timing are easily predicted, implemented, and tested.
2) Achieve 100-MHz worst-case system operation (4.5 V, 105°C) for a broad-band time switch containing 96K of two-port SRAM with memory power dissipation less than 500 mW.
3) Create a reusable design with fine grain modularity up to a maximum 64K contiguous block size as specified in Table I.
4) Provide multiport functional capability (up to four ports).
5) Exploit the existing BiCMOS process technology, which has no memory enhancements in its flow, to yield a high-density memory beyond that achievable with a standard six-transistor (6-T) cell.

These objectives were achieved using a synchronous self-timed design style. The result is a four-member family of DRAM and multiport SRAM built around 6-, 8-, and 12-transistor SRAM cells (for one-, two-, four-port functions) and a 4-T one-port DRAM cell. Each member has virtually identical schematics and is capable of operating at 5.5 ns or better nominal cycle times over the entire modularity range listed in Table I.

The achievement of a single, reusable design covering this broad range of size and functionality has not been previously reported. Previous works on modular memory such as [2]–[5] have not employed internal self-timing and thus do not have the simple synchronous interface presented here. Although other fixed-block-size, self-timed RAM's have been reported

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