2020 25th IEEE European Test Symposium (ETS)

MBIST Support for Reliable eMRAM Sensing

Jongsin Yun
Mentor, A Siemens Business
Wilsonville, USA
jongsin_yun@mentor.com

Benoit Nadeau-Dostie
Mentor, A Siemens Business
Ottawa, Canada
benoit_nadeau-dostie@mentor.com

Martin Keim
Mentor, A Siemens Business
Wilsonville, USA
martin_keim@mentor.com

Cyrille Dray
ARM
Sophia Antipolis, France
Cyrille.Dray@arm.com

Mehdi Boujamaa
ARM
Sophia Antipolis, France
Mehdi.Boujamaa@arm.com

***Abstract*—eMRAM (embedded Magnetoresistive Random Access Memory) is an attractive solution in many non-volatile memory applications because of its small size, fast operation speed, and good endurance. However, due to a relatively small on/off resistance separation, it is a challenge to set an optimal reference resistance to reliably differentiate between a read memory data "1" and "0". Several trimming circuits are described in the literature to finely adjust a reference resistance value. These circuits are controlled from chip inputs causing time-consuming tests and off-chip engineering analysis. This paper presents a fully automated on-chip trimming process leveraging existing memory BIST (Built-In Self-Test) resources. It analyzes a massive amount of array property data with a minimal number of tests and optimizes the reference trim settings on-chip without the need for any external intervention.**

Keywords—MRAM, yield, trim, reference, read operation.

I. Introduction

STT (Spin-Transfer Torque)-MRAM is a type of memory that encodes data as a spin polarity of magnets in its ferromagnetic metal layer. Based on the polarity of the layer, the resistivity of the MRAM cell can be switched to either a high (anti-parallel, R_{AP}) or a low (parallel, R_P) value as shown in Fig. 1. The switching of a memory datum is achieved by spin-polarized tunneling current flowing through MTJ (Magnetic Tunnel Junction) which exerts torque on the local magnetization. Slonczewski [1] and Brinkman [2] well explained the switching mechanisms and tunneling conductance behaviors. Several studies show fast switching and high endurance of MRAM to propose MRAM as a potential replacement solution for last level cache memory [3-6].

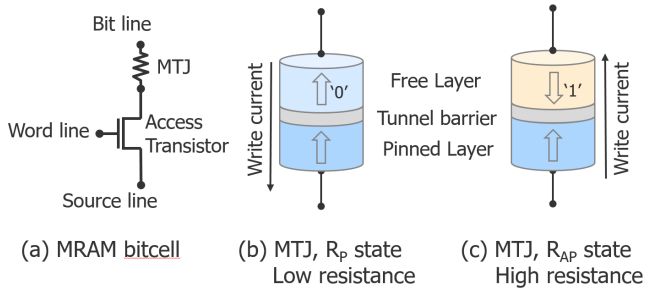

Fig. 1. The component of MRAM bitcell and its MTJ states

During Read operation, an MTJ resistance in a selected bitcell (R_{bit}) is compared with a reference resistance (R_{REF}). The read value is said to be "1" ("0") when its resistance is higher (lower) than that of R_{REF}. The resistance comparison is done by amplifying the differential of Bit Line (BL) discharging rates between the active BL and the reference BL.

An example of On and Off state resistances distribution of an MRAM is illustrated in Fig. 2 (a). To read all memory data correctly, the reference resistance value must be set lower than any R_{AP} state ("1") resistance and, at the same time, higher than any R_P state ("0") resistance. The reference resistance should be set between the distribution tails of R_P and R_{AP}. These tail bits are weakest bits in the array that is unstably changing by process update, array configuration, total array size, temperature use case, etc. Setting R_{REF} is especially challenging in MRAM because the On and Off state resistance separation is 1 or 2 orders of magnitude smaller in MRAM with respect to other types of resistive memories. Moreover, inherent variations from a large memory array and inhomogeneous temperature sensitivity between R_P and R_{AP} makes it even more challenging to set the correct reference resistance.

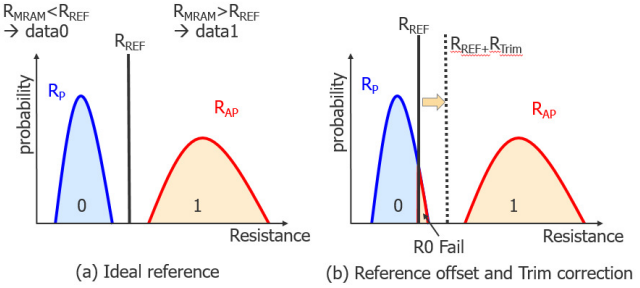

Fig. 2. distribution of MRAM Resistance for value "1" and "0" with sensing reference resistance setting.

A hardware preset R_{REF} may become inadequate for some of the bit-cells due to process update and other variances that happen after the design completion. This reference setting will incorrectly interpret some of the logical "0" state memory data as a logical "1" and hence cause a Read0 (R0) fail as we illustrate in Fig. 2 (b). Reference trimming circuits are suggested in recent MRAM application literature [3, 4] to accommodate this issue. The authors connect switchable series resistances to the reference BL to add additive resistance R_{Trim} into R_{REF}. This shifts the overall reference resistance value to a proper value. Such a trimming circuit allows post-manufacturing fine-tuning of the reference resistance from the device IOs. The reference trim adjustment process improves the read margin for both of the data types '1' and '0', therefore, increasing reliable sensing of the stored logical value and increase yield.

Collecting and analyzing the full set of memory properties is another challenge. It requires an impractically large amount of test resource to measure and analyze analog properties of a full array, such as resistance value of each cell at the state of "1" and "0". If only a small number of cells would be sampled for the test, it may be difficult to capture the tail behavior of

978-1-7281-4312-5/20/$31.00 ©2020 IEEE