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(54) **METHOD AND APPARATUS FOR TESTING HIGH PERFORMANCE CIRCUITS**

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(52) **U.S. Cl.** **714/724**; 714/726; 714/729; 714/731
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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,349,587	A		9/1994	Nadeau-Dostie et al.	714/729
5,450,418	A	*	9/1995	Ganapathy	714/735
5,889,788	A	*	3/1999	Pressly et al.	714/726
6,145,105	A	*	11/2000	Nadeau-Dostie et al.	714/726
6,327,684	B1	*	12/2001	Nadeau-Dostie et al.	714/731
6,327,685	B1	*	12/2001	Koprowski et al.	365/201
6,442,722	B1	*	8/2002	Nadeau-Dostie et al.	714/731

FOREIGN PATENT DOCUMENTS

EP 0 549 130 A2 6/1993

* cited by examiner

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(57) **ABSTRACT**

A method for at-speed testing high-performance digital systems and circuits having combinational logic and memory elements that may be both scannable and non-scannable is performed by enabling at least two clock pulses during a capture sequence following a shift sequence. The method provides for initialization of any non-scannable memory elements via the scannable memory elements at the beginning of the test before an at-speed test is performed. During initialization, control logic generates a signal to disable the generation of system clock pulses for capture. Instead, only one clock cycle derived from the test clock or a system clock is generated to initialize the non-scannable elements. The number of shift sequences required depends on the maximum number of non-scannable elements that must be traversed between two scannable memory elements. During the same initialization period, the output response analyzer is disabled since unknown data values will present in the stream of data shifted out. A test controller is clocked a test clock and includes a clock generation module for generating shift and capture clocks. The test clock can be an independent and asynchronous clock or derived from the system clock. The test can also be performed by using only the test clock in the case only the test clock is available or for diagnostic and debug purposes.

44 Claims, 4 Drawing Sheets