US006145105A

United States Patent [19]

Nadeau-Dostie et al.

[11] **Patent Number: 6,145,105**

[45] **Date of Patent: Nov. 7, 2000**

[54] **METHOD AND APPARATUS FOR SCAN TESTING DIGITAL CIRCUITS**

[75] Inventors: **Benoit Nadeau-Dostie**; **Jean-François Côté** , both of Aylmer; **Dwayne Burek**, Nepean, all of Canada

[73] Assignee: **LogicVision, Inc.**, San Jose, Calif.

[21] Appl. No.: **09/192,839**

[22] Filed: **Nov. 16, 1998**

Related U.S. Application Data

[63] Continuation of application No. 08/752,499, Nov. 20, 1996.

[51] **Int. Cl.**[7] **G01R 31/28**

[52] **U.S. Cl.** **714/726**

[58] **Field of Search** 714/726, 727, 714/728, 733, 736, 30; 324/765

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,503,537	3/1985	McAnney	714/728
5,329,533	7/1994	Lin	714/727
5,349,587	9/1994	Nadeau-Dostie et al.	714/727
5,459,736	10/1995	Nakamura	714/727
5,519,714	5/1996	Nakamura et al.	714/727
5,533,032	7/1996	Johnson	714/733
5,614,838	3/1997	Jaber et al.	324/765
5,627,841	5/1997	Nakamura	714/731

OTHER PUBLICATIONS

Kee Sup Kim and Len Schultz, "Multi–Frequency, Multi–Phase Scan Chain," IEEE International Test Conference 1994, Paper 11.1, pp. 323–330.

Primary Examiner—Albert De Cady
Assistant Examiner—Jason Greene
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel LLP; Norman R. Klivans

[57] **ABSTRACT**

A method and digital system for testing scannable memory and combinational networks. The scannable memory is configurable into several scan chains. Each chain may have a different effective clock rate, as determined by respective clock enable signals. The method and digital system allow scan testing of digital circuits that use a single operational clock rate and several functional clock enable signals to effect slower lock operating rates. The digital system includes memory elements having scan enable and clock enable inputs.

28 Claims, 9 Drawing Sheets