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(19) **United States**(12) **Patent Application Publication**
Nadeau-Dostie et al.(10) **Pub. No.: US 2005/0240790 A1**(43) **Pub. Date: Oct. 27, 2005**(54) **CLOCKING METHODOLOGY FOR
AT-SPEED TESTING OF SCAN CIRCUITS
WITH SYNCHRONOUS CLOCKS**(52) **U.S. Cl. 713/400**(75) **Inventors: Benoit Nadeau-Dostie, Gatineau (CA);
Jean-Francois Cote, Chelsea (CA);
Fadi Maamari, San Jose, CA (US)**(57) **ABSTRACT**

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A clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in a scan circuit, each path originating from a source memory element in one of the domains and terminating at a destination memory element in another of the domains and comprises selectively aligning either a capture edge or a launch edge of the clock of each domain with a corresponding edge of at least one other domain of the interacting synchronous clock domains to determine the cross-domain paths to be tested between a source domain and a destination domain; clocking memory elements in each domain at respective domain clock rates to launch signal transitions from source memory elements in source domains; and for each pair of interacting clock domains under test, capturing, in the destination domain, circuit responses to signal transitions launched along paths originating from the source domain and selectively disabling capturing, in the source domain, of circuit responses to signal transitions launched along paths originating from the destination domain.

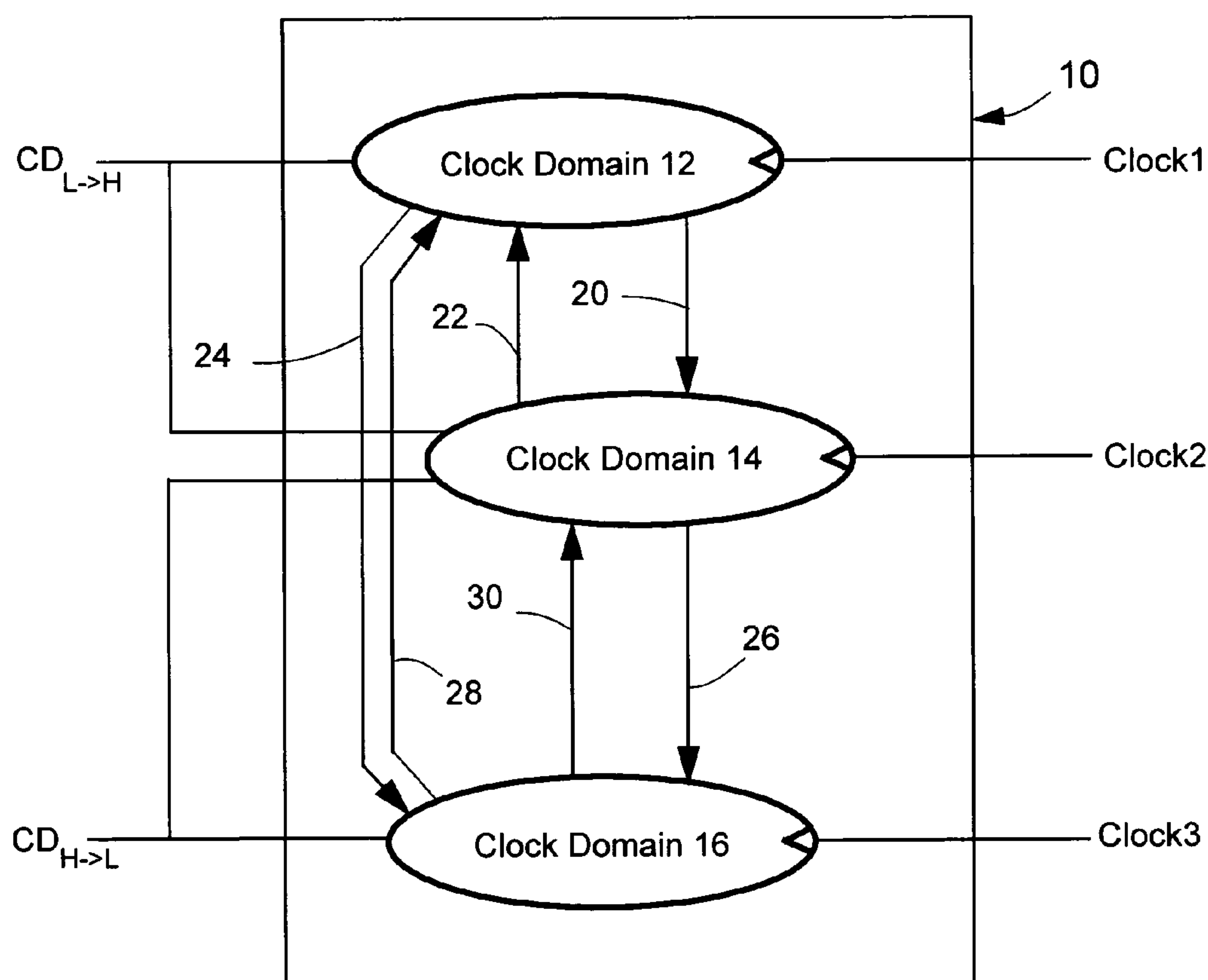
(73) **Assignee: LogicVision, Inc., San Jose, CA (US)**(21) **Appl. No.: 11/060,407**(22) **Filed: Feb. 18, 2005****Related U.S. Application Data**(60) **Provisional application No. 60/564,210, filed on Apr. 22, 2004. Provisional application No. 60/579,649, filed on Jun. 16, 2004.****Publication Classification**(51) **Int. Cl.⁷ G06F 13/42**

Fig. 1.

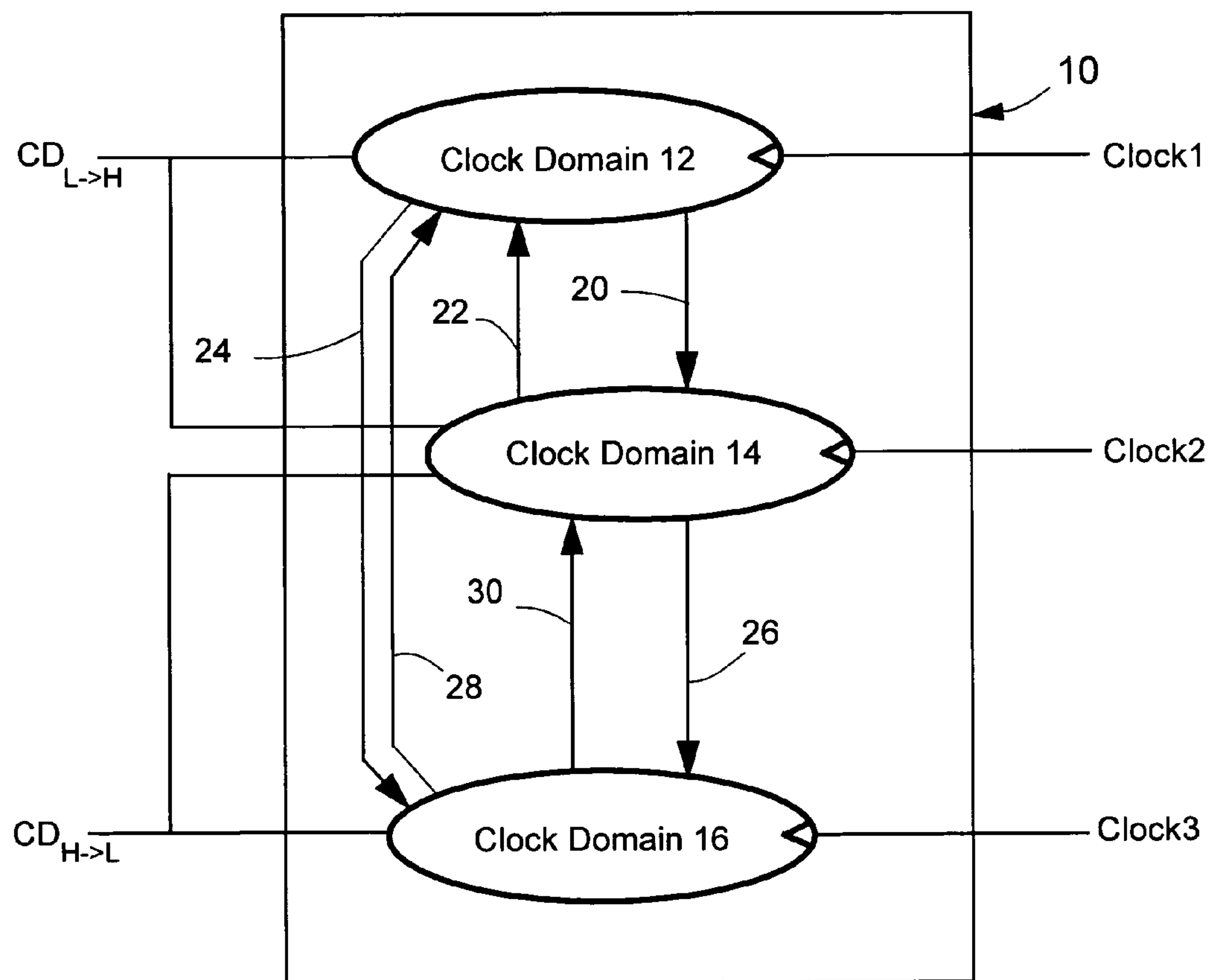


Fig. 2a.

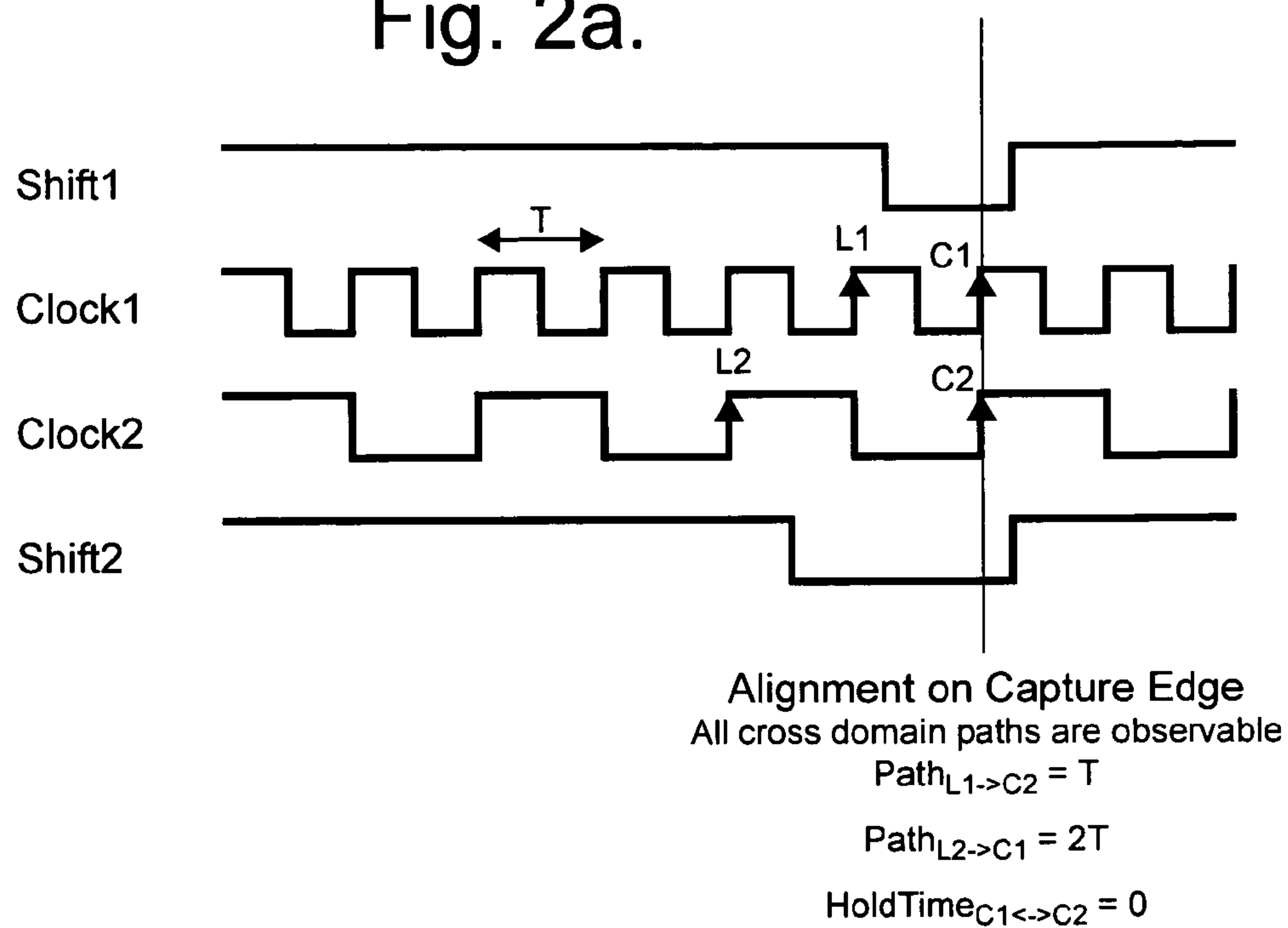


Fig. 2b.

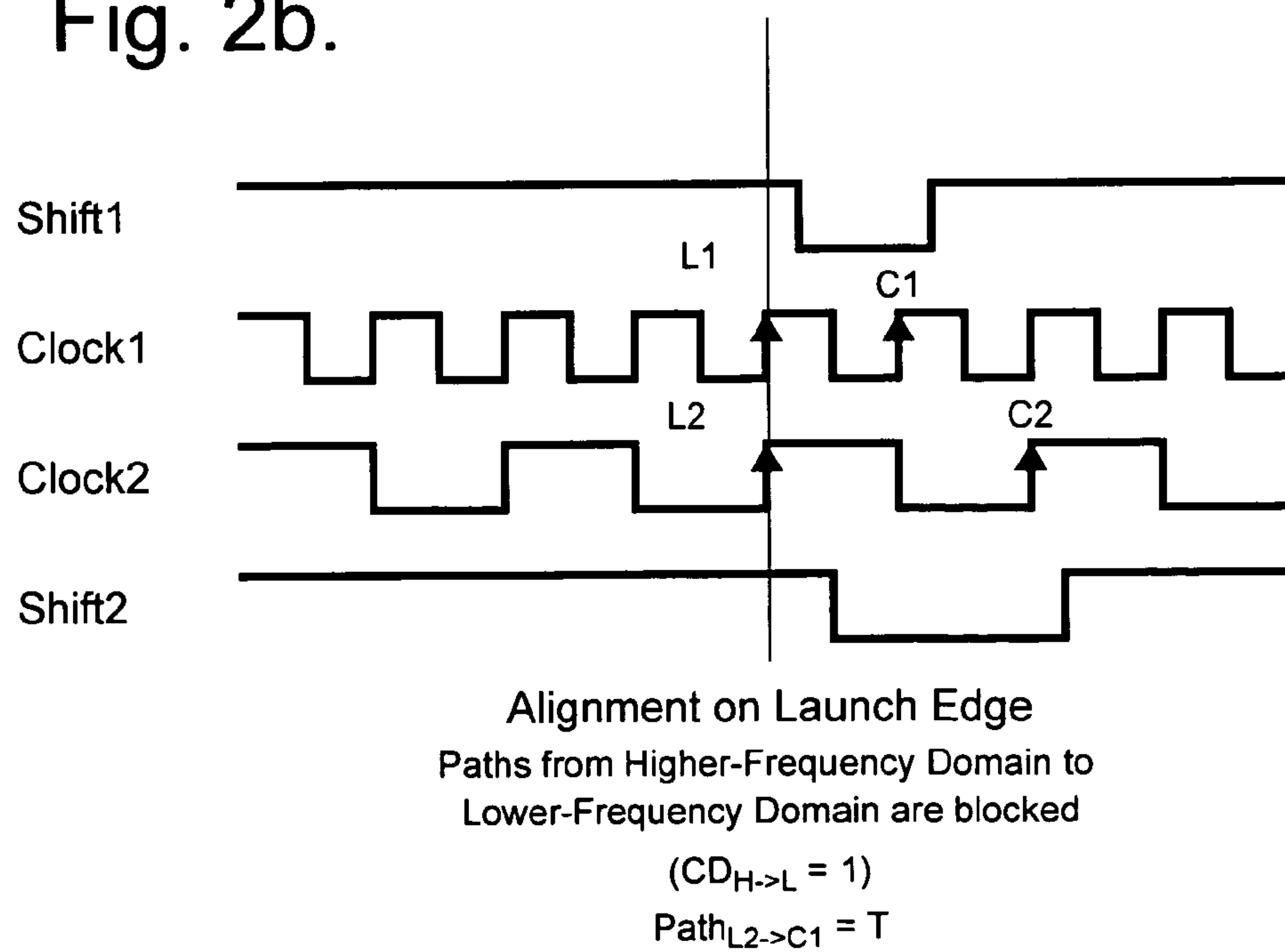


Fig. 3a.

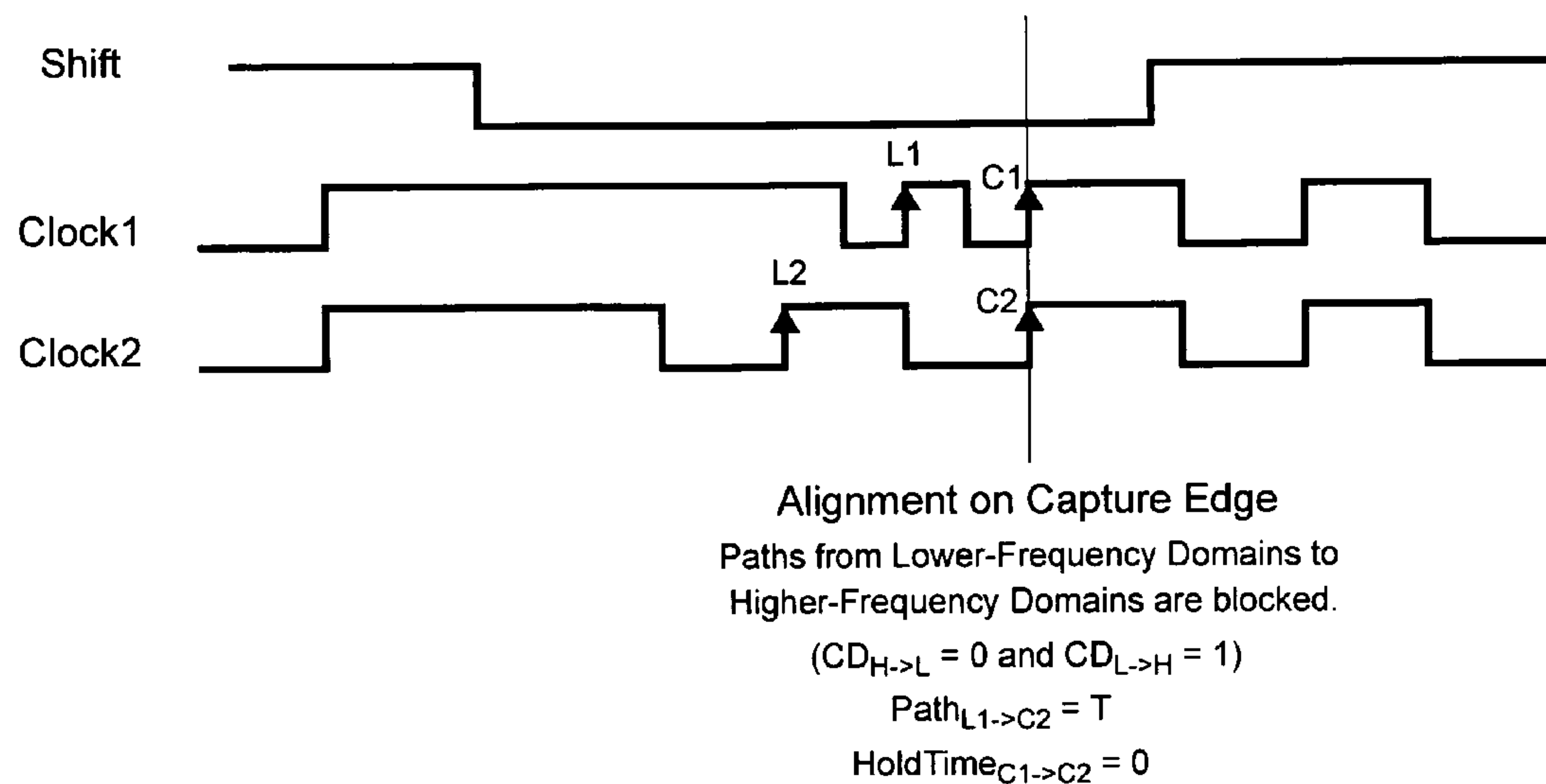
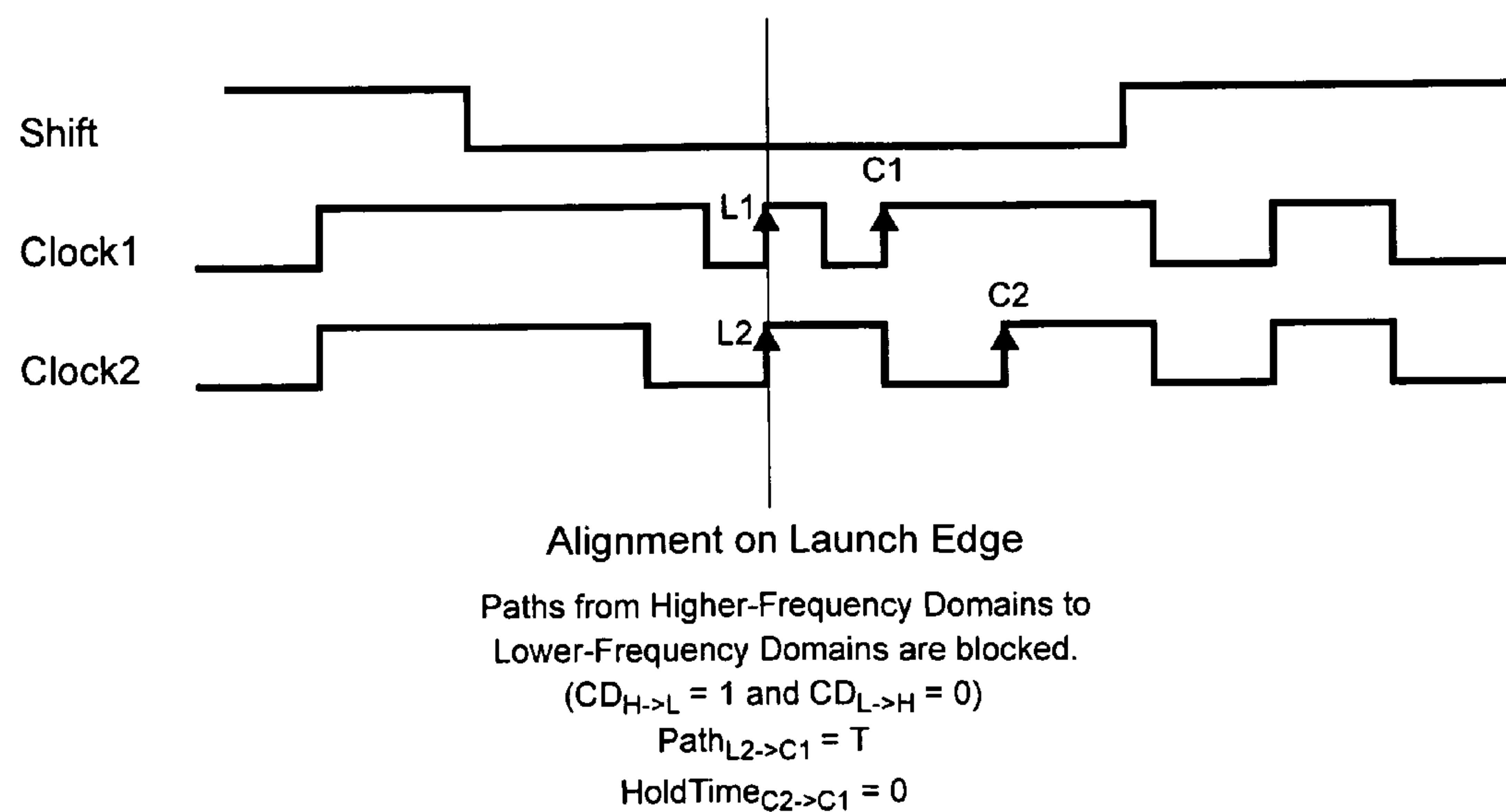


Fig. 3b.



CLOCKING METHODOLOGY FOR AT-SPEED TESTING OF SCAN CIRCUITS WITH SYNCHRONOUS CLOCKS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Patent Application Ser. Nos. 60/564,210 and 60/579,649 filed Apr. 22, 2004, and Jun. 15, 2004, respectively, both incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention generally relates to integrated circuits and, more specifically, to at-speed testing of scan circuits having interacting synchronous clock domains.

[0004] 2. Description of Related Art

[0005] Scan circuits consist of logic and memory elements which are configurable in a shift mode and a capture mode. Scannable memory elements are organized into scan chains. Shift mode is used to load test patterns into scan chains in a circuit and unload circuit responses from the circuit. Capture mode is used to capture circuit responses to the test patterns.

[0006] Delay tests are performed by launching a signal transition from a source memory element and capturing the effect of the signal transition at a destination memory element. Two methodologies are used to perform delay tests: launch-on-shift, also known as "single capture", and launch-on-capture also known as "double capture". Performing delay tests on Interacting synchronous clock domains present particular problems.

[0007] U.S. Pat. No. 5,349,587 issued on Sep. 20, 1994, for "Multiple Clock Rate Test Apparatus for Testing Digital Systems" (Docket No. NTPAT001), U.S. Pat. No. 6,145,105 Issued on Nov. 7, 2000 for "Method and Apparatus for Scan Testing Digital Circuits" (Docket No. LVPAT002US), and U.S. Pat. No. 6,115,827 issued on Sep. 5, 2000 for "Clock Skew Management Method and Apparatus (Docket No. LVPAT008US), all incorporated herein by reference, disclose methods of testing circuits having interacting clock domains.

[0008] Nadeau-Dostie et al. U.S. Pat. No. 5,349,587 discloses a method for testing paths between memory elements that are clocked by different clocks which are synchronous to each other using the launch-on-shift method. Paths from a lower frequency domain to a higher frequency domain are tested for a propagation time equal to the period of the lower-frequency clock. While this test provides fair coverage of delay defects and simplifies the analysis of the circuit (the circuit to be analyzed is combinational, i.e., sequential depth is 0), it is sometimes desirable to test for a propagation time equal to the period of the higher-frequency clock. The patent does not disclose a method by which this can be achieved. Another limitation of the method is that it does not address the case for which launch-on-capture clocking methodology is used.

[0009] Other known methods test for cross-domain path propagation times equal to the period of the highest frequency clock, but the sequential depth of the circuit is such

that the coverage of delay defects is relatively low and the circuit analysis time for fault simulation and test generation is prohibitive.

SUMMARY OF THE INVENTION

[0010] The present invention seeks to provide a clocking method for at-speed testing of cross-domain paths between synchronous clock domains for a propagation time equal to the period of the higher frequency clock, which minimizes the sequential depth of the circuit to be analyzed and which can be used for both launch-on-shift and launch-on-capture methodologies.

[0011] For tests using launch-on-shift methodology, the circuit to be analyzed is combinational and, therefore, has a sequential depth of 0. For circuits using launch-on-capture methodology, the circuit to be analyzed has a sequential depth of 1. The method is particularly useful in a self-test environment because of the predictability of the signal values captured by the scannable memory elements.

[0012] The method of the present invention is generally defined as a clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in a scan circuit. Each cross-domain path originates from a source memory element in one of the domains and terminates at a destination memory element in another of the domains and each memory element forms part of a scan chain in the circuit. The method comprises:

[0013] selectively aligning either a capture edge or a launch edge of the clock of each domain with a corresponding edge of at least one other domain of the interacting synchronous clock domains to determine the cross-domain paths to be tested between a source domain and a destination domain;

[0014] clocking memory elements in each domain at respective domain clock rates to launch signal transitions from source memory elements in source domains;

[0015] for each pair of interacting clock domains under test, capturing, in the destination domain, circuit responses to signal transitions launched along paths originating from the source domain and selectively disabling capturing, in the source domain, of circuit responses to signal transitions launched along paths originating from the destination domain; and

[0016] determining that a delay defect exists on a cross-domain path when a circuit response captured in its associated destination memory element is different from an expected response.

[0017] In one embodiment, paths from higher-frequency domains to lower-frequency domains are tested for a propagation time corresponding to the period of the clock which controls source memory elements in higher-frequency domains by aligning the capture edge of the clock of all of the synchronous clock domains, clocking the memory elements at respective domain clock rates to launch signal transitions from the source memory elements and capturing circuit responses in all destination memory elements in lower-frequency domains. Paths from lower-frequency-domains to higher-frequency domains are disabled. Paths from lower-frequency domains to higher-frequency domains are

tested for a propagation time corresponding to the period of the clock which controls destination memory elements in higher-frequency domains by aligning the launch edge of the clock of all of the synchronous clock domains, clocking the memory elements at respective domain clock rates to launch signal transitions from the source memory elements and capturing circuit responses in all destination memory elements in higher-frequency domains. Paths from higher-frequency domains to lower-frequency domains are disabled.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings in which:

[0019] **FIG. 1** diagrammatically illustrates a simple circuit having three interacting synchronous clock domains;

[0020] **FIG. 2a** illustrates capture edge alignment waveforms of a dual clock alignment for launch-on-shift methodology, according to an embodiment of the present invention, to enable all paths from higher-frequency domains to lower-frequency domains to be tested for a propagation time corresponding to the period of source memory elements, the period of the higher frequency clock;

[0021] **FIG. 2b** illustrates launch clock alignment waveforms of a dual clock alignment for launch-on-shift methodology, according to an embodiment of the present invention, to enable all paths from lower-frequency domains to higher-frequency domains to be tested for a propagation time corresponding to the period of destination memory elements, the period of the higher frequency clock, according to an embodiment of the present invention;

[0022] **FIG. 3a** illustrates capture edge alignment waveforms of a dual clock alignment for launch-on-capture methodology, according to an embodiment of the present invention, to enable all paths from higher-frequency domains to lower-frequency domains to be tested for a propagation time corresponding to the period of source memory elements; and

[0023] **FIG. 3b** illustrates launch edge alignment waveforms of a dual clock alignment for launch-on-capture methodology, according to an embodiment of the present invention, to enable all paths from lower-frequency domains to higher-frequency domains to be tested for a propagation time corresponding to the period of destination memory elements.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0024] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components and circuits have not been described in detail so as not to obscure aspects of the present invention.

[0025] The present invention uses a dual clock alignment to detect delay defects on cross-domain paths that originate at a source memory element in one domain and terminate at

a destination memory element in another domain. The dual clock alignments are alignment of capture edges and alignment of launch edges. The first clock alignment aligns the capture edge of all interacting synchronous clock domains under test to enable all paths from higher-frequency domains to lower-frequency domains to be tested for a propagation time corresponding to the period of source memory elements—the period of the higher frequency clock. The second clock alignment aligns the launch edge of all clock domains under test to enable all paths from lower-frequency domains to higher-frequency domains to be tested for a propagation time corresponding to the period of destination memory elements—the period of the higher frequency clock.

[0026] In the launch-aligned embodiment, the capture operation of destination memory elements which could cause an increase of the sequential depth of the circuit is suppressed. These are paths from higher-frequency domains to lower-frequency domains. In the capture-aligned embodiment, paths from lower-frequency domains to higher-frequency domains would cause an increase of the sequential depth. In launch-on-capture methodology, circuitry is provided to disable such paths, whereas in launch-on-shift methodology, such circuitry is not necessary. Capture suppression can be performed by configuring the memory element in a non-capture mode, such as shift mode or hold mode. The hold mode can be implemented by adding a holding multiplexer to a scannable memory element or by gating the clock of the memory element. The hold time between two clock domains is verified concurrently with verification of the propagation time between two domains.

[0027] **FIG. 1** diagrammatically illustrates a simple circuit 10 having three interacting synchronous clock domains 12, 14 and 16 with respective clocks Clock1, Clock2 and Clock3 and cross-domain paths. The frequencies of these clocks are multiples of each other. For example, Clock1 might have a frequency F with an associated period $T=1/F$, Clock2 has frequency $F/2$ with associated period $2T$, Clock3 has frequency $F/4$ with period $4T$. Each domain includes one or more scan chains (not shown) having memory elements (not shown) which are configurable in shift mode, used for loading test patterns and unloading circuit responses to the test patterns, and in capture mode, used for capturing circuit responses, as is well known in the art. The cross-domain paths originate at the output of a source memory element in one of the domains and terminate at the input of a destination memory element in another of the domains. Destination memory elements in each domain also receive a capture disable signal, CD, used for selectively disabling the capture operation of a destination memory element, as described below. For simplicity, the following description describes only the interaction between domains 12 and 14.

[0028] **Launch-On-Shift Methodology**

[0029] **FIGS. 2a** and **2b** show dual clock alignment waveforms for launch-on-shift methodology. **FIG. 2a** shows four signals. Shift1 is a shift enable signal used to configure memory elements controlled by Clock1 in shift mode. Shift2 serves the same purpose for memory elements controlled by Clock2. Clock1 and Clock2 are synchronous and their respective clock periods are T and $2T$. In the example, Shift1 and Shift2 are active high.

[0030] Signal transitions launched from a Clock1 edge are labeled L1 and transitions launched from a Clock2 edge are

labeled **L2**. In accordance with launch-on-shift methodology, these transitions are launched from memory elements that are configured in shift mode. After the launch occurs, the memory elements are configured in capture mode (inactive value of Shift1 and Shift2) and a capture operation occurs on the Clock1 edge labeled **C1** and on the Clock2 edge labeled **C2**.

[0031] In accordance with one step of the method of the present invention, capture edges **C1** and **C2** are aligned during the capture operation. With this alignment, all cross-domain paths are observable. Paths **20** originating from source memory elements controlled by the higher-frequency clock (Clock1) and terminating at destination memory elements controlled by the lower-frequency clock (Clock2) are tested for a propagation time of T —the period of the higher frequency clock. Paths **22** originating from source memory elements controlled by the lower-frequency clock (Clock2) and terminating at destination memory elements controlled by the higher-frequency clock (Clock1) are tested for a propagation time of $2T$ —the period of the lower frequency clock. The hold time relationship between Clock1 and Clock2 is also tested in both directions. These tests are performed by comparing a captured circuit response against a predetermined circuit response. For example, if a defect causes **C2** to be late to the point where the signal value captured at **C2** depends on the signal value captured at **C1**, instead of the signal values launched on **L1** and **L2** exclusively, this defect will be detected by an incorrect value in the captured circuit response.

[0032] In accordance with another step of the present invention, launch edges **L1** and **L2** are aligned prior to a capture operation. This alignment is used to test paths from lower-frequency domains to higher-frequency domains. In **FIG. 2b**, these are paths **L2**→**C1**. Paths originating from source memory elements controlled by the higher-frequency clock (Clock1) and terminating at destination memory elements controlled by the lower-frequency clock (Clock2) (paths **L1**→**C2**) are blocked by suppressing or disabling the capture operation of the destination memory elements. This is achieved by applying a Capture Disable signal, CD_{H-L} , to the appropriate destination memory elements. This minimizes the sequential depth of the circuit. If the capture operation is not suppressed, the signal value captured at **C2** will depend on the signal value captured at **C1**, instead of the signal values launched from **L1** and **L2** exclusively. In the waveforms shown, the circuit remains combinational which simplifies analysis significantly, both fault simulation and test pattern generation.

[0033] A control signal determines the edge alignment to be used and the suppression of the capture operation of destination memory elements which would cause an increase of circuit sequential depth for a given clock alignment. The control signal can be generated by an embedded test controller or an external tester as is the case for signal ClkAlignment in Applicant's co-pending Application No. 60/564,210, supra, which also describes a method by which the edges can be aligned. The value of the edge alignment signal can be selected randomly for each scan vector or kept constant for a group of scan vectors.

[0034] In general, for circuits having more than two frequencies, the capture edge of all clock domains under test may be aligned first. This alignment will enable all paths

from higher-frequency domains to lower-frequency domains to be tested for a propagation time corresponding to the period of the clock of source memory elements—the period of the higher-frequency clock. The hold time between all clock domains is also verified.

[0035] The following description describes the interaction between domains **12**, **14** and **16**. Clock domain **16** is clocked by a Clock3 (not shown) which has a period $4T$ and which is synchronous with respect to Clock1 and Clock2. The launch edge **L3** and capture edge **C3** of clock domain **16** are not shown. In accordance with an embodiment of the present invention, capture edges **C1**, **C2** and **C3** are aligned first. Paths **20** from clock domain **12** to clock domain **14** (paths **L1**→**C2**) and paths **24** from clock domain **12** to clock domain **16** (paths **L1**→**C3**) are all tested for a propagation time of T . Paths **26** from clock domain **14** to clock domain **16** (paths **L2**→**C3**) are tested for a propagation time of $2T$ —the period of the higher-frequency clock.

[0036] The second clock alignment aligns the launch edge of the clock of all clock domains. This alignment tests all paths from lower-frequency to higher-frequency domains for a propagation time corresponding to the period of the destination memory element—the period of the higher frequency clock. Therefore, paths **22** from clock domain **14** to clock domain **12** (paths **L2**→**C1**) and paths **28** from clock domain **16** to clock domain **12** (paths **L3**→**C1**) are tested for a propagation time of T and paths **30** from clock domain **16** to clock domain **14** (paths **L3**→**C2**) are tested for a propagation time of $2T$.

[0037] Paths from higher-frequency domains to lower-frequency domains, i.e., paths **L1**→**C2**, paths **L1**→**C3** and paths **L2**→**C3** (paths **20**, **24**, and **26** in **FIG. 1**), are blocked to limit the sequential depth of the circuit. In fact, the offending paths are better described by **L1**→**C1**→**C2**; **L1**→**C1**→**C3**; **L2**→**C2**→**C3**.

[0038] Destination memory elements can receive signal transitions from several clock domains, including its own. Thus, some useful paths are blocked when such a destination memory element receives signal transitions from domains having frequencies that are both higher and lower than its own. While this situation should be relatively rare and the test will still cover most delay defects, if it is desired to improve the test, a third clock alignment, in which some launch edges are aligned and some capture edges are aligned, can be used to test paths which were previously blocked.

[0039] In the foregoing example, paths from clock domain **16** to clock domain **14** that end at a destination memory element that also receives signals from clock domain **12** cannot be tested for a propagation time of $2T$. The paths are tested for a propagation time of $4T$ instead. However, a third clock alignment which aligns launch edges **L2** and **L3** and capture edges **C1** and **C2** will allow testing of paths from clock domain **16** to clock domain **14** (paths **L3**→**C2**) correctly. For this clock alignment, the paths **L1**→**C2** need not be blocked, thus allowing for testing for a propagation time of $2T$ on paths **L3**→**C2**, if desired.

[0040] In the examples above, it is possible that some paths will be longer than the period of the source or the destination memory element. There are at least two solutions to this problem. The first is to use the solution described and

claimed in Applicants' U.S. Pat. No. 6,145,105 (Applicants' Docket LVPAT002) that will cause the launch edge of the source memory element to occur earlier than that used by other memory elements of the same clock domain. The other is to use the clock alignment control signal to suppress the capture of destination memory elements.

[0041] Launch-On-Capture Methodology

[0042] FIGS. 3a and 3b show waveforms for dual clock alignment for launch-on-capture methodology. Three signals are shown. Shift is a shift enable signal used to configure all memory elements in shift mode. Clock1 and Clock2 are synchronous and their respective clock period is T and 2T. Signal transitions are launched from the Clock1 edge labeled L1 and from the Clock2 edge labeled L2. It will be noted that these transitions are launched from memory elements that are configured in capture mode (Shift is active high).

[0043] In accordance with the present invention, capture edges C1 and C2 are aligned to test paths from source memory elements controlled by higher-frequency clock, Clock1, to destination memory elements controlled by lower-frequency Clock2 for a propagation time of T—the period of the higher frequency clock. The hold time relationship from Clock1 to Clock2 is also tested ($\text{HoldTime}_{c1 \rightarrow c2} = 0$). Paths from lower-frequency clock domain 14 to higher-frequency clock domain 12 are suppressed to minimize the sequential depth of the circuit.

[0044] Launch edges L1 and L2 are aligned to test paths from lower-frequency clock domain 14 to higher-frequency clock domain 12 for a propagation time of T while paths from higher-frequency clock domain 12 to lower-frequency clock domain 14 are blocked. Hold time from Clock2 to Clock1 is also tested.

[0045] The control signal to select the clock alignment is generated in the manner explained for the launch-on-shift methodology, except that both the control signal and its inverted value are used to generate Capture Disable control signals labeled CD_{H-L} and CD_{L-H} in **FIG. 3**. CD_{L-H} suppresses paths from lower-frequency clock domain 14 to higher-frequency clock domain 12. CD_{H-L} suppresses paths from higher-frequency clock domain 12 to lower frequency clock domain 14.

[0046] Again, for circuits with more than two frequencies, a first clock alignment aligns the capture edge of all clocks. This will enable all paths from higher-frequency domains to lower-frequency domains to be tested for a propagation time corresponding to the period of the source memory element—the higher-frequency clock. Paths from lower-frequency domains to higher-frequency domains are blocked. The hold times from higher-frequency domains to lower-frequency domains are also tested.

[0047] As in the launch-on-shift methodology, some useful paths are blocked when a memory element receives signal transitions from domains having clock frequencies that are both higher and lower than its own. The clock alignment solution presented above can be used to test all useful paths. A partial solution using the method proposed in U.S. Pat. No. 6,115,827 can be used instead of using a third clock alignment in order to reduce complexity. For example, a destination memory element of clock domain 14 receiving signals from source memory elements of clock domain 16 and clock domain 12 would have its capture suppressed

whenever the launch edges are aligned or the source memory element of clock domain 16 is allowed to capture. It is otherwise allowed to capture on capture edge C2 as long as the source memory element in clock domain 16 is configured in hold mode on its launch edge L3.

[0048] Again, In the examples above, it is possible that some paths are longer than the period of the source or the destination memory element. There are at least two solutions to this problem and they are similar to the ones used for the launch-on-shift case. The first is to use the solution of U.S. application Ser. No. 09/773,541 filed Feb. 2, 2001 for “Method for Scan Testing of Digital Circuits, Integrated Circuit for Use Therewith and Program Product for Incorporating Test Method into Circuit” (Docket No. LVPAT031US) that will cause the launch edge of the source memory element to occur earlier than that used by other memory elements in the same clock domain. The other solution is to use the control signal to suppress the capture of destination memory elements.

[0049] In summary, it will be seen that the present invention provides a clocking methodology for at-speed testing of cross-domain paths between synchronous clock domains for a propagation time equal to the period of the higher frequency clock as well as testing for hold time violations. The method minimizes the sequential depth of the circuit and that the method can be used for both launch-on-shift and launch-on-capture methodologies.

[0050] Although the present invention has been described in detail with regard to preferred embodiments and drawings of the invention, it will be apparent to those skilled in the art that various adaptations, modifications and alterations may be accomplished without departing from the spirit and scope of the present invention. Accordingly, it is to be understood that the accompanying drawings as set forth hereinabove are not intended to limit the breadth of the present invention, which should be inferred only from the following claims and their appropriately construed legal equivalents.

What is claimed is:

1. A clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in a scan circuit, each said path originating from a source memory element in one of said domains and terminating at a destination memory element in another of said domains and each said memory element forming part of a scan chain in said circuit, said method comprising:

selectively aligning either a capture edge or a launch edge of the clock of each domain with a corresponding edge of at least one other domain of said interacting synchronous clock domains to determine the cross-domain paths to be tested between a source domain and a destination domain;

clocking memory elements in each domain at respective domain clock rates to launch signal transitions from source memory elements in source domains;

for each pair of interacting clock domains under test, capturing, in the destination domain, circuit responses to signal transitions launched along paths originating from the source domain and selectively disabling capturing, in the source domain, of circuit responses to signal transitions launched along paths originating from the destination domain; and

determining that a delay defect exists on a cross-domain path when a circuit response captured in its associated destination memory element is different from an expected response.

2. A method as defined in claim 1, further including, repeating a test with the other of said capture edge and launch edge selected.

3. A method as defined in claim 1, further including, selecting the edge to be aligned for each scan vector applied to said scan circuit.

4. A method as defined in claim 1, further including, selecting the same edge to be aligned for each vector of a group of scan vectors applied to said scan circuit.

5. A method as defined in claim 1, further including, randomly selecting the edge to be aligned for each scan vector applied to said scan circuit.

6. A method as defined in claim 1, said selectively disabling capturing including suppressing a capture operation of destination memory elements which could cause an increase of the sequential depth of the circuit.

7. A method as defined in claim 1, further including, performing said selectively aligning and selectively capturing under control of a clock edge alignment signal.

8. A method as defined in claim 1, further including, for circuits employing launch-on-shift methodology, suppressing paths from a higher-frequency domain to lower-frequency domain when said launch edge is selected.

9. A method as defined in claim 1, said suppressing paths comprises configuring destination memory elements in said paths in a non-capture mode.

10. A method as defined in claim 9, said non-capture mode being either a shift mode or a hold mode.

11. A method as defined in claim 1, further including, for circuits employing launch-on-capture methodology, suppressing paths from lower-frequency domains to higher-frequency domains when the selected edge is the capture edge and suppressing paths from higher-frequency domains to lower-frequency domains when the selected edge is the launch edge.

12. A method as defined in claim 1, said selectively aligning either a capture edge or a launch edge including generating an edge alignment signal for selecting between a capture edge alignment and a launch edge alignment; and

said selectively disabling capturing circuit responses in destination domains including applying a control signal to destination memory elements in destination domains to enable or disable capturing a circuit response therein.

13. A method as defined in claim 1, further including, for a circuit having more than two synchronous clock domains, aligning the capture edge of the clock of all said more than two clock domains to enable all paths from higher-frequency domains to lower-frequency domains to be tested for a propagation time corresponding to the period of higher frequency clocks and to verify the hold time between all clock domains.

14. A method as defined in claim 13, further including, aligning the launch edge of the clock of all of said more than two clock domains to enable all paths from lower-frequency to higher-frequency domains to be tested for a propagation time corresponding to the period of the destination memory element while blocking paths from higher-frequency domains to lower-frequency domains.

15. A method as defined in claim 14, further including, aligning launch edges of some of said more than two clock domains and aligning capture edges of remaining clock domains.

16. A method as defined in claim 1, further including, for a circuit having more than two synchronous clock domains, aligning the capture edge of the clock of all said more than two clock domains to enable all paths from higher-frequency domains to lower-frequency domains and blocking paths from lower-frequency domains to higher-frequency domains to test for a propagation time corresponding to the period of higher frequency clocks and verifying the hold time between all clock domains.

17. A method as defined in claim 16, further including, aligning the launch edge of the clock of all of said more than two clock domains and blocking paths from higher-frequency domains to lower-frequency domains to enable all paths from lower-frequency to higher-frequency domains to be tested for a propagation time corresponding to the period of the destination memory element.

18. A method as defined in claim 17, further including, aligning launch edges of some of said two or more clock domains and aligning capture edges of remaining clock domains.

19. A clocking method for at-speed scan testing for delay defects in cross-domain paths of interacting synchronous clock domains in scan circuits, each said path originating at a source memory element in one of said domains and terminating at a destination memory element in another of said domains and each said memory element forming part of a scan chain in said circuit, said method comprising, while performing a scan test:

testing paths from higher-frequency domains to lower-frequency domains for a propagation time corresponding to the period of the clock which controls source memory elements in said higher-frequency domains by aligning the capture edge of the clock of all said synchronous clock domains, clocking said memory elements at respective domain clock rates to launch signal transitions from said source memory elements therein, capturing circuit responses in destination memory elements in interacting lower-frequency domains while disabling capturing, in said higher-frequency domains, of circuit responses to signal transitions launched from said interacting lower-frequency domains; and

testing paths from lower-frequency domains to higher-frequency domains for a propagation time corresponding to the period of the clock which controls destination memory elements in higher-frequency domains by aligning the launch edge of the clock of all said synchronous clock domains, clocking said memory elements at respective domain clock rates to launch signal transitions from said source memory elements therein; capturing circuit responses in destination memory elements in interacting higher-frequency domains while disabling capturing, in said interacting lower-frequency domains, of circuit responses to signal transitions launched from said higher-frequency domains and

determining that a delay defect exists on a cross-domain path when a circuit response captured in its associated destination memory element is different from an expected response.

20. A method as defined in claim 19, said selectively disabling capturing including suppressing the capture operation of any destination memory elements which could cause an increase of the sequential depth of the circuit.

21. A method as defined in claim 19, further including, testing paths in which destination memory elements that were not selected to capture a circuit response by aligning launch edges of the clock of some of said clock domains and aligning capture edges of remaining clock domains prior to launching a signal transition from source memory elements and capturing circuit responses in said destination memory elements.

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