ScanBist
A Multi-frequency Scan-Based BIST Method

Benoit Nadeau-Dostie, Dwayne Burek, Abu S. M. Hassan

Bell-Northern Research Ltd.
P.O. Box 3511 Station C
Ottawa, Ontario, Canada K1Y 4H7

Abstract

This paper presents a BIST technique that allows the synchronization of multiple scan chains clocked at different frequencies. The technique is used to improve performance testing of scannable circuits. A few new design rules and small modifications to the existing ATPG were necessary to implement the technique.

Introduction

Built-in Self-test (BIST) is gaining popularity as a means to address test issues at the different packaging levels of digital systems. One of the benefits of BIST is the fact that no patterns need to be stored in the test equipment, which is simply required to provide a clock and a few control signals. This is especially important when high-performance systems are being tested. BIST also makes the chip/board/system more independant of the specific test resources available at each manufacturing stage. BIST is also a convenient way of applying more test patterns to compensate for the weaknesses of the stuck-at fault model [Pan90].

Specialized self-test circuits for embedded blocks (memories, PLAs, etc...) have reached a good level of maturity and adequate quality-area-performance trade-offs can usually be made based on the existing methods. However, there is much room for innovation in the field of BIST for unstructured or random logic that needs to be tested for performance given the various design styles.

It is frequent, in telecommunications applications, to design circuits requiring to operate of different frequencies derived from one (or more) reference frequency. For example, communication protocols can be embedded in a hierarchical fashion in a single frame of data and several finite-state machines, working at appropriate sub-frequencies, can be used to extract embedded protocols by simple decimation of the input sequence. Using sub-frequencies derived from a master clock instead of the master clock itself can save power, reduce electromagnetic interference and reduce silicon area.

Scan techniques have been traditionally used to generate very high quality test for faults detectable at low speed. The speed of application of the scan patterns is typically limited to the lowest of the inverse of the longest propagation path delay found on the chip or the frequency of the test clock often not optimized for high speed operation. Delay faults are not adequately tested in such an environment.

In this paper we describe a BIST technique for scan-based designs, called ScanBist, that removes some of the barriers for performance testing in a scan environment. The first section provides an overview of the technique. The BIST hardware, the clocks synchronization, the fault coverage considerations and the software support associated with this technique are addressed in separate sections. Conclusions and results are also presented.

Overview of ScanBist

ScanBist is a BIST technique for scan-based designs that allows synchronization of multiple chains running at different frequencies. The frequencies can be generated by division of a reference (system) clock or driven from primary inputs or both. The technique is a significant improvement over the well-known STUMPS method [Bar82] developed by IBM. The synchronization of the various scan chains is such that the performance of the circuit can be tested in an environment that is as close as possible to the reality. An exhaustive stuck-at and transition fault coverage analysis can be performed using a fault simulator for combinational circuits.

INTERNATIONAL TEST CONFERENCE 1992
0-8186-3167-8/92 $3.00 © 1992 IEEE

Authorized licensed use limited to: Siemens AG GBS B&S SOL GMS. Downloaded on September 13,2024 at 14:02:54 UTC from IEEE Xplore. Restrictions apply.