US011789487B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 11,789,487 B2**
(45) **Date of Patent: Oct. 17, 2023**

(54) **ASYNCHRONOUS INTERFACE FOR TRANSPORTING TEST-RELATED DATA VIA SERIAL CHANNELS**

(71) Applicant: **Siemens Industry Software Inc.**, Plando, TX (US)

(72) Inventors: **Benoit Nadeau-Dostie**, Gatineau (CA); **Jean-Francois Cote**, Davie, FL (US)

(73) Assignee: **Siemens Industry Software Inc.**, Plano, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 67 days.

(21) Appl. No.: **17/498,085**

(22) Filed: **Oct. 11, 2021**

(65) **Prior Publication Data**

US 2023/0110161 A1 Apr. 13, 2023

(51) **Int. Cl.**
G06F 1/12 (2006.01)
G06F 1/06 (2006.01)

(52) **U.S. Cl.**
CPC . ***G06F 1/12*** (2013.01); ***G06F 1/06*** (2013.01)

(58) **Field of Classification Search**
CPC G06F 1/10; G06F 1/12
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,900,753	A	5/1999	Cote et al.	
7,761,755	B1 *	7/2010	Payakapan	G01R 31/31922 714/724
8,862,954	B1 *	10/2014	Wang	G01R 31/3177 714/731
11,409,931	B1 *	8/2022	Kaur	G06F 30/333
2002/0147951	A1 *	10/2002	Nadeau-Dostie	G01R 31/318552 714/731
2011/0260767	A1 *	10/2011	Devta-Prasanna	G01R 31/318552 327/285
2013/0117618	A1 *	5/2013	Kukreja	G01R 31/318552 714/E11.148
2014/0035645	A1 *	2/2014	Narayanan	G11C 29/32 327/212
2020/0124665	A1 *	4/2020	de Bakker	G01R 31/31726

* cited by examiner

Primary Examiner — Phil K Nguyen

(57) **ABSTRACT**

A circuit comprises: a first clock gating device clocked by a first clock signal and configured to generate first clock pulses when a shift enable signal is active, a first transition detecting device clocked by a second clock signal and configured to generate shift gating pulses when detecting active transitions of the first clock pulses, a second clock gating device clocked by the second clock signal and configured to generate shift clock pulses based on the shift gating pulses to clock second scan elements for a shift operation with first scan elements clocked by the first clock signal, and a first retiming device triggered by active pulse edges of the first clock signal and configurable to hold a value for the shift operation. The circuit may further comprise a delay generating device configured to generate delayed shift gating pulses for generating the shift clock pulses.

16 Claims, 14 Drawing Sheets