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**Nadeau-Dostie et al.**

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(54) **METHODS FOR AT-SPEED TESTING OF MEMORY INTERFACE**

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USPC ..... **714/726**; 714/733; 714/742

(58) **Field of Classification Search**
USPC ..... 714/726, 733, 742
See application file for complete search history.

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(57) **ABSTRACT**

Methods for at-speed testing of a memory interface associated with an embedded memory comprise two write operations in succession, two read operations in succession, and a capture operation using scan cells. The write and read operations are performed during a single clock burst, two separate clock bursts in a clock signal, or two separate clock bursts in separate clock signals.

**31 Claims, 17 Drawing Sheets**