ScanBist:
A Multifrequency Scan-Based BIST Method

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The authors present ScanBist, a low-overhead, scan-based built-in self-test method along with its performance in several designs. A novel clock synchronization scheme allows at-speed testing of circuits.

BUILT-IN SELF-TEST is gaining popularity as a means to address test issues at the different packaging levels of digital systems. BIST does not require that patterns be stored in the test equipment, which simply provides a clock and a few control signals. This feature becomes especially important when testing high-performance systems. BIST makes the chip, board, and system more independent of the specific test resources available at each manufacturing stage. It also provides a convenient method of applying more test patterns to compensate for the weaknesses of the stuck-at fault model.[1]

Specialized self-test circuits for embedded blocks (such as memories and programmable logic arrays) have reached a good level of maturity, and existing methods provide the basis for making adequate quality-area-performance trade-offs. However, BIST has a great deal of room for innovation, particularly in unstructured or random logic that requires testing for performance when a variety of design styles apply. At the same time, the new techniques that provide this capability should not significantly increase either the implementation cost or the design interval of the system.

In telecommunications applications, designers often create circuits that operate at different frequencies derived from at least one reference frequency. For example, designers embed communication protocols in a hierarchical fashion in a single frame of data. Several finite-state machines, working at appropriate subfrequencies, then extract the embedded protocols by simple decimation of the input sequence. Using subfrequencies derived from a master clock instead of the master clock itself saves power, reduces electromagnetic interference, and reduces silicon area.

Traditionally used to generate very high quality tests for faults detectable at low speed, Scan has also demonstrated efficiency in testing for delay faults by accurately controlling all clock phases from a tester.[2] However, BIST does not lend itself to this approach. LeBlanc developed a scan-based BIST solution, LSSD on-chip self-test (LOCST), that is applicable at all levels of system integration.[3] However, he used a single test frequency and limited the speed of application of the scan patterns generated by the BIST circuitry to the lowest frequency used in the system. Therefore, part of the logic operates at an untested speed in systems with more than one frequency.

Overview of ScanBist

Figure 1 (next page) shows a block diagram of the ScanBist implementation. The IEEE Standard 1149.1 test access port (TAP)[4] connects to a macro circuit called the ScanBist core. In turn,

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