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(54) **METHOD FOR TESTABILITY ANALYSIS AND TEST POINT INSERTION AT THE RT-LEVEL OF A HARDWARE DEVELOPMENT LANGUAGE (HDL) SPECIFICATION**

(75) Inventors: **Samir Boubezari**, Mountain View, CA (US); **Eduard Cerny**; **Bozena Kaminska**, both of Montreal (CA); **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

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*Primary Examiner*—Matthew Smith

*Assistant Examiner*—A. M. Thompson

(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A method is provided for producing a synthesizable RT-Level specification, having a testability enhancement from a starting RT-Level specification representative of a circuit to be designed, for input to a synthesis tool to generate a gate-level circuit. The method includes the steps of performing a testability analysis on a Directed Acyclic Graph by computing and propagating Testability Measures forward and backward through VHDL statements, identifying the bits of each signal and/or variable, and adding test point statements into the specification at the RT-Level to improve testability of the circuit to be designed. The computation of Controllability and Observability method is purely functional, and does not subsume the knowledge of a gate-level implementation of the circuit being analyzed.

**36 Claims, 7 Drawing Sheets**

