US006829730B2

(12) **United States Patent**
Nadeau-Dostie et al.

(10) **Patent No.: US 6,829,730 B2**
(45) **Date of Patent: Dec. 7, 2004**

(54) **METHOD OF DESIGNING CIRCUIT HAVING MULTIPLE TEST ACCESS PORTS, CIRCUIT PRODUCED THEREBY AND METHOD OF USING SAME**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 788 days.

(21) Appl. No.: **09/843,307**

(22) Filed: **Apr. 27, 2001**

(65) **Prior Publication Data**

US 2002/0184562 A1 Dec. 5, 2002

(51) **Int. Cl.**[7] **G06F 11/27**
(52) **U.S. Cl.** **714/30**; 714/31; 714/724; 714/729; 714/734; 716/1
(58) **Field of Search** 714/25, 30, 31, 714/37, 38, 724, 727, 729, 733, 734; 703/23, 24, 25, 26, 27, 28; 716/1, 4

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,884,023	A		3/1999	Swoboda et al.
6,073,254	A		6/2000	Whetsel
6,115,763	A	*	9/2000	Douskey et al. 714/727
6,324,662	B1	*	11/2001	Haroun et al. 714/724
6,385,749	B1	*	5/2002	Adusumilli et al. 714/30
6,408,413	B1	*	6/2002	Whetsel 714/727
6,425,100	B1	*	7/2002	Bhattacharya 712/38

OTHER PUBLICATIONS

Alves, G.R. et al., Using the BS Register for Capturing and Storing n–bit Sequences in Real Time, IEEE Proceeding of the European Test Workshop. May 1999. pp. 130–135.
Hamilton, C. et al., Methods for Boundary Scan Access of Built–In Self–Test for Field Programmable Gate Arrays. IEEE Proceedings of Southeastcon. Mar. 1999. pp. 69–78.
Steven F. Oakland, "Considerations for Implementing IEEE 1149.1 On System–on–a–Chip Integrated Circuits", International Test Conference 2000 Proceedings, Oct. 3–5, 2000, p. 628–637.
Lee Whetsel, "An IEEE Based Test Access Architecture for ICs With Embedded Cores", International Test Conference 1997 Proceedings, Nov. 1–6, 1997.

* cited by examiner

Primary Examiner—Robert Beausoliel
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

In a circuit with multiple Test Access Port (TAP) interfaces, the TAPs are arranged into groups, with secondary TAPs in one or more groups and a master TAP in another group, the master TAP having an instruction register with bits for storing a group selection code; a Test Data Output (TDO) circuit responsive to the group selection code connects the group TDO of one of the groups to the circuit TDO; and, for each secondary TAP group, a group Test Data Input (TDI) circuit responsive to a shift state signal for selectively connecting the group TDI to the circuit TDI or to the output of a padding register having its input connected to the circuit TDI, and its output connected to an input of the group TDI circuit; and a group TMS circuit responsive to a predetermined TAP selection code associated with the group for producing a group TMS signal for each TAP in the group.

51 Claims, 6 Drawing Sheets