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Nadeau-Dostie et al.

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(54) **METHOD FOR SCAN TESTING OF DIGITAL CIRCUIT, DIGITAL CIRCUIT FOR USE THEREWITH AND PROGRAM PRODUCT FOR INCORPORATING TEST METHODOLOGY INTO CIRCUIT DESCRIPTION**

(75) Inventors: **Benoit Nadeau-Dostie**, Aylmer (CA); **Jean-François Côté**, Chelsea (CA)

(73) Assignee: **LogicVision, Inc.**, San Jose, CA (US)

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(58) **Field of Search** 326/16; 714/726–731; 713/500

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Primary Examiner—Guy J. Lamarre
(74) *Attorney, Agent, or Firm*—Eugene E. Proulx

(57) **ABSTRACT**

A method for at-speed scan testing of circuits having scannable memory elements which source multi-cycle paths having propagation delays that are longer than the period of a system clock used during normal operation comprises loading a test stimulus into the scannable memory elements; performing a capture operation, including configuring in capture mode throughout the capture operation, non-source memory elements and multi-cycle path source memory elements which have a predetermined maximum capture clock rate which is the same as or higher than the clock rate of the capture clock; and configuring in a hold mode during all but the last cycle of the capture operation and in capture mode for the last cycle, source memory elements which have a predetermined maximum capture clock rate which is lower than the clock rate of the capture clock; applying at least two clock cycles of the capture clock; and unloading test response data captured by said scannable memory elements.

65 Claims, 7 Drawing Sheets