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(54) **CLOCK CONTROLLER FOR AT-SPEED TESTING OF SCAN CIRCUITS**

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(57) **ABSTRACT**

A test clock controller for generating a test clock signal for scan chains in integrated circuits having one or more clock domains, comprises a shift clock controller for generating a shift clock signal for use in loading test patterns into scan chains in the clock domains and for unloading a test response patterns from the scan chains and for generating a burst phase signal after loading a test pattern; and a burst clock controller associated with each of one or more clock domains and responsive to a burst phase signal for generating a burst of clock pulses derived from a respective reference clocks and including a first group of burst clock pulses having a selected reduced frequency relative to the reference clock and a second group of burst clock pulses having a frequency corresponding to that of the reference clock.