A new hardware fault insertion scheme for system diagnostics verification

Benoit Nadeau-Dostie[‡], Harry Hulvershorn[†], Saman M. I. Adham[†]
[†]Northern Telecom, P.O. Box 3511, Station C, Ottawa, Ontario, Canada K1Y 4H7
[‡]LV Software (Canada) Inc., 1525 Carling Avenue, Suite 404, Ottawa, Ontario, Canada K1Z 8R9

Abstract

A new fault insertion method to help debug diagnostic software of telecommunications systems is described. The method makes use of Boundary Scan to inject multiple and un-correlated faults in a telecom system carrying traffic. Both hardware and software implementation aspects are discussed. The new method allows the use of structural test as part of diagnostics software to locate faults.

I. Introduction

Fault insertion (also known as fault injection) has been used for many years to evaluate the effectiveness of diagnostic software. Even though it is possible to perform this evaluation using simulation, it is usually difficult because of the absence of proper tools and models. A common way of performing this verification is still to inject faults around components of a board using switches or other similar hardware. Usually only a few carefully chosen faults could be inserted using this primitive mechanism. For each revision of a board, a few boards are selected and modified to add the fault injection means. This method is becoming less practical because it is becoming necessary to inject more faults in more complex systems and, at the same time, the physical access to components and tracks of the board is reduced. The process has several drawbacks. It is expensive since the modifications on the selected boards are done after the board is designed. Faults are injected into limited number of tracks on the board which in turn results in low fault coverage.

This is why alternate methods are needed in modern telecommunications systems. Recently, several authors demonstrated how Boundary Scan (Bscan) [4] could be used to insert faults in complex systems containing Application Specific Integrated Circuits (ASICs) [1-3]. We first review those schemes. We then describe a significant improvement over the method introduced by Wilcox et al [3]. This improvement is essential to the verification of diagnostic software making use of structural tests (including all the ones involving Bscan) to locate faults. The new scheme retains all the other benefits of Wilcox's. Multiple un-correlated faults can be injected at the same time while the system is running. No extra delay is inserted in the Bscan cells to inject the faults. Finally, existing Boundary scan cell layouts can be reused to implement a complete fault insertion cell. Those benefits are traded off against area.

A few applications of this new fault insertion method are demonstrated. Several aspects of the system software required to generate and apply faults is also described. Limitations of the scheme are discussed before we conclude.

II. Review of previous schemes

Sedmak [2] suggests three ways to inject faults at the output of ASICs. For example, all outputs of a given ASIC can be faulted using standard Bscan instructions (HIGHZ, CLAMP or EXTEST). Another way is to load

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