

US006760874B2

(12) United States Patent Côté et al.

(10) Patent No.: US 6,760,874 B2 (45) Date of Patent: US 6,004

(54)	TEST ACCESS CIRCUIT AND METHOD OF
` ′	ACCESSING EMBEDDED TEST
	CONTROLLERS IN INTEGRATED CIRCUIT
	MODULES

(75) Inventors: **Jean-François Côté**, Chelsea (CA); **Benoit Nadeau-Dostie**, Aylmer (CA)

(73) Assignee: LogicVision, Inc., San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this

patent is extended or adjusted under 35 U.S.C. 154(b) by 84 days.

(21) Appl. No.: 10/139,294

(22) Filed: May 7, 2002

(65) Prior Publication Data

US 2003/0212524 A1 Nov. 13, 2003

(51)	Int. Cl. ⁷	•••••	G01R	31/28
------	-----------------------	-------	------	-------

(56) References Cited

U.S. PATENT DOCUMENTS

4,348,743 A	*	9/1982	Dozier	713/502
4,896,258 A	*	1/1990	Yamaguchi et al	712/236
5.928.374 A	*	7/1999	Shimizu et al	714/724

6,006,347 A	*	12/1999	Churchill et al 714/724	
6,191,603 B1		2/2001	Muradali et al.	
2002/0040458 A1	*	4/2002	Dervisoglu et al 714/729	

FOREIGN PATENT DOCUMENTS

WO WO 01/53844 A1 7/2001

OTHER PUBLICATIONS

Dervisoglu, "A Unified DFT Architecture for Use with IEEE 1149.1 and VSIA/IEEE P15000 Compliant Test Access Controllers", Design Automation Conference, Jun. 18–22, 2001.

* cited by examiner

Primary Examiner—Albert Decady
Assistant Examiner—Dipakkumar Gandhi
(74) Attorney, Agent, or Firm—Eugene E. Proulx

(57) ABSTRACT

A test access circuit (TAC) for use in controlling test resources including child test access circuits (TACs) and/or test controllers, in an integrated circuit, comprises an enable input for enabling or disabling access to the test resources, a test port associated with each test resource, each test port including a test port enable output for connection to an enable input of an associated test resource; and an input for receiving a serial output of the associated test resource; and a selector for selecting a test resource for communication therewith.

53 Claims, 5 Drawing Sheets

