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(54) **METHOD FOR AT-SPEED TESTING OF MEMORY INTERFACE USING SCAN**

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(57) **ABSTRACT**

A method and a circuit of testing of a memory interface associated with an embedded memory in a semiconductor circuit involves writing to two memory locations in succession; reading the two memory locations in succession in the same order in which the two memory locations were written; capturing output data from the memory interface; and analyzing captured output data to determine whether said captured output data corresponds to expected data.