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[54] **MULTIPLE CLOCK RATE TEST APPARATUS FOR TESTING DIGITAL SYSTEMS**

[75] Inventors: **Benoit Nadeau-Dostie,** Aylmer; **Abu S. M. Hassan,** Nepean; **Dwayne M. Burek,** Nepean; **Stephen K. Sunter,** Nepean, all of Canada

[73] Assignee: **Northern Telecom Limited,** Montreal, Canada

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[58] **Field of Search** 371/22.3, 22.4, 22.5, 371/22.6, 27

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Primary Examiner—Robert W. Beausoliel, Jr.
Assistant Examiner—Joseph E. Palys
Attorney, Agent, or Firm—C. W. Junkin

[57] **ABSTRACT**

In methods and apparatus for testing a digital system, scannable memory elements of the digital system are configured in a scan mode in which the memory elements are connected to define a plurality of scan chains. A test stimulus pattern is clocked into each of the scan chains at a respective clock rate, at least two of the clock rates being different from one another. The memory elements of each scan chain are then configured in a normal operation mode in which the memory elements are interconnected by the combinational network for at least one clock cycle at a highest of the respective clock rates. The memory elements are then reconfigured in the scan mode, and a test response pattern is clocked out of each of the scan chains at its respective clock rate. The methods and apparatus are particularly useful for testing digital systems such as digital integrated circuits in which different memory elements are clocked at different rates during normal operation.

19 Claims, 7 Drawing Sheets