US 20230178172A1

(19) **United States**

(12) **Patent Application Publication**

Yun et al.

(10) **Pub. No.: US 2023/0178172 A1**

(43) **Pub. Date: Jun. 8, 2023**

(54) **REFERENCE BITS TEST AND REPAIR USING MEMORY BUILT-IN SELF-TEST**

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(21) Appl. No.: **17/906,303**

(22) PCT Filed: **Mar. 18, 2021**

(86) PCT No.: **PCT/US2021/022871**

§ 371 (c)(1),
(2) Date: **Sep. 14, 2022**

Related U.S. Application Data

(60) Provisional application No. 63/000,517, filed on Mar. 27, 2020.

Publication Classification

(51) **Int. Cl.**
G11C 29/54 (2006.01)
G11C 29/56 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 29/54*** (2013.01); ***G11C 29/56004*** (2013.01)

(57) **ABSTRACT**

A memory-testing circuit configured to perform a test of reference bits in a memory. In a read operation, outputs of data bit columns are compared with one or more reference bit columns. The memory-testing circuit comprises: a test controller and association adjustment circuitry configurable by the test controller to associate another one or more reference bit columns or one or more data bit columns with the data bit columns in the read operation. The test controller can determine whether the original one or more reference bit columns have a defect based on results from the two different association.