A 200 MHz 0.8 μm BiCMOS MODULAR MEMORY FAMILY OF DRAM AND MULTIPORT SRAM

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Abstract: A family of modular memories has been designed in a 0.8 μm BiCMOS process based on a synchronous self-timed architecture. Nominal access and cycle times are 5 ns for 64KBit blocks of 1, 2 and 4 port SRAM as well as a DRAM using a four transistor (4T) core cell.

INTRODUCTION

The goal in developing the modular RAM family for the Northern Telecom Electronics Ltd. 0.8 μm BiCMOS Telecom process (BATMOS) [1], summarized in Table 1, was to design circuitry which could be adapted with few changes to implement SRAM, multiport SRAM and 4T DRAM over the modularity ranges outlined in Table 2. The result is a four member family with virtually identical schematics, and layout optimized to achieve high density and speed. This paper will discuss the modular self-timed specification and design, its extension to multiport and dynamic RAM cells, and the measured performance.

Table 1: BATMOS Process Summary

Vertical NPN:	Emitter size (min)	0.8 × 4.0 μm
	F_t	11 GHz
NMOS and PMOS LDD:	Lmin	0.8 μm
	VTP / VTN	-0.85 / 0.80 V
	tox	17.5 nm
Interconnect:	Metal 1 line 0.8 μm, pitch 2.0 μm	
	Metal 2 line 0.8 μm, pitch 2.0 μm	
	Metal 3 line 1.0 μm, pitch 2.4 μm	
	Stacked via and contact structures	
	Local Interconnect	

Table 2: RAM Family Modularity Range

Parameter	Min	Step	Max
Words	8	1	8K
I/O Bits per Word	1	1	64
Total Bits	8	–	64K
Rows	4	2	256
Columns	2	2	256
Columns per I/O Bit	2	2	32
Row Address Bits	2	1	8
Column Address Bits	1	1	5

SELF-TIMED RAM SPECIFICATION

The specifications for the modular memory family are geared directly for ease of use by the system designer and integration within a synchronous design methodology. A read cycle timing diagram for a generic port is shown in Figure 1.

A self-timed memory architecture is used with a registered CMOS interface on all input pins. This provides the best possible integration of embedded memory into large synchronous ICs since the interface timing is similar to an edge triggered flip-flop. Worst case setup and hold times are 3 ns and 0 ns respectively. This natural interface to a synchronous system also allows the creation of simple bus cycle models for the memory which map easily into high level synthesis tools.

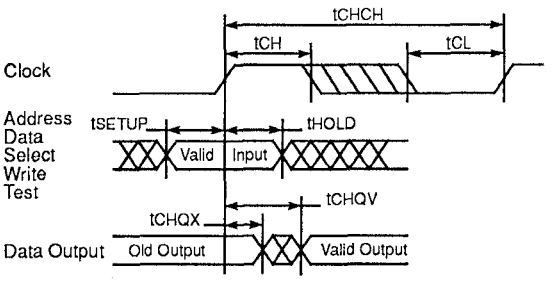

Figure 1: Read Cycle Timing Specification

The buffered outputs of all registers are available to the system designer and can be used, for example, to form counters and scan registers. They also constitute the majority of circuitry required for a Built in Self Test (BIST) circuit [2]. Characterizing the memory block and the input registers with an analog simulator as a single unit and modeling it as such at the logic level, improves the accuracy of the analysis of system timing paths through the RAM. The system designer need not rely on a logic simulator and pre-layout wire load estimates to margin the critical register-to-memory input timing.

The self-timed shut down yields a power dissipation characteristic that is inversely proportional to clock frequency and independent of duty cycle making it well suited to both high and low speed applications. In addition, the length of the active portion of the cycle decreases with faster process conditions. As a result, the power dissipation is less sensitive to process and temperature than other RAMs which depend on level sensitive clock or enable inputs that must be derived from a fixed duty cycle system clock. A synchronous memory select pin is also included to allow system level block subdecoding. Since unselected blocks draw no current, this is useful for trading off power and area at the chip level when constructing large memory functions.

Two test modes are included to provide compatibility with the SCAN and memory BIST test methodologies used at BNR. The first test mode reconfigures the memory data input / output path to a scan compatible mode in which the data inputs bypass the memory core and are transferred directly to the data output pins. This ensures controllability of the memory outputs during scan testing of the logic around the RAM. The

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