



US011929136B2

(12) **United States Patent**
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(10) **Patent No.:** **US 11,929,136 B2**
(45) **Date of Patent:** **Mar. 12, 2024**

(54) **REFERENCE BITS TEST AND REPAIR
USING MEMORY BUILT-IN SELF-TEST**

(52) **U.S. Cl.**
CPC **G11C 29/54** (2013.01); **G11C 29/56004**
(2013.01)

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(58) **Field of Classification Search**
None
See application file for complete search history.

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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

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(21) Appl. No.: **17/906,303**

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(22) PCT Filed: **Mar. 18, 2021**

PCT International Search Report and Written Opinion of Interna-
tional Searching Authority dated Jul. 6, 2021 corresponding to PCT
International Application No. PCT/US2021/022871 filed Mar. 18,
2021.

(86) PCT No.: **PCT/US2021/022871**
§ 371 (c)(1),
(2) Date: **Sep. 14, 2022**

(Continued)

(87) PCT Pub. No.: **WO2021/194827**
PCT Pub. Date: **Sep. 30, 2021**

Primary Examiner — Guerrier Merant

(65) **Prior Publication Data**
US 2023/0178172 A1 Jun. 8, 2023

(57) **ABSTRACT**

A memory-testing circuit configured to perform a test of
reference bits in a memory. In a read operation, outputs of
data bit columns are compared with one or more reference
bit columns. The memory-testing circuit comprises: a test
controller and association adjustment circuitry configurable
by the test controller to associate another one or more
reference bit columns or one or more data bit columns with
the data bit columns in the read operation. The test controller
can determine whether the original one or more reference bit
columns have a defect based on results from the two
different association.

Related U.S. Application Data

(60) Provisional application No. 63/000,517, filed on Mar.
27, 2020.

(51) **Int. Cl.**
G11C 29/54 (2006.01)
G11C 29/56 (2006.01)

10 Claims, 10 Drawing Sheets

