Logic Gates and Their Differences

1. Functional Differences

Gate	Symbol Description	Logical Expression	Output Behavior
AND	D-shaped gate	Q = A·B	High (1) only when both inputs are 1
NAND	AND with output bubble	Q = ¬(A·B)	Low (0) only when both inputs are 1, otherwise high
OR	Curved input gate	Q = A + B	High (1) when at least one input is 1
NOR	OR with output bubble	Q = ¬(A + B)	High (1) only when both inputs are 0
XOR	OR with extra curved input line	Q = A ⊕ B	High (1) only when inputs are different
XNOR	XOR with output bubble	Q = ¬(A ⊕ B)	High (1) when inputs are the same
NOT	Triangle with output bubble	Q = ¬A	Inverts the input

2. Truth Table Overview

A	B	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

3. Circuit-Level Differences

- AND / NAND: Often implemented using series transistors (current flows only when both inputs are high).
- OR / NOR: Use parallel transistors (current flows if either input is high).
- XOR / XNOR: Combine AND, OR, and NOT gates internally; more complex transistor networks.
- NOT: Simplest gate, just one transistor stage.