TCES 330, Spring 2013
Final Exam

General Comments:

Follow the directions very carefully. You will be graded partly on how well you can follow these directions. This exam requires you to modify your Lab B processor design as described below. When you are finished notify me and we will upload your exam to Moodle.

Turn in this paper copy of the exam, too. Be sure your name is on this page.

Do NOT connect to the Internet unless told to do so. Do NOT use your cell phone in any fashion during this exam except for emergency purposes; keep your cell phone out of view. Do not consult any other individual except for an instructor. This is an **open book** exam. You may use your text books, your notes, my slides, the lab assignments, Altera tutorials, etc.

When you develop your code, consider the following:

- **Copy** your Lab B processor to a new folder called "Final." Be sure to save the original in case you need to refer to it again.
- None of the pin assignments will change for this exercise.
- Your initial Data Memory file will not change.
- Pay close attention to the warnings you get when you compile.
- Use comments appropriately. Make sure your name appears in module you need to write for this exam (there's only one).

There are no 'trick' questions. This exam is a straight-forward test of your abilities to write Verilog HDL programs and to verify them.

Seventh Instruction:

Your job is to add a seventh instruction called COPY. This instruction copies the data in some register file location to another register file location. That is, this is a register-to-register copy. The instruction looks like this:

COPY RFs, RFd = 0111 rs_3 rs_2 rs_1 rs_0 0000 rd_3 rd_2 rd_1 rd_0

Where RFs (and rs) stands for the source register
RFd (and rd) stands for the destination register
The Copy instruction always starts with 4'b0111 (4'h7)
The four bits of 0 in the middle are unused (don't care)

Example:

COPY RF3, RFB has the bit pattern 0111 0011 0000 1011 (16'h730B)

This would cause the contents of register 3 to be copied to register 4'hB (which is 4'd11).

Test Program

Test your new instruction with the following program. This should also be the program in your instruction memory when you turn in your final. All numbers shown are hexadecimal:

```
LOAD  D5,  RF2   // loads data in location 5 into register 2
COPY  RF2, RF8   // copies contents of register 2 to register 8
COPY  RF2, RFA   // copies contents of register 2 to register A
STORE RF8, D8    // stores contents of register 8 in data location 8
STORE RFA, DA    // stores contents of register A in data location A
Then figure out how to add 16'h00E8 to the contents of register A and store the
sum in data location B. You can use any instructions and any registers to do
this.
HALT
```

Question

What is Fmax (maximum clock speed) for your processor? Answer this question in the comments of your top-level Verilog module.

Comments:

- You do not have to change your initial data memory (from Lab B).
- You will need to load a new program (your test program) into Instruction Memory.
- Any time you change a *.mif file you need to delete the folders
  `\db` and
  `\incremental_db`
  and then recompile your project.
- After you run your program you should look at data memory using the In-System Memory Content Editor. You should find "01A6" in memory locations 5, 8, and A.