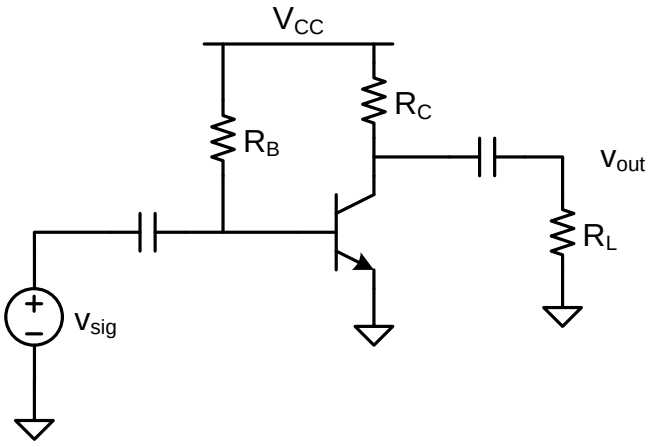
15 Active Loads

The common emitter amplifier in its simplest configuration is this.



It has open circuit voltage gain given by

$$\begin{aligned} A_v &= -g_m R_C \,||\, r_o \\ &\approx -g_m R_C \qquad (R_c << r_o) \\ &= -I_C R_C / V_t \end{aligned}$$

To increase the gain (in absolute value) we can increase I_C or R_C. But there is a limit to the gain that can be achieved since

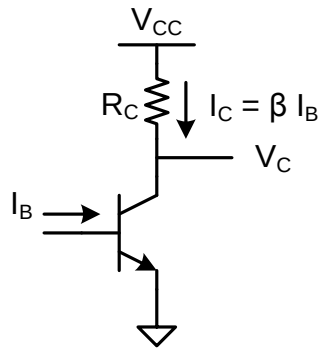
$$I_C R_C \le V_{CC} - 0.3\ V$$

is necessary to keep the transistor out of saturation. Increasing supply voltage appreciably, if at all, is not usually an option. And voltage swing considerations further limit the available gain.

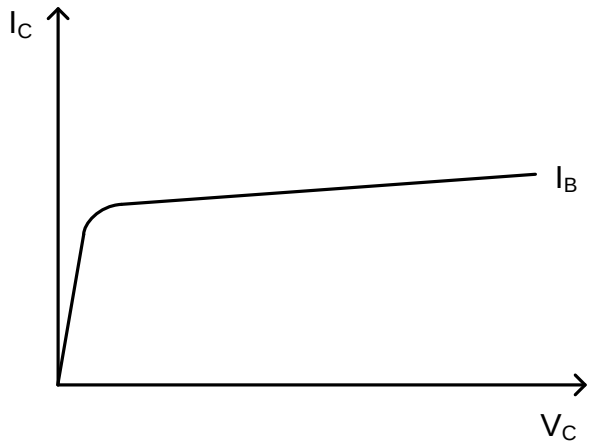
To achieve gains in excess of the limitation considered above, we can replace R_C by an active load. It has the effect of providing a large resistance to small signals, producing

high voltage gain, but much lower effective resistance to the DC bias current, preventing saturation. (By load, for now, we refer to the collector resistor, or other device at that location that replaces R_C, and not R_L.)

First we recall the idea of a load line. The collector current of the common emitter transistor and its load, R_C, determine the DC collector voltage.

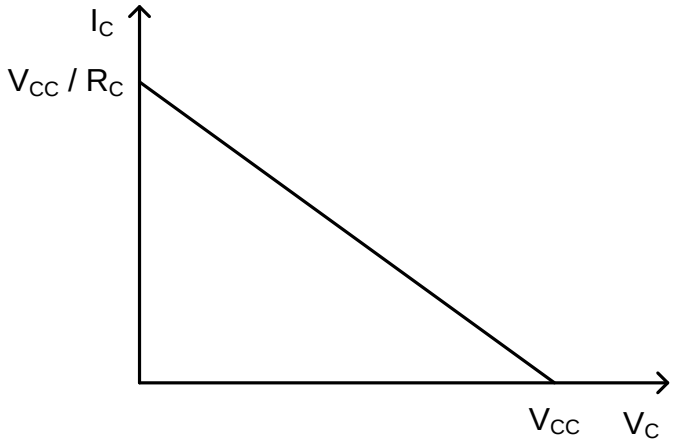


For the transistor, I_C and V_C are related by the transistor characteristic curve, plotted below for the particular base current, I_B.

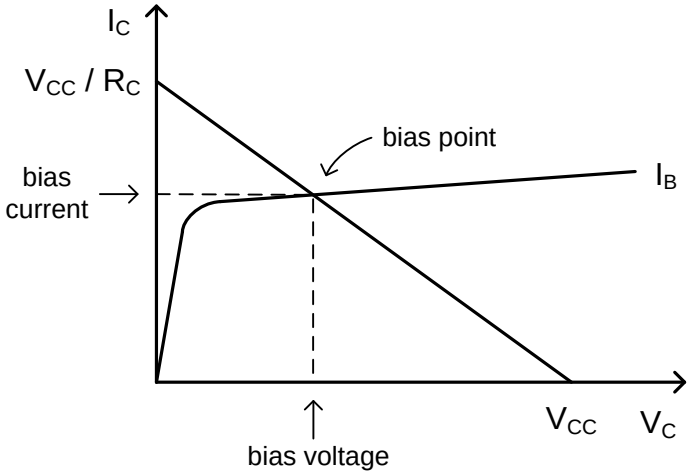


The familiar active mode region is the nearly horizontal part of the curve. Saturation occurs at the left near the vertical axis where the curve falls steeply to zero. The DC bias point will be somewhere along the curve depending on the value of V_{CC} and R_C.

For the collector resistor, the relationship between I_C and V_C is given by $V_C = V_{CC} - I_C R_C$ or $I_C = (V_{CC} – V_C) / R_C$. This can be plotted on the same I_C vs. V_C axes with intercepts at V_{CC} for $I_C = 0$ and V_{CC} / R_C for $V_C = 0$. The slope of the line is $1 / R_C$.

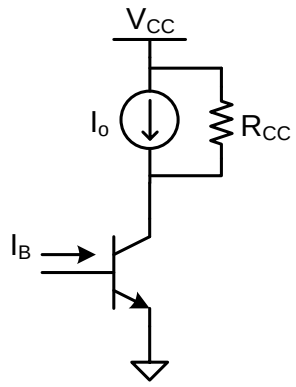


This is the same I_C and V_C of the transistor characteristic curve and the DC bias point must be somewhere on this line. So if we put these two curves on the same graph, the intersection will be the bias point, the only point that satisfies the I_C vs. V_C requirement for both the transistor and the collector resistor simultaneously.



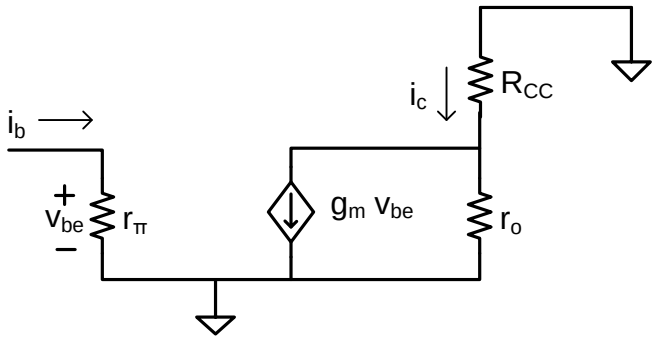
We call the resistor curve a load line on the transistor characteristic. Note that a different value of R_C changes the slope of the load line and its intercept on the vertical axis and, consequently, the bias point of the transistor.

Now we return to our replacement for R_C that will give us increased gain. That replacement will be a current source. Consider first a Norton equivalent circuit.



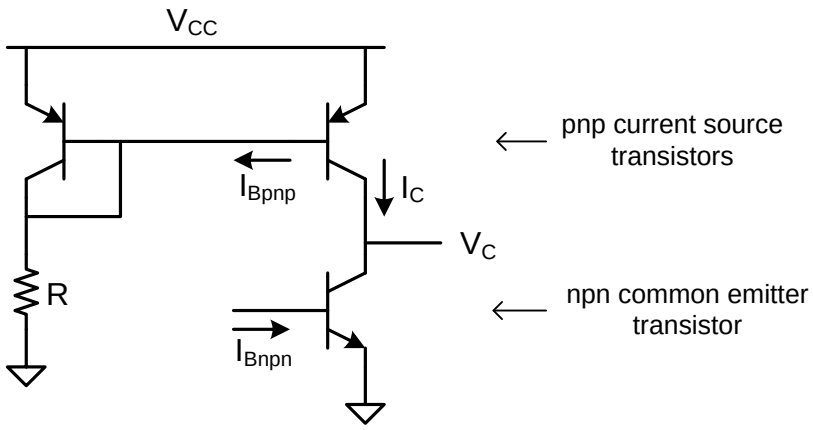
The current source must provide the current required by the transistor while allowing the transistor to remain in active mode. Recall that the transistor collector current will vary slightly as collector voltage changes (r_o effect). So the current source would be conveniently set to provide transistor collector current with a collector voltage perhaps at V_{CC} / 2 or so. Collector current would be a combination of I_o and current through R_{CC}, the output resistance of the current source.

Then for small signals, in particular a change in base current, i_b, the additional collector current, i_c, must be supplied by a change in collector voltage and some additional current flowing through R_{CC}. That additional current may flow in either direction depending on whether i_c is positive or negative, meaning that the total current through R_{CC} may increase or decrease. In the small signal circuit, R_{CC} goes to ground (rather than to V_{CC}) and the ideal current source is an open circuit. Small signal collector current flows to ground or from ground.



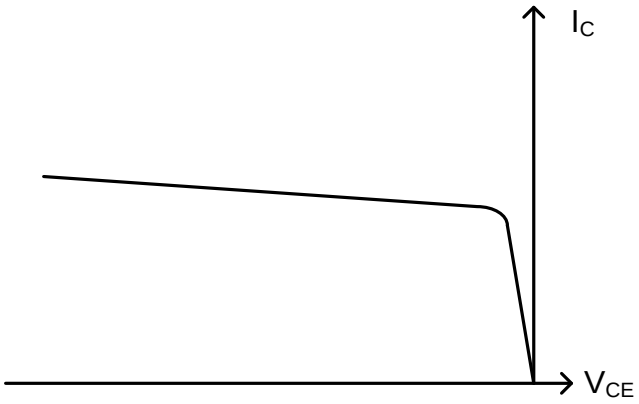
The DC bias collector current is supplied primarily by I_o. AC currents flow through R_{CC}. The collector resistance for small signals, R_{CC}, is not limited by the transistor or any circuit constraints, only by the quality of the current source (for an ideal current source, $R_{CC} = \infty$).

For our amplifier, we use a current mirror. But because we need a source of current and not a sink of current, we must use the pnp version rather than the npn version.

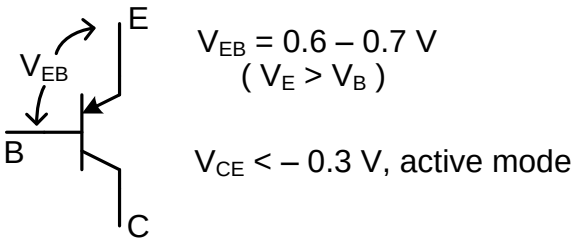


The characteristic curve, I_C vs. V_C, for the pnp transistor becomes the load line for the common emitter npn transistor from which we determine the bias point and the effective collector resistance, called a dynamic resistance in this case because it is not the usual fixed or static resistance of an ordinary resistor.

The pnp transistor has this characteristic curve.

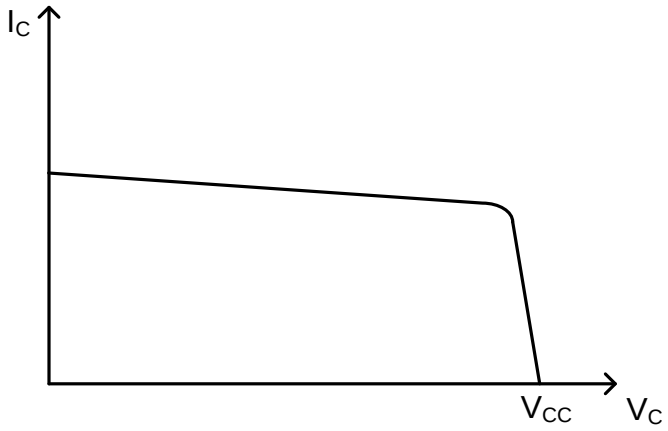


It is very similar to the npn curve, except that V_{CE} must be negative for active mode. We have also made the accommodation to take I_C as a positive current even though the convention is that I_C is negative for pnp transistors in active mode.



$V_E > V_B$ to forward bias the emitter-base junction. $V_C < V_B$ to reverse bias the collector-base junction.

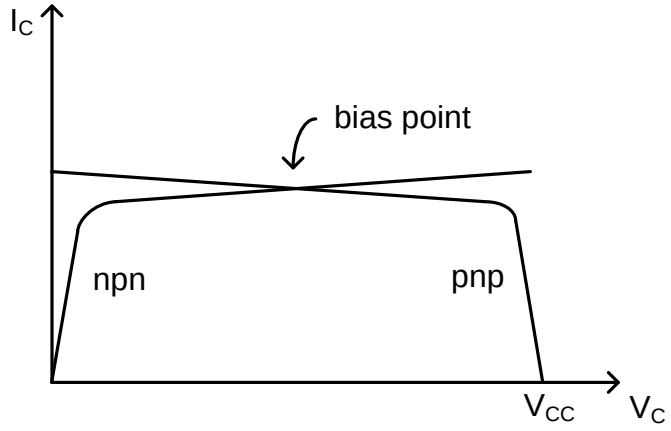
We can replot the pnp characteristic as I_C vs. V_C rather than vs. V_{CE} by noting that $V_{CE} = V_C - V_{CC}$ or $V_C = V_{CE} + V_{CC}$. So values on the V_C axis are just values on the V_{CE} axis moved to the right by V_{CC}. For example, $V_{CE} = 0$ becomes $V_C = 0 + V_{CC} = V_{CC}$. The characteristic cure on the I_C vs. V_C axes is then



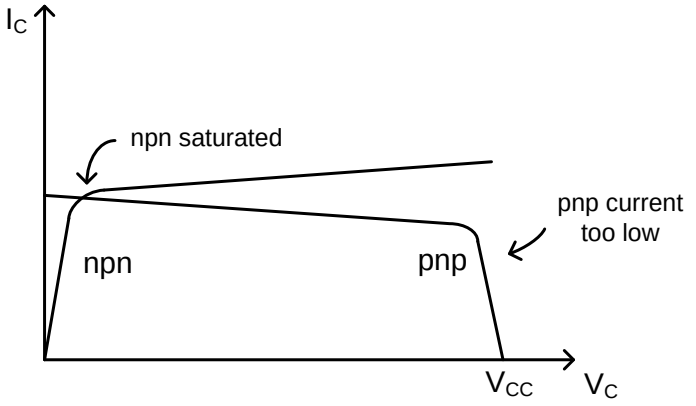
where the graph is shifted to the right by V_{CC}.

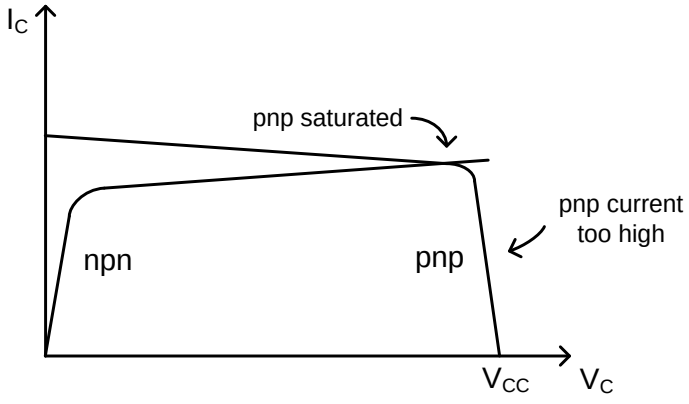
Now we have a common set of axes, I_C and V_C, that we can use to plot the characteristic curves for both the npn and pnp transistors. At the bias point, the collector currents and collector voltages of the two transistors must be the same. That

situation occurs at the intersection of the two characteristic curves.



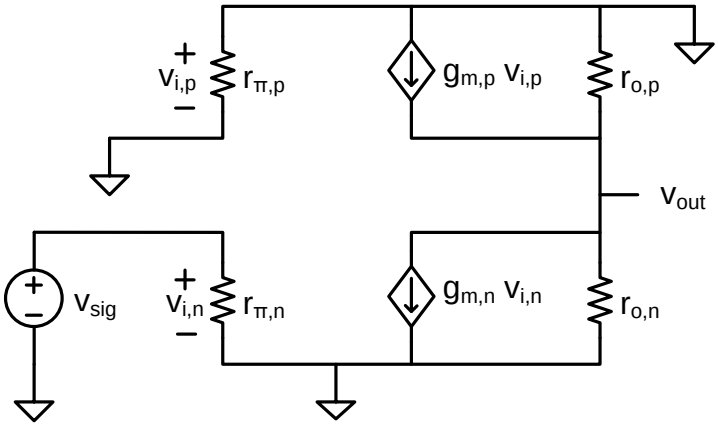
And because these characteristic curves move up and down as base current of either device changes, it should be clear that we must adjust the base current of the pnp current source transistor to provide very nearly the collector current demanded by the npn transistor. Any appreciable mismatch will move the intersection of the two curves to the right or left and saturate one transistor or the other.





Depending on the output resistance of the transistors, this matching can be quite demanding. For large r_o, the slope of the characteristic curves in the active region is very small (slope = $1/r_o$) and the bias point will be very sensitive to small changes in base and collector currents. We'll return to that problem later.

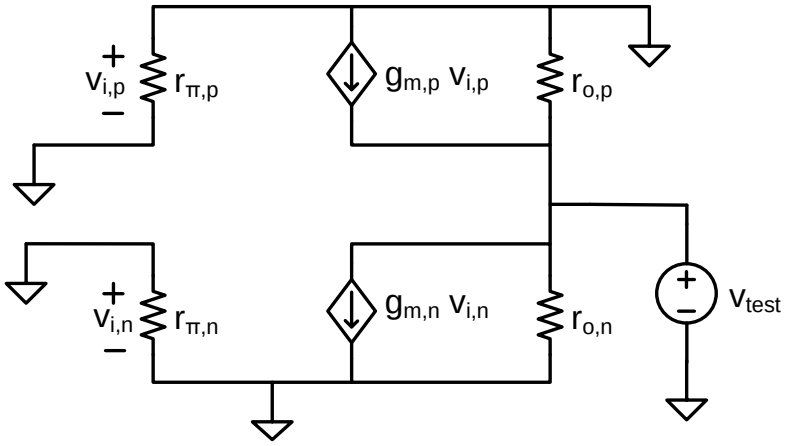
The small signal circuit of our common emitter amplifier with active load is shown below. The subscripts n and p indicate the npn and pnp transistor, respectively. The pnp small signal model has the emitter node at the top, which is connected to supply (AC ground).



The circuit includes two approximations. First the left pnp transistor in the current mirror has been replaced by a ground at the pnp emitter. Recall from the small signal analysis of the two-transistor npn current mirror that the transistor controlling the current flow could be replaced by a ground connection because of the low resistance path through that transistor that included a base-collector short. We have also ignored a base biasing resistor for the npn transistor which has no effect on the output resistance and usually little effect on the input resistance.

Next we apply a test source at v_{out} to find R_{out}, as shown below. The result is easy to see.

$$R_{out} = r_{o,n} \,||\, r_{o,p}$$

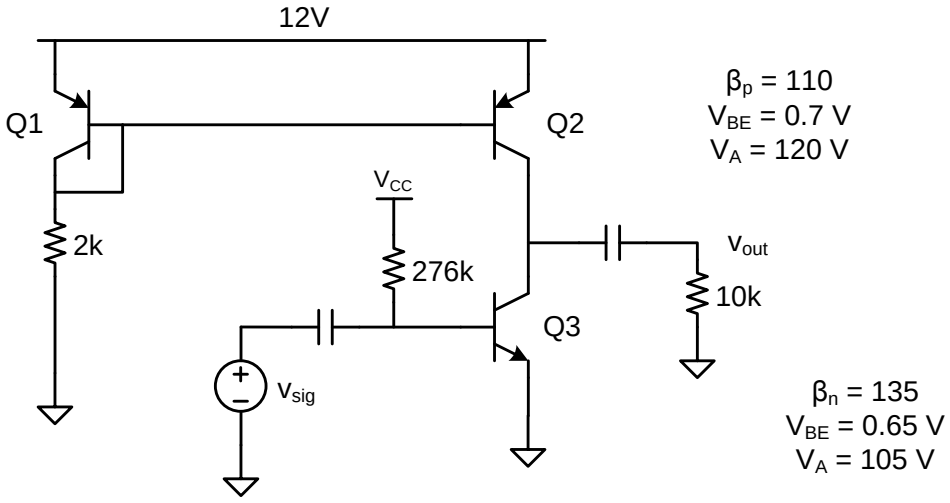


Then the open circuit voltage gain becomes

$$A_v = -g_m R_{out} = -g_m r_{o,n} \,||\, r_{o,p}$$

and R_C has been replaced by the output resistance, $r_{o,p}$ of the current source transistor. With collector currents on the order of 1mA, we can easily obtain output resistance in the range of 20 kΩ to 50 kΩ. Open circuit voltage gains are easily in excess of 1000 because of the very large output resistance. Of course such high output resistance is only useful for large load resistance at the amplifier output or overall gain will suffer.

Example 15-1



Find the DC bias point and the overall voltage gain.

Solution:

The current mirror has current on the left side given by

$$I = (12 V - 0.7 V) / 2 k\Omega = 5.65 mA$$
$$I_{C2} = I_o = (1 - 2/\beta_p) I = 5.55 mA \text{ for Q2}$$

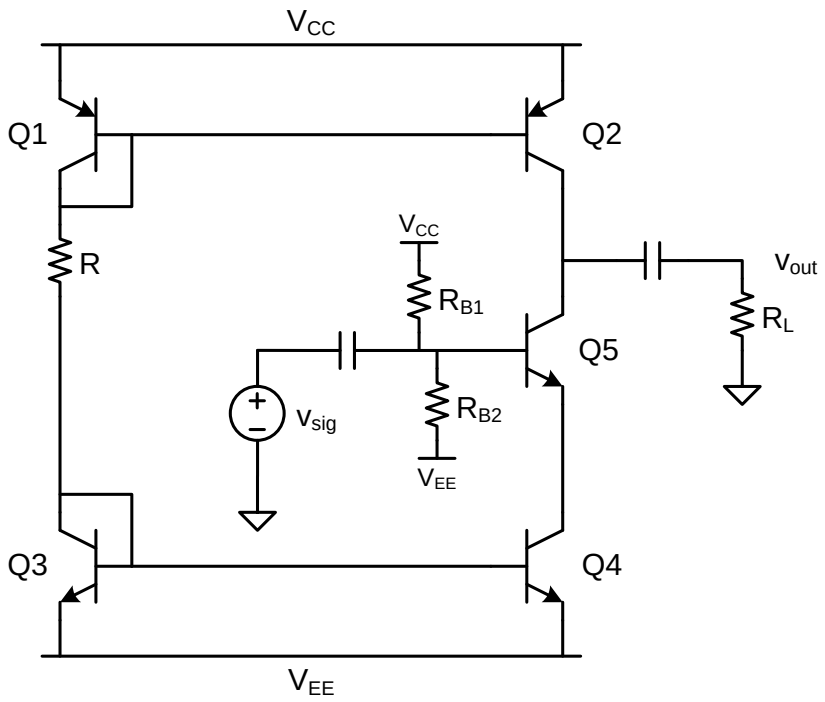
The npn transistor, Q3, has current

$$I_{B3} = (12 V - 0.65) / 276 k\Omega = 41 \mu A$$
$$I_{C3} = 135 \bullet 41 \mu A = 5.54 mA$$

The collector currents of Q2 and Q3 are closely matched so that neither Q2 nor Q3 will be forced into saturation. Then we have

$$g_m = 5.55 mA / .026 V = 213 mA/V$$
$$r_{o,p} = 120 V / 5.55 mA = 21.6 k\Omega$$
$$r_{o,n} = 105 V / 5.55 mA = 18.9 k\Omega$$
$$R_{out} = 21.6 k\Omega \,||\, 18.9 k\Omega = 10.1 k\Omega$$
$$A_v = - g_m R_{out} = - 213 mA/V \; 10.1 k\Omega = - 2150$$
$$A_{overall} = A_v (R_L / (R_{out} + R_L) = - 2150 (10k / 20k)$$
$$= - 1075$$

Now we return to the problem of matching npn and pnp collector currents. One solution is shown in the amplifier circuit below where the Q5 emitter current is now established by a current source that is tied to the same current source that provides Q5 collector current, forcing the two to match, as is detailed below.



The pnp current mirror, Q1 and Q2, supplying collector current to npn common emitter transistor, Q5, is now integrated with an npn current mirror, Q3 and Q4, that sets the emitter current of Q5. The voltage divider on the base of Q5 sets the base and emitter voltage of Q5, but the emitter current is controlled by the current source. The dual current mirror provides equal currents to the Q5 collector and emitter since Q1 and Q3 have equal currents.

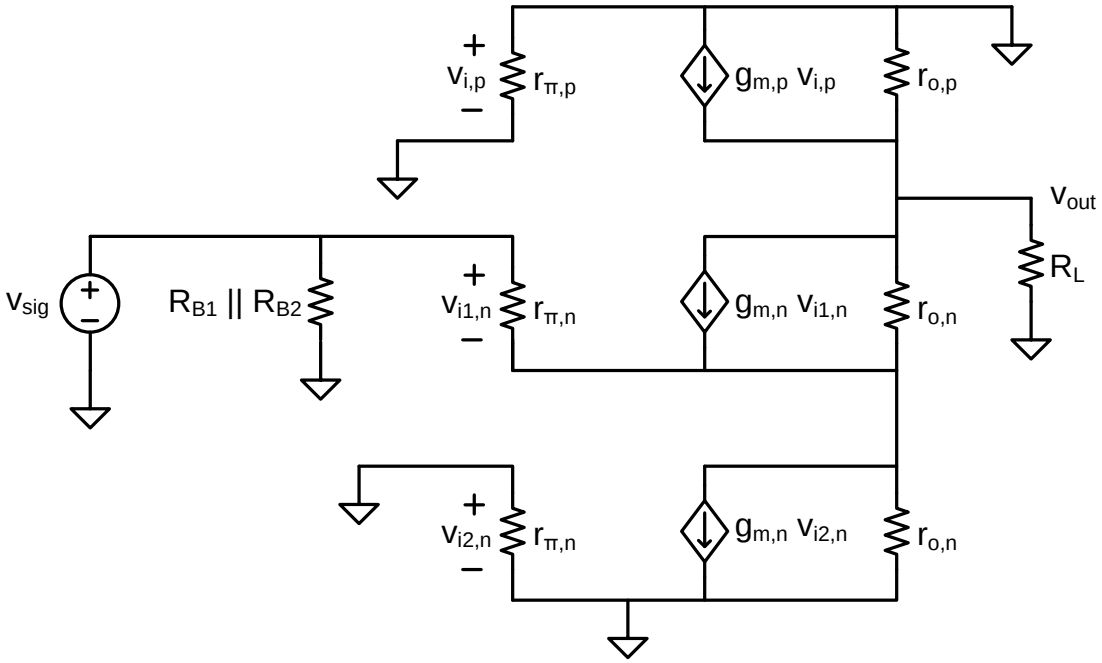
The Q5 collector and emitter currents are very nearly equal to the mirror current, given by

$$I = \frac{V_{CC} - V_{BE,n} - V_{EB,p} - V_{EE}}{R}$$

The voltage at the emitter of Q5 will be 0.6 – 0.7 V below the base voltage set by the voltage divider. The collector voltage of Q2 and Q5 will lie between V_{CC} and the divider voltage such that both transistors will operate in active mode.

The small signal circuit for this configuration is given below. We again replace current

mirror transistors, Q1 and Q3, with ground connections.



Both npn's are shown with the same r_π, g_m and r_o. They have the same I_C and, if identical, will then have the same small signal parameters.

This is now seen to be a common emitter amplifier with active load, dynamic collector resistance of $r_{o,p}$, and emitter degeneration, resistance of $r_{o,n}$. We have previously worked out the amplifier characteristics for a common emitter with emitter degeneration.

$$A_v = -g_m R_{out} / (1 + g_m R_E)$$
$$R_{out} = R_C$$

However, we ignored r_o in that case because $r_o >> R_C$. Now R_C has become the transistor output resistance, $r_{o,p}$, and our previous approximation is not valid. But part of our previous result does still hold. Emitter degeneration reduces voltage gain by a factor $1 + g_m R_E$ which now becomes $1 + g_{m,n} r_{o.n}$ and we have

$$A_v = -g_{m,n} R_{out} / (1 + g_{m,n} r_{o.n})$$

For R_{out}, we refer to a similar circuit we analyzed in the section on current sources on page 14-9. The npn current source with emitter resistors has an approximate small signal circuit identical to what we have here for Q5 where R_E in that case is now replaced by $r_{o,n}$ of Q4. The output resistance for the current source with emitter resistors was found to be $R_{out} = r_o (1 + g_m r_\pi \,||\, R_E)$ which now becomes

$$R_{out} = r_{o,n} (1 + g_{m,n} r_{\pi,n} \,||\, r_{o,n})$$

This does not include the Q2 collector resistor which is just a parallel addition to this result. The result for R_{out} for the actively loaded amplifier with a dual current source is

$$\begin{aligned} R_{out} &= r_{o,p} \;||\; r_{o,n} (1 + g_{m,n} r_{\pi,n} \,||\, r_{o,n}) \\ &\approx r_{o,p} \end{aligned}$$

The approximation comes about because we typically have the case

$$\begin{aligned} 1 + g_{m,n} r_{\pi,n} \,||\, r_{o,n} &\approx g_{m,n} r_{\pi,n} \,||\, r_{o,n} \\ &\approx g_{m,n} r_{\pi,n} \\ &\approx \beta_n \end{aligned}$$

and we have

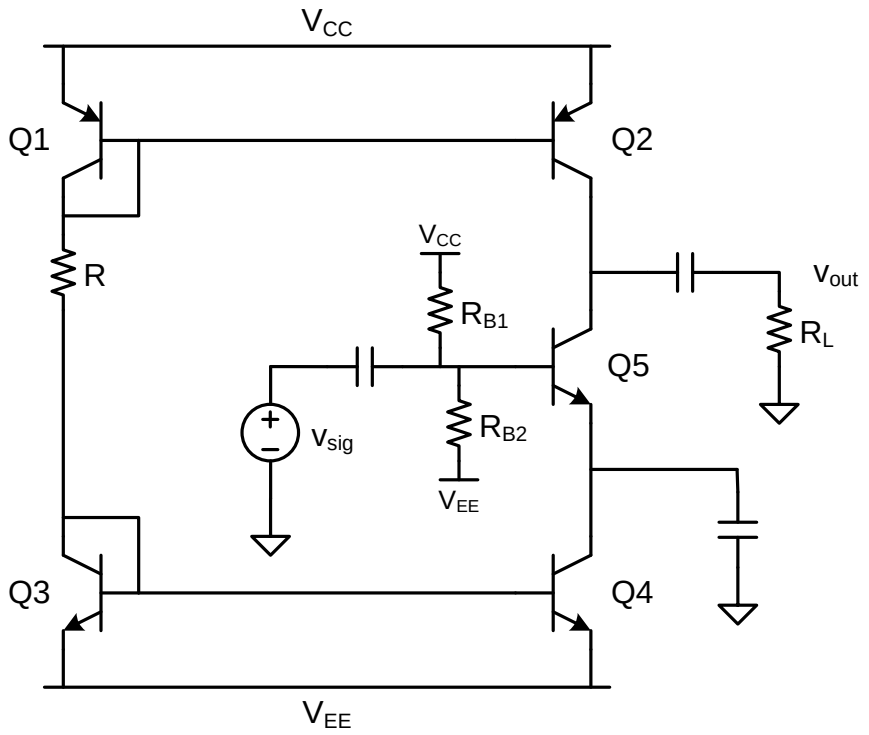
$$\begin{aligned} r_{o,p} \;||\; r_{o,n} (1 + g_{m,n} r_{\pi,n} \,||\, r_{o,n}) &\approx r_{o,p} \;||\; r_{o,n} \beta_n \\ &\approx r_{o,p} \end{aligned}$$

For open circuit voltage gain we get

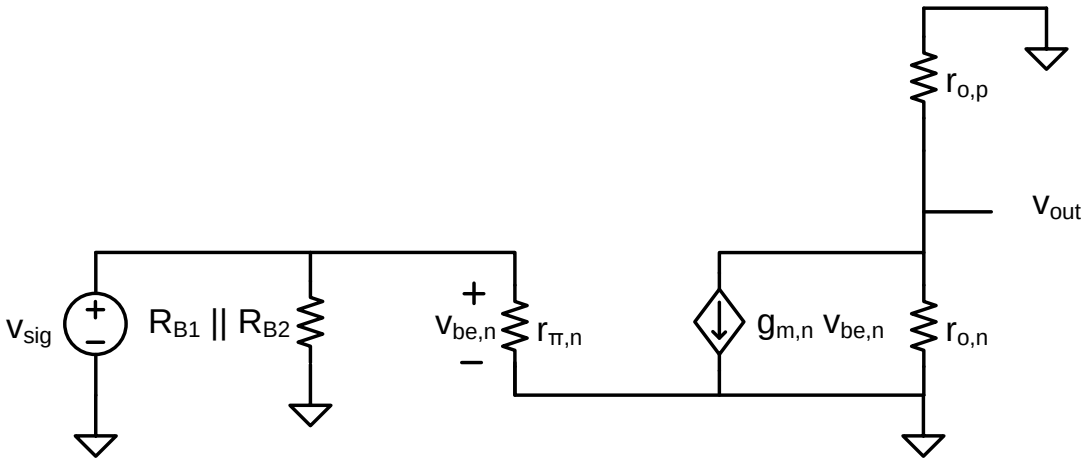
$$\begin{aligned} A_v &= - g_{m,n} R_{out} / (1 + g_{m,n} r_{o.n}) \\ &\approx - g_{m,n} r_{o,p} / (1 + g_{m,n} r_{o.n}) \\ &\approx - r_{o,p} / r_{o.n} \end{aligned}$$

The net result is that with emitter degeneration we have essentially lost the increased gain we achieved with the active load of $r_{o,p}$. We can reclaim that gain by adding a

bypass capacitor across the emitter resistor, that is, the current mirror transistor, Q4, shown below. The bypass capacitor removes the emitter resistor for small signals and eliminates the loss of voltage gain associated with the emitter resistor.



The essential elements of the small signal circuit for this amplifier are shown below.



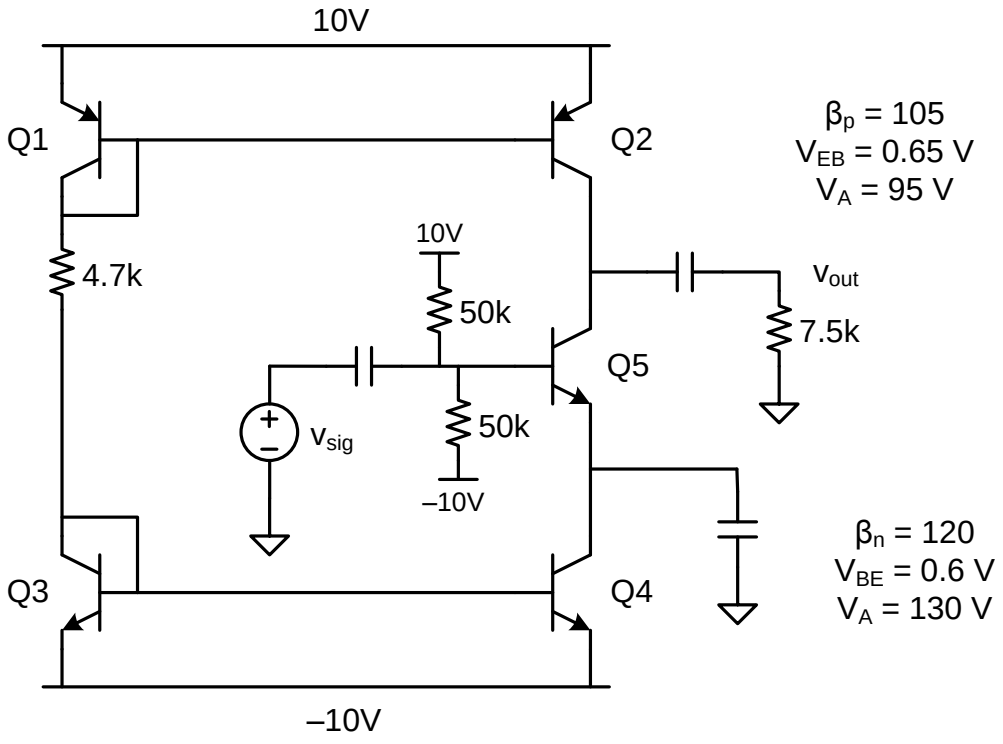
The linear amplifier parameters are just those for the common emitter (without emitter degeneration), now with a dynamic load of $r_{o,p}$ and an output resistance of $r_{o,n} \,||\, r_{o,p}$.

$$A_v = -g_{m,n}\, r_{o,n} \,||\, r_{o,p}$$
$$R_{in} = R_{B1} \,||\, R_{B2} \,||\, r_{\pi,n}$$
$$R_{out} = r_{o,n} \,||\, r_{o,p}$$
$$G_m = -g_{m,n}$$

We have large output resistance and large gain. To increase input resistance, we could use a Darlington pair for just the common emitter transistor while still achieving the dual current source bias situation for the collector currents.

Example 15-2

Find the DC bias point for the dual current mirror common emitter amplifier shown below. What is the overall voltage gain?



Solution:

For the current mirror

$$I = (20 \text{ V} - 0.65 \text{ V} - 0.6 \text{ V}) / 4.7 \text{ k}\Omega = 4.0 \text{ mA}$$

This is the current for all five transistors. Q5 will adjust its emitter voltage to accommodate the collector current of Q4. For Q5 we have

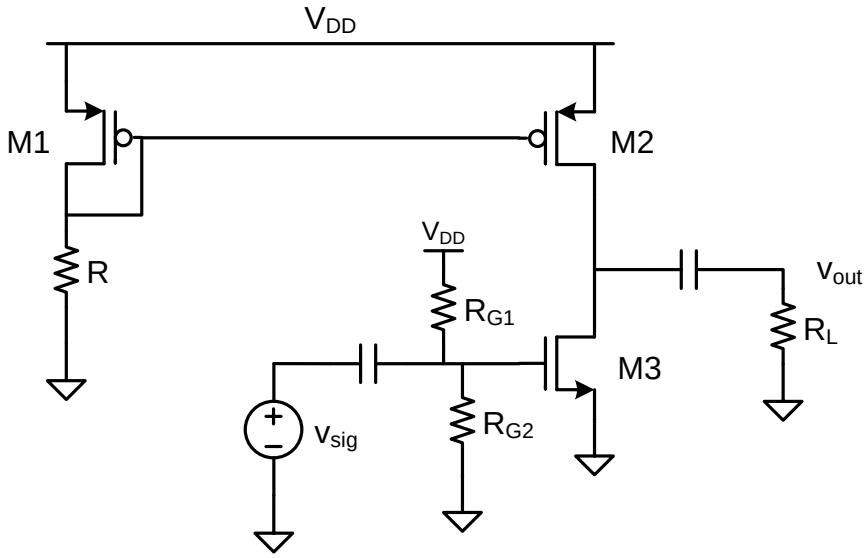
$$I_B = 4.0 \text{ mA} / 120 = 33 \mu\text{A}$$
$$(10 \text{ V} - V_B) / 50 \text{ k}\Omega = (V_B + 10 \text{ V}) / 50 \text{ k}\Omega + 33 \mu\text{A}$$

The second equation relates the current through R_{B1} and R_{B2} which differ by 33 μA, the Q5 base current. Solving that equation, we get $V_B = -0.83$ V which gives us a Q5 emitter voltage of about – 1.43 V.

Now we calculate the linear amplifier parameters and the overall voltage gain.

$$g_m = 4.0 \text{ mA} / .026 \text{ V} = 154 \text{ mA/V}$$
$$r_{o,p} = 95 \text{ V} / 4.0 \text{ mA} = 24 \text{ k}\Omega$$
$$r_{o,n} = 130 \text{ V} / 4.0 \text{ mA} = 32 \text{ k}\Omega$$
$$R_{out} = 24 \text{ k}\Omega \,||\, 32 \text{ k}\Omega = 13.7 \text{ k}\Omega$$
$$A_v = -154 \text{ mA/V } 13.7 \text{ k}\Omega$$
$$= -2110$$
$$A_{overall} = -2110 (7.5 \text{ k}\Omega / (13.7 \text{ k}\Omega + 7.5 \text{ k}\Omega)$$
$$= -746$$

Active loads can also be used with MOSFET common source amplifiers.



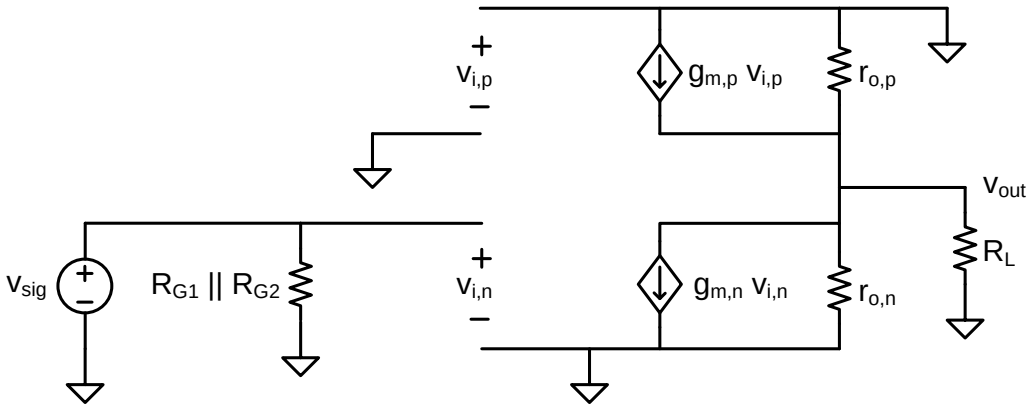
The p-channel drain current I_D is found from the two equations

$$I_D = \mu_p C_{ox,p} (W_p / L_p) \tfrac{1}{2} (V_{GS,p} - V_{th,p})^2$$

$$V_{DD} + V_{GS,p} - I_D R = 0$$

where $V_{GS,p} < 0$ and $V_{th,p} < 0$ for p-channel devices.

The small signal circuit, with the approximation of a virtual ground at the gate of M2, similar to what we used for the BJT case, is



From this circuit we readily get these results, very similar to the BJT case.

$$R_{in} = R_{G1} \,||\, R_{G2}$$
$$R_{out} = r_{o,n} \,||\, r_{o,p}$$
$$A_v = -g_{m,n} (r_{o,n} \,||\, r_{o,p})$$

The next step in the development of the common source amplifier with active load would be to use the dual current source to match drain currents of the n-channel common source transistor with the p-channel active load. We could then bypass the n-channel current source transistor to increase gain, like the BJT case. The results would be the same as we obtained above. The advantage of the MOSFET version of this amplifier is that we can maintain a very large input resistance even with the bypass capacitor included.