TCES 330

Homework for Tuesday, April 8

Homework 0 for Tuesday, April 8

- Implement f1 and f2 from B&V Problem 2.58(a) (2.44(a) in the second edition) in one module in Quartus using Verilog operators and continuous assignments. Use the Netlist Viewer (Technology Map Viewer) to demonstrate 2.58(b) (2.44(b)). This will work best if you rename f1 to f and f2 to g in your Verilog module. Call this project Prob258 and put it in a folder called Prob258.

- Do B&V Problem 2.60 (2.46 in the second edition) as stated in the text. Make a Quartus project called Prob260, put it in a folder called Prob260, and compile your code. Use the Netlist Viewer (RTL Viewer) to verify that your circuit looks like Figure 2.32a (Figure 2.27a in the second edition).

- Do B&V Problem 2.61 (2.47 in the second edition) but use Verilog operators and continuous assignments rather than gate level primitives. Use the Netlist Viewer (RTL Viewer) to verify that your circuit looks like Figure 2.32b (Figure 2.27b). Call this project Prob261 and put it in a folder called Prob261.

- Zip all three Quartus project folders together and submit the zip file on Moodle. We'll discuss the format for this in class.

Lab for Tuesday, April 8

- Watch the screen-cast video: Simple Quartus Project. You can find it by following the link “Link to My Videos“ on Moodle.
- Read through the file “Homework 1” which is Altera’s “Laboratory Exercise 1.” We will start this exercise in Lab on Tuesday.