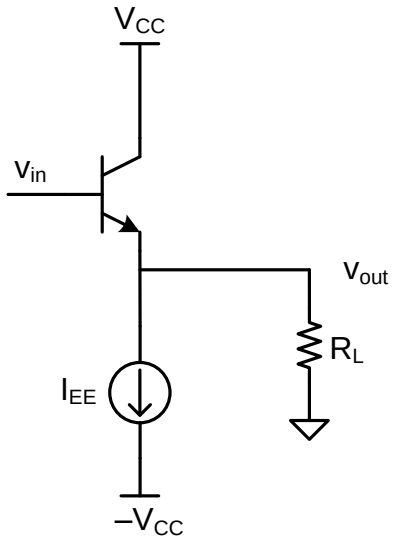
17 Push-pull output

The output stage of an amplifier should, generally, have a low output resistance to be able to drive low resistance loads without excessive loss of voltage gain or power.

We already know of one type of single transistor amplifier with low output resistance. The emitter follower or source follower can have output resistance as low as a few Ohms.

A version of the emitter follower capable of driving a load to nearly $\pm V_{CC}$ is shown below.

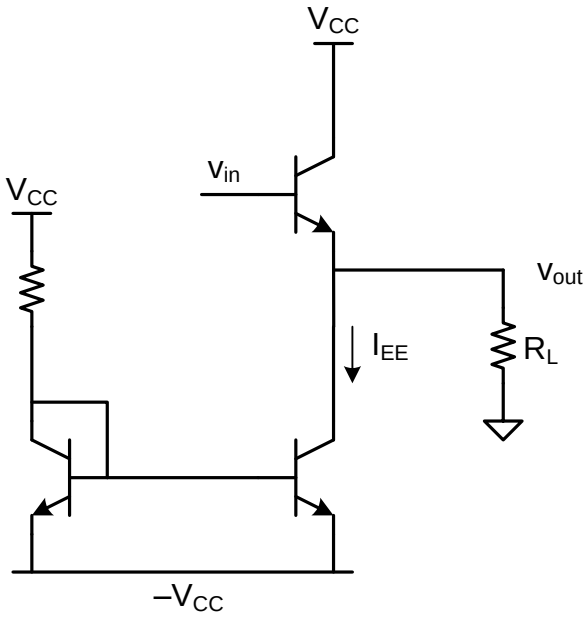


For simplicity, the load is DC coupled and the DC level of the input to the base of the follower is assumed to be at or near zero Volts.

The emitter resistor of the follower has been replaced by a current source to enable the follower amplifier to have a negative voltage swing of nearly $-V_{CC}$. Recall the limitations on the negative voltage swing with an emitter resistor. The negative swing will go no lower than what the current flow through the load resistor and then through the emitter resistor to low supply will allow when the transistor is turned off. With a

current source in place of the emitter resistor, currents as large as I_{EE} can be pulled through the load taking v_{out} to a voltage equal to $- I_{EE} / R_L$. If we choose $- I_{EE} / R_L = - V_{CC}$, then the negative voltage swing at the output is $- V_{CC}$ for an ideal current source and nearly $- V_{CC}$ for a real current source.

For a current mirror used as the current source, the output can be pulled low until the output transistor of the current source saturates. If the lower supply is $- V_{CC}$, the voltage swing is limited to about 0.3 V above $- V_{CC}$.



The <u>positive</u> voltage swing at the follower output is limited by saturation of the follower transistor which is again within about 0.3 V of V_{CC}. So we have output swing of almost $\pm V_{CC}$.

While this output stage functions nearly to $v_{out} = \pm V_{CC}$, there is a serious disadvantage. For $v_{out} = 0$ V, no power is delivered to the load but power is being dissipated as current I_{EE} flows through the transistor and the current source between $+ V_{CC}$ and $- V_{CC}$. That total power is

$$P = 2 V_{CC} I_{EE}$$

This stand-by power represents power loss and generates heat in the follower and current mirror transistors. When an output signal is present, the fraction of power delivered to the load is, at best, a small fraction of the power consumed by the output stage, as we will see below. This output stage is inefficient in terms of delivered power.

To quantify the efficiency of the output stage, consider a sine wave signal at the load with an amplitude of V_{CC}, the maximum that can be delivered (ignoring the 0.3 V saturation limitation) .

$$v_L = V_{CC} \sin \omega t$$

where $\omega = 2\pi / T$ and T = period of the sine wave. Then the current to R_L is

$$i_L = v_L / R_L = (V_{CC} / R_L) \sin \omega t$$

and the power to R_L is

$$p_L = v_L i_L = (V_{CC}^2 / R_L) \sin^2 \omega t$$

If we average this over one cycle we get

$$\begin{aligned} < p_L > &= \frac{1}{T} \int_0^T \frac{V_{CC}^2}{R_L} \sin^2 \omega t \, dt \\ &= \frac{1}{T} \frac{V_{CC}^2}{R_L} \int_0^T \sin^2 \omega t \, dt \\ &= \frac{1}{T} \frac{V_{CC}^2}{R_L} \int_0^T \tfrac{1}{2} (1 - \cos 2\omega t) \, dt \\ &= \frac{1}{T} \frac{V_{CC}^2}{R_L} \tfrac{1}{2} [t - (1 / 2\omega) \sin 2\omega t] \Big|_0^T \\ &= \frac{1}{T} \frac{V_{CC}^2}{R_L} \tfrac{1}{2} T \end{aligned}$$

where $\sin 2\omega T = \sin 4\pi = 0$. Finally we have for the average power delivered to the load

$$< p_L > = \frac{V_{CC}^2}{2 R_L}$$

Now the power provided by the power supply is

$$P_{supply} = V_{supply} \bullet I_{supply}$$

For the + V_{CC} voltage supply, the current is I_{EE} plus what goes to the load.

$$I_{+VCC} = I_{EE} + (V_{CC} / R_L) \sin \omega t$$

The sinusoidal contribution can be positive or negative. When it is negative, current flows from the load and contributes part of the I_{EE} current to the current source, reducing the current drawn from the $+V_{CC}$ supply. When it is positive, it adds to the I_{EE} drawn by the current source. The average power from the + V_{CC} supply is

$$< P_{+VCC} > = \frac{1}{T} \int_0^T V_{CC} (I_{EE} + \frac{V_{CC}}{R_L} \sin \omega t) \, dt$$

$$= \frac{1}{T} \int_0^T V_{CC} I_{EE} \, dt + \frac{1}{T} \int_0^T \frac{V_{CC}^2}{R_L} \sin \omega t \, dt$$

The second term on the right is exactly zero since the average of the sine over one cycle is zero. Then we have

$$< P_{+VCC} > = V_{CC} I_{EE}$$

For the – V_{CC} voltage supply, the current is – I_{EE}. So we have

$$< P_{-VCC} > = – V_{CC} (– I_{EE}) = V_{CC} I_{EE}$$

The total average power from the two power sources is then

$$< P_{supply} > = 2 V_{CC} I_{EE}$$

$$= 2 V_{CC}^2 / R_L$$

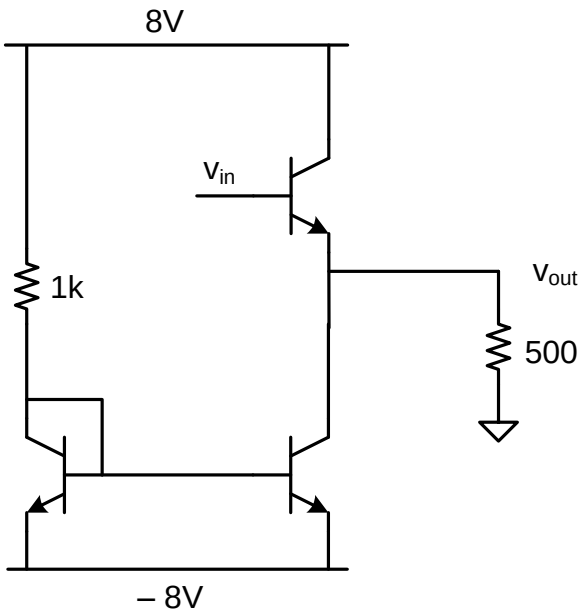
The power efficiency of the output stage is the ratio of the power delivered to the load to the power from the supply.

$$< p_L > / < P_{supply} > = (V_{CC}^2 / 2 R_L) / (2 V_{CC}^2 / R_L)$$
$$= 1 / 4$$

This is also the <u>maximum</u> power efficiency since the output amplitude is V_{CC} and I_{CC} is set to V_{CC} / R_L. We have only 25% efficiency for the output voltage driven sinusoidally to $\pm V_{CC}$. For smaller output swing the efficiency decreases and, in addition, we have the problem of stand-by power.

Example 17-1

Find the stand-by power for this output stage neglecting the power used by the left side of the current source (which <u>doubles</u> the power required). What is the power delivered to the load at maximum output voltage swing, neglecting small saturation voltages? What is the power delivered to the load at one half maximum voltage swing?



Solution:

The current source output is approximately

$$2\ V_{CC} / R\ =\ 16\ V / 1\ k\Omega\ =\ 16\ mA.$$

The stand-by power is

$$P_{supply}\ =\ 2\ V_{CC}\ I_{supply}\ =\ 16\ V\ 16\ mA\ =\ 256\ mW$$

This is also the average power from the supply when an output signal is present.

The average power to the load at ± 8 V swing is

$$< p_L >\ =\ V_{CC}^2 / 2\ R_L\ =\ 64\ V^2 / 1\ k\Omega\ =\ 64\ mW$$

And the efficiency in this case is, as expected,

$$64\ mA / 256\ mW\ =\ 25\%$$

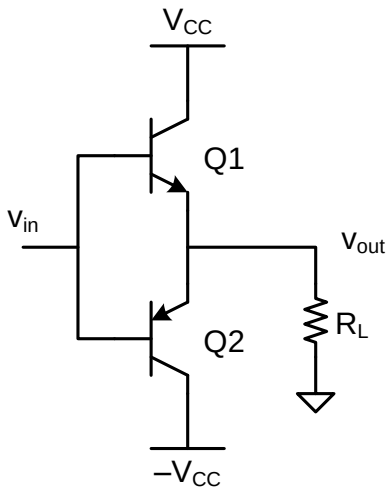
The average power to the load at ± ½ V_{CC} = ± 4 V swing is

$$< p_L >\ =\ (\ V_{CC} / 2\ )^2 / 2\ R_L\ =\ 16\ V^2 / 1\ k\Omega\ =\ 16\ mW$$

with an efficiency of

$$16\ mA / 256\ mW\ =\ 6.25\%$$

An improved version of a follower output stage, called a push-pull, is shown below. It has improved power efficiency and eliminates the problem of stand-by power. It is constructed using two complementary emitter followers where one acts to pull the load high and the other acts to pull (push) the load low.



The npn transistor, Q1, is able to pull the output voltage nearly to V_{CC} while the pnp transistor, Q2, can pull the load low to nearly $-V_{CC}$. When $v_{out} > 0$, Q1 is in active mode and $v_{in} - v_{out} \approx 0.6$ V. (We'll assume base-emitter voltage of about 0.6 V for both npn and pnp transistors, although for pnp the polarity is reversed, $V_{BE,pnp} = -V_{BE,npn}$.) With Q1 conducting, Q2 is necessarily shut off since the Q2 base-emitter junction is reverse biased. The opposite situation also holds. When $v_{out} < 0$, Q2 conducts, $v_{in} - v_{out} \approx -0.6$ V and Q1 is shut off. So only one transistor conducts in active mode at one time. For $v_{in} = v_{out} = 0$, neither transistor is on and there is, consequently, no stand-by power.

But note that there is an input voltage range $-0.6 \text{ V} \le v_{in} \le 0.6$ V where the output remains at or near zero. v_{in} must rise to about 0.6 V before Q1 starts to deliver current to the load and v_{in} must fall to about – 0.6 V before Q2 starts to pull current from the load. The output follows the input with a 0.6 V lag and creates the ~1.2 V region about $v_{in} = 0$ where there is no output response. We'll see later how this can be addressed.

The power efficiency of this output stage is calculated similarly to that for the single follower stage. For a maximum sinusoidal output, we again have

$$< p_L > = \frac{V_{CC}^2}{2 R_L}$$

For the + V_{CC} supply, current is delivered only to the load and only while $v_{out} > 0$. (We'll ignore the 0.6 V offset.)

$$< P_{+VCC} > = \frac{1}{T}\int_0^T V_{CC}\, i_L\, dt$$

$$= \frac{1}{T}\int_0^{T/2} V_{CC}\,\frac{V_{CC}}{R_L}\,\sin \omega t\, dt$$

where the current is non-zero only for the first half cycle, $0 \le t \le T/2$, but we still carry out the average over one complete cycle. Then

$$< P_{+VCC} > = \frac{1}{T}\,\frac{V_{CC}^2}{R_L}\int_0^{T/2} \sin \omega t\, dt$$

$$= \frac{1}{T}\,\frac{V_{CC}^2}{R_L}\,\frac{1}{\omega}\,(-\cos \omega t)\Big|_0^{T/2}$$

$$= \frac{1}{T}\,\frac{V_{CC}^2}{R_L}\,\frac{T}{2\pi}\,(-\cos \omega T/2 + \cos 0)$$

$$= \frac{V_{CC}^2}{R_L}\,\frac{1}{2\pi}\,(-\cos \pi + \cos 0)$$

The result is

$$< P_{+VCC} > = \frac{1}{\pi}\,\frac{V_{CC}^2}{R_L}$$

The result for the − V_{CC} supply is identical.

$$< P_{-VCC} > = \frac{1}{\pi}\,\frac{V_{CC}^2}{R_L}$$

And we get finally that the total average power from the voltage supplies is given by

$$< P_{supply} > = \frac{2}{\pi}\,\frac{V_{CC}^2}{R_L}$$

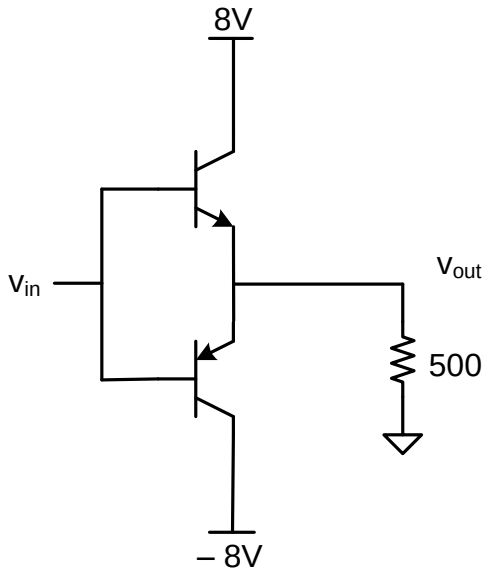
So for the efficiency at maximum output voltage swing we get

$$< p_L > / < P_{supply} > = (V_{CC}^2 / 2 R_L) / (2/\pi) (V_{CC}^2 / R_L)$$
$$= \pi / 4$$

This is 78.5% and more than 3x our previous result for the single follower output stage. Much less power is absorbed by the transistors for the push-pull configuration making it operate with lower heat dissipation and at lower temperature.

Example 17-2

Find the power delivered to the load and the power dissipated in the transistors at ± 8 V output swing and at ± 4 V output swing.



Solution:

At ± 8 V output swing, the average power to the load is

$$< p_L > = V_{CC}^2 / 2 R_L = 64 V^2 / 1 k\Omega = 64 mW$$

while the total power from the supply is

$$< P_{supply} > \; = \; (2 / \pi) \, V_{CC}^2 / R_L \; = \; 81.5 \text{ mW}$$

with an efficiency

$$64 \text{ mW} / 81.5 \text{ mw} \; = \; 0.785$$

The power dissipated in the transistors

$$< P_{dissipated} > \; = \; 81.5 \text{ mW} - 64 \text{ mW} \; = \; 17.5 \text{ mW}$$

For ± 4 V output swing, the average power to the load is

$$< p_L > \; = \; (V_{CC} / 2)^2 / 2 \, R_L \; = \; 16 \text{ V}^2 / 1 \text{ k}\Omega \; = \; 16 \text{ mW}$$

The average power delivered by the power supply is

$$< P_{supply} > \; = \; 2 \, \frac{1}{T} \int_0^T V_{CC} \, i_L \, dt$$

$$= \; 2 \, \frac{1}{T} \int_0^{T/2} V_{CC} \, \frac{V_{CC}}{2 \, R_L} \, \sin \omega t \, dt$$

$$= \frac{2}{\pi} \, \frac{V_{CC}^{\,2}}{2 \, R_L} \; = \; 40.7 \text{ mW}$$

with an efficiency, in this case, of

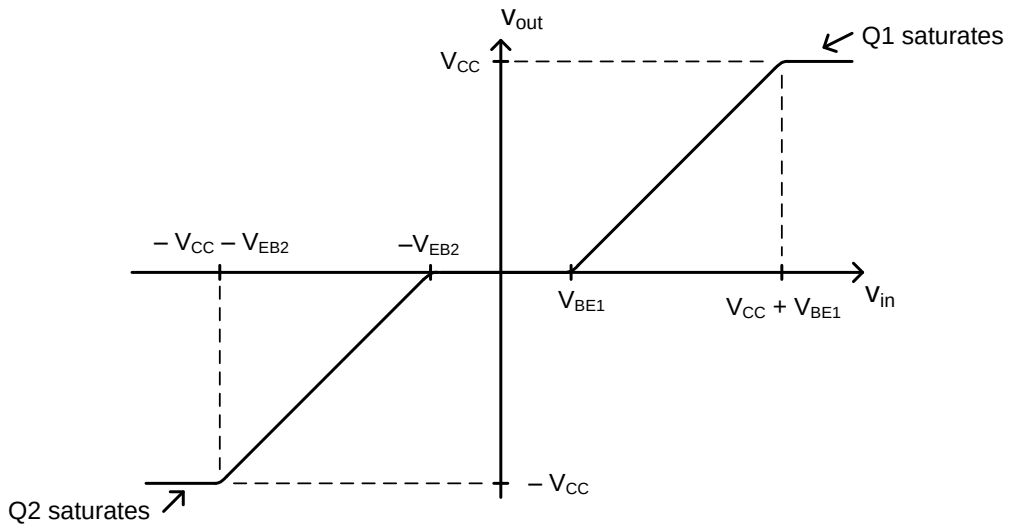
$$16 \text{ mW} / 40.7 \text{ mW} \; = \; 39\%$$

The power dissipated in the transistors

$$< P_{dissipated} > \; = \; 40.7 \text{ mW} - 16 \text{ mW} \; = \; 24.7 \text{ mW}$$

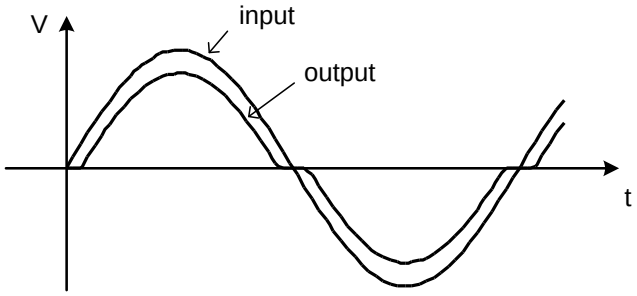
Note that the efficiency drops off by just one half when the voltage swing is one half of the supply voltage.

The input-output characteristic for the push-pull output stage including the base-emitter voltage offset is shown below. (Q1 = npn follower, Q2 = pnp follower)



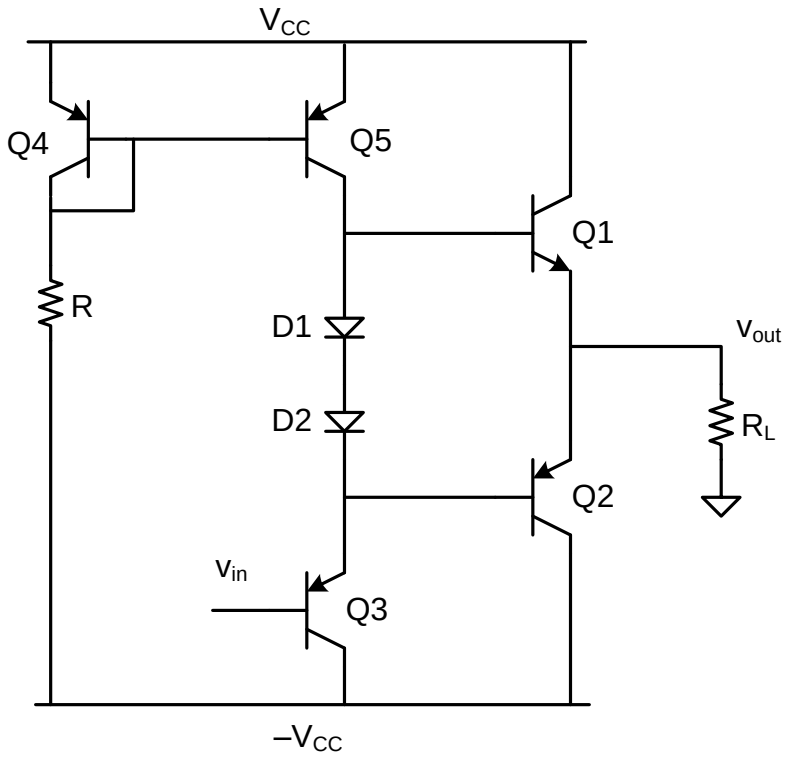
The output follows the input with a lag of V_{BE} (for the npn) and saturates when the output nears the $+V_{CC}$ supply voltage (within about 0.3 V, not indicated in the graph).

For the sinusoidal input we have been considering, the input and output would look something like this.



The output displays the offset near zero Volts as it crosses the horizontal axis both going positive and going negative.

An improved output stage that alleviates the transition zone problem is the following.



Transistors Q1 and Q2 serve the same complementary follower function. The input to Q1 and Q2 are now driven by separate voltages that differ by two diode forward voltage drops ≈ 1.2 V. Those voltages follow v_{in} by means of the pnp follower, Q3. Current is provided to D1 and D2 and to Q3 by the current mirror, Q4 and Q5. That current can be kept to a reasonably low level since only enough current is needed to maintain D1, D2, and Q3 in the "on" state while also providing the small base current required by Q1 during positive output swing.

The current, and power, supplied to the current source Q4 and Q5 and to D1 and D2 and Q3 need not substantially degrade the overall efficiency of the output stage.

With DC coupling at the input and output, this configuration has an offset between v_{in} and v_{out} of 2 V_{BE}, but the crossover region has been eliminated.