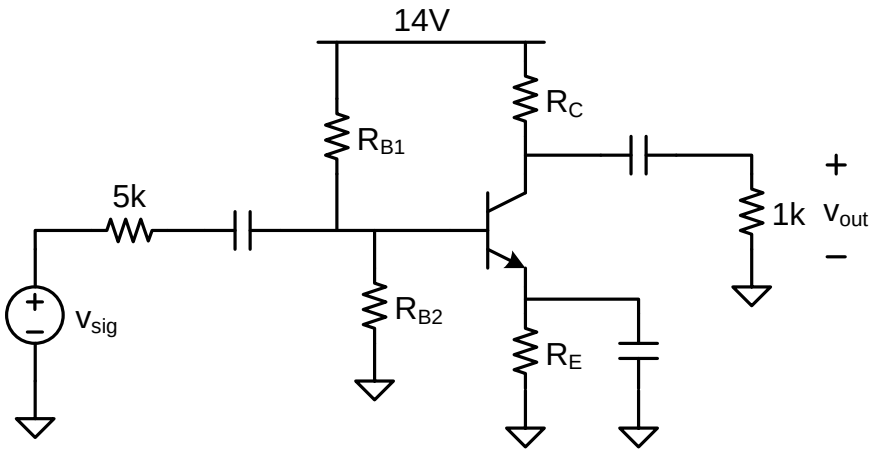
12 Multistage amplifiers

Most amplifiers consist of two or more stages that are cascaded together. The gain of a multistage amplifier is the product of the gains of the separate stages along with the losses realized between the output resistance of one stage and the input resistance of the subsequent stage. There also remain losses at the input of the first stage and the output of the last stage related to input signal resistance and load resistance, respectively.

Multistage amplifiers typically combine stages of different types, working together to achieve the overall amplification requirements. The specific combination of amplifier stages depends on specific requirements although a typical objective is to move toward the ideal voltage amplifier with large input resistance, small output resistance, and large voltage gain.

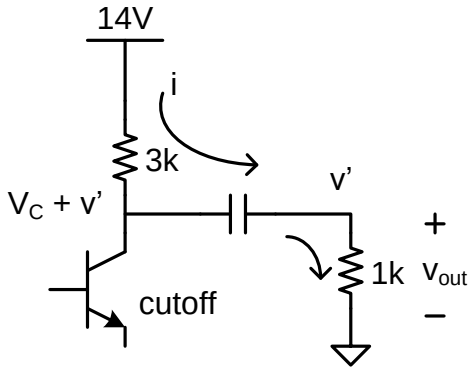
Our focus in this section will be to examine a particular two stage amplifier and to follow the design process to meet specifications. Those specifications include an overall voltage gain of at least – 50 with a source resistance of 5 kΩ and a load resistance of 1 kΩ, and ±1 V output voltage swing. We have a single power supply of 14 V and our npn transistors have $\beta_{min} = 150$, $V_{BE} = 0.7$ V, and $V_A = 90$ V. Let's first see what we can do with a single common emitter stage.



To be insensitive to variations in β, we'll use emitter degeneration and a voltage divider network to bias the base. Bypassing the emitter will increase voltage gain.

We'll try a collector-emitter current of 3 mA, set the emitter voltage at 3 V and the collector voltage at 5 V which gives us some margin to make the ± 1 V swing at the output. So we have R_E = 1 kΩ, R_C = 3 kΩ, and the voltage on the base is 3.7 V.

With an emitter voltage of 3 V and a collector voltage of 5 V, the negative swing on the collector is almost 1.7 V where the transistor goes into saturation. The positive swing, on the other hand, is limited by the current that can be supplied to the load through the collector resistor. When the voltage on the base decreases, the transistor collector takes less current, the collector voltage rises, and current starts to flow to the load. When the transistor base voltage goes low enough that the transistor takes no current (it is in cutoff), then the current flow is just through R_C and R_L (AC current). This sets the maximum rise in the voltage at the collector and the maximum voltage across the load.



$$i = [14\ V - (V_C + v')] / 3\ k\Omega = v' / 1\ k\Omega$$

For V_C = 5 V, we get v' = 2.2 V, well above our minimum positive swing of 1 V.

For β insensitivity, we want the base divider current to be at least 10x the base current to the transistor. Maximum transistor base current is 3 mA / 150 = 20 μA (minimum β) and then the minimum divider current is 200 μA.

$14\ V / (R_{B1} + R_{B2}) = 200\ \mu A$

$R_{B1} + R_{B2} = 14\ V / 200\ \mu A = 70\ k\Omega$

$R_{B2} \bullet 200\ \mu A = 3.7\ V$

$R_{B2} = 19\ k\Omega$

$R_{B1} = 51\ k\Omega$

The calculation of R_{B1} and R_{B2} is not exact. The current in R_{B1} is somewhat greater than that in R_{B2} (they differ by I_B) but this should get us close enough.

With $I_C = 3$ mA, we have

$g_m = 3\ mA / .026\ V = 115\ mA / V$

$r_\pi = 150 / 115\ mA / V = 1.3\ k\Omega$ (minimum)

$r_o = 90\ V / 3\ mA = 30\ k\Omega$

Then we have

$R_{in} = R_{B1} \parallel R_{B2} \parallel r_\pi$ (R_E bypassed)

$= 51k \parallel 19k \parallel 1.3k = 1.2\ k\Omega$

$R_{out} = R_C \parallel r_o$

$= 3k \parallel 30k = 2.7\ k\Omega$

$A_v = -g_m R_{out}$

$= -115\ mA / V \bullet 2.7\ k\Omega = -310$

Finally,

$$A_{overall} = A_v \frac{R_{in}}{R_{sig} + R_{in}} \frac{R_L}{R_{out} + R_L}$$

$$= -310 \frac{1.2k}{5k + 1.2k} \frac{1k}{2.7k + 1k} = -16$$

This is considerably short of our spec of – 50. And there is not much we can do to get substantial improvement. We chose $I_C = 3$ mA. If we were to choose something greater to increase g_m and the voltage gain, we would have to decrease R_C by the same factor since we can't allow the DC voltage on the collector to fall. So there is no improvement in open circuit voltage gain by increasing I_C.

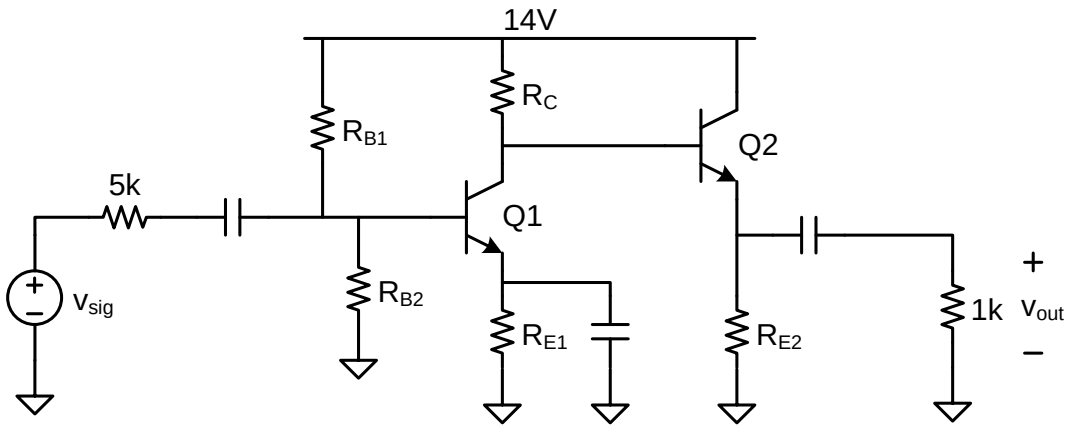
$$V_C = V_{CC} - I_C R_C \rightarrow I_C R_C \text{ is fixed}$$
$$A_v = -g_m R_{out} \approx -g_m R_C = I_C R_C / V_t \rightarrow A_v \text{ is fixed}$$

At the same time, larger I_C and smaller R_C would have two other effects. Larger I_C decreases r_π and R_{in} and increases the loss at the input that results from the resistor ratio $R_{in} / (R_{sig} + R_{in})$. But smaller R_C decreases R_{out} and reduces the loss at the load from the resistor ratio $R_L / (R_{out} + R_L)$. The effects tend to offset.

$$R_{in} = R_{B1} \,||\, R_{B2} \,||\, r_\pi \approx r_\pi = \beta V_t / I_C$$
$$R_{out} = R_C \,||\, r_o \approx R_C$$

On the other hand, choosing something smaller for I_C (< 3 mA) and compensating the gain with a larger R_C doesn't get us much further. The effects still tend to offset with opposite contributions. It is true that for the present design, the loss at the input is greater than the loss at the output because of the relative differences between R_{in} and R_{sig} and between R_{out} and R_L such that an increase in both R_{in} and R_{out} could be a net increase in gain. But there is no opportunity for sufficient improvement to meet our specification. Additionally, we must be aware that an increase in R_C will decrease the positive voltage swing at the output.

The two stage amplifier we'll use for this design problem is a first stage common emitter followed by a second stage emitter follower.



The follower has no voltage gain so we'll focus the common emitter on larger input resistance and adequate voltage gain. The larger output resistance of the common emitter is accommodated by the high input resistance of the follower. Also, the follower has a low output resistance which will drive the 1 kΩ load more efficiently.
We DC couple the two stages (Q1 collector to Q2 base). We could place a series capacitor in that connection allowing different voltages for the collector of the common emitter and the base of the emitter follower. But it is often better to make a DC connection to avoid filtering effects and to avoid the necessity of separate biasing resistors for the follower base. In this case, the Q1 collector voltage is entirely compatible with the Q2 base voltage and we can avoid a coupling capacitor. We'll also assume we can make the approximation that the base current of Q2 is much smaller than the collector current of Q1 such that the V_{C1} is determined by only R_C and I_{C1}, neglecting I_{B2}.

Recall that the follower stage is not unilateral. So we can't use the linear amplifier model we developed earlier. But we can write for the overall two-stage amplifier gain

$$A_{overall} = A_{v1} \frac{R_{in1}}{R_{sig} + R_{in1}} \frac{R_{in2}}{R_{out1} + R_{in2}} A_2$$

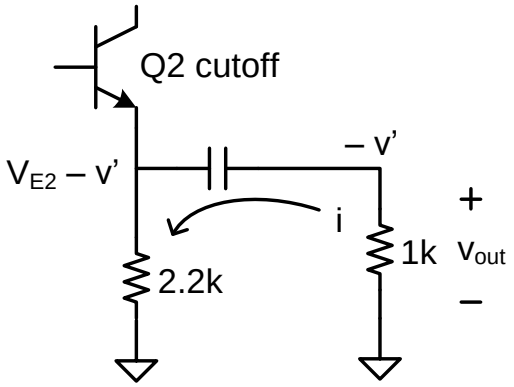
A_{v1} is the open circuit gain of the first stage. The term involving R_{in1} is the voltage divider effect at the input of the first stage. The term involving R_{in2} is the voltage divider effect between the two stages. And A_2 is the overall gain of the second stage that includes the load resistor, R_L but no input signal resistance. Note that R_{in2} involves R_L as well since the second stage is not unilateral.

So now we have, from previous results

$$A_{v1} = -g_{m1} R_{out1}$$
$$R_{in1} = R_{B1} \,||\, R_{B2} \,||\, r_{\pi 1}$$
$$R_{out1} = R_C \,||\, r_{o1}$$
$$R_{in2} = r_{\pi 2} + \beta (R_{E2} \,||\, R_L \,||\, r_{o2})$$
$$A_2 = g_{m2} (R_{E2} \,||\, R_L \,||\, r_{o2} \,||\, 1/g_{m2})$$

The design process can now go something like this. We choose collector currents and find resistor values for DC biasing. Then calculate small signal transistor parameters and, finally, the overall voltage gain. We will reduce the collector current in Q1 compared to our single stage design allowing the input resistance to rise and then compensate the open circuit gain with an increase in R_C. We'll try cutting I_{C1} in half to 1.5 mA and double R_C to 6 kΩ. To keep the same emitter voltage, we also double R_{E1} to 2 kΩ. With half the collector current and half the base current as a result, we can double the base resistors to improve input resistance even more but still maintain β insensitivity. The positive voltage swing at the Q1 collector will be reduced, but a calculation like we did previously gives us 1.3 V, still within spec.

For the emitter follower stage, the base voltage will be 5 V, the same as the Q1 collector, and the emitter voltage about 4.3 V. We would like to choose a relatively large value for R_{E2} that provides increased follower gain and input resistance. But the negative voltage swing requirement places an upper limit on R_E. If we choose $|I_E|$ = 2 mA and R_E = 4.3 V / 2 mA = 2.2 kΩ, we make the following calculation of maximum negative voltage swing.



When the input to Q2 falls, the negative swing limit is reached with Q2 reaches cutoff. Then the only current that flows is i as shown. v_{out} drops to – v' and the emitter voltage drops to V_{E2} – v'. With the DC bias voltage, V_{E2} = 4.3 V,

$$i = (4.3 - v') / 2.2\ k\Omega = v' / 1\ k\Omega$$

Solving this we get v' = 1.3 V and we have adequate negative swing. Note that this limit occurs because for v_{out} to go any lower, there would have to be current flowing into the emitter connection of Q2 which cannot happen in active mode.

Note that positive voltage swing at the follower output is limited only by V_{CC} regardless of DC collector current. v_{out} can rise with emitter voltage until the transistor saturates. So we'll choose I_{C2} = 2 mA and R_{E2} = 2.2 kΩ for the follower stage.

We also note that the base current to Q2 will be 2 mA / 150 = 21 μA which is much less than I_{C1} = 1.5 mA, an assumption we made earlier regarding the calculation of V_{C1}.

For Q2 we find the following.

$$g_{m2} = 2 \text{ mA} / .026 \text{ V} = 77 \text{ mA / V}$$
$$r_{\pi 2} = 150 / 77 \text{ mA / V} = 1.9 \text{ k}\Omega \text{ (minimum)}$$
$$r_{o2} = 90 \text{ V} / 2 \text{ mA} = 45 \text{ k}\Omega$$
$$R_{in2} = r_{\pi 2} + \beta (R_{E2} \,||\, R_L \,||\, r_{o2})$$
$$= 1.9\text{k} + 150 (2.2\text{k} \,||\, 1\text{k} \,||\, 45\text{k})$$
$$= 103 \text{ k}\Omega$$
$$A_2 = g_{m2} (R_{E2} \,||\, R_L \,||\, r_{o2} \,||\, 1/g_{m2})$$
$$= 77 \text{ mA / V} (2.2\text{k} \,||\, 1\text{k} \,||\, 45\text{k} \,||\, 1/77 \text{ mA / V})$$
$$= 0.98$$

For Q1, we now have I_{C1} = 1.5 mA and R_C = 6 kΩ and we will double the resistors in the base voltage divider since base current has been cut in half. New values of base resistance are R_{B1} = 103 kΩ and R_{B1} = 37 kΩ and we make the following calculations for Q1 parameters.

$$g_{m1} = 1.5 \text{ mA} / .026 \text{ V} = 58 \text{ mA / V}$$
$$r_{\pi 1} = 150 / 58 \text{ mA / V} = 2.6 \text{ k}\Omega \text{ (minimum)}$$
$$r_{o1} = 90 \text{ V} / 1.5 \text{ mA} = 60 \text{ k}\Omega$$

$R_{in1} = R_{B1} \,||\, R_{B2} \,||\, r_{\pi 1}$ (R_E bypassed)

$= 103k \,||\, 37k \,||\, 2.6k = 2.4\ k\Omega$

$R_{out1} = R_C \,||\, r_{o1}$

$= 6k \,||\, 60k = 5.5\ k\Omega$

$A_{v1} = -g_{m1} R_{out1}$

$= -58\ mA / V\ 5.5k = -319$

We know that we have adequate voltage swing at the output but we also need adequate voltage swing between the stages of the amplifier. First, note that the overall gain of the second stage is 0.98. So a swing of just slightly more than ± 1 V at the input of the second stage will meet our spec. For the common emitter first stage, the negative swing is V_{CE} – 0.3 V = 1.7 V as before. The positive swing depends on the load seen at the output, which is now R_{in2} = 103 kΩ. This very large input resistance gives us a large positive swing, nearly to V_{CC}.

Now the overall gain of the two-stage amplifier is

$$A_{overall} = A_{v1} \frac{R_{in1}}{R_{sig} + R_{in1}} \frac{R_{in2}}{R_{out1} + R_{in2}} A_2$$

$$A_{overall} = -319 \left(2.4k / (5k + 2.4k) \right) (103k / (5.5k + 103k) .98 = -96$$

This easily meets our specification.

We carried out these calculations with a minimum β of 150. If β = 250, the overall gain is up to – 128 where the increase comes from larger base resistance that increases R_{in} for both stages.

Finally, we verify our results with B2spice simulation and obtain the following table. The first two columns are simulation results for β = 150 and β = 250 followed by our design calculations.

Two-stage amplifier design results

	β = 150	β = 250	design
I_{C1}	1.4 mA	1.4 mA	1.5 mA
I_{C2}	2.2 mA	2.1 mA	2.0 mA
V_{B1}	3.4 V	3.5 V	3.7 V
V_{C1}	5.6 V	5.3 V	5.0 V
V_{E2}	4.9 V	4.7 V	4.3 V
$A_{Voverall}$	– 91	– 123	– 96 @ β = 150

Simulation results are reasonable. The lower voltage on the Q1 base and higher voltage on the Q1 collector are a consequence of the approximate base divider calculation. A more carefully calculated value of V_{B1} would be reduced making I_{C1} smaller and V_{C1} higher. Larger β should improve the approximation and it does.