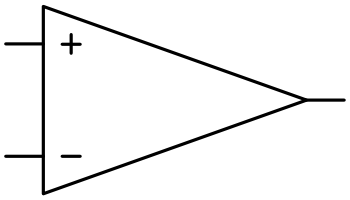
18 Operational Amplifiers

An operational amplifier is a differential input, single-ended output, high gain amplifier with high input resistance and low output resistance. It is typically configured with an external negative feedback network that provides well-controlled amplifier output.

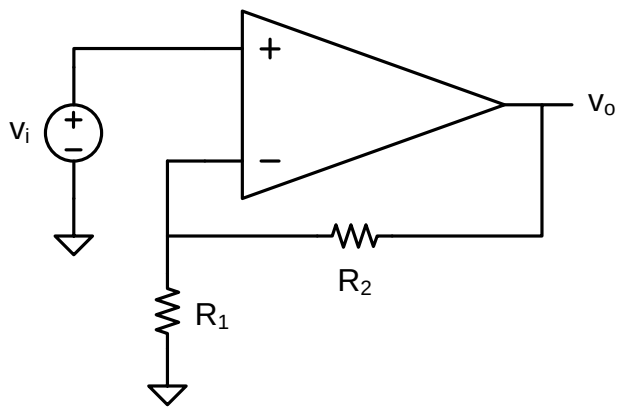
The op amp symbol is



where differential inputs are inverting (−) and non-inverting (+) and the output is at the right. Power supply inputs to the op amp are not shown. They are often ± V_{supply} but can also be + V_{supply} and ground. For many versions of the op amp, the output is able to swing most or nearly all of the voltage range between supply voltages.

The input to an op amp is differential with a large CMRR. When the non-inverting input is at a higher voltage than the inverting input, the output is driven high. It is driven low for the reverse situation. Op amp voltage gain is usually greater than 100,000 and often on the order of 1,000,000. Input resistance is usually greater than 1MΩ resulting in very small input currents.

The idea of negative feedback is best illustrated by an example.



The feedback network consists of resistors R_1 and R_2. When a positive input, v_i, is first applied, the output is driven high as the non-inverting input voltage is greater than the inverting input voltage. But as the output, v_o, increases, the inverting input voltage increases due to the feedback. The voltage fed back to the inverting input is

$$v_- = v_o R_1 / (R_1 + R_2)$$

where the very large input resistance at the inverting input imposes a very small (negligible) load on the voltage divider consisting of R_1 and R_2. And as feedback voltage increases it tends to drive the output down because it is applied to the inverting input. It is negative feedback.

The output voltage, v_o, finally settles at a voltage high enough that the inverting input voltage is very nearly equal to the input voltage, v_i. Because of the very large gain of the op amp, only a very small difference in the two input voltages is necessary to bring the output to a level within the range of its voltage swing ($\approx \pm V_{supply}$).

Because the inverting input reaches a level very nearly equal to the non-inverting input, we usually assume both input voltages are equal when analyzing a negative feedback circuit. Then we have

$$v_- = v_i = v_o R_1 / (R_1 + R_2)$$

from which we obtain

$$\begin{aligned} v_o &= v_i (R_1 + R_2) / R_1 \\ &= v_i (1 + R_2 / R_1) \end{aligned}$$

The gain of the amplifier with this feedback network is just

$$v_o / v_i = 1 + R_2 / R_1$$

By selecting values of R_1 and R_2 we can design an amplifier of any positive gain greater than one (and << A, the op amp gain). This is a non-inverting amplifier configuration.

Example 18-1

Using an op amp operating with ± 10 V supplies, design a non-inverting amplifier with a gain of 25 where the feedback network draws no more than 1 mA from the op amp output.

Solution:
The gain of the non-inverting amplifier is

$$v_o / v_i = 1 + R_2 / R_1 = 25$$
$$R_2 / R_1 = 24$$

The current drawn by the series connection of R_1 and R_2 is (with no current to the inverting input), at maximum output

$$10 \text{ V} / (R_1 + R_2) = 1 \text{ mA}$$
$$R_1 + R_2 = 10 \text{ k}\Omega$$

The two equations in R_1 and R_2 are solved to obtain

$$R_1 = 400 \ \Omega$$
$$R_2 = 9.6 \text{ k}\Omega$$

These are minimum values for R_1 and R_2. A multiple of R_1 and R_2 greater than one provides the same amplification at lower current drawn from the output.

We now analyze the non-inverting op amp circuit more closely, without assuming input voltages are equal. We have the following.

$$v_o = A (v_+ - v_-) = A (v_i - v_-)$$

where A is the voltage gain of the op amp. The feedback is

$$v_- = v_o R_1 / (R_1 + R_2)$$

Eliminating v_- between these two equations, we get

$$v_o = A [v_i - v_o R_1 / (R_1 + R_2)]$$

We solve this for v_o and get

$$v_o = v_i \frac{1 + R_2 / R_1}{1 + (1/A) (1 + R_2 / R_1)}$$

This result includes finite op amp gain, A. But because A is very large, we can approximate by neglecting the second term in the denominator with the 1/A factor and get our previous result.

$$v_o \approx v_i (1 + R_2 / R_1)$$

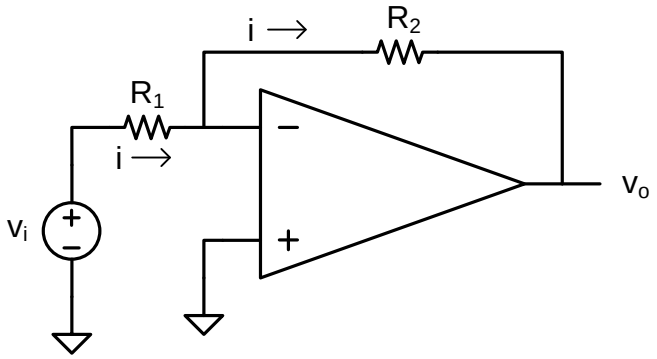
In analyzing or designing op amp circuits with negative feedback, we will almost always neglect the small effect of large but finite op amp gain. That is to say we will usually assume the op amp input voltages are equal. We will further assume, because the resistance at the op amp inputs is very large, that no current flows to the op amp inputs. These two rules then form the basis of almost all of our negative feedback op amp analysis.

Op amp rules for simplified analysis of negative feedback circuits:

(1) The op amp input voltages are equal.

(2) The op amp input currents are zero.

The next example we'll examine is the inverting amplifier configuration.



For v_i positive, the output is initially driven negative, pulling the inverting input down (negative feedback). Current flows from the source, v_i, through R_1 and R_2 to the output. Because the non-inverting input is grounded, the inverting input must end up at zero volts. For current, i, flowing from v_i, we get

$$v_i - i R_1 = 0$$
$$0 - i R_2 = v_o$$

Eliminating i between these two equations we get

$$v_i / R_1 = - v_o / R_2$$

or

$$v_o = v_i (- R_2 / R_1)$$

and we have an amplifier with a negative gain.

$$v_o / v_i = - R_2 / R_1$$

We can also make an inverter with this configuration. If $R_1 = R_2$, we have

$$v_o / v_i = - 1$$

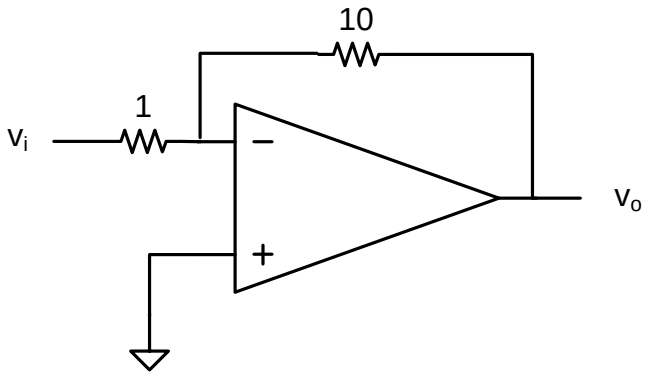
and

$$v_o = - v_i$$

Example 18-2

An op amp with a differential voltage gain of 500,000 is designed as an inverting amplifier with a gain of $-R_2 / R_1 = -10$ What are the precise voltages at the v_- terminal and at the output for a 1 V input?

Solution:



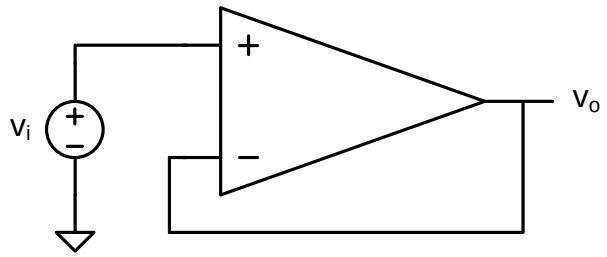
This op amp is designed for a gain of – 10. We can choose any resistance values with a 10:1 ratio. 10 and 1 are convenient. The terminal and output voltages are found from

$$v_+ = 0$$
$$A (v_+ - v_-) = v_o$$
$$(v_i - v_-) / 1 = (v_- - v_o) / 10$$

Taking $v_i = 1$ V, we solve these equations to obtain

$$v_o = -10 \text{ V} / (1 + 11 / A)$$
$$= 9.9998 \text{ V}$$
$$v_- = 20 \mu\text{V}$$

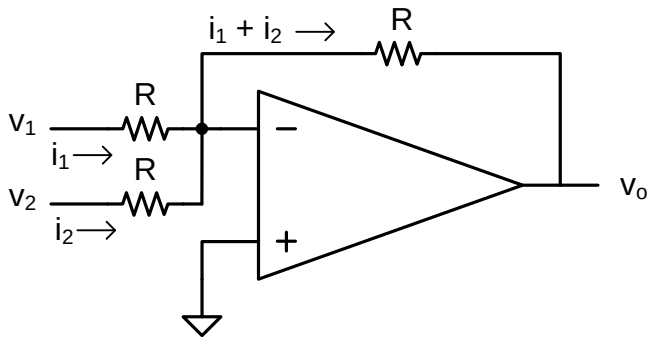
A follower is constructed from an op amp using the non-inverting amplifier configuration with $R_1 = \infty$ and $R_2 = 0$. The gain is then one.



$$v_o = v_i (1 + R_2 / R_1) = v_i$$

This follower has very low effective output resistance. The output, v_o, follows v_i within a few millivolts or less driving any load within the output current capability of the op amp.

A summing amplifier is a modification of the inverting configuration.



The inverting input must be at zero volts.

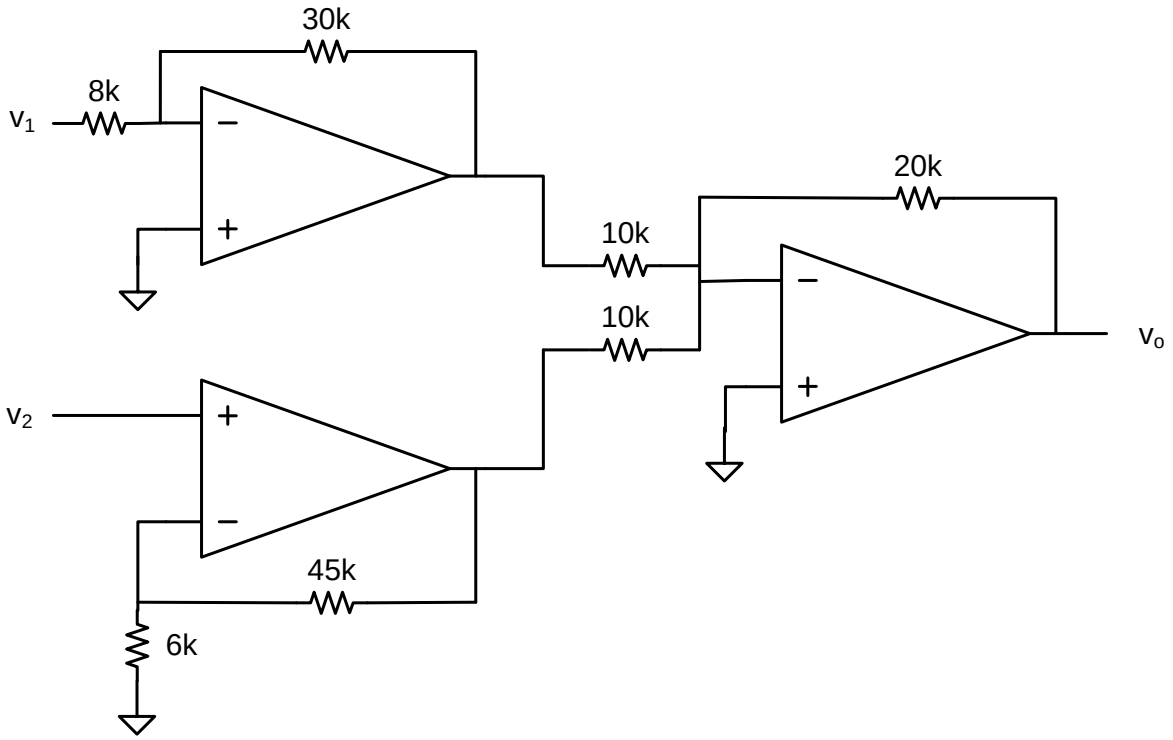
$$i_1 = v_1 / R$$
$$i_2 = v_2 / R$$
$$v_o = -(i_1 + i_2) R$$
$$= -(v_1 / R + v_2 / R) R$$
$$= -(v_1 + v_2)$$

This summing amplifier also inverts. A subsequent op amp stage that inverts again could be included to get an overall result, $v_o = v_1 + v_2$.

By adjusting values of resistance, a weighted sum can also be constructed. In particular, reducing the input resistor for one of the input voltages by a factor, f, will multiply that voltage in the output by the same factor. See Example 18-4.

Example 18-3

Find the output voltage of this op amp circuit.



Solution:

The upper left op amp is an inverting amplifier with a gain of – 30 / 8 = – 3.75. The lower left is a non-inverting amplifier with a gain of 1 + 45 / 6 = 8.5. The right op amp is a summing (and inverting) amplifier that also has a gain of 2 because of the 20 kΩ feedback resistor compared to the 10 kΩ input resistors. The result is a final output of

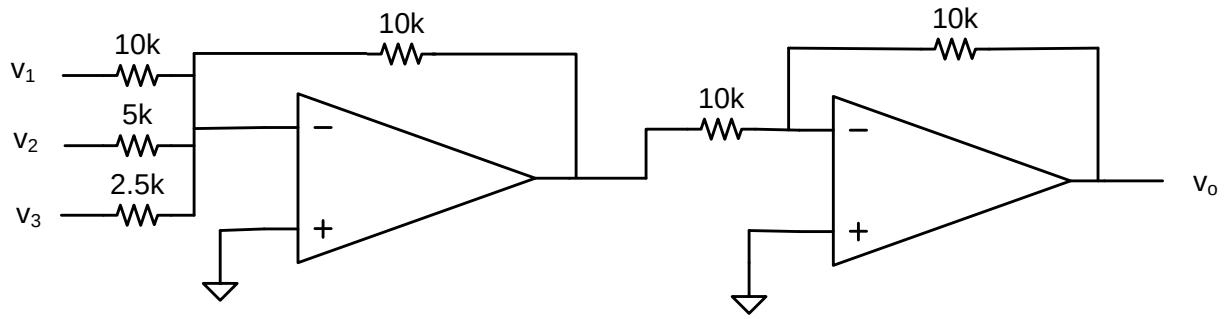
$$v_o = -3.75\, v_1 \bullet (-2) + 8.5\, v_2 \bullet (-2) = 7.5\, v_1 - 17\, v_2$$

Example 18-4

Design a weighted, summing amplifier with a non-inverting output, $v_o = v_1 + 2\,v_2 + 4\,v_3$.

Solution:

This will require a summing amplifier with different input resistors in the ratio of 1:1/2:1/4 and an inverting amplifier as a last stage to create an overall non-inverted output. The following is one possibility.



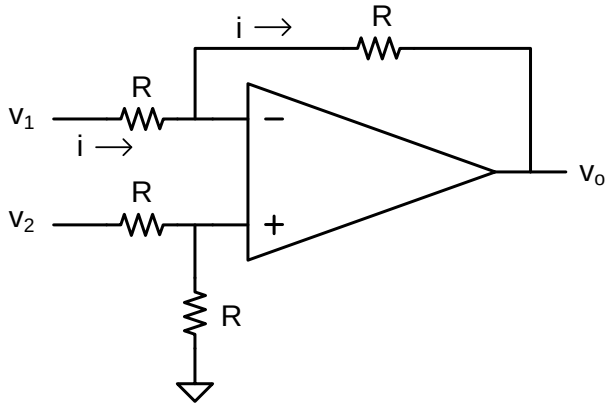
If i_1, i_2, and i_3 are the input currents for v_1, v_2, and v_3, respectively, then for the first stage, we have an output voltage of

$$\begin{aligned} v &= -(i_1 + i_2 + i_3)\,10k \\ &= -[\,(v_1 / 10k) + (v_2 / 5k) + (v_3 / 2.5k)\,]\,10k \\ &= -(v_1 + 2\,v_2 + 4\,v_3) \end{aligned}$$

With the final stage inversion, we get

$$\begin{aligned} v_o &= -v \\ &= v_1 + 2\,v_2 + 4\,v_3 \end{aligned}$$

A <u>subtractor</u> is formed with this configuration.



$$v_+ = v_2 \, R / (R + R) = \tfrac{1}{2} v_2$$

$$v_- = v_1 - i R = v_+ = \tfrac{1}{2} v_2$$

$$i R = v_1 - \tfrac{1}{2} v_2$$

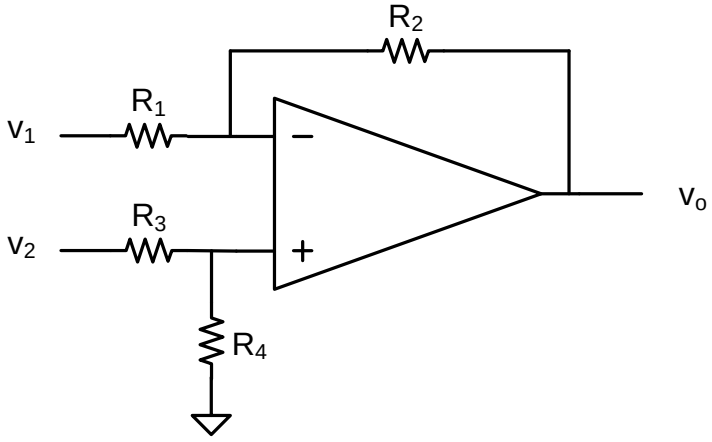
$$v_o = v_- - i R$$

$$= \tfrac{1}{2} v_2 - (v_1 - \tfrac{1}{2} v_2)$$

$$= v_2 - v_1$$

Note that another way to analyze this circuit is to use superposition. Consider input v_1 with v_2 set to zero. It becomes an inverting amplifier with $v_o = - v_1$. Then consider input v_2 with v_1 set to zero. Now it becomes a non- inverting amplifier with $\tfrac{1}{2} v_2$ at the non-inverting input. This results in $v_o = v_2$ so that the inverting input is pulled up to $\tfrac{1}{2} v_2$. Adding the two results, $v_o = v_2 - v_1$.

To implement a weighted subtractor, we use particular values for the input and feedback resistors of the subtractor to achieve the weighting.



By superposition, for v_1 alone with $v_2 = 0$,

$$v_o = -(R_2 / R_1) v_1$$

and for v_2 with $v_1 = 0$,

$$v_+ = v_2 R_4 / (R_3 + R_4)$$
$$v_- = v_o R_1 / (R_1 + R_2) = v_+$$
$$v_o = [R_4 / (R_3 + R_4)] [(R_1 + R_2) / R_1] v_2$$

Adding the separate solutions for v_1 and v_2, get

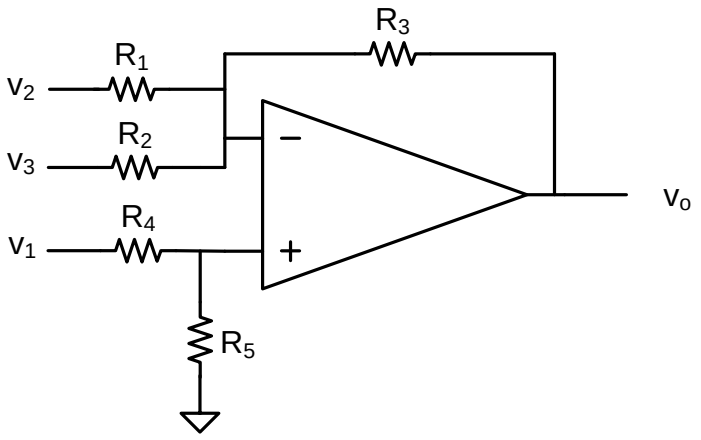
$$v_o = [R_4 / (R_3 + R_4)] [(R_1 + R_2) / R_1] v_2 - (R_2 / R_1) v_1$$

Example 18-5

Design an op amp circuit that has the output, $v_o = 3 v_1 - 2 v_2 - 4 v_3$.

Solution:

We can implement this in a number of ways. We'll use a single subtractor op amp with two input sources to the inverting input of the op amp.



By superposition, v_2 and v_3 with $v_1 = 0$ produces the output

$$v_o = -(R_3 / R_1)\, v_2 - (R_3 / R_2)\, v_3$$

For v_1 with v_2 and v_3 set to zero, we get

$$v_+ = v_1 R_5 / (R_4 + R_5)$$
$$v_- = v_o R_1 \,||\, R_2 / (R_3 + R_1 \,||\, R_2) = v_+$$
$$v_o = v_1 [R_5 / (R_4 + R_5)] / [R_1 \,||\, R_2 / (R_3 + R_1 \,||\, R_2)]$$

Combining results

$$v_o = v_1 [R_5 / (R_4 + R_5)] / [R_1 \,||\, R_2 / (R_3 + R_1 \,||\, R_2)] - (R_3 / R_1)\, v_2 - (R_3 / R_2)\, v_3$$
$$= 3 v_1 - 2 v_2 - 4 v_3$$

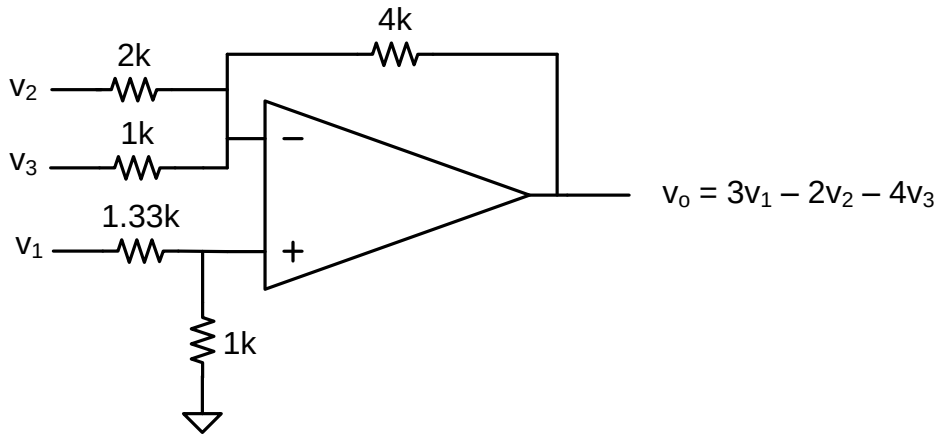
To solve, we first look at the inverted outputs and choose $R_2 = R$. Then $R_3 = 4$ R and $R_1 = 2$ R and we are left with

$$[R_5 / (R_4 + R_5)] / [R_1 \,||\, R_2 / (R_3 + R_1 \,||\, R_2)] = [R_5 / (R_4 + R_5)] / [1 / 7] = 3$$

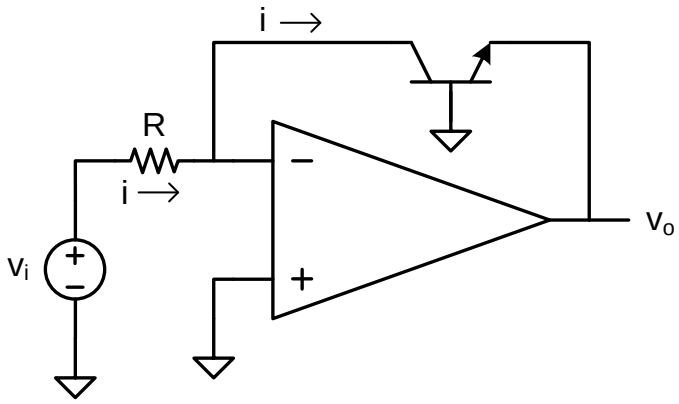
and we have

$$R_5 / (R_4 + R_5) = 3 / 7$$

If $R_5 = R$, then we have $R_4 = (4 / 3)\, R$. Choosing R = 1 kΩ, one solution becomes



A log converter can be constructed from an op amp and a bipolar transistor.



The current, i, flows to the collector of the npn transistor. The transistor is turned on by the emitter going low to about 0.6 – 0.7 V. The collector current is related to V_{BE} by

$$I_C = I_S \exp (V_{BE} / V_t)$$

where I_S is the saturation current associated with the exponential dependence of I_C on V_{BE}. This can also be written

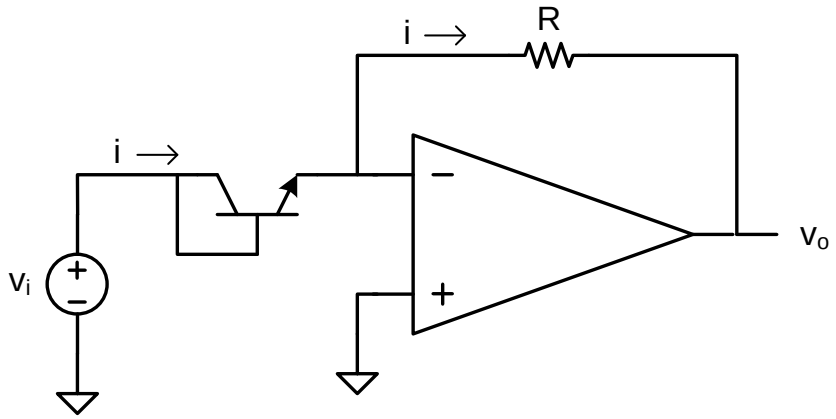
$$V_{BE} = V_t \ln (I_C / I_S)$$

So we have

$$\begin{aligned} v_o &= - V_{BE} = - V_t \ln (I_C / I_S) \\ &= - V_t \ln (i / I_S) \\ &= - V_t \ln (v_i / I_S R) \end{aligned}$$

We have at the output, a constant, $– V_t$, multiplied by the natural log of v_i over another constant, $I_S R$. These constants are necessary to set the scale of the input, v_i, since we cannot take the natural log of a voltage, and to give units to the output, v_o, since the natural log of a number has no units. The negative sign can be eliminated with an inverting amplifier. Note that the log converter is restricted to positive input voltages.

Now an anti-log converter can also be constructed.



The input, v_i, passes current through the diode-connected transistor.

$$i = I_S \exp (v_i / V_t)$$

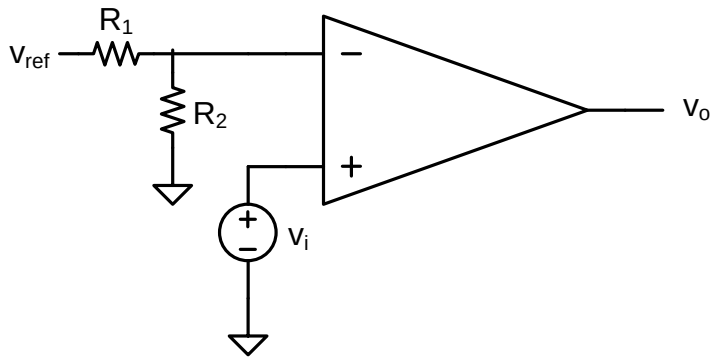
We also have

$$v_o = - i R$$
$$= - I_S R \exp (v_i / V_t)$$

and the output, v_o, depends exponentially on v_i (anti-log). Again we need constants to provide scale and units and the negative sign can be eliminated with an inverter. And like the log converter, the anti-log converter is restricted to positive input voltages

With log and anti-log converters, along with adders and subtractors, we can form series of op amps that will multiply (add logs) and divide (subtract logs) input voltages. For example, to multiply two voltages, we would generate the logs of the two voltages, then add the logs, and finally take the anti-log to produce the product of the inputs.

Two additional very frequently used op amp circuits that do not use negative feedback are the comparator and the Schmitt trigger. A comparator simply produces an output voltage that indicates whether or not an input voltage exceeds a second fixed voltage. The configuration is shown below.



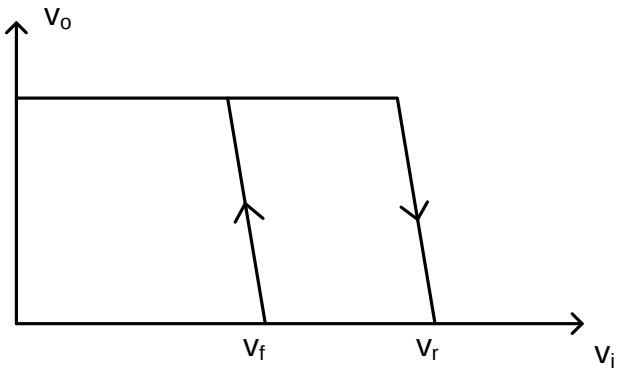
Without feedback and as much as a few millivolts difference in the inputs, the comparator output is simply the voltage limit that the op amp can deliver, usually near the supply voltages to the op amp.

The voltage at the inverting input is

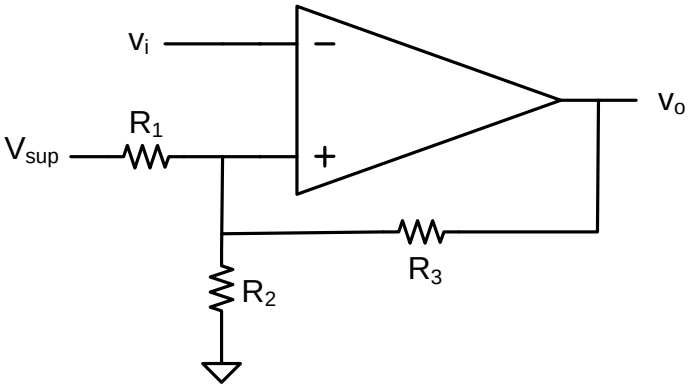
$$v_- = v_{ref} \; R_2 / (R_1 + R_2)$$

and is the critical voltage for v_i at which the output will switch between its extreme values. If the input, v_i, is greater than v_-, the output, v_o, goes to $v_{o\,max}$, the maximum output for the op amp. And if the input is less than v_-, the output goes to $v_{o\,min}$, the minimum output for the op amp.

A Schmitt trigger senses the relative level of an input signal and, like a comparator, indicates whether the input exceeds a critical voltage level. But the transition of the output for a rising input occurs at a different level than that for a falling input. The transition on a rising input is at a higher level than for a falling input. This has the effect of providing some noise immunity in the output, avoiding multiple transitions of the output when the input does not make a smooth transition through the switching voltage. The effect is called hysteresis. Below is the input/output characteristic of the Schmitt trigger.



With the output high and as the input is rising, the output falls at $v_i = v_r$. The output won't rise again until the input goes as low as v_f. This leads to a single transition as the input rises rather than repeated transitions if noise makes the input cross a single critical voltage more than once. This is the Schmitt trigger circuit.



For simplicity, assume v_o has an output range $0 \rightarrow V_{sup}$. Then for $v_o = 0$, we get

$$v_+ = [\, R_2 \,||\, R_3 \,/\, (\, R_1 + R_2 \,||\, R_3 \,) \,]\, V_{sup} = v_f$$

When $v_o = V_{sup}$, we get

$$v_+ = [\, R_2 \,/\, (\, R_2 + R_1 \,||\, R_3 \,) \,]\, V_{sup} = v_r$$

It is easy to show $v_r > v_f$ for any choice of R_1, R_2, R_3. As one example, take $R_1 = R_2 = R_3 = R$. Then

$$v_f = [\, \tfrac{1}{2} R \,/\, (\, R + \tfrac{1}{2} R \,) \,]\, V_{sup} = \tfrac{1}{3} V_{sup}$$

$$v_r = [\, R \,/\, (\, R + \tfrac{1}{2} R \,) \,]\, V_{sup} = \tfrac{2}{3} V_{sup}$$

Example 18-6

Design a Schmitt trigger that has $v_r = 0.8\ V_{sup}$ and $v_f = 0.2\ V_{sup}$.

Solution:

$$v_r = [\ R_2 / (\ R_2 + R_1 \,||\, R_3\ )\ ]\ V_{sup} = 0.8\ V_{sup}$$

$$v_f = [\ R_2 \,||\, R_3 / (\ R_1 + R_2 \,||\, R_3\ )\ ]\ V_{sup} = 0.2\ V_{sup}$$

We cancel V_{sup} to obtain

$$R_2 / (\ R_2 + R_1 \,||\, R_3\ ) = 0.8$$

$$R_2 \,||\, R_3 / (\ R_1 + R_2 \,||\, R_3\ ) = 0.2$$

We can choose one of the resistors because it is only resistor ratios that are important. Let $R_2 = 1$.

$$1 / (\ 1 + R_1 \,||\, R_3\ ) = 0.8$$

$$R_1 \,||\, R_3 = 0.25$$

$$1 \,||\, R_3 / (\ R_1 + 1 \,||\, R_3\ ) = 0.2$$

$$R_1 = 4 \bullet 1 \,||\, R_3$$

Combining the second and fourth equations,

$$(\ 4 \bullet 1 \,||\, R_3\ ) \,||\, R_3 = 0.25$$

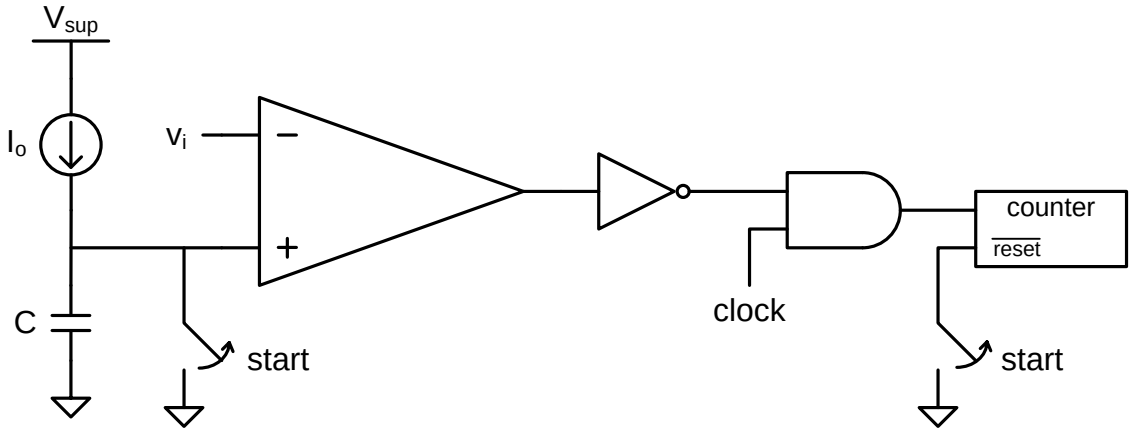
This is solved to obtain $R_3 = 1/3$. Then after some more algebra, $R_1 = 3$.

Checking: $R_2 / (\ R_2 + R_1 \,||\, R_3\ ) = 1 / (\ 1 + 3 \,||\, 1/3\ ) = 0.8$

$R_2 \,||\, R_3 / (\ R_1 + R_2 \,||\, R_3\ ) = 1 \,||\, 1/3 / (\ 3 + 1 \,||\, 1/3\ ) = 0.2$

We can multiply the values, $R_1 = 3$, $R_2 = 1$, and $R_3 = 1/3$, by any convenient resistance, say 10 kΩ, to obtain usable resistances, $R_1 = 30$ kΩ, $R_2 = 10$ kΩ, and $R_3 = 3.33$ kΩ.

For one final example of an op amp circuit, we consider an analog-to-digital converter. The ADC receives an analog voltage level and converts it to a digital signal of a certain number of bits and for some particular input voltage range. The speed of the converter is determined by the number of conversions it can make in one second. There are a number of different schemes that implement an ADC. One approach is shown below. It uses a comparator to sense when a ramping voltage signal reaches the level of the input signal that is to be converted.



The input voltage to be converted is v_i. The switches are both initially closed which discharges the capacitor and resets the counter. For $v_i > 0$, the output of the comparator is low and the input to the AND gate is high. At "start", the counter counts clock cycles at rate, r, while the capacitor charges and provides a linear voltage ramp to the non-inverting op amp input. After time, Δt, the counter has total counts, $N = r\,\Delta t$, the charge delivered to the capacitor is $I_o\,\Delta t$, and the voltage on the capacitor is $v_c = I_o\,\Delta t / C$. When v_c reaches and exceeds the level of the input voltage, v_i, the comparator output goes high and counting stops. Then we have

$$N = r\,\Delta t = r\,(v_i\,C / I_o)$$

The final digital count, N, is proportional to the input voltage, v_i. The scale between the analog level and the digital conversion is controlled by the current source, I_o, the capacitance, C, and the clock rate, r. The number of bits for the digital conversion is

$\log_2 (N_{max} + 1)$ where N_{max} is the count for $v_{i,max}$, the maximum input voltage. The maximum conversion rate is r / N_{max}.

Example 18-7

An analog-to-digital converter samples an analog level between zero and 5 V and converts to eight bits. If the capacitor used in the conversion is 0.001 μF, what minimum current source and minimum clock rate are required for 1000 samples per second?

Solution:

The capacitor must charge to 5 V in no more than one millisecond. The charge on the capacitor at 5 V is

$$Q = CV = 0.001 \times 10^{-6} \text{ F} \cdot 5 \text{ V} = 5 \times 10^{-9} \text{ Coulombs}$$

That charge is accumulated in Δt = 1ms by current, I_o.

$$5 \times 10^{-9} \text{ Coulombs} = I_o \Delta t = I_o \cdot 0.001 \text{ s}$$
$$I_o = 5 \text{ μA}$$

The clock must count to a full 8 bits = 255 decimal in the same 1 ms.

$$r = 255 / .001 \text{ s} = 2.55 \times 10^5 \text{ Hz}$$
