
THE UNIVERSITY *of* EDINBURGH

# Daybook digital system

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## Experiment 1: The Half-Adder Arithmetic Function

*06/03/2024*

This experiment aims to test one of the core operations in arithmetic. More specifically this experiment aims to construct a half adder circuit using CD4011 (quad 2-input NAND gate) and CD4030 (quad 2-input XOR gate) integrated circuits. This is a fundamental way of using budling block to add two 1-bit binary numbers. The set up shown below in figure 1.

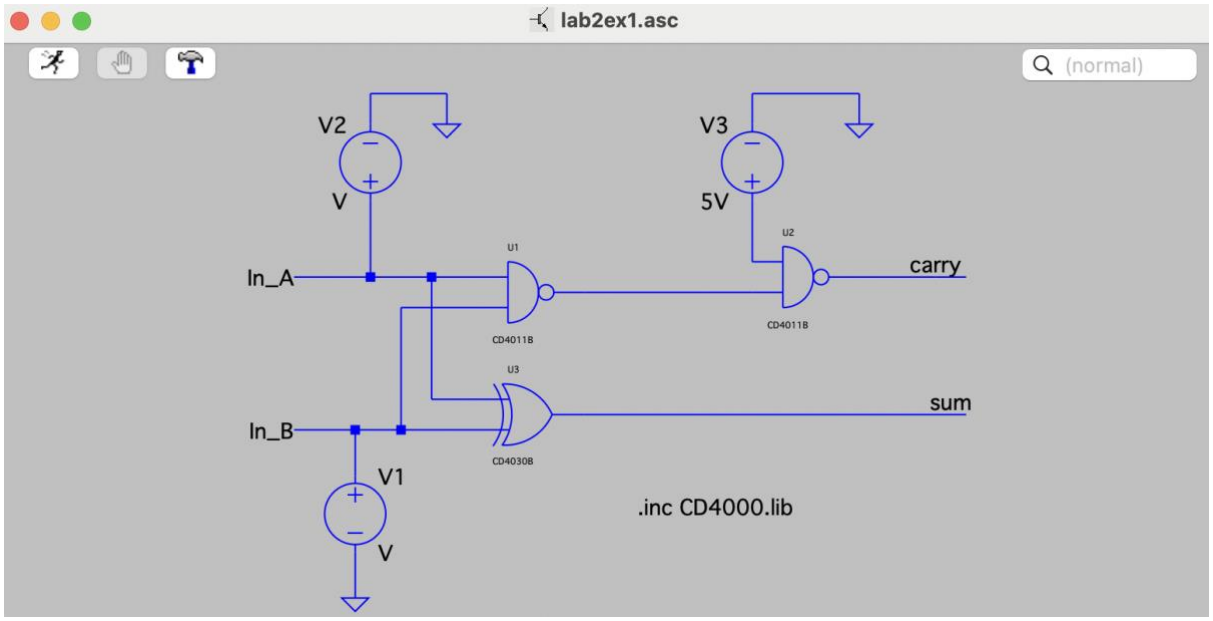


*Figure 1 set up experiment 1.*

In the truth table below, 0 represents 0V and 1 represents 5V. The experiment changes V1 and V2 to obtain the result of the experiment displayed in table 1.

*Table 1 result experiment 1.*

| V1 | V2 | SUM | CARRY |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

## Experiment 2 RS latch

*06/03/2024*

This experiment aims to investigate an RS latch. RS latches are important as they combine a NOR and NAND gates and is used for storing one bit of data. These circuit also have the ability to set and reset its output state based on the provided output.

Prior to the experiment we first set up two simple invertor which are made using a single NAND gate as shown below in figure 2.

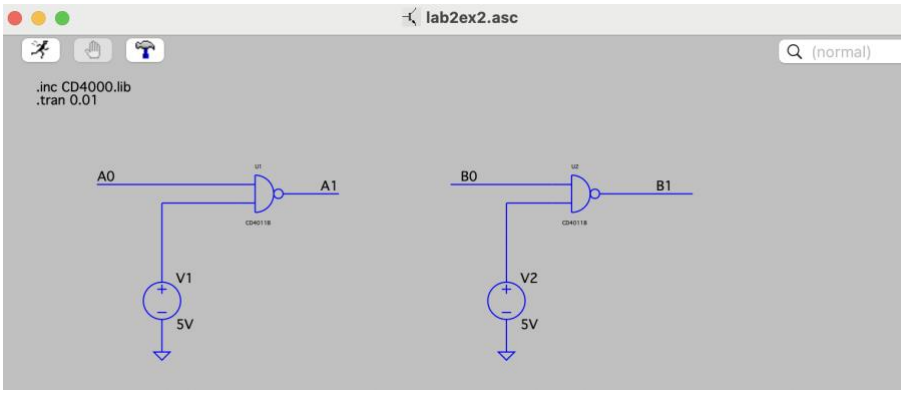


*Figure 2 Two inverter made using NAND gate.*

After setting this up like this I connected A1 and B0 to see this relationship. This circuit might be seen as useless, but they are often used as buffer. Buffers are important as they ensure a high input and a low impedance output.

After this we disconnect the connection between A1 and B0 and we connected it to create a RS latch making one of the simple latch structures. The final set up for experiment two is shown in figure 3.

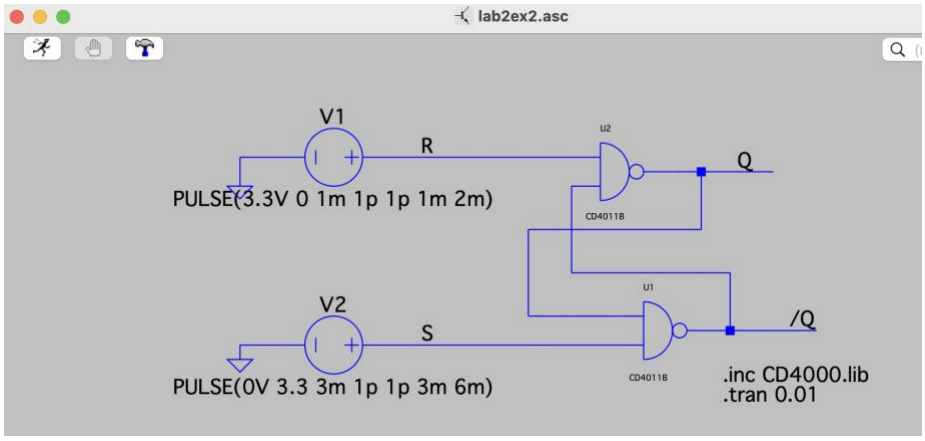


*Figure 3 Set up experiment 2 (RS latch)*

As we run the simulation changing the voltage on V1 and V2 using PWL we obtain the result displayed in table 2.

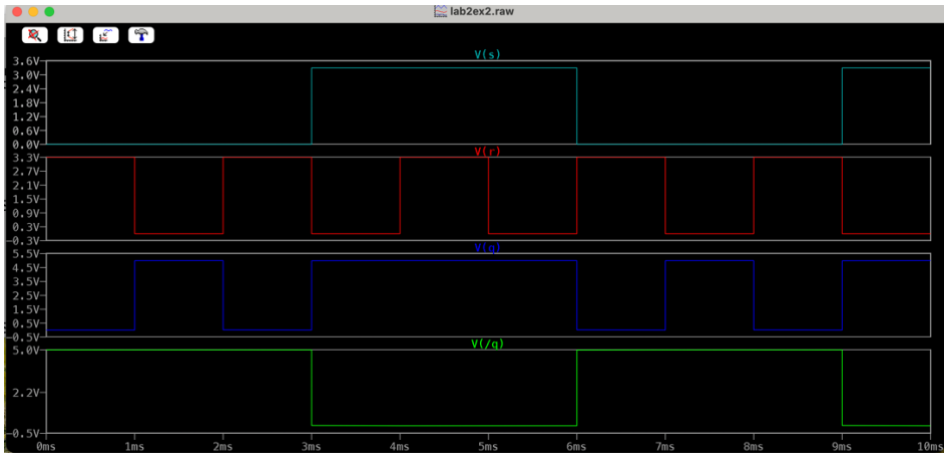


*Figure 4 Graph of experiment 2 result.*

From the result in figure 4 we can deduce the truth table shown in table 2.

*Table 2 result experiment 2.*

| V1 (R) | V2(S) | Q | /Q |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |

The truth table shows the RS latch working correctly. When invalid inputs are inputted R=1 and S=1), the latch remains it the state it was in previously. As shown by outputs Q and /Q which show to be at 0. In addition, when the latch has both input at o the state is also maintained. If the simulation begins with both inputs as 1, he latches would switch between states to do the lack of reference of any previous state and that's why set has to come first. These concepts are depicted in the diagram in figure 5 below.

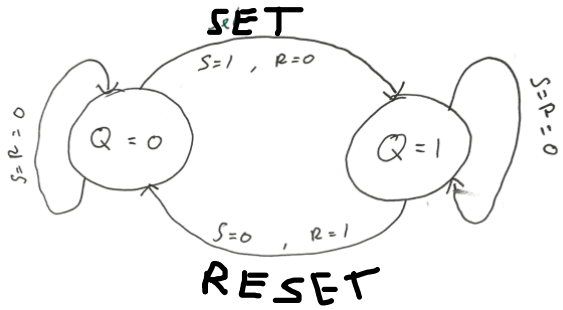


*Figure 5 State diagram RS latch.*

## Experiment 3: The D latch

*06/03/2024*

In this experiment we are modifying the RS latch into a D latch ensuring that changes to R and S only affect the latch's state when the enable signal is high. In a D latch when the enable input is low (disabled) the D latch holds its current state regardless of its input. When it is enabled, it updates its state based on the D input. The set up for the first part of this experiment is shown in figure 4.

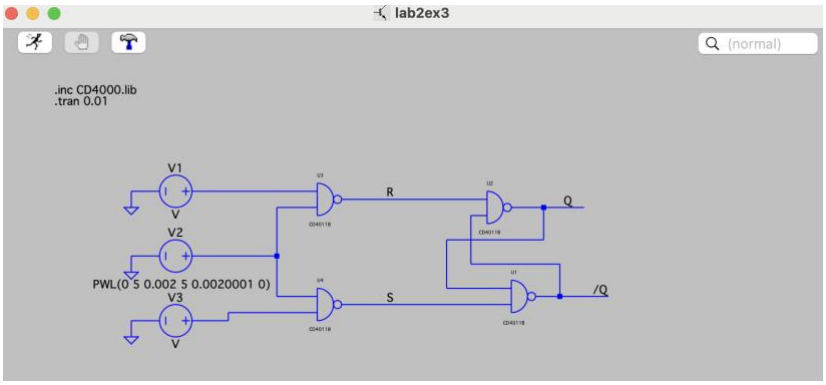


*Figure 6 D latch experiment 3.*

*Table 3 Result experiment 3.*

| S | R | Enabled/ disabled | Q | /Q |
|---|---|---|---|---|
| 0 | 0 | 0 | - | - |
| 0 | 0 | 1 | - | - |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

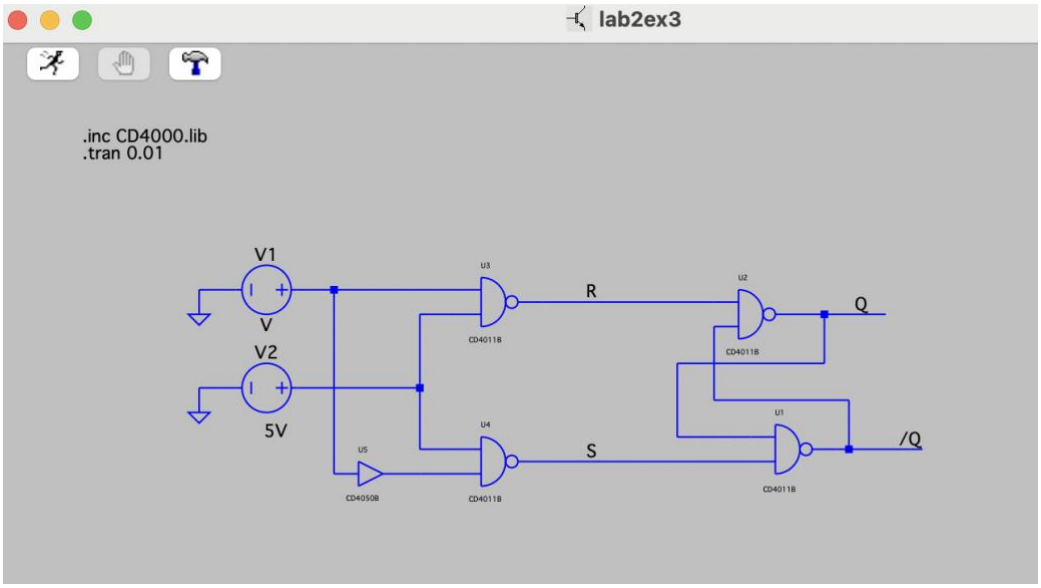


*Figure 7 D-latch using an inverter.*

*Table 4 Result of experiment 3 using the inverter.*

| S/R | Enabled or disabled | Q | /Q |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

## Experiment 4

*06/03/2024*

Experiment 4 looks at the properties of a D flip flop as an integrated circuit. It will aim to compare this to the D latch constructed in experiment 3. It will also investigate the propagation delay, set and hold time that takes place when connecting 2 D Flip-Flop together. After doing the simple D flip-flop simulation we connect a second one together. The set up for this is shown below in figure 8.

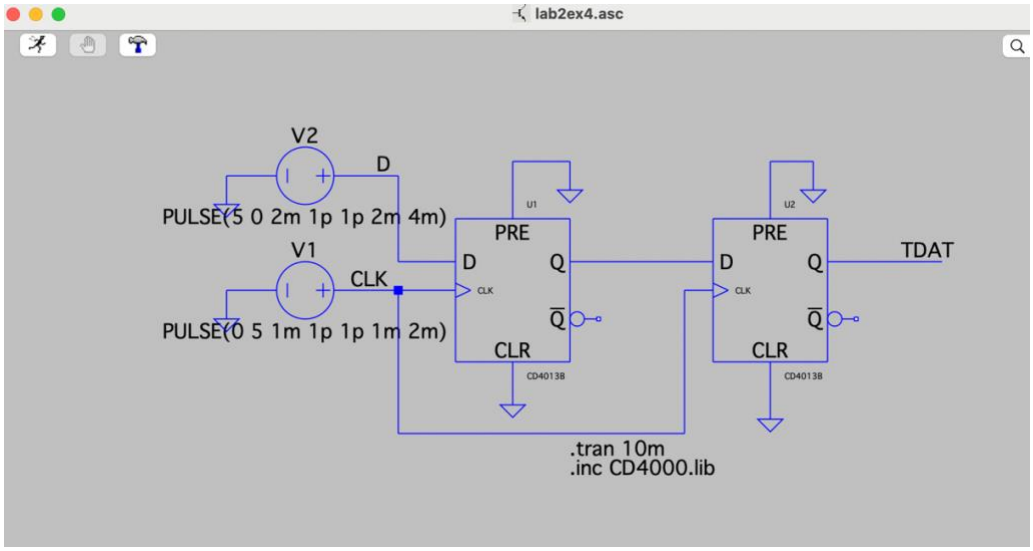


*Figure 8 Experiment 4 set up.*

And when running the simulation, we can observe the graph in figure 9.

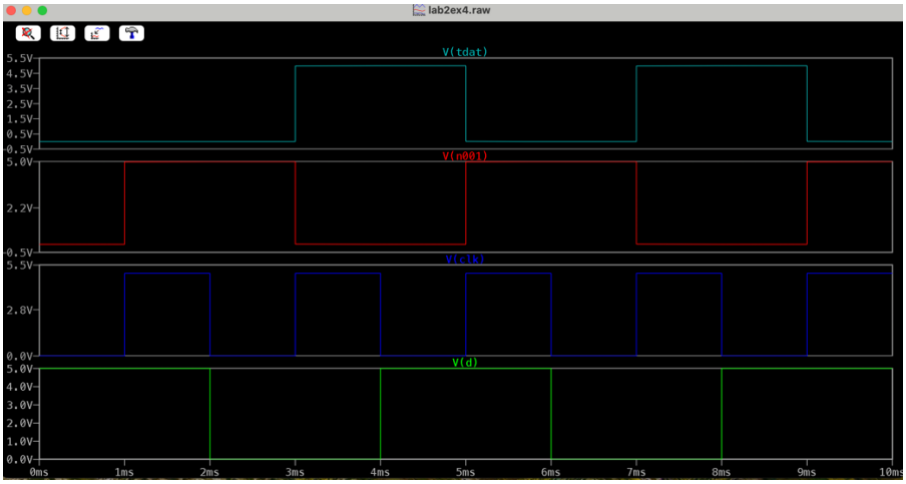


*Figure 9 Experiment 4 results.*

Using this we can zoom in to find the propagation delay. This is better shown in figure 10.

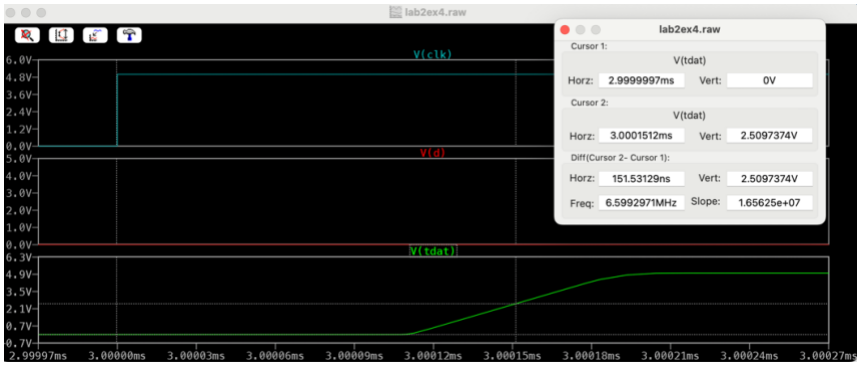


*Figure 10 Propagation delay.*

By looking at the positive end of the clock and measuring the time for the 50% mark. The propagation delay is found to be 151.5ns.

For the set and hold time it is not possible to obtain them from a functionality of LTspice. However, it is possible to find them by trial and error.

We can first set the delay to 100ns and observe the following results.

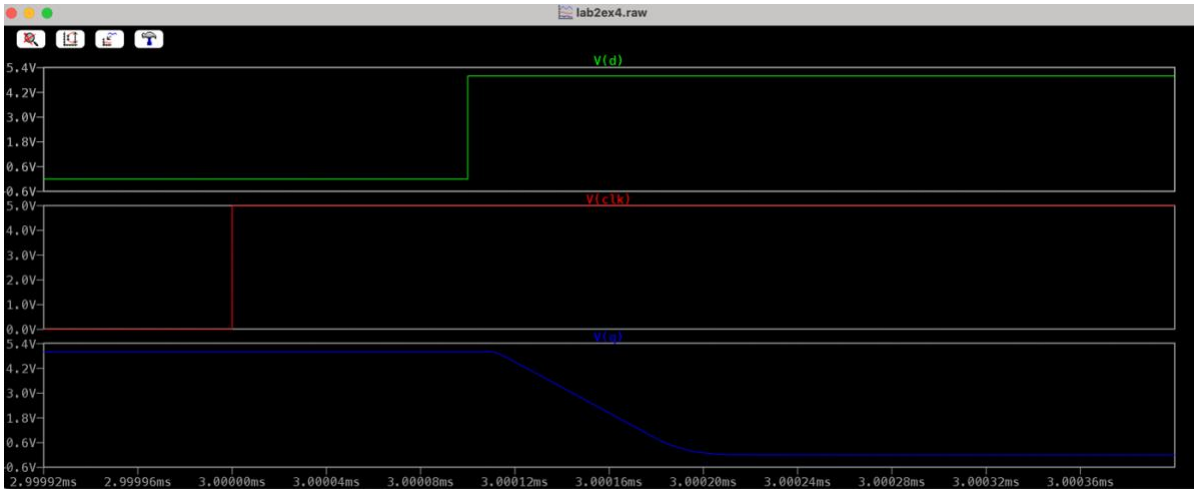


*Figure 11 Delay of 100ns.*

As we can see in this everything is working correctly, and the output is displayed as the rising edge of the clock. When changing the delay time to 10ns we observe the graph shown in Figure 12.

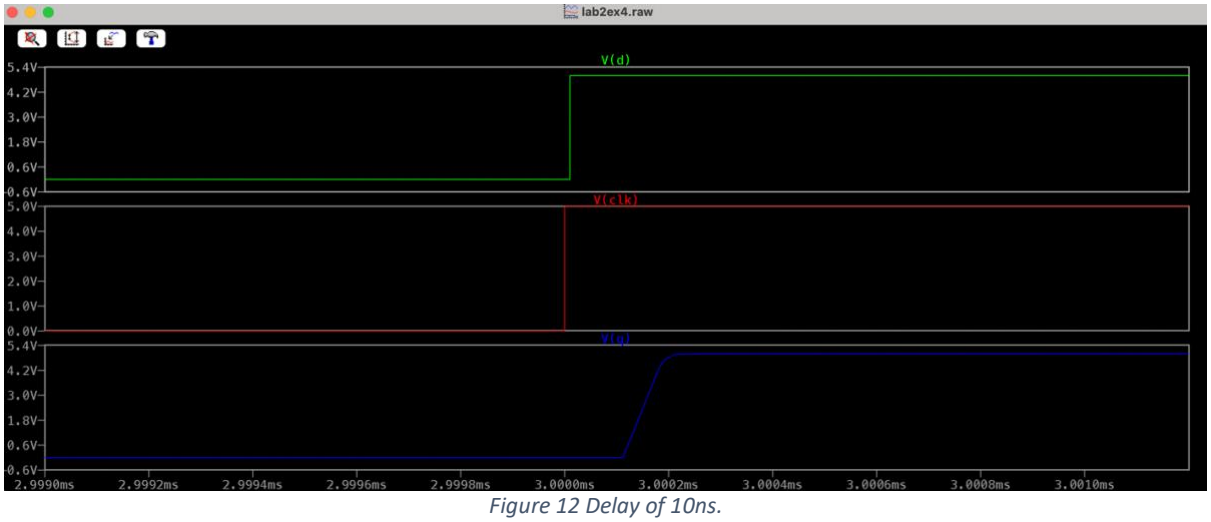


*Figure 12 Delay of 10ns.*

We can see from figure 12 that the rising edge of the clock is still before the input change (when D is low) but the output changes to high. Showing a hold time violation. Therefore, we can deduce that the hold time has an order of magnitude of 10ns.

Finally, the set time cannot be found from this simulation despite numerous attempts of setting the delay to 1fs.

## Experiment 5 Shift register

*06/03/2024*

From the knowledge of experiment 4 and prior ones we are now aiming to construct a 4-Bit shift resistor using logic. By applying the same logic, we can get the graph shown below in figure 13.

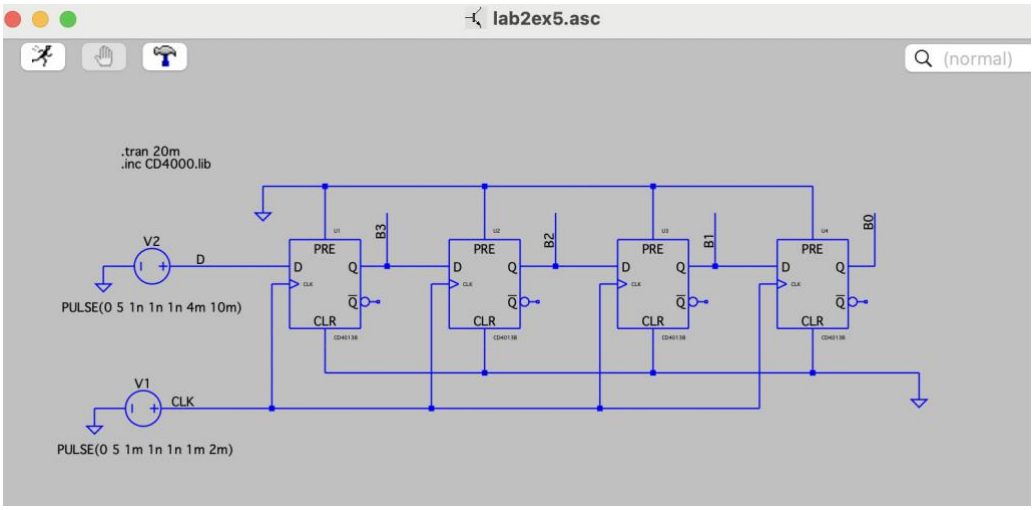


*Figure 13 Experiment 5 set up.*

And by running this simulation we obtain the result below. (LTspice crashed when adding more than 5 plot so I had to do them separately but the two were taken when running the same circuit.)

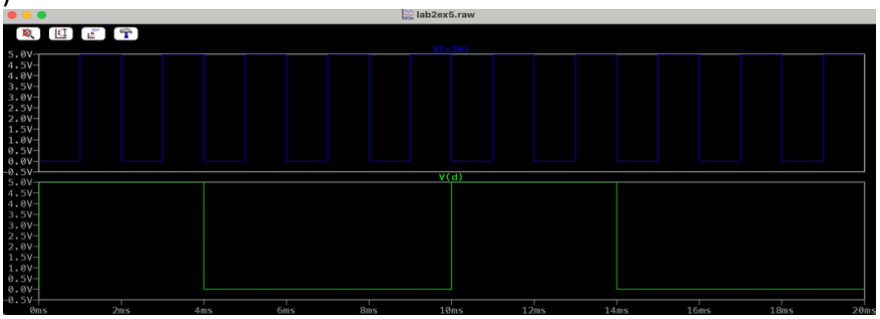


*Figure 14 Clock and D input graph.*

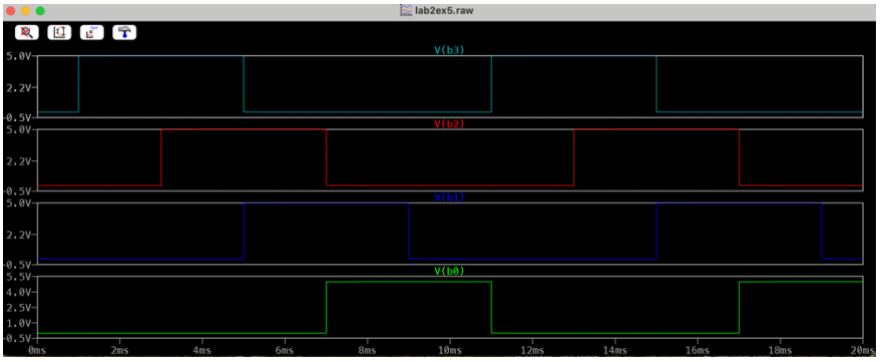


*Figure 15 Outputs of experiment 5.*

In order to demonstrate my knowledge and expand my interest I tried to investigate a 8-Bit shift register and the set-up is shown below.

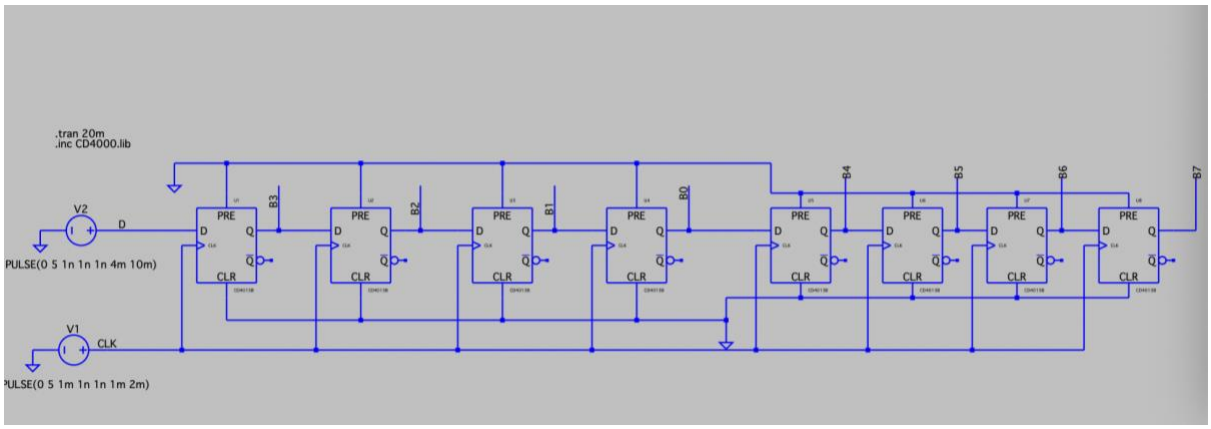


*Figure 16 8-Bit shift register set up.*

And when running this simulation obtained the following.

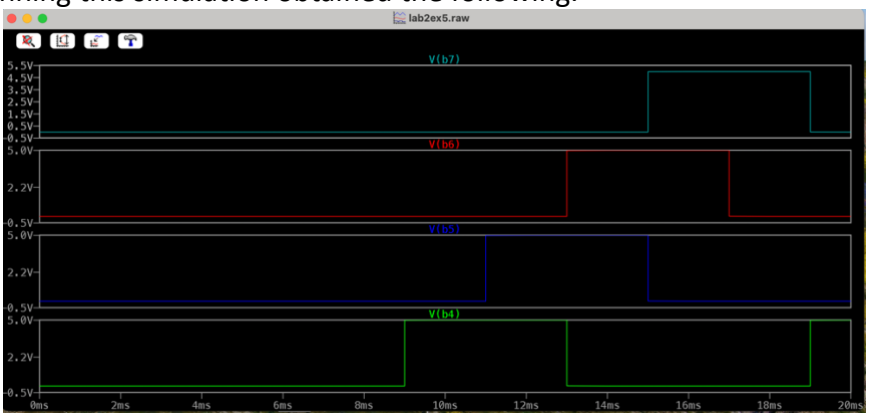


*Figure 17 Result experiment 5 8-Bit shift register.*

Figure 17 shows the result of the 4-Bit part that have been added. When researching into the graphs and especially when comparing it to the other signal. By looking at all of this we can conclude that increasing the size of the shift resistor does not have an impact on the delays in the circuit. It can be assumed that in real life delay can be introduced due to interference or natural capacitance.