THE UNIVERSITY *of* EDINBURGH

Daybook digital system

Lucas Salhani (s2235848)

February 7, 2024

1 Lab 1 week 3

1.1 Setting up

31/01/2024

During the first lab we set up LTspice. Because of some mac issues the CD4000 document did not show up when opening LTspice. The tutor was not able to fix this issue and I decided to come again for the lab taking place the next day as advised by one of the tutors
01/02/2024

In this session one of the tutors managed to understand and solve my problem and I could start the exercises. The library ".inc CD4000.lib" is included for Ltspice to know where to find the information for the chip to run.

1.2 Experiment 1

01/02/2024

In this experiment, we are looking at the voltage transfer characteristic and logic transition threshold. To do this we are using the CD4000 library that we downloaded earlier. This allows us to use a CMOS NAND gate which has been simplified in a three-pin chip. We have two input pins which we connect to 5V (high) and another one is connected to a PWL signal which we set up as seen in Figure 1. As we run the simulation for 0.3 seconds we obtain the graph in figure 1.

Using this graph we can find out the threshold voltage by looking at the intersection. By zooming in and using the cursor on LTspice we can find out the threshold voltage to be at 2.4999869V which occurs at 4.9999739ms as shown in figure 2, when comparing this to the data sheet (can be found in figure 1 Typical voltage transfer characteristic) we find a value of 2.5V. This concludes a good accuracy found exper-

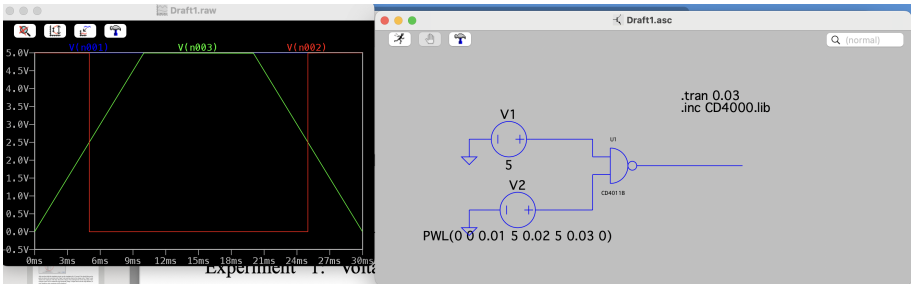

Figure 1: picture of graph and circuit

imentally. It can also be added that the the threshold voltage is happening at 4.5 and 24.5ms respectively.

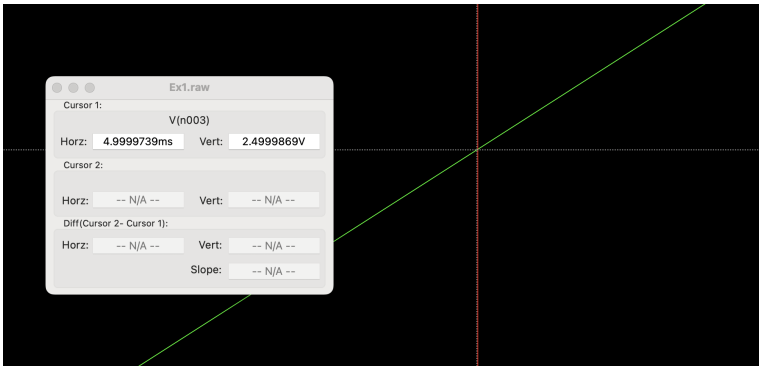

Figure 2: Threshold voltage

1.3 Experiment 2

01/02/2024

This experiment looks at the rise and fall time for the CD4011B. The PWL has been commanded to use times of 0.1×10^{-10} and 0.2×10^{-10}. This is done so the voltage transition time is reduced and easy to compare with he rise time and fall time. Running the simulation gives us the graph shown in Figure 3. The next step is to look at the time it takes for the signal to go from 10% to 90% of the

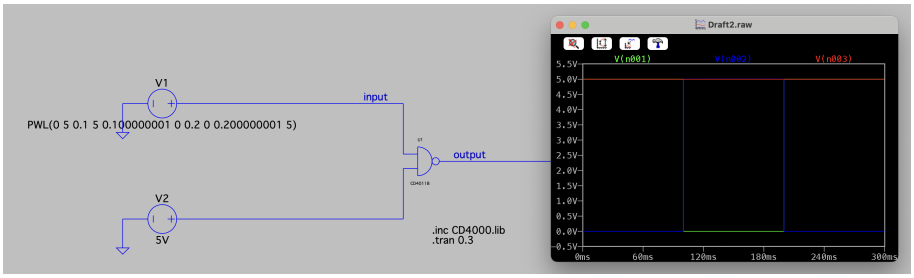

Figure 3: Rise and fall graph

The settings for the PWL are listed in table 1. As the transition time is very small compared to the run time of the experiment the graph can be very misleading until we significantly zoom in to find the rise and fall graphs and allow us to gather values.

Time[s]	Value[V]
0	5
0.1	5
0.10000001	0
0.2	0
0.20000001	5

Table 1: Settings for the PWL

Figures 4 and 5 show the rise and fall respectively. Using the LTspice cursor we are able to find the transition time. As we look at the Datasheet (Fig. 6) we can see that the typical transition time at 5 volts is 100ns. When comparing this to the result gathered in the simulation we can see that they are much lower. 65.7ns and 65.9ns respectively.

It can be concluded that the times were significantly slower due to the fact that we were running a simulation and the simulation was creating near-ideal conditions. When running experiments in real life other components could affect this which it is not sure that the program takes into account

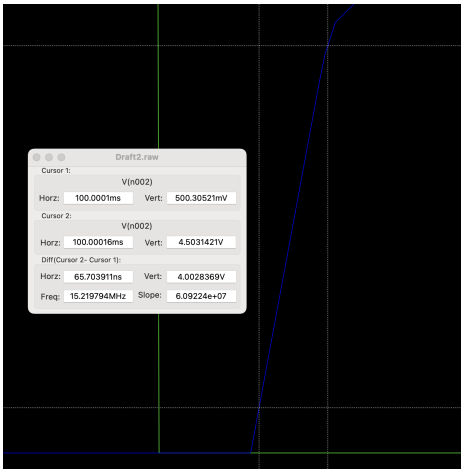

Figure 4: Graph for rise time

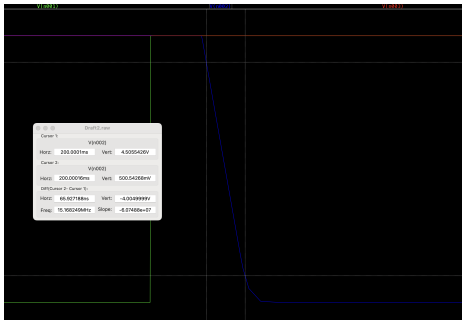

Figure 5: Graph for fall time

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	125	250	ns
	10	60	120	
	15	45	90	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

Figure 6: Data sheet (Dynamic electrical characteristics)

1.4 Experiment 3

01/02/2024

Using the same circuit from experiment 2 we are now looking at the propagation delay. The setup is the same as for experiment 2. Using the cursor I have found the propagation delay to be 127.49516ns which is a bit longer than the time of 100ns found in the datasheet in Fig.6 but this is still in between the typical and the max.

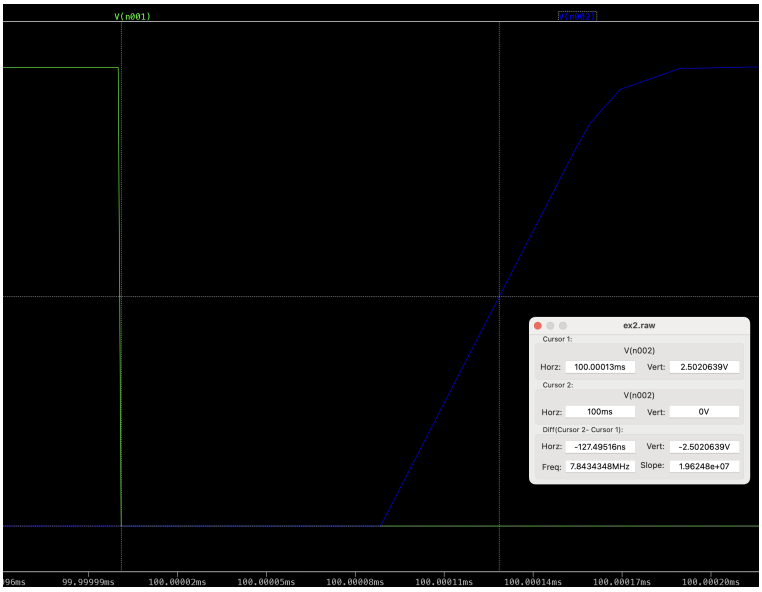

Figure 7: Propagation delay

1.5 Experiment 4

01/02/2024

In this experiment, we are investigating a logic gate and creating a truth table to figure out how it operates.

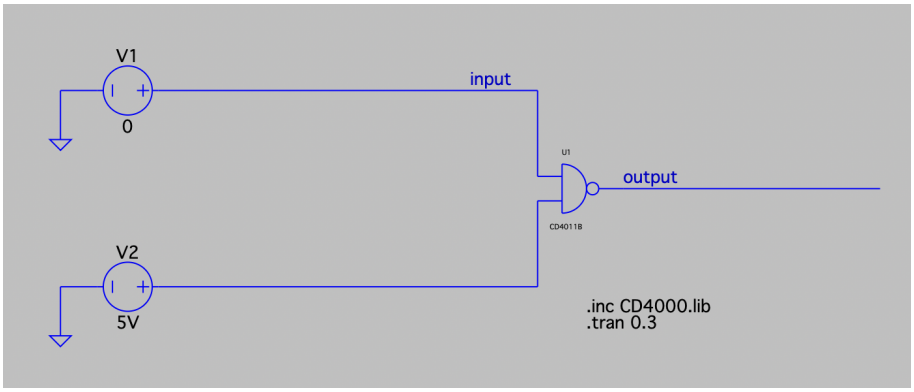

Figure 8: Propagation delay

In Figure 8 we can see the circuit used to test the logic gate. We then simulated 0 and 1 using 0 and 5 volts respectively on V1 and V2.

V1	V2	Output
1	1	0
1	0	1
0	1	1
0	0	1

Table 2: Truth table for logic gate

The truth table (table 2) tells us that the CD4011B operates as a NAND gate as it is the opposite of an AND gate.

1.6 Experiment 5

01/02/2024

This experiment aims to construct a 3-bit XOR function and how it acts as we scale it for N bit. To explore this we will construct a truth table looking at all the possibilities to explore when the output is high. The results found are displayed in the table below(Table 3).

S1	S2	S3	Output
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	1
0	1	1	0
0	1	0	1
0	0	1	1
0	0	0	0

Table 3: Truth table for experiment 5

Looking at this table it is possible to conclude that when N is an even number the output will be 0 and for odd numbers it will be high (represented as a 1 but it is 5 volts in the simulation).