Leandro Saraco

Software Engineer - Artificial Intelligence

Software Engineer with 6+ years of experience developing software for a semiconductor company. Combining my electronic and programming skills to provide high quality EDA (Electronic Design Automation) software that significantly reduce manual efforts during the design of an integrated circuit. I am used to work with teams worldwide, in any timezone.

Linkedin: https://linkedin.com/in/leandrosaraco
Github: https://github.com/lsaraco

Contact

Email: leandrosaraco@gmail.com
Phone number: +541165939794
Location: Buenos Aires, Argentina
Date of birth: 09/18/1995
Citizenship: Argentina, Italy (EU)

Skills

- **Languages:**
  - C
  - C++
  - Python
  - Verilog
- **Technologies / Frameworks:**
  - Pandas
  - Scikit-Learn
  - Pytest
  - Airflow
  - Metaflow
  - OpenCV
  - Docker
  - AWS
- **Database:**
  - PostgreSQL
  - MongoDB
- **Other tools:**
  - Postman
  - Jira
- SVN:
  - Git
  - Gitlab
  - CI/CD

Language

English: Proficient. TOEIC Certified.

Spanish: Native.

Experience

2022 - Present
Allegro Microsystems
Automation - Mixed Signals Verification Engineer

- Enhanced verification infrastructure by building custom python scripts for regressions.
- Automated testcases using coverage-driven verification with randomization.
- Experience building CNNs and RNNs for automatic signal classification.
- Developed microservices with REST APIs using FastAPI for efficient communication.
- Built software to auto detect anomalies on simulation log files using neural networks..
- Analysis and failure detection of inductive and position sensors for electric vehicles.
- Automatic reports using APIs (for example to Gitlab or Jama).
- Scrum Agile methodology.

- **Tech stacks:** Python, Machine Learning, docker, AWS, CNN, Git, CI/CD, Jira.

2018 - 2022
Allegro Microsystems
Sr. Layout Engineer / Software developer

- Software developer for IC Layout generation and automation during 4+ years, using C, C++ and Python for EDA (Electronic Design Automation).
- Developer of a software to validate layouts in a batch fashion and run several tests which include DRC (Design Rules), LVS, PERC, ESD and parasitic simulations.
  - Project duration: 2 years.
  - Now used among all layout engineers of the company to verify their designs.
- Integration of layout development flow with Gitlab (Cadence <-> Gitlab integration).
- Benchmark and analysis of Cadence and Siemens software used for simulation.
- Automated QA verification of hardware simulation tools written in Python and C++.

- **Tech stacks:** Python, C, C++, Pytest, Cadence Skill, Lisp.

Education

2024 - Present
Universidad de Buenos Aires (UBA)
MS Artificial Intelligence

- Courses completed: probabilistic, data analysis, machine learning, computer vision, MLOps, deep learning, natural language processing (NLP), and time series analysis.
- Achieved an average score of 9/10 in the first year.

2014 - 2020
Universidad Tecnológica Nacional (UTN FRBA)
BS Electronic Engineering

- Six-year degree (BS + MS equivalent).
- Score: 8.96 / 10