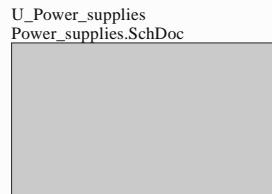
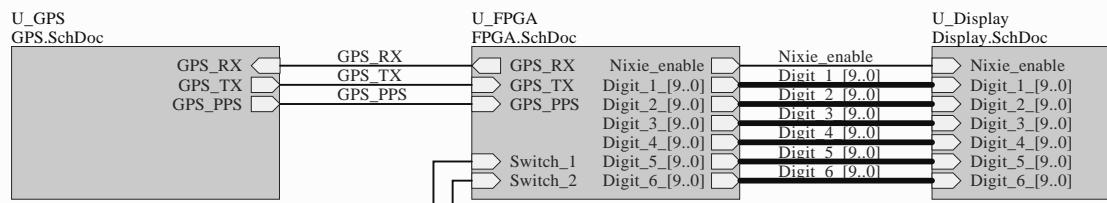


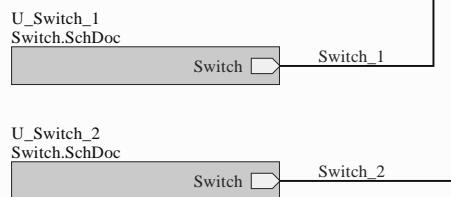
A



B



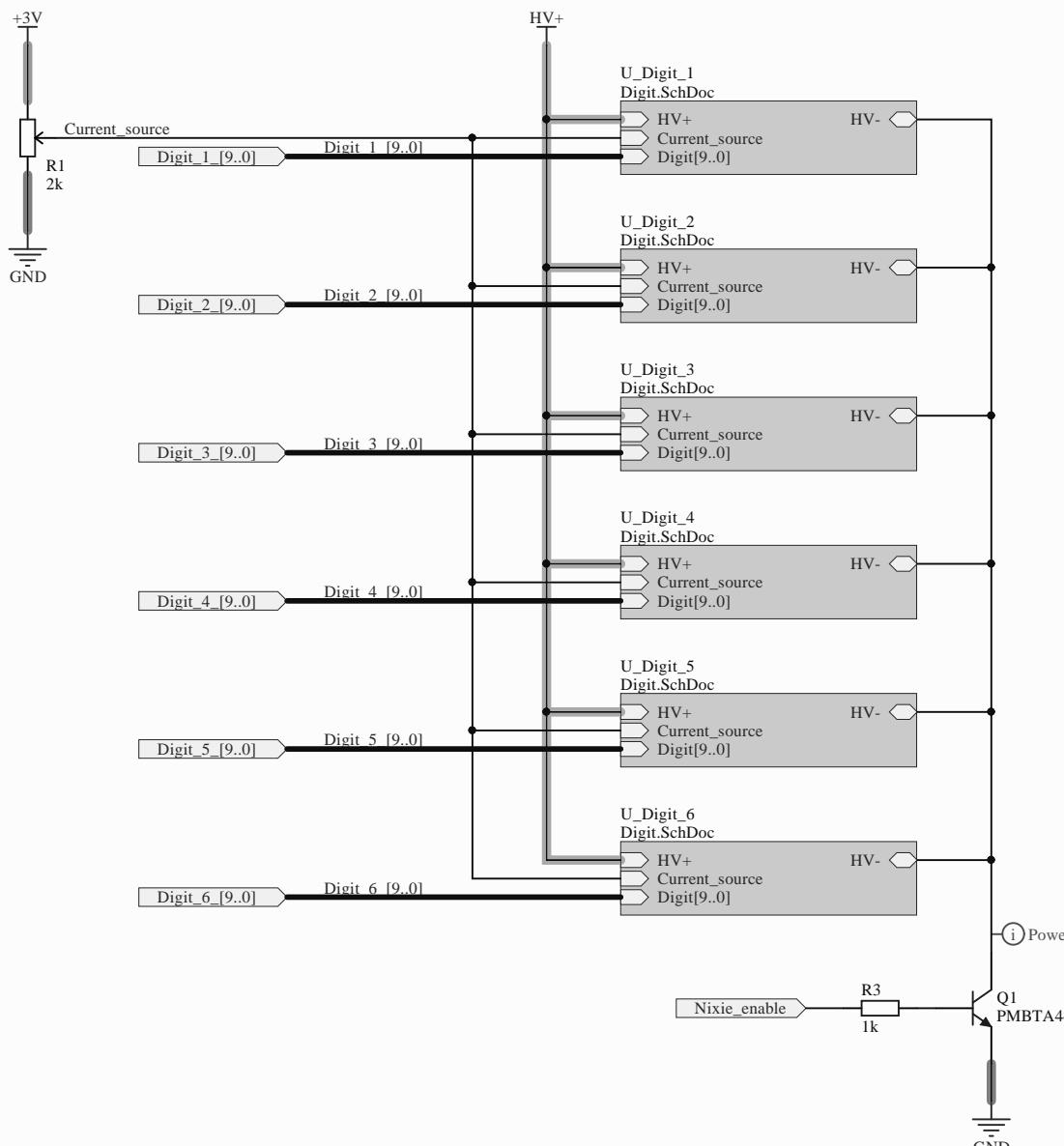
C



D

Title <i>Nixie top level</i>			L. Sartory
Size: A4	Number:1	Revision:A1	<i>Nixie clock with GPS synchronization</i>
Date: 02.03.2018	Time: 14:44:52	Sheet1 of 14	Altium
File: D:\Misc\Nixie\Schematics\Nixie_top.SchDoc			

A



B

C

D

A

B

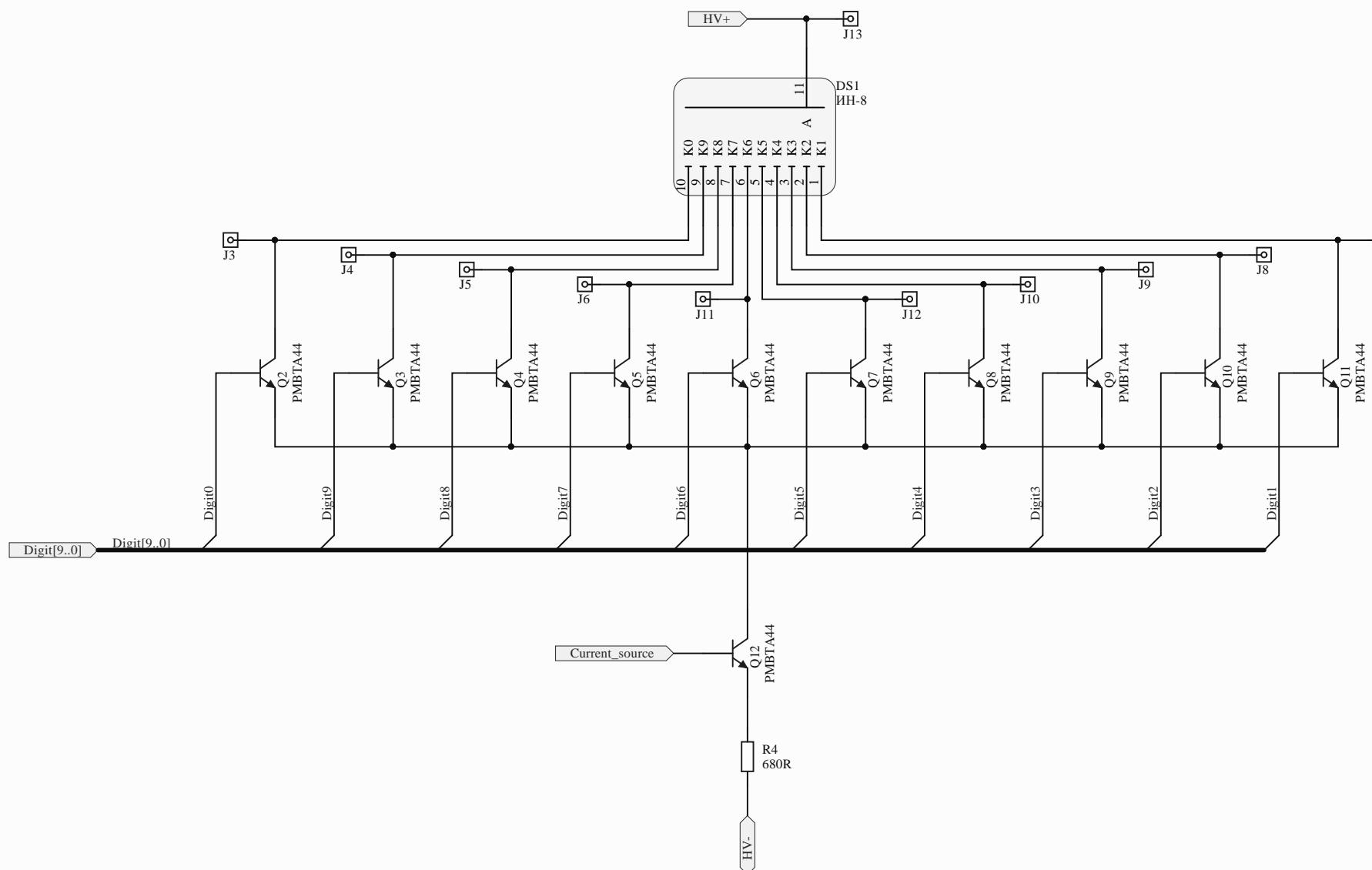
C

D

Title <i>Nixe display array</i>		
Size: A4	Number: 2	Revision: A1
Date: 02.03.2018	Time: 14:44:52	Sheet2 of 14
File: D:\Misc\Nixie\Schematics\Display.SchDoc		

L. Sartory
Nixie clock
with GPS synchronization

Altium



Title **Single Nixie digit**

Size: A4	Number: 3	Revision: A1
Date: 02.03.2018	Time: 14:44:52	Sheet 3 of 14
File: D:\Misc\Nixie\Schematics\Digit.SchDoc		

L. Sartory
Nixie clock
with GPS synchronization

Altium

A

A

B

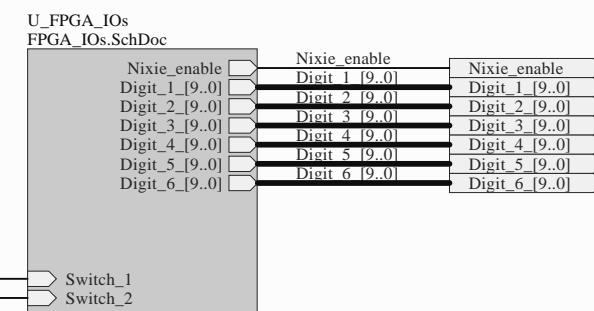
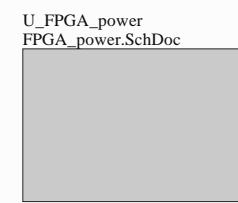
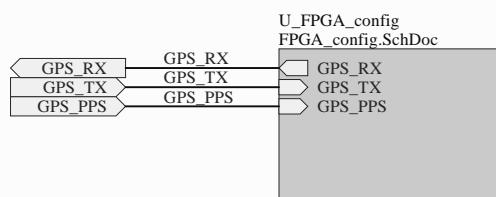
F

6

6

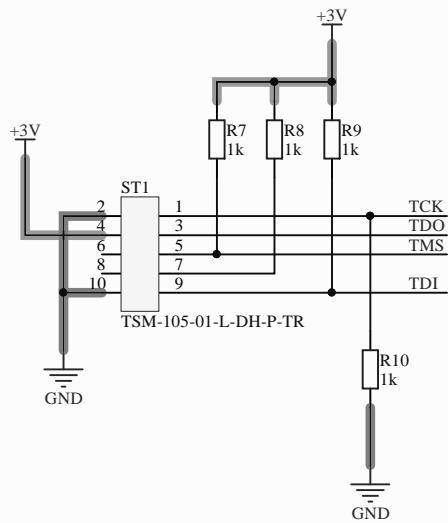
1

1

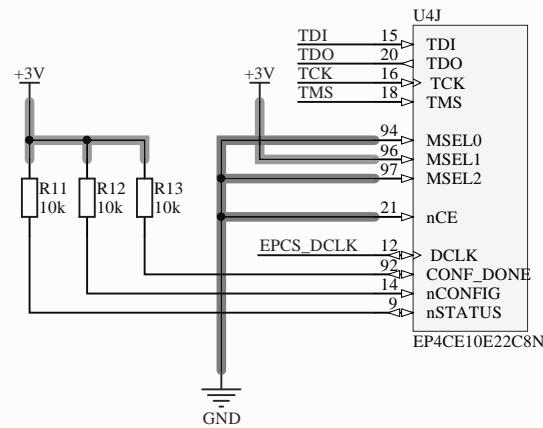


Title FPGA top level			<i>L. Sartory</i>	
Size: A4	Number:4	Revision: A1	<i>Nixie clock with GPS synchronization</i>	
Date: 02.03.2018	Time: 14:44:52	Sheet 4 of 14		
File: D:\Misc\Nixie\Schematics\FPGA.SchDoc				

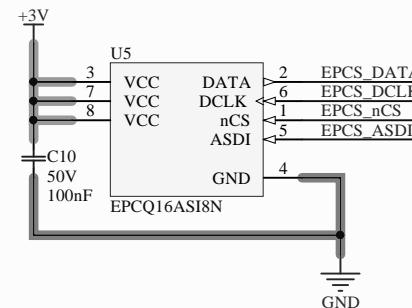
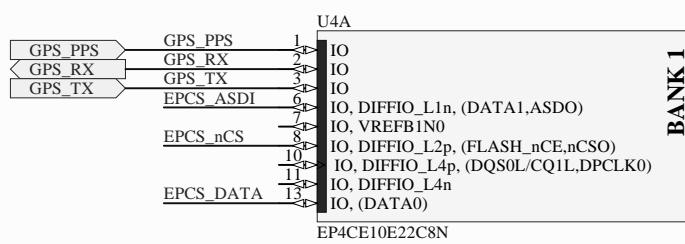
A

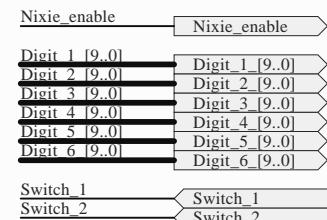
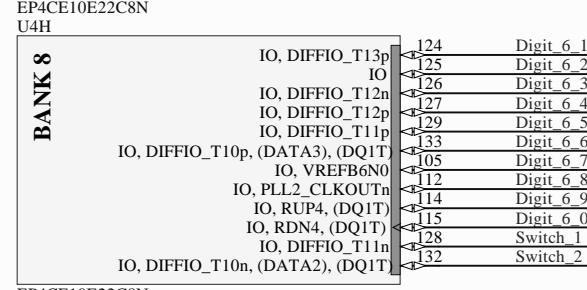
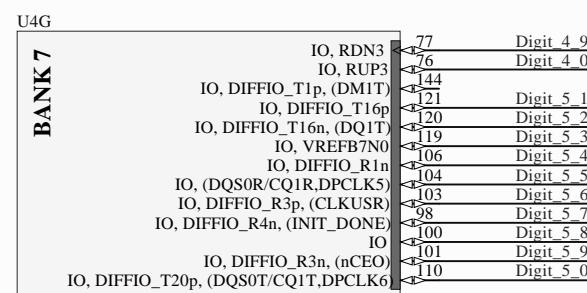
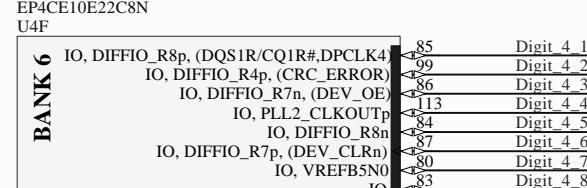
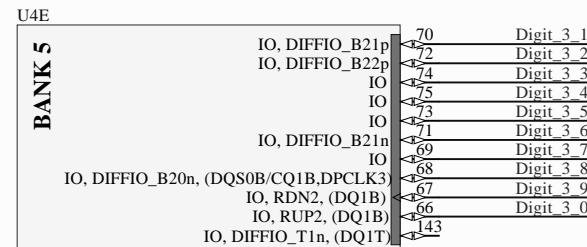
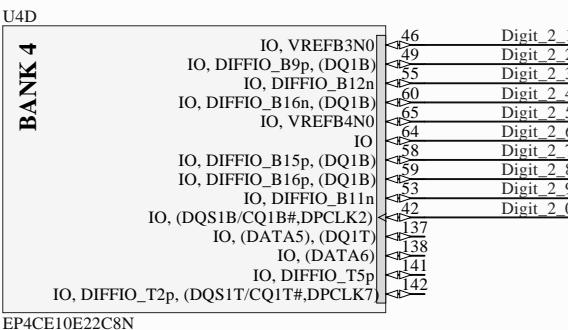
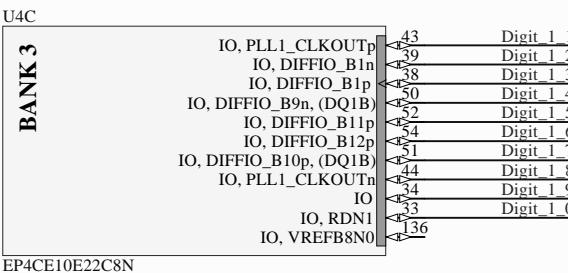
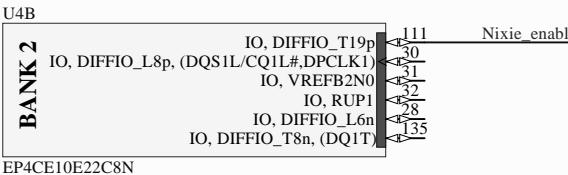
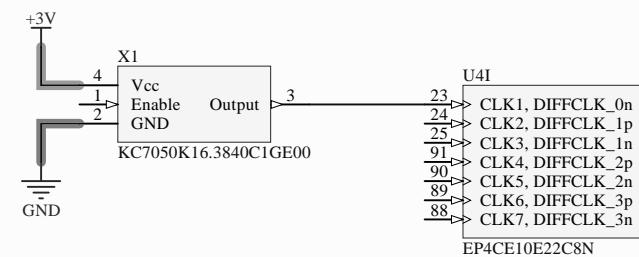


B



C



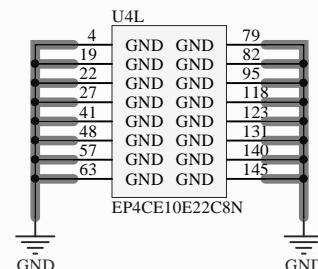
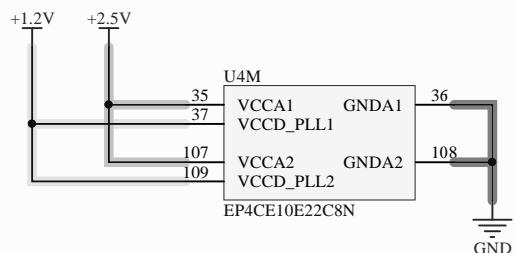


Title FPGA I/Os		
Size: A4	Number: 6	Revision: A1
Date: 02.03.2018	Time: 14:44:52	Sheet 6 of 14
File: D:\Misc\Nixie\Schematics\FPGA_IOs.SchDoc		

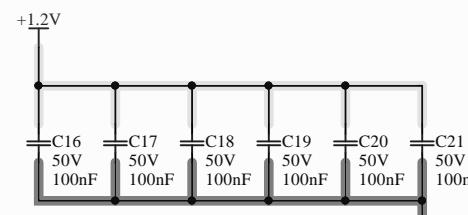
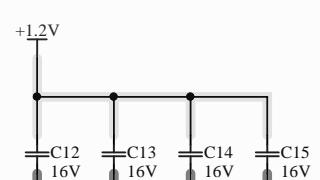
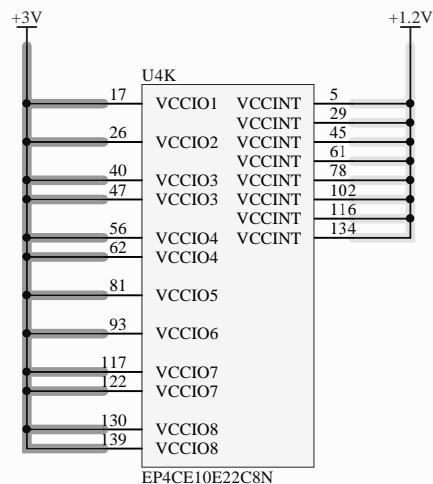
L. Sartory
Nixie clock
with GPS synchronization



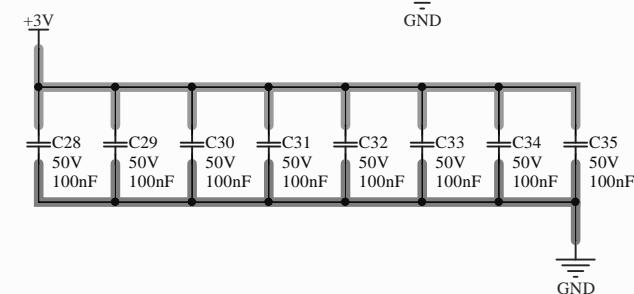
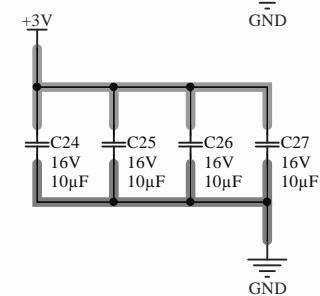
A



B



C



D

Title **FPGA power supply**

Size: A4	Number: 7	Revision: A1
Date: 02.03.2018	Time: 14:44:52	Sheet 7 of 14
File: D:\Misc\Nixie\Schematics\FPGA_power.SchDoc		

L. Sartory

Nixie clock
with GPS synchronization**Altium**

A

A

B

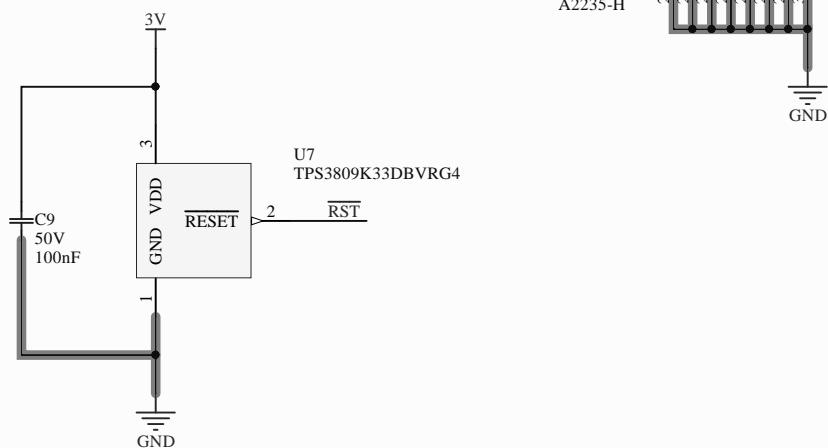
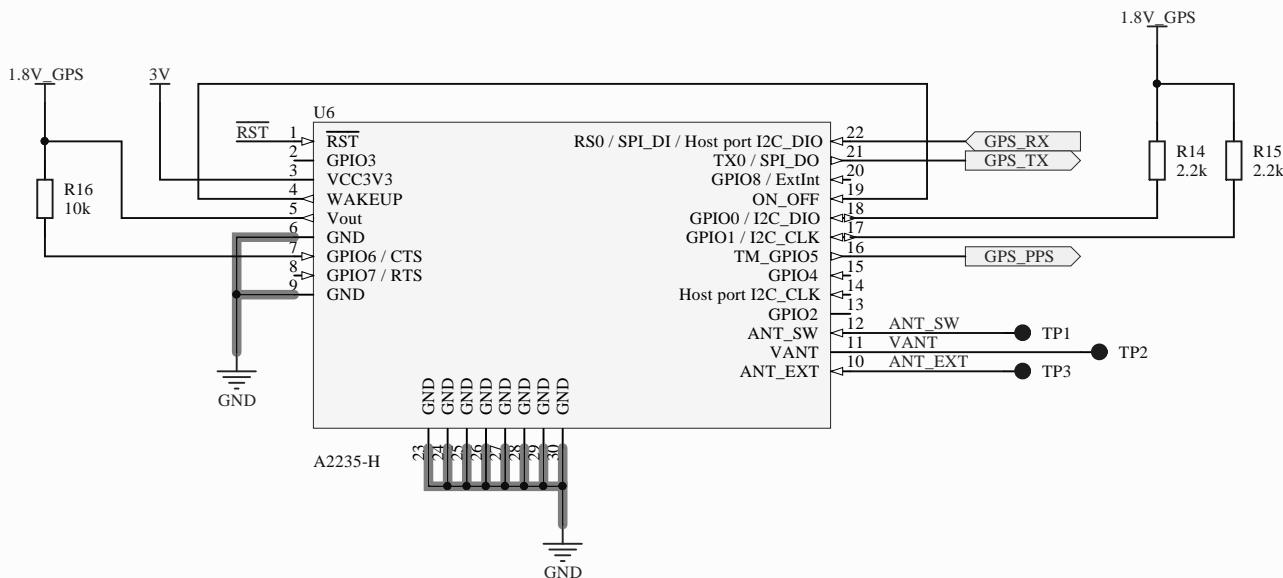
B

C

C

D

D

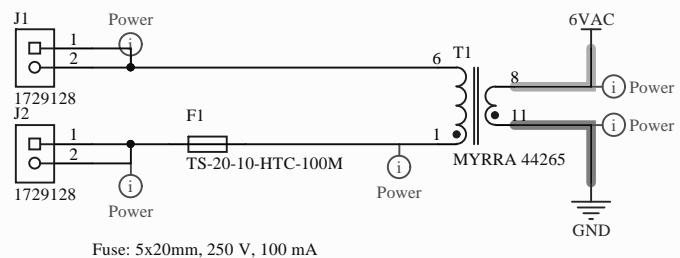
Title **GPS module**

Size: A4	Number: 8	Revision: A1
Date: 02.03.2018	Time: 14:44:52	Sheet 8 of 14
File: D:\Misc\Nixie\Schematics\GPS.SchDoc		

L. Sartory

Nixie clock
with GPS synchronization**Altium**

A



B

C

D

U_3_0V_regulator
3.0V_regulator.SchDoc

U_2_5V_regulator
2.5V_regulator.SchDoc

U_1_2V_regulator
1.2V_regulator.SchDoc

U_HV_supply
HV_supply.SchDoc

Title **Power supplies top level**

Size: A4	Number:9	Revision:A1
Date: 02.03.2018	Time: 14:44:52	Sheet9 of 14
File: D:\Misc\Nixie\Schematics\Power_supplies.SchDoc		

L. Sartory
Nixie clock
with GPS synchronization



A

A

B

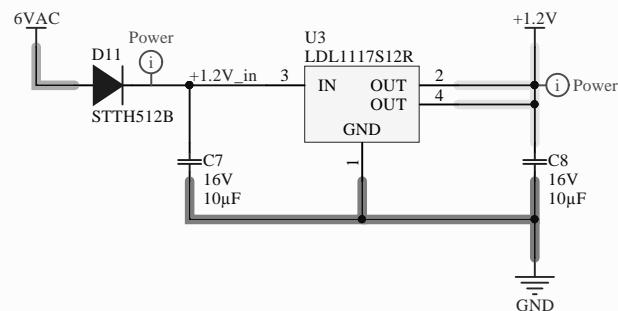
B

C

C

D

D



Title 1.2V FPGA power supply		
Size: A4	Number:10	Revision:A1
Date: 02.03.2018	Time: 14:44:52	Sheet10 of 14
File: D:\Misc\Nixie\Schematics\1.2V_regulator.SchDoc		

L. Sartory
Nixie clock
with GPS synchronization

Altium

A

A

B

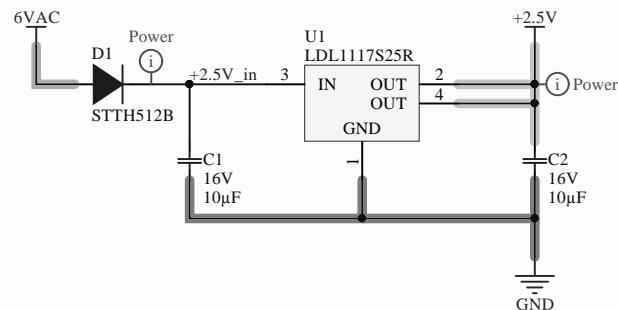
B

C

C

D

D



Title 2.5V FPGA power supply		
Size: A4	Number: 11	Revision: A1
Date: 02.03.2018	Time: 14:44:52	Sheet 11 of 14
File: D:\Misc\Nixie\Schematics\2.5V_regulator.SchDoc		

L. Sartory
Nixie clock
with GPS synchronization



A

A

B

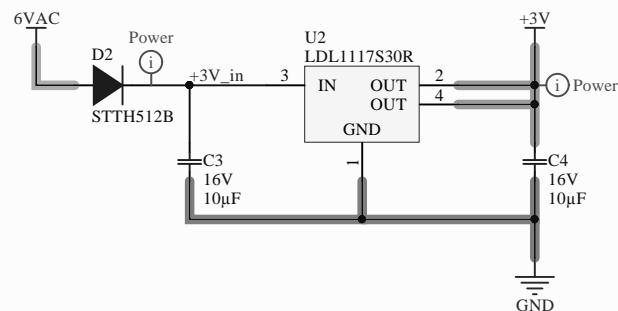
B

C

C

D

D



Title 3.0V digital power supply		
Size: A4	Number:12	Revision:A1
Date: 02.03.2018	Time: 14:44:52	Sheet12 of 14
File: D:\Misc\Nixie\Schematics\3.0V_regulator.SchDoc		

L. Sartory
Nixie clock
with GPS synchronization



A

A

B

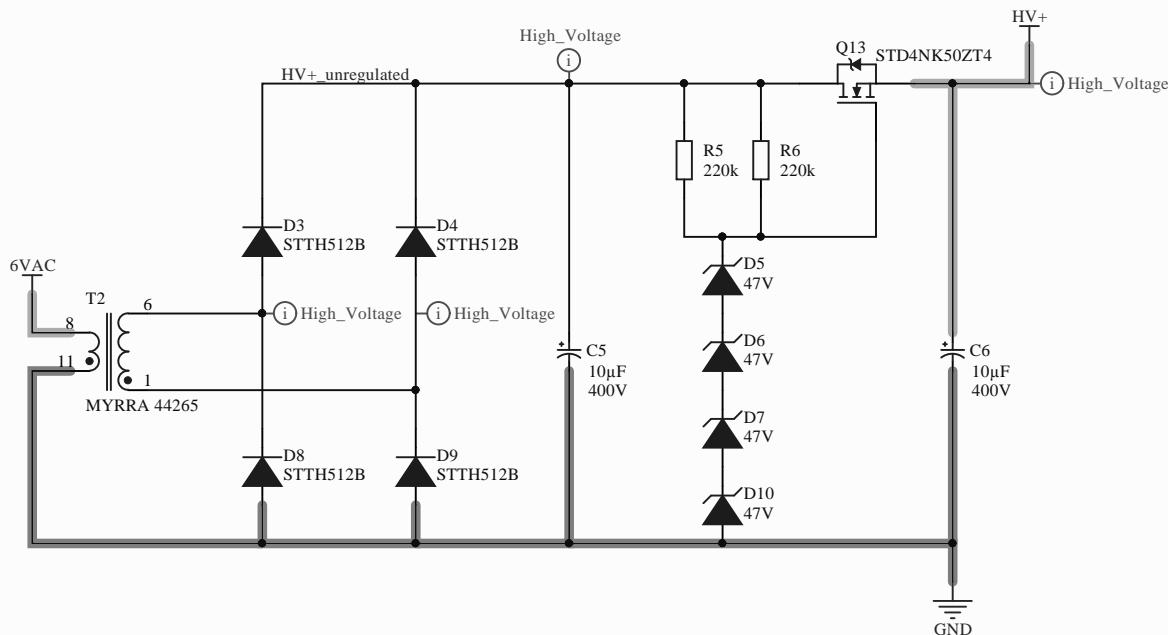
B

C

C

D

D

Title **High-voltage power supply**

Size: A4 Number:13 Revision:A1

Date: 02.03.2018 Time: 14:44:52 Sheet13 of 14

File: D:\Misc\Nixie\Schematics\HV_supply.SchDoc

L. Sartory

Nixie clock
with GPS synchronization**Altium**

A

A

B

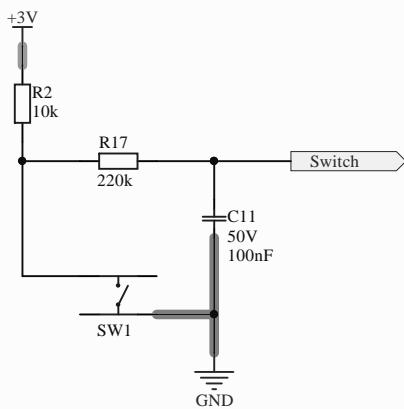
B

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C

D

D

**Title *Debounced switch***

Size: A4 Number:14 Revision:A1

Date: 02.03.2018 Time: 14:44:53 Sheet14 of 14

File: D:\Misc\Nixie\Schematics\Switch.SchDoc

L. Sartory
Nixie clock
with GPS synchronization

Altium®

