# Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)

**Structure**

The structure of a MOSFET is illustrated in fig??. The nMOS transistor is realized on a body of p-type silicon substrate. Two regions of the substrate, called source region and drain region, are heavily doped with n+ silicon. Between the n-regions a silicon dioxide (SiO2) layer is grown on top of the substrate. A metal gate electron is deposited on top of the oxide layer. Ohmic contacts are attached to source and drain region, as well as the substrate.

Where an n-region interfaces with the p-type silicon body a pn-junction forms. Source and drain region are separated by the highly resistive substrate and initially resemble two diodes. The area between source and drain region is referred to as “channel-region”.

Inversely, a pMOS transistor comprise an n-type substrate and p+ regions. The next sections refer to the nMOS depicted in fig ??, ?? and ??. The same principles also apply for pMOS. Charge carriers of pMOS and nMOS are holes and electrons, respectively.

The substrate electrode (B) is grounded and is not considered a functional terminal of the MOSFET. The transistor is there for referred to as a three-terminal device, where the terminals are source (S), drain (D) and gate (G).

The basic MOSFET composition is symmetrical. “Source” and “drain” merely indicate which terminal supplies (source) and which collects (drain) charge carriers. Conventional current flows from drain to source.

**Channel formation**

Adjusting input voltage to the gate terminal alters device conductivity. In order for current to flow between source and drain terminals an electrical connection must be made between the two. Without any voltage difference between gate and source the transistor in fig?? simply resembles two diodes, between which no electricity flows. The channel-region is highly resistive and does not permit charge carriers of the source-region to travel to the drain-region.

Increasing up to or beyond a threshold voltage (which is determined during fabrication) generates a conducting channel between S and D terminal. Voltage applied to gate gives rise to an electric field in the oxide layer. In the nMOS, a positive V\_GS pushes holes (charge carriers of the substrate) downwards and leaves bound electrons of acceptor atoms exposed. Furthermore, the electric field pulls abundant electrons from the n-regions into the channel-region. With sufficiently large gate voltage $()$, enough electrons accumulate across the substrate-oxide interface to invert a thin layer of the p-type substrate into n-type. The inversion layer in an nMOS is also referred to as n-channel (and p-channel in pMOS). It connects source-region to drain-region such that charge carriers can flow from one end to the other.

**Current-Voltage Relationship**

Any additional V\_GS increase beyond threshold extends the channel deeper into the substrate. The overdrive voltage (OV) is defined as in []. Raising V\_OV increases channel charge proportionally. With more available carriers the device conductivity increases.

Assuming a gate voltage above critical threshold, electrons can flow freely between n-regions through the channel. The relationship between drain current i\_D and drain-to-source voltage v\_DS is depicted in fig??. Without any voltage ($$) to coach the electrons in a specific direction the channel current is zero (i\_D=0). This can be changed by introducing a small potential drop across the channel which promotes electron flow from source to drain. Slowly raising V\_DS increases the current linearly. Proceeding to larger V\_DS the growth of i\_D slows down due to increasing channel resistivity.

When V\_DS approaches V\_TH the channel feels a notable negative potential drop across terminals S and D. As a result, the channel becomes asymmetrical in shape. It appears thicker near the source-end and tapers off linearly towards the drain-end.

**Saturation mode**

When v\_DS=V\_OT the channel becomes “pinched-off” and its depth is reduced to zero at drain end. Any further increase beyond this point has no effect on neither drain current nor the channel. Drain current is independent of v\_DS and remains constant at the value reached when v\_DS=V\_OT. In other words, channel electrons have reached carrier velocity saturation (i.e. maximum velocity). [R. Jacob Baker] At this point, the MOSFET transistor is said to be in saturation mode.

Though the channel-drain interface is non-existent, current persistently flows. Electrons at the channel end drift through the depletion region separating them from drain.

**Circuit Switch**

In a circuit, a saturated MOS transistor works like a switch, current either flows (switch ON) or it does not (switch OFF). If input voltage applied to G is high, an n-channel forms in nMOS and current passes though, the switch is “ON”. In pMOS, a high input voltage does not create a p-channel and no current passes the transistor, the switch is “OFF”. Reversely, a low voltage turns nMOS “OFF” and pMOS “ON”.

# CMOS

By controlling device conductivity, electronical signals can be switch on/off. A combination of complementary MOS transistors in a circuit makes a CMOS transistor (pMOS + nMOS = CMOS), shown in Fig. ??.

Circuit Logic

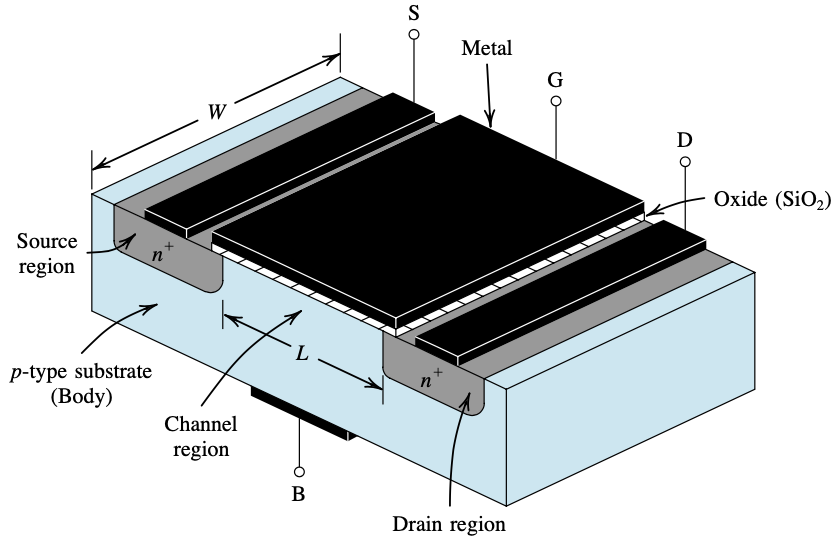
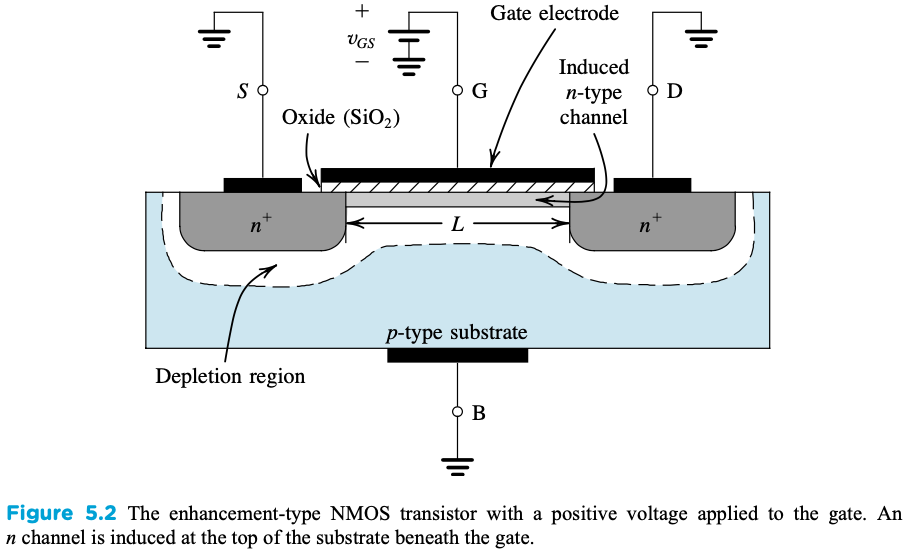
Low power consumption

In a p-substrate

**CMOS**

* **Circuit logic**
* **Low power consumption**

**Figures**



**A close up of a map

Description automatically generated**

A picture containing clock

Description automatically generated