Sinusoidal Frequency Doublers Using Operational Amplifiers

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Abstract—**This paper proposes a simple sinusoidal frequency-doubling circuit employing operational amplifiers (op amps) with resistors as the only external components. The realization method makes use of the inherent translinear loop at the output stage of the op amp as a means to perform frequency doubling. The response of the circuit is discussed and experimentally demonstrated.**

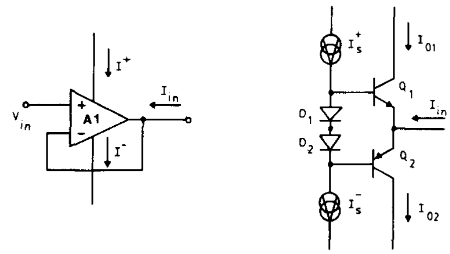
I. Introduction

In COMMUNICATION AND instrumentation systems, there are situations in which it is necessary to double the frequency of a sinusoidal signal. Usually, two approaches can be used to realize a sinusoidal frequency doubling circuit. The first approach is the use of an analog multiplier, where the two input terminals of the multiplier are connected together to form the common input terminal [1]. The second approach, which has received much attention recently [2]–[5], employs the square-law characteristic of a translinear configuration of bipolar junction transistor arrays. However, both approaches require a specific device or circuit in order to double the frequency of a sinusoidal signal.

It is well known that, because of its availability, an op amp has come to play quite an important role in the design of electronic circuits and its use has also become economically attractive. Therefore, if the realization scheme employs an op amp as a basic circuit building block, it will provide the construction of a simple and inexpensive sinusoidal frequency doubler. Although op amps were employed in the realization method given in [5], it also requires a translinear circuit. Furthermore, closely matched transistors are also needed. In this article, a simple frequency doubler circuit is proposed. The technique is based on the translinear characteristic of bipolar junction transistors which already exist within the output stage of a general-purpose op amp. Only 3 op amps and 6 resistors are required to implement the method. In addition, alternative schemes are also included.

II. Basic Principle

Figure 1(a) shows a unity gain voltage-controlled voltage source (VCVS) constructed with an op amp. The currents, I^+ and I^- denote respectively the positive-supply current and the negative-supply current of the amplifier. This circuit will be used as a basic element to realize the sinusoidal frequency-doubling circuit and a clear understanding of its characteristic is of value. For a general-purpose op amp, its output stage is usually a class-AB amplifier employing a complementary pair of transistors as shown in Fig. 1(b). The dc current I_S passing through the diode-connected transistors D_1 and D_2 biases transistors Q_1 and Q_2 in order to operate in a forward active region. In fact the circuit of Fig. 1(b) is a good approximation of a dual translinear loop comprising transistors Q_1, Q_2, D_1, and D_2 [6], [7]. Thus, the relation of the currents I_{o1}, I_{o2}, I_S and the input signal current I_{in} can be approximately given by



(a) (b)

Fig. 1. (a) A voltage follower constructed with an op amp. (b) Typical class *AB* output stage of an op amp.

$$I_{o1} = \left\{(4I_S^2 + I_{in}^2)^{1/2} - I_{in}\right\}/2 \quad (1)$$

$$I_{o2} = \left\{(4I_S^2 + I_{in}^2)^{1/2} + I_{in}\right\}/2 \quad (2)$$

where it should be noted that when $I_{in} = 0$, the currents $I_{o1} = I_{o2} = I_S$, and the relation of the currents I^+, I^-, I_{o1}, and I_{o2} are

$$I^+ \cong I_B^+ + I_{o1} \quad (3)$$

$$I^- \cong I_B^- + I_{o2} \quad (4)$$

where the current I_B is the quiescent bias current, including the bias current I_S, drawn by the op amp. In general, the magnitude of the quiescent bias currents I_S and I_B are quite variable from op amp to op amp and the exact values can be measured by the method in [7].

III. Circuit Description

The proposed sinusoidal frequency-doubling circuit is shown in Fig. 2. The op amps $A1$ and $A2$ (connected in the form of voltage-followers) and a converting resistor

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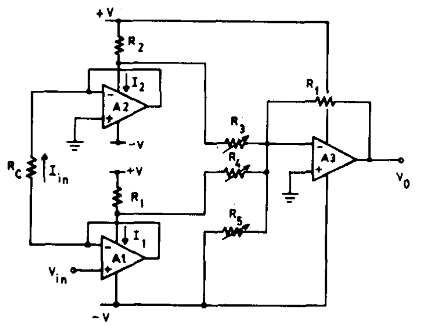

Fig. 2. The proposed sinusoidal frequency doubler.

R_C form a differential voltage-to-current converter, converting an input voltage V_{in} into a signal current $I_{in} = V_{in}/R_C$. Owing to this signal current, the supply-line currents I_1 and I_2 of the op amps $A1$ and $A2$, respectively, are modified. By making use of the (1) through (4), the currents I_1 and I_2 can, respectively, be expressed as

$$I_1 = I_{B1}^{+} + \left\{(4I_{S1}^2 + I_{in}^2)^{1/2} + I_{in}\right\}/2 \tag{5a}$$

$$I_2 = I_{B2}^{+} + \left\{(4I_{S2}^2 + I_{in}^2)^{1/2} - I_{in}\right\}/2 \tag{5b}$$

for $V_{in} > 0$ and

$$I_1 = I_{B1}^{+} + \left\{(4I_{S1}^2 + I_{in}^2)^{1/2} - I_{in}\right\}/2 \tag{6a}$$

$$I_2 = I_{B2}^{+} + \left\{(4I_{S2}^2 + I_{in}^2)^{1/2} + I_{in}\right\}/2 \tag{6b}$$

for $V_{in} < 0$. The supply-line currents I_1 and I_2 are then sensed by the resistors R_1 and R_2, respectively, and the voltage drops across the resistors are delivered to the summing amplifier, which is formed by the op amp $A3$ and the resistors R_3, R_4, and R_f. Ideally, it is required that R_1 and R_2 are closely matched and the op amps $A1$ and $A2$ are closely matched, i.e., $R_1 = R_2 = R_S$, $I_{B1}^{+} = I_{B2}^{+} = I_B$ and $I_{S1} = I_{S2} = I_S$. Assuming that $I_1 >> I_{R4}$ and $I_2 >> I_{R3}$, where I_{R3} and I_{R4} are the currents through resistances R_3 and R_4, respectively, and if we set $R_3 = R_4 = R_A$, then the output voltage of the summing amplifier can be given by

$$\begin{aligned} V_o &= V_{o1} + V_{o2} \\ &= \left\{2k_1 I_B + R_f \cdot V\left((1/R_5) - (2/R_A)\right)\right\} \\ &\quad + k_1(4I_S^2 + I_{in}^2)^{1/2} \end{aligned} \tag{7}$$

where $k_1 = R_S R_f / R_A$ and V is the power-supply voltage. We can see that the second term of (7) or V_{o2} is in the form of a root-sum-of-squares relation. It is this term that exhibits the frequency-doubling action.

For a sinusoidal input signal $V_{in} = V_m \sin wt$, the input signal current I_{in} is equal to $I_m \sin wt$, where $I_m = V_m/R_C$. Substituting the signal current into (7), then without loss of generality, the output voltage V_{o2} can be written as

$$V_{o2} = 2I_S k_1 (1 + k_2 \sin^2 wt)^{1/2} \tag{8}$$

where $k_2 = I_m^2/4I_S^2$. The term between brackets can be expanded by using the power series of the form

$$\sqrt{1+X} = 1 + (1/2)X - (1/8)X^2 + (1/16)X^3 - \cdots .$$

Then (8) becomes

$$V_{o2} = 2I_S k_1 (a_{dc} + a_1 \cos 2wt + a_2 \cos 4wt + \cdots) \tag{9}$$

where a_{dc}, a_1, a_2, $\cdots$ represent the magnitudes of the dc and the harmonic components and

$$\left.\begin{aligned} a_{dc} &\cong 1 + 0.25k_2 - 0.047k_2^2 + 0.0195k_2^3 \\ &\quad - 2.26 \times 10^{-3}k_2^4 \\ a_1 &\cong -0.25k_2 + 0.0625k_2^2 - 0.0293k_2^3 \\ &\quad + 1.953 \times 10^{-3}k_2^4 \\ a_2 &\cong -0.0156k_2^2 + 0.01172k_2^3 - 1.71 \times 10^{-3}k_2^4. \end{aligned}\right\} \tag{10}$$

It is clearly seen that V_{o2} contains only even harmonic components. If an appropriate value of k_2 is chosen, the higher harmonic components can be ignored. Then V_{o2} will approximately contain only the dc component and a signal component at twice the input frequency or

$$V_{o2} \cong 2I_S k_1 (a_{dc} + a_1 \cos 2wt). \tag{11}$$

Substituting the above result into (7), we get

$$\left.\begin{aligned} V_o &\cong V_{DC} + V_{DOUBLE} \\ &\cong \left\{2k_1(I_B + a_{dc} \cdot I_S) + R_f \cdot V\left((1/R_5) \right.\right. \\ &\quad \left.\left. - (2/R_A)\right)\right\} + 2a_1 k_1 I_S \cos 2wt. \end{aligned}\right\} \tag{12}$$

We found that for $k_2 < 0.20$ a harmonic distortion of less than 2 percent can be achieved. It should be noted that the V_{dc} component of (12) can be easily removed by including resistor R_5 connected to a negative power supply voltage, as shown in the Fig. 2, and R_5 can be given by

$$R_5 = R_A \cdot V / \left\{2\left\{V - (I_B + a_{dc}I_S)R_S\right\}\right\}. \tag{13}$$

A procedure for constructing the frequency-doubling circuit follows:

(a) Measure the value of the op amp quiescent bias currents I_B and I_S, using the method of [7].

(b) Choose R_1 and R_2 such that the dc voltage drop across R_1 and R_2 are approximately equal to $(V_{CC} - 1.5)/2$.

(c) Specify the value of V_m and choose R_C such that $k_2 < 0.2$.

(d) Choose R_3, R_4, and R_f for an appropriate value of k_1.

(e) Adjust R_5 such that the $V_{dc} = 0$.

IV. Experimental Result and Discussion

To demonstrate the performance of the technique, the circuit in Fig. 2 was constructed. The amplifiers employed were monolithic op amp LF 351's. Selectively

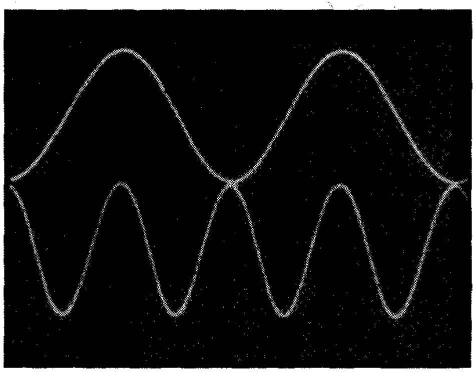

Fig. 3. Frequency doubler waveforms. Top: input waveform 2 V/div. Bottom: output waveform 0.02 V/div. Time base: 10 μS/div.

matched op amps were employed for the amplifiers, $A1$ and $A2$. The quiescent bias currents I_B and I_S of the amplifiers $A1$ and $A2$ were measured to be 1.29 and 0.69 mA, respectively. All the resistors used were in the form of ± 1-percent tolerance resistors, where $R_1 = R_2 = 2.8$ kΩ, $R_3 = R_4 = 30$ kΩ, $R_f = 5.6$ kΩ and $R_C = 5$ kΩ. To minimize the error due to mismatching of the op amps $A1$ and $A2$, a 100 Ω variable resistor was also connected in series with the resistors R_3 and R_4.

The input and output waveforms of the sinusoidal frequency-doubling circuit are shown in Fig. 3. The peak input voltage V_m is set to 1.5 V and then $k_2 = 0.19$, since $R_C = 5$ kΩ. The amplitude of the output waveform of the 2-wt component has a peak value of 0.03 V, which is in close agreement with the value predicted by (11). Harmonic distortion of less than 1.5 percent was measured.

It should be noted that two major disadvantages exist in this realization scheme. Firstly, since the method uses op amps, which have limited bandwidth it is only suitable for a low frequency application. The measured bandwidth of the circuit is about 50 KHz. Secondly, the construction of circuit in Fig. 2 will be inconvenient in practice due to the use of closely matched op amps. However, this disadvantage can be overcome by using one of the alternative circuits shown in Fig. 4. In Fig. 4(a), a unity gain current mirror formed by transistors Q_1, Q_2, Q_3, and Q_4 is used to reflect the negative-supply-line current of the op amp $A1$ to the resistor R_2. For the method in Fig. 4(b), the supply-line currents I_1 and I_2 of the op amp $A1$ are sensed by resistors R_1 and R_2, respectively, and then the voltage drops across the resistors are delivered to the difference amplifier formed by op amp $A2$ and resistors R_3, R_4, R_5, R_{f1}, and R_{f2}. Although this circuit provides the construction of a frequency-doubling circuit using an op amp as the only active element, it requires closely matched resistors, i.e., $R_1 = R_2$, $R_3 = R_4$, $R_{f1} = R_{f2}$.

For a dual op amp, like LF 353, LF412, and LF442 op amps, 2 op amps are constructed in the same package and their positive-supply-lines are connected together as well as the negative supply lines, the sinusoidal frequency-doubling circuit as shown in Fig. 5 can be employed. The

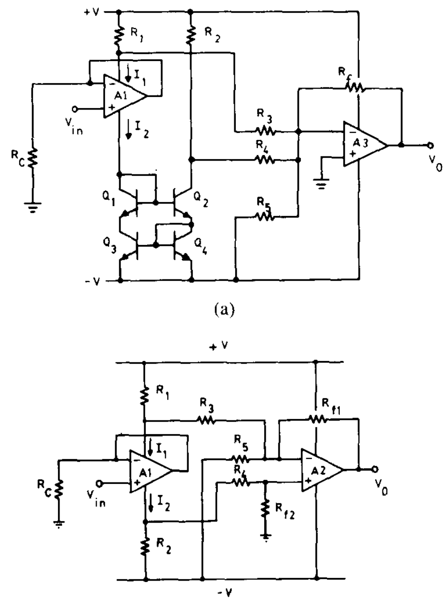

Fig. 4. Frequency doubling circuits employing (a) op amps and a current mirror, (b) op amps and resistors.

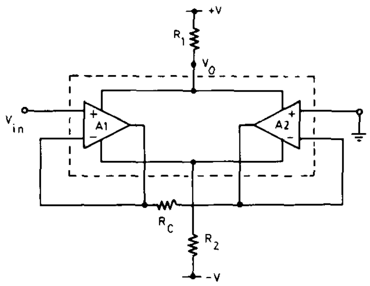

Fig. 5. Frequency doubler constructed with a dual op amp.

2-wt component can then be monitored from the voltage drop across the supply-line current sensor R_1. The resistor R_2 can then be used to adjust the small error due to mismatching of the supply-line currents.

V. Conclusion

It has been demonstrated in this article that a sinusoidal frequency doubler can be designed by using only op amps and resistors. The frequency doubling action is exploited by employing the dual translinear characteristic associated within the output stage of a general-purpose op amp, where this characteristic can be monitored from the supply-line currents. In our proposed circuit, two closely matched resistors are employed to sense the supply-line currents of the voltage-follower and then summing up to produce an output voltage which is in the form of a root-sum-of-squares relation. It is this relation that provides the output signal with a frequency that is twice that of the input frequency. Since the realization scheme employs a general-purpose op amp, it is expected that the method would be beneficial where an analog multiplier is not easily available.

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