Development of a Low-Cost FPGA-Based SSVEP BCI Multimedia Control System

Kuo-Kai Shyu, *Member, IEEE*, Po-Lei Lee, Ming-Huan Lee, *Student Member, IEEE*, Ming-Hong Lin, Ren-Jie Lai, and Yun-Jen Chiu, *Student Member, IEEE*

***Abstract*—This paper proposes a low-cost field-programmable gate-array (FPGA)-based brain–computer interface (BCI) multimedia control system, different from the BCI system, which uses bulky and expensive electroencephalography (EEG) measurement equipment, personal computer, and commercial real-time signal-processing software. The proposed system combines a customized stimulation panel, a brainwave-acquisition circuit, and an FPGA-based real-time signal processor and allows users to use their brainwave to communicate with or control multimedia devices by themselves. This study also designs a light-emitting diode stimulation panel instead of cathode ray tube or liquid-crystal display used in existing studies, to induce a stronger steady-state visual evoked potential (SSVEP), a kind of EEG, used as the input signal of the proposed BCI system. Implementing a prototype of the SSVEP-based BCI multimedia control system verifies the effectiveness of the proposed system. Experimental results show that the subjects' SSVEP can successfully control the multimedia device through the proposed BCI system with high identification accuracy.**

***Index Terms*—Field-programmable gate array (FPGA), low-cost brain–computer interface (BCI), steady-state visual-evoked potential (SSVEP).**

I. Introduction

PATIENTS suffering from severe motor disabilities, such as amyotrophic lateral scleroses (ALS), spinocerebellar ataxia (SCA), and other paralyzed patients, may have limited motion while constrained on a hospital bed. Developing a self-care system for patients to personally control or communicate with external devices reduces the nursing labor load and facilitates patient autonomy. Thus, studies have presented eye-tracking systems [1], [2] for physically impaired people to control devices. Chen [3] designed a head-operated computer mouse interface for people with disabilities, but this system requires patients to rotate the neck.

Brain–computer interface (BCI) systems acquire electroencephalography (EEG) data from the human brain, then recognize and translate the specific brain signal patterns into the device control command through the signal-processing algorithm [4]. Sutter [5] developed a visual evoked potential (VEP)-based BCI system with a screen displaying 64 symbols to evoke the subject's VEP. Depending on the VEP pattern, the system recognizes the symbol gazed at by the subject. The sensory stimulation of one's visual field elicits VEP data, which records from the surface of the visual cortex [5]. Visual stimuli flashing at the center of the visual field creates a higher potential than flashes at the periphery of the visual field. Steady-state visual evoked potential (SSVEP) is an EEG signal response to the flickering visual stimulus with a frequency higher than 6 Hz [6]. Cheng *et al.* [7] implemented a SSVEP-based BCI system in a PC-based environment, and focused on allowing the patient to ring the mobile phone. Wang *et al.* [8] proposed a SSVEP BCI system to determine the gazing direction of the user for controlling the output device. Many BCI systems have been proposed [7]–[12] based on the SSVEP. Gao *et al.* [13] proposed a digital signal processor (DSP) design, a SSVEP-based BCI system, and implemented the fast Fourier transform (FFT) algorithm in the DSP for detecting stimulus frequencies.

Most SSVEP-based BCI systems mentioned before are based on the frequency-encoding technique. Wang *et al.* [14] and T. Kluge and M. Hartmann [15] demonstrated using phase encoding in the SSVEP-based BCI system, and estimated the phase shift from the complex spectrum values of the stimulus frequency. The proposed SSVEP-based BCI system in this paper is based on the phase encoding flashing light technique [16]. In this technique, different phase sequences (i.e., 0°, 90°, 180°, and 270°) at the same flickering frequency drive the flickering visual stimuli. The proposed SSVEP-based BCI system is different from those attention-dependence SSVEP-based BCI systems [17], [18] which do not require any target gazing. Several studies have demonstrated that the SSVEP-based BCI system can achieve accuracies ($\sim 90\%$) much superior to those attention-dependence systems ($\sim\ 75\%$). Subjects' attention level in the attention-dependence systems is easily affected by various mental states, such as fatigue, arousal, attention level, etc. The application in this study demands high accuracy for command control; therefore, we chose an SSVEP-based BCI system in our implementation. Moreover, the signal-processing algorithm was designed in the field-programmable gate array (FPGA). If using frequency encoding SSVEP BCI, the FFT is necessary. However, the stimulus frequency detection in the phase encoding-based SSVEP BCI is not needed. Consequently, the phase encoding-based SSVEP BCI reduces complexity and reconfigurable gate arrays consumption of the FPGA design. Logic elements (LEs) consumption of major signal-processing circuits in the FPGA for phase (epochs segment/average) and

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The authors are with the Department of Electrical Engineering, National Central University, Jhong-Li, Taoyuan 320, Taiwan (e-mail: kkshyu@ee.ncu.edu.tw; pllee@ee.ncu.edu.tw; 92541009@cc.ncu.edu.tw; 965201081@cc.ncu.edu.tw; 965201074@cc.ncu.edu.tw; 975401014@cc.ncu.edu.tw).

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frequency (FFT) encoding are 884 LEs and 4068 LEs, respectively. The amplitude versus frequency response curves for the SSVEP-based system of a subject is nonlinear [8]. Thus, it is difficult to arrange multiple flickering frequencies linearly in the frequency encoding-base BCI. This research therefore chose the phase encoding-based SSVEP BCI for using less frequency to drive multiple stimuli. The reasons for a FPGA-based circuit design are as follows. Since FPGA contains reconfigurable gate arrays and large amounts of embedded memory [19], [20], it is suitable for implementing a digital signal processing algorithm rapidly. Moreover, FPGA realizes parallel architectures and increases system performance. The parallel architecture not only processes high-volume data more efficiently, but also performs multiple tasks at the same time. Therefore, researches have implemented many systems using FPGAs [21]–[23].

The current study implements a low-cost FPGA-based SSVEP BCI multimedia control system, so patients suffering from ALS or severe paralysis can self-control the entertainment equipment. The proposed system contains several main parts. First, this research designed a light-emitting diode (LED) stimulation panel with four flickering visual stimuli and an SSVEP acquisition circuit to evoke and acquire the subject's SSVEP, respectively. This study uses the acquisition circuit instead of expensive EEG measurement equipment. Second, this paper designed an analog-to-digital-converter (ADC) module board, without using peripherals necessarily used in PCs, such as universal serial bus (USB) data-acquisition (DAQ) devices or a DAQ peripheral component interconnect (PCI) card to quantify the acquired SSVEP signal. Third, an FPGA implements an SSVEP signal processor by hand-coding VHSIC hardware description language (VHDL). This investigation used the FPGA-based SSVEP signal processor instead of the bulky personal computer with signal-processing software. In this way, more patients can afford such a convenient BCI system. Fourth, the radio-frequency (RF) command transmitter and receiver circuits were designed for communicating the recognition result (multimedia control command) immediately and wirelessly. Finally, to feedback the SSVEP recognition result to the subject (patient) simultaneously, this study implemented a biofeedback voice-output circuit.

The proposed BCI system processes SSVEP data to recognize the visual stimulus where the subject is looking. By identifying the stimulus gazed at by the subject, the corresponding/desired multimedia device control command can be found. The present system requires user's visual sensation ability in a visual stimulating environment, which belongs to a dependent BCI system. The other EEG signals, such as mu rhythms and slow cortical potentials (SCP), are independent BCIs in which the system does not require their muscular control of gaze direction [4]. Attention-dependence SSVEP-based BCI systems do not need target gazing. Generating the EEG signal in this case depends mainly on the user's intent, not on the precise eye orientation; it also belongs to independent BCI systems [4]. Compared to the eye-tracking system or electrooculography (EOG)-based system, the present SSVEP-based approach is a dependent BCI system which still requires eye movement. Nevertheless, the focus of this paper is on developing a low-cost FPGA-based SSVEP BCI control system which provides an alternative choice for patients to control multimedia devices by measuring their SSVEPs.

The main contributions of the proposed BCI system are twofold. The first is that the system integrates multimedia into the BCI system. The second is that this BCI system, to the authors' best knowledge, is the first design of a low-cost FPGA-based BCI system. Finally, experimentation demonstrates the effectiveness of the proposed BCI system.

II. Materials and Methods

A. System Configuration

Fig. 1 shows the block diagram of the proposed low-cost FPGA-based SSVEP BCI multimedia control system, which includes: 1) a handmade stimulation panel, 2) a customized SSVEP acquisition module board, 3) an ADC module board, 4) a SSVEP signal processor, 5) a biofeedback speaker, and 7) a multimedia device. The stimulation panel contains four visual stimuli labeled with multimedia control command symbols ( ,  ,  , and ). Four visual stimuli flash at one flickering frequency (21 Hz) but with four different phases (0°, 90°, 180°, and 270°). The customized SSVEP acquisition module board first acquires the subject's SSVEP signal, which includes: a preamplifier, filter, a postamplifier, and dc bias adjustment circuits. Then, an ADC module board quantifies the acquired SSVEP signal $\mathrm{SSVEP}_{\mathrm{Acquired}}$. Later, an SSVEP signal-processing algorithm processes the quantified SSVEP signal, which is implemented in an FPGA, called the SSVEP signal processor in this paper. The main hardware blocks implemented in the FPGA include an ADC module board controller, a third-order infinite impulse response (IIR) band-pass filter, an epochs segment/average circuit, a phase identification circuit, memory block, and a flickering signal generator. Once the SSVEP signal processor recognizes the visual stimulus that the subject is staring at, the processor sends the corresponding/desired control command to the multimedia device through the RF command transmitter. The proposed system also uses the voice–output circuit and speaker to feedback the recognition result to the subject simultaneously.

B. Visual Stimulation

The stimulation panel contains four flickering visual stimuli (multimedia control commands). Each visual stimulus contains one white LED. The amplitude of the fundamental frequency in the SSVEP evoked by the LED visual stimulus is significantly larger than that evoked by other visual stimuli (i.e., CRT or LCD) [24]. The LED-based visual stimulation also lowers cost because the costs include: 1) LEDs (white LED $\times 4$); 2) drive circuits (resister $\times 8$ transistor $\times 4$); and 3) an acrylic stimulation panel case. The CRT or LCD display/scan circuits do not need to implement and also reduce complexity of the FPGA hardware design. For controlling the multimedia, visual stimuli are covered with a tracing paper printed with multimedia control symbols: through the symbols:  ,  ,  , and  , where means to play or pause the selected multimedia file (movie or song); is to stop the multimedia; and mean to scroll displayed items, or adjust the volume up and down, respectively, during playback. Each visual stimulus is labeled with one multimedia control symbol to represent a device control command.

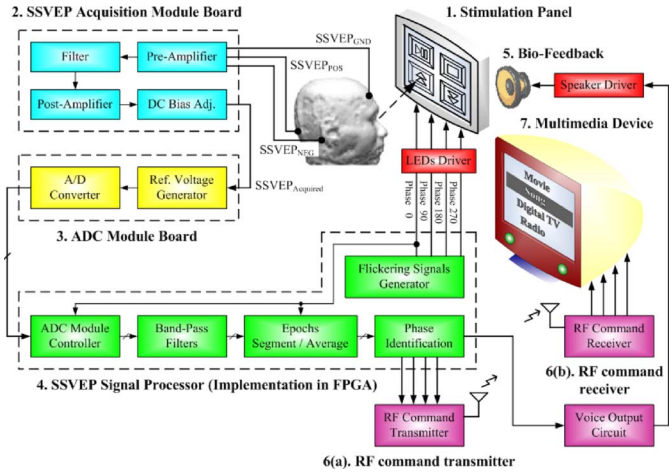

Fig. 1. Block diagram of the low-cost FPGA-based SSVEP BCI multimedia control system.

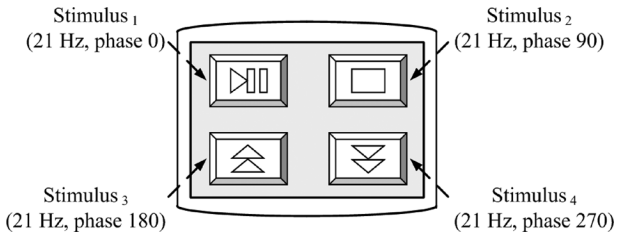

Fig. 2. Layout of visual stimulation panel.

Four flashing stimuli are designed based on the phase encoding flashing light technique [16]; four flickering visual stimuli are driven by four phase sequences (0°, 90°, 180°, and 270°) at the same flickering frequency, 21 Hz, respectively (stimulus$_1$ ⏯: 0°, stimulus$_2$ ⏹: 90°, stimulus$_3$ ⏫: 180°, and stimulus$_4$ ⏬: 270°). Controlling the time delay of the flickering signal generators designed in FPGA produces the phase sequences. The flickering frequency in this study is high frequency for better visualization. However, the amplitude response versus flickering frequency of a subject is nonlinear [8]. Thus, one could pick up a flickering frequency with better response as the flickering frequency in the SSVEP-based BCI system. But amplitude versus frequency response curves for different subjects are different. This research examined and calculated SSVEP amplitude responses (accuracies) versus different flickering frequencies (15 Hz– 29 Hz) for subjects who participated in the experiments to decide the flickering frequency used in the proposed BCI system. The flickering frequency, 21 Hz, was then selected as the frequency in which most subjects had better accuracy. Fig. 2 illustrates the layout of the visual stimulation panel, including four visual stimuli (stimulus_1, stimulus_2, stimulus_3, and stimulus_4), symbolized by multimedia control icons (⏯, ⏹, ⏫, and ⏬), respectively.

C. SSVEP Acquisition Circuit

Three gold-plated EEG electrodes (Grass Technologies, F-E5GH, disc electrodes with 1-cm diameter) acquire the SSVEP signal from the scalp. The first electrode $\text{SSVEP}_{\text{POS}}$ is placed at the occipital region O_Z (based on the International EEG 10–20 system [25]), the second electrode $\text{SSVEP}_{\text{NEG}}$ is placed at the right mastoid, and the bipolar signal ($\text{SSVEP}_{\text{POS}}$ to $\text{SSVEP}_{\text{NEG}}$) with respect to the ground electrode (third electrode, $\text{SSVEP}_{\text{GND}}$) is placed at the forehead position Fp_Z. Fig. 3 illustrates the block diagram of the SSVEP acquisition module board. Since the magnitude of the SSVEP signal recorded from the scalp is very small ($\sim 50\ \mu$V), the SSVEP bipolar signal is first amplified by a preamplifier using an instrumentation amplifier, INA 128, (Gain setting, *Gain*: 1000). The current research used the INA 128 because it has high gain and high input impedance as well as a good common-mode rejection ratio (CMRR) ($\text{CMRR}_{21\ \text{Hz}}$: 130 dB). The preamplified SSVEP signal was first filtered by a low-pass active second-order Butterworth filter (cutoff frequency f_C: 22 Hz) and then filtered by a high-pass one (cutoff frequency f_C: 20 Hz). To remove power-line interference (60 Hz) from SSVEP signals effectively, this work also used a 60-Hz notch filter following active filters. The filtered SSVEP signals were amplified again by using a postamplifier circuit (gain setting, $Gain_{\text{MAX}}$: 201) to adjust the filtered SSVEP signals with peak-to-peak voltages in the range of -2.5 to 2.5 V. Finally, this work adopted a dc bias adjustment circuit to adjust the output $\text{SSVEP}_{\text{Acquried}}$ voltage level, so that the following SSVEP acquisition module board easily digitized $\text{SSVEP}_{\text{Acquried}}$ into the desired range (peak-to-peak voltage range: 0–5 V). The SSVEP acquisition circuits were integrated onto a printed-circuit board (PCB), and the total current consumption was about 65.4 mA.

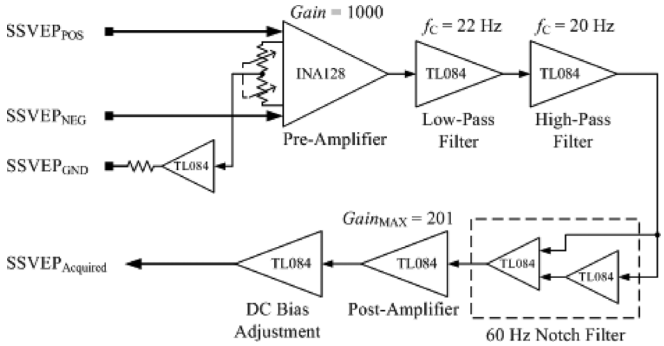

Fig. 3. Block diagram of the SSVEP acquisition module board.

D. ADC Module Board

The ADC module board connects the acquired SSVEP signal $\text{SSVEP}_{\text{Acquried}}$ to the SSVEP signal processor. To reduce the FPGA's input/output (I/O) ports expenditure, the ADC chip is the 8-pin dual in-line package (DIP) with serial control interface [serial peripheral interface (SPI)] devices, MicroChip MCP3201. The resolution and maximum sampling rate of the ADC are 12 b and 100 ksamples/s.

E. SSVEP Signal Processor

For implementing a BCI system without using a personal computer accompanied with commercial signal processing software, the SSVEP signal-processing algorithm was implemented in the Altera Cyclone EP2C20Q FPGA [26], called the SSVEP signal processor in this paper. The hardware was implemented

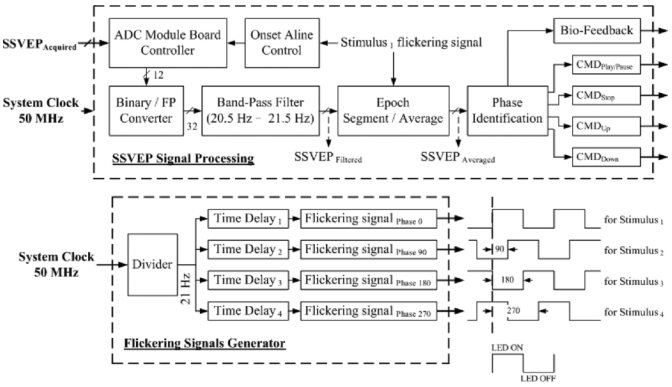

Fig. 4. Block diagram of the internal circuit of the proposed SSVEP signal processor.

by hand coding the VHDL code. These codes were compiled, synthesized, and fitted by using Quartus II [27]. Fig. 4 shows the block diagram of the internal circuit of the proposed SSVEP signal processor.

First, the SSVEP signal $\mathrm{SSVEP}_{\mathrm{Acquried}}$, outputted from the SSVEP acquisition module board was sampled at 8 kHz with 12-b resolution through the ADC module board and ADC module board controller designed in the FPGA. For phase identification, the study collected quantified SSVEP data from the onset of the $\mathrm{stimulus}_1$ flicking signal. The quantified data were converted from a 12-b binary to a 32-b single-precision float point (FP) (IEEE 754 standard) by the binary/FP converter immediately.

Second, the SSVEP data were then filtered through a third-order IIR band-pass filter (cutoff frequency: 20.5 Hz – 21.5 Hz) to obtain the filtered SSVEP signal $\mathrm{SSVEP}_{\mathrm{Filtered}}$. The FP [28] arithmetic allows numbers to be represented in a wider range because of its ability to automatically scale numbers. Therefore, this study implemented and used the hardware FP arithmetic units, including addition, subtraction, multiplication, division, and square root in the SSVEP signal processor. The format of the IEEE 745 standard for single-precision FP is 32 b wide, and the FP number value is calculated by

$$\mathrm{FP}_{\mathrm{Value}} = (-1)^s(1 \cdot f) \times 2^{(e-127)} \tag{1}$$

where s is the sign bit used to specify the sign of the floating-point numbers, e is an 8-b quantity called the bias-exponent field, and f has 23 bits storing the fraction of floating-point numbers. Fig. 5 shows the block diagram of the implemented floating-point arithmetic, which includes three main stages:

Stage 1) unpacks $\mathrm{FP_A}$ and $\mathrm{FP_B}$;

Stage 2)operation (addition, subtraction, multiplication, division, or square-root) between $1 \cdot f_{\mathrm{A}}$ and $1 \cdot f_{\mathrm{B}}$;

Stage 3)normalizes and packs the results of stage 2 f_{Y}.

Third, this study adopted the averaging method in the SSVEP processing algorithm to suppress interference. A total of 30 epochs, and 380 sample points for each epoch were segmented and collected based on the onset of the $\mathrm{stimulus}_1$ flicking signal (sampling rate: 8 kHz, flicking frequency: 21 Hz, $1/21 \div 1/8\,\mathrm{k} \fallingdotseq 380$). These epochs were then averaged to obtain the average SSVEP signal $\mathrm{SSVEP}_{\mathrm{Averaged}}$ in the time domain.

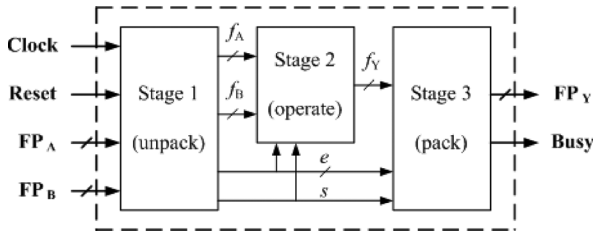

Fig. 5. Block diagram of the implemented floating-point arithmetic.

Finally, based on the phase encoding flashing light technique, the stimulus (multimedia command symbol: ⏯, ⏹, ⏫, and ⏬) that the subject is staring at can be recognized by finding the phase of $\mathrm{SSVEP}_{\mathrm{Averaged}}$. The following description is on the phase identification method.

When the power of the proposed BCI system is turned on, the system goes into phase identification mode, where only the $\mathrm{stimulus}_1$ is presented and flashed at 21 Hz with 0° phase delay. First, the proposed system requests the subject to gaze at the $\mathrm{stimulus}_1$ for obtaining enough epochs (1080 epochs in our current design), and these epochs are averaged to obtain the referenced SSVEP signal, $\mathrm{SSVEP}_{\mathrm{Referenced}}$. Then, finding the delay time of the highest peak in $\mathrm{SSVEP}_{\mathrm{Referenced}}$, obtains the reference time delay t_{Ref}. In the phase identification mode, the system obtains the reference time delay t_{Ref} automatically, and the subject only needs to focus on the $\mathrm{stimulus}_1$ during this mode. After getting t_{Ref}, this information (value) is stored and available for the entire period when the subject uses the proposed BCI system. Fig. 6 demonstrates the acquired SSVEP data (subject A) for filtering, segmenting, and averaging. First, $\mathrm{SSVEP}_{\mathrm{Acquried}}$ and $\mathrm{SSVEP}_{\mathrm{Filtered}}$ are quantified and segmented based on the onset of the $\mathrm{stimulus}_1$ flicking signal in the application mode, respectively. Then, $\mathrm{SSVEP}_{\mathrm{Averaged}}$ is obtained after averaging 30 epochs segmented from $\mathrm{SSVEP}_{\mathrm{Filtered}}$. The time delay t_{Avg} of the highest peak in $\mathrm{SSVEP}_{\mathrm{Averaged}}$ is calculated for identifying the visual stimulus gazed by the subject. In the proposed system, because four flickering visual stimuli are driven by four phase delay sequences, 0°, 90°, 180°, and 270°, respectively, the corresponding t_{Avg} for each visual stimulus can be predicted from t_{Ref}. Fig. 6 shows the SSVEP data measured from subject A, and the reference time delay t_{Ref} is 6.17 ms. Since the phase delay between two visual stimuli is 90°, the time delay (interval) between two visual stimuli is $t_{\mathrm{Intv}} = [(1 \div 8\,\mathrm{k}) \times 380] \div 4 =$ 11.875 ms, where 8 k is the sampling rate, and 380 denotes the number of samples for the flickering frequency, 21 Hz. Therefore, the predicted time delay for each visual stimulus is calculated by the following equation:

$$t^j_{\mathrm{Avg\_Predicted}} = t_{\mathrm{Ref}} + [(j-1) \times t_{\mathrm{Intv}}] \tag{2}$$

where $j = 1$, 2, 3, and 4 are the visual stimulus numbers. The corresponding $\mathrm{stimulus}_j$ the user focuses on can be identified after comparing the predicted time delay $t^j_{\mathrm{Avg\_Predicted}}$, and actual gazing time delay t_{Avg}. To ensure the identification result, the current work confirmed the final multimedia control command after successfully detecting the same result twice.

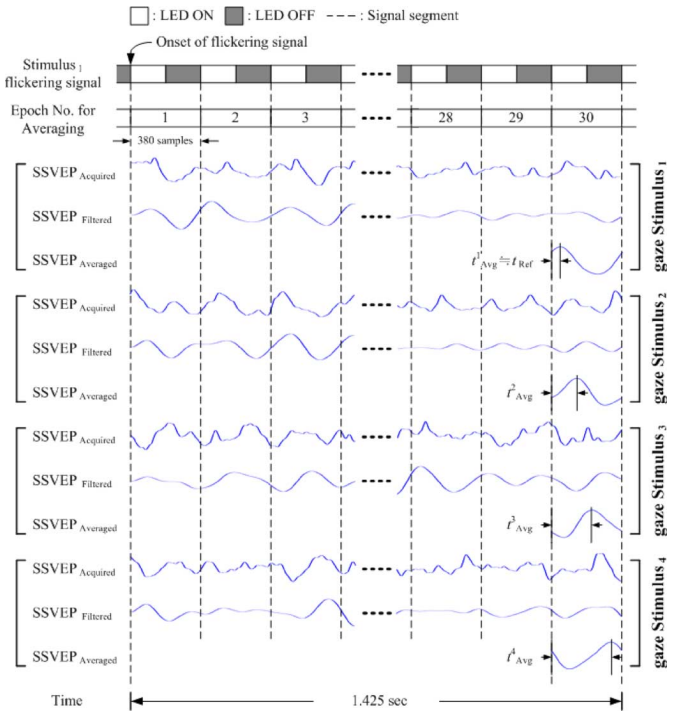

Fig. 6. Demonstration of the acquired SSVEP data filtering, segmenting, and averaging.

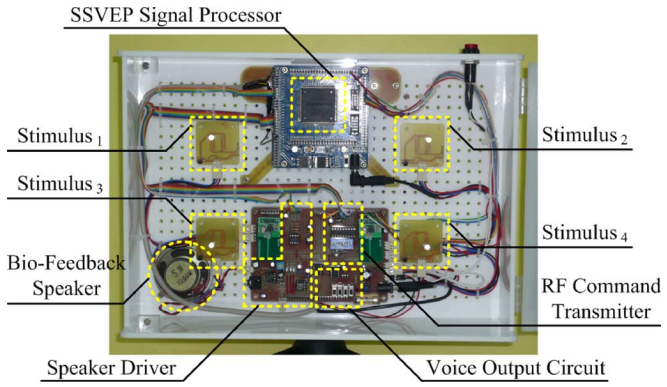

Fig. 7. Photograph inside the handmade stimulation panel.

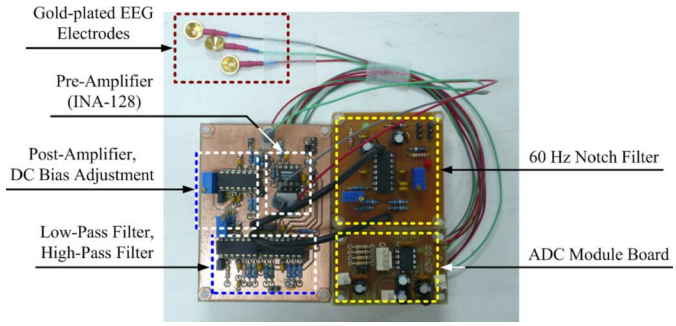

Fig. 8. Photograph of the SSVEP acquisition module board and ADC module board.

Since four flickering visual stimuli are driven by four phase delay sequences (0°, 90°, 180°, and 270°) at the same flickering frequency, 21 Hz, a flickering signal generator is designed in FPGA. First, the system clock (50 MHz) is divided into the flickering frequency, 21 Hz, then, controlling the sequence output time delay produces the four-phase delay sequence signals.

F. Other Circuits

1) Voice Output Circuit: The current work designed the bio-feedback voice output circuit for feedbacking the SSVEP recognition result to the subject. A microphone amplifier/filter and ADC module boards recorded and quantified voice data (i.e., play, pause, stop, scroll up, and scroll down). Digital voice data were then stored into an electrically erasable programmable read-only memory (EEPROM) device, MicroChip 25LC1024. When the SSVEP signal processor identifies the visual stimulus focused on by the subject, the corresponding voice data reads out from the EEPROM and converts to the analog signal through a digital-to-analog converter (DAC) circuit (MicroChip MCP4921). Finally, the corresponding voice signal speaks through the audio power amplifier device. The National Semiconductor LM386, was adopted as the speaker driver to drive the biofeedback speaker, outputting the corresponding voice signal.

2) RF Command Transmitter and Receiver: The current design sends out the corresponding multimedia control command according to the identified SSVEP to control the multimedia device through the RF command transmitter. The Holtek series encoder HT12E and series decoder HT12D are used in RF transmit module (TG-11A) and receive module (TG-11B), respectively. The HT12E encoder encodes information consisting of eight address bits and four data bits for multimedia commands. The programmed addresses/data are transmitted together (series) with header bits via the RF transmit module. Once the decoder HT12D receives serial data from the RF receive module, it decodes information with 8-b addresses and 4-b data, comparing the serial input data three times sequentially with its local address. If no error occurs, the input data codes (multimedia commands) are decoded and then transferred to the output pins (connecting to the multimedia device) of the HT12D. The operation frequency of transmit and receive modules is 413 MHz.

III. Experimental Results

Seven subjects (ages 23 to 32) with related SSVEPs were recorded from the O_Z ($SSVEP_{POS}$) located on the subject's scalp (over the visual cortex) based on the International EEG 10–20 system [24]. The reference electrode ($SSVEP_{NEG}$) was placed at the right mastoid, and the ground electrode ($SSVEP_{GND}$) was placed at the forehead electrode. The subject sat in front of the stimulation panel about 45 cm and focused on one of the flickering visual stimuli. Fig. 7 shows circuits inside the handmade stimulation panel, including the SSVEP signal processor (implementation in FPGA), four visual stimuli, the RF command transmitter, the voice output circuit, the speaker driver, and the biofeedback speaker, etc. Each visual stimulus flickering uses only one white LED. The FPGA used to implement the SSVEP signal processor is Altera Cyclone EP2C20Q. Fig. 8 shows the photograph of the customized SSVEP acquisition module board and ADC module board. The experiment used three gold-plated EEG

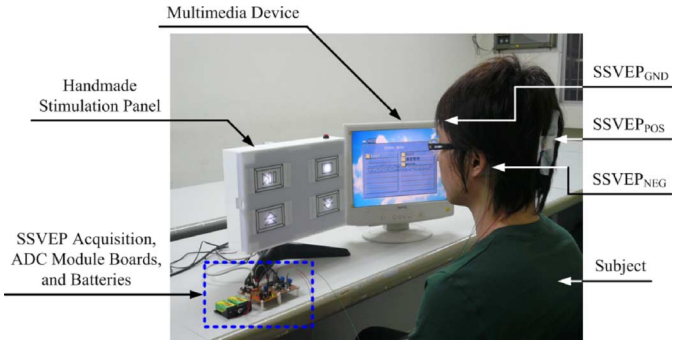

Fig. 9. Photograph of the SSVEP-based BCI multimedia device control system, with a subject participating in the experiment.

electrodes for acquiring the SSVEP signal from the scalp. The SSEVP acquisition module board included a preamplifier, filter, a postamplifier, and dc bias adjustment circuits. Two 9-V NI-MH rechargeable batteries supplied power to the SSVEP acquisition module board and ADC module board.

Fig. 9 shows a subject taking part in the proposed BCI system testing experiment. Four visual stimuli labeled with multimedia control command symbols (⏯, ⏹, ⏫, and ⏬) were arranged in the stimulation panel. Four flickering visual stimuli flashed at the same flickering frequency (21 Hz), but with four predefined phase delays (0°, 90°, 180°, and 270°), respectively. The customized SSVEP acquisition and ADC module boards acquired and quantified the subjects' SSVEP signal. The quantified SSVEP signal processes through the proposed SSVEP signal processor. Finally, the recognized result transmits through the RF command transmitter and then simultaneously feedbacks to the subject by the speaker.

Table I lists the results of identified command sequences from each subject during the test experiment. The experiment asked each subject to look at the corresponding stimulus one by one following the given command sequence (⏯ ⏹ ⏫ ⏬ ⏯ ⏹ ⏫ ⏬).

Table I shows the identified commands, total time, accuracy, command transfer interval (CTI), and information transfer rate (ITR), noting that the proposed BCI system works well and seven subjects reached high average identification accuracy 89.29%. The ITR is an important metric for evaluating the classifier performance of a BCI system. The ITR is computed by

$$\mathrm{ITR} = \left\{ \log_2 N + P\log_2 P + (1-P)\log_2\left[\frac{(1-P)}{(N-1)}\right] \right\} \times \left\{ \frac{60}{\mathrm{CTI}} \right\} \quad (3)$$

where N is the total number of stimuli and P is the accuracy [17]. The stimulation panel in the current study contained only four flickering visual stimuli ($N = 4$), and the mean ITR of the seven subjects who participated in the experiments was 24.67 b/min. Some previous studies have more flickering visual stimuli ([7]: 13; [9]: 25; [11]: 12; [13]: 48), and have higher ITRs (please see Table II). To improve the ITR, the system has to increase the command number by implementing a narrower phase margin between any two adjacent visual stimuli. Table II compares performances between the proposed system and previous studies. Three subjects had good identification results (100%), whereas two subjects showed poor identification accuracy (75%). The reason for these bad results could be that: 1) subjects lacked experience in the SSVEP-based BCI system, and did not know how to focus attention on the corresponding visual stimulus, 2) lower SNR due to individual variance caused

TABLE I
RESULTS OF THE PRODUCING COMMAND SEQUENCE: ⏯ ⏹ ⏫ ⏬ ⏯ ⏹ ⏫ ⏬ FROM SEVEN SUBJECTS

Subject	Identified commands (wrong underlined)	Total time (s)	Accuracy (correct / total)	CTI (s/cmd)	ITR (bits/min)
A	⏯ ⏹ ⏫ ⏬ ⏯ ⏹ ⏫ ⏬	26	100% (8/8)	3.25	36.92
B	⏯ ⏹ ⏫ ⏬ ⏯ ⏹ ⏫ ⏬	31	100% (8/8)	3.88	30.93
C	⏯ ⏹ ⏫ ⏫ ⏯ ⏹ ⏫ ⏬	32	87.5% (7/8)	4	18.87
D	⏯ ⏹ ⏫ ⏬ ⏯ ⏹ ⏫ ⏯	29	87.5% (7/8)	3.63	20.8
E	⏯ ⏹ ⏫ ⏬ ⏯ ⏯ ⏫ ⏯	37	75% (6/8)	4.63	10.27
F	⏯ ⏹ ⏫ ⏬ ⏯ ⏹ ⏫ ⏬	28	100% (8/8)	3.5	34.29
G	⏯ ⏹ ⏫ ⏹ ⏯ ⏯ ⏫ ⏬	28	75% (6/8)	3.5	13.59
Average		30.14	89.29%	3.77	24.67

TABLE II
COMPARISON BETWEEN THE PROPOSED SYSTEM AND PREVIOUS STUDIES

		Accuracy	CTI (s/cmd)	ITR (bits/min)	# of Stimuli
Proposed system	Phase Coding	89.29%	3.77	24.67	4
Cheng et al. [7]	Frequency Coding	78%	6.17	27.15	13
Friman et al. [9]		97.5%	5.28	27	25
Jia et al. [11]		94.8%	4.52	46.68	12
Gao et al. [13]		87.5%	3.8	68	48

TABLE III
COST COMPARISON BETWEEN PC-BASED AND FPGA-BASED BCI SYSTEM (IN US DOLLAR)

	EEG signal measurement equipment		Customized SSVEP measurement circuit	
SSVEP signal acquisition	ADInstrument Power Lab	≒ $2000	SSVEP acquisition module	≒ $20
	PC-based		FPGA-based	
SSVEP signal quantification	NI USB DAQ	≒ $169	ADC module	≒ $5
Real-time SSVEP signal processing	Personal computer	≒ $500	Altera EP2C20Q FPGA	≒ $100
Total		≒ $2669		≒ $125

by SSVEP amplitude, stimulus frequency, or electrode location. Subjects took different lengths of time to complete the task because to ensure the identified result, the same stimulus must be successfully detected in two consecutive times (two decisions). If two decisions in 60 epochs are not the same, the counter will reset. Only when two identical decisions are sequentially obtained will the identified command be outputted. This study designed a low-cost FPGA-based SSVEP BCI multimedia control system. Table III compares general costs between the existing EEG equipment-based/PC-based BCI system and the proposed FPGA-based system. The cost of the FPGA-based SSVEP BCI system with a customized SSVEP measurement circuit is much cheaper than the PC-based system with EEG signal measurement equipment. The FPGA-based BCI system also reduces complexity and maintenance costs, compared with the PC-based BCI system. Consequently, more seriously disabled patients can afford the BCI system.

The prototype of the SSVEP-based BCI multimedia device control system implemented in this paper verifies the feasibility of the low-cost BCI system. The proposed BCI system easily extends to other applications, such as fan or light control. Voice data used for the bioeedback also easily change for different languages, because the corresponding voice data (i.e., turn on/off the fan or light) easily rerecords into the EEPROM device through the microphone amplifier/filter and ADC module boards.

IV. CONCLUSION

This study successfully demonstrates the design of the low-cost FPGA-based SSVEP BCI multimedia control system. This research constructs a handmade stimulation panel to evoke the subject's SSVEP signal. Instead of using expensive EEG measurement equipment and universal-serial-bus (USB) or PCI DAQ cards, the current work designs an SSVEP acquisition circuit and an ADC module board to acquire and quantify the SSVEP. This research also adopts an FPGA to implement the SSVEP signal-processing algorithm. The design allows online processing of the SSVEP signal without the bulky personal computer accompanied with commercial signal-processing software. Furthermore, this study designs the RF transmitter/receiver and biofeedback voice output circuits for wirelessly communicating the SSVEP recognition result to external devices (multimedia device in this paper) and subject, respectively. Finally, experimental results verify the effectiveness of the proposed SSVEP-based BCI multimedia device control system through implementing the SSVEP-based BCI multimedia device control system. The current work realizes a low-cost SSVEP BCI computer-free system. The proposed SSVEP-based BCI multimedia device control system possibly allows seriously disabled patients to take greater care of themselves.

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Kuo-Kai Shyu (M'98) received the B.S. degree in electrical engineering from Tatung Institute of Technology, Taipei, Taiwan, in 1979, and the M.S. and Ph.D. degrees in electrical engineering from the National Chung-Kung University, Tainan, in 1984 and 1987, respectively.

In 1988, he joined the National Central University, Jhong-Li, where he is currently a Professor of the Department of Electrical Engineering. He had been the Chairman of the Department from 2004 to 2007. From 1988 to 1999, he was a Visiting Scholar with the Electrical and Computer Engineering Department, Auburn University, Auburn, AL. His teaching and research interests include variable structure control systems and signal processing with applications in motor control, power electronics, and biomedical systems.

Po-Lei Lee was born in 1973. He received the B.S. degree in electrical engineering from National Cheng-Kung University, Taiwan, in 1995, and the Ph.D. degree from the Institute of Biomedical Engineering, National Yang-Ming University, Taiwan, in 2000.

From 2001 to 2005, he was a Postdoctoral Fellow in the Taipei Veterans General Hospital, researching the signal and image-analysis procedures for electroencephalography and magnetoencephalography signals. He joined the Department of Electrical Engineering, National Central University, Taiwan, in 2005. His research interests include signal and image processing of EEG and MEG signals as well as designing the EEG-based brain–computer interfaces.

Ming-Huan Lee (S'09) was born in Taipei, Taiwan, in 1977. He received the B.S. degree in electronic engineering from the National United University, Miao-Li, in 2001, the M.S. degree in electrical engineering from the Chung-Hua University, Hsinchu, in 2003, and is currently pursuing the Ph.D. degree in electrical engineering at the National Central University, Jhong-Li.

His current research interests include algorithm hardware (FPGA or DSP) implementation, signal processing with applications in biomedical systems, and brain–computer interface design.

Mr. Lee received the Outstanding Research Graduate Student Award from the National Central University in 2008.

Ming-Hong Lin was born in Taipei, Taiwan, in 1984. He received the B.S. degree in electrical engineering from the National Chin Yi University of Technology, Taichung, Taiwan, in 2007, and the M.S. degree in electrical engineering from the National Central University, Jhong-Li, in 2009.

His current research interests include algorithm hardware implementation and signal processing.

Ren-Jie Lai was born in Yilan, Taiwan, in 1985. He received the B.S. degree in electrical engineering from the National Chin-Yi University of Technology, Taichung, Taiwan, in 2007, and the M.S. degree in electrical engineering from the National Central University, Jhong-Li, in 2009.

His current research interests include analog circuit implementation and biosignal processing.

Yun-Jen Chiu (S'09) was born in Kaohsiung, Taiwan, in 1984. He received the B.E. degree in electric engineering and the M.E. degree in automatic control engineering from the National Dong Hwa University, Hualien, Taiwan, in 2006 and 2008, respectively, and is currently pursuing the Ph.D. degree at the National Central University, Jhong-Li.

His current research interests include algorithm hardware implementation and signal processing.