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Release 14.6 Map P.68d (nt64)
Xilinx Map Application Log File for Design 'top'

Design Information
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Command Line   : map -intstyle pa -w fsm.ngd
Target Device  : xc7k325t
Target Package : ffg900
Target Speed   : -2
Mapper Version : kintex7 -- $Revision: 1.55 $
Mapped Date    : Sat Dec 07 13:07:49 2013

WARNING:LIT:701 - PAD symbol "Push_Buttons_TRI_I[0]" has an
undefined
   IOSTANDARD.
WARNING:LIT:702 - PAD symbol "Push_Buttons_TRI_I[0]" is not
constrained (LOC) to
   a specific location.
Mapping design into LUTs...
Running directed packing...
Running delay-based LUT packing...
Updating timing models...
INFO:Map:215 - The Interim Design Summary has been generated
in the MAP Report
   (.mrp).
Running timing-driven placement...
Total REAL time at the beginning of Placer: 1 mins 55 secs
Total CPU  time at the beginning of Placer: 1 mins 51 secs

Phase 1.1  Initial Placement Analysis
Phase 1.1  Initial Placement Analysis (Checksum:c69c7d96) REAL
time: 2 mins 27 secs

Phase 2.7  Design Feasibility Check
INFO:Place:834 - Only a subset of IOs are locked. Out of 27
IOs, 15 are locked
   and 12 are not locked. If you would like to print the names
of these IOs,
   please set the environment variable
XIL_PAR_DESIGN_CHECK_VERBOSE to 1.
Phase 2.7  Design Feasibility Check (Checksum:c69c7d96) REAL
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time: 2 mins 27 secs

Phase 3.31  Local Placement Optimization
Phase 3.31  Local Placement Optimization (Checksum:abecd095)
REAL time: 2 mins 27 secs

Phase 4.2  Initial Placement for Architecture Specific Features
....
Phase 4.2  Initial Placement for Architecture Specific Features
(Checksum:da70bdeb) REAL time: 2 mins 40 secs

Phase 5.30  Global Clock Region Assignment
Phase 5.30  Global Clock Region Assignment (Checksum:da70bdeb)
REAL time: 2 mins 40 secs

Phase 6.3  Local Placement Optimization
....
Phase 6.3  Local Placement Optimization (Checksum:88be3dc)
REAL time: 2 mins 48 secs

Phase 7.5  Local Placement Optimization
Phase 7.5  Local Placement Optimization (Checksum:99f259cb)
REAL time: 2 mins 48 secs

Phase 8.8  Global Placement
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Phase 8.8  Global Placement (Checksum:b82947e) REAL time: 5
mins 13 secs

Phase 9.5  Local Placement Optimization
Phase 9.5  Local Placement Optimization (Checksum:b82947e)
REAL time: 5 mins 14 secs

Phase 10.18  Placement Optimization
Phase 10.18  Placement Optimization (Checksum:a91e59a6) REAL
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time: 7 mins 5 secs

Phase 11.5  Local Placement Optimization
Phase 11.5  Local Placement Optimization (Checksum:a91e59a6)
REAL time: 7 mins 5 secs

Phase 12.34  Placement Validation
Phase 12.34  Placement Validation (Checksum:a91e59a6) REAL
time: 7 mins 6 secs

Total REAL time to Placer completion: 9 mins 19 secs
Total CPU  time to Placer completion: 8 mins 59 secs
Running post-placement packing...
Writing output files...
WARNING:PhysDesignRules:372 - Gated clock. Clock net

uBlaze_i/axi_hwicap_0/axi_hwicap_0/HWICAP_CTRL_I/icap_statemac
hine_I1/icap_ns
   tate_cs[3]_PWR_54_o_Mux_51_o is sourced by a combinatorial
pin. This is not
   good design practice. Use the CE pin to control the loading
of data into the
   flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net
dynamic_i/clk_1hz is
   sourced by a combinatorial pin. This is not good design
practice. Use the CE
   pin to control the loading of data into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net

uBlaze_i/axi_hwicap_0/axi_hwicap_0/HWICAP_CTRL_I/icap_statemac
hine_I1/icap_ns
   tate_cs[3]_PWR_52_o_Mux_47_o is sourced by a combinatorial
pin. This is not
   good design practice. Use the CE pin to control the loading
of data into the
   flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net

uBlaze_i/axi_hwicap_0/axi_hwicap_0/HWICAP_CTRL_I/icap_statemac
hine_I1/icap_ns
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   tate_cs[3]_PWR_53_o_Mux_49_o is sourced by a combinatorial
pin. This is not
   good design practice. Use the CE pin to control the loading
of data into the
   flip-flop.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM1_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM2_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM3_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
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WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM4_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM8_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM7_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO
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_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM5_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.RX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM6_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM1_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM3_RAMD_O>
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   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM7_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM8_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM4_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
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NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM2_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM6_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/QSPI_FLASH/QSPI_FLASH/QSPI_LEGACY_MD_GEN.QSPI_CORE_I
NTERFACE_I/FIFO

_EXISTS.TX_FIFO_II/USE_2N_DEPTH.V6_S6_AND_LATER.I_ASYNC_FIFO_B
RAM/U0/xst_fifo

_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mr
am_RAM5_RAMD_O>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0_d_bram_ctrl_2_microblaze_0_bram_block_B
RAM_Addr[30]>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performance.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[14].ram32m_i_RAMD_D1_O> is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performance.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[15].ram32m_i_RAMD_D1_O> is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performance.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[8].ram32m_i_RAMD_D1_O> is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performance.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[13].ram32m_i_RAMD_D1_O> is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performance.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[10].ram32m_i_RAMD_D1_O> is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa

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nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[7].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[2].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[12].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0_d_bram_ctrl_2_microblaze_0_bram_block_B
RAM_Addr[31]>
   is incomplete. The signal does not drive any load pins in
the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[3].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[1].ram32m_i_RAMD_D1_O>
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is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[0].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[11].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[5].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[4].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[9].ram32m_i_RAMD_D1_O>
is incomplete.
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   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:367 - The signal

<uBlaze_i/microblaze_0/microblaze_0/MicroBlaze_Core_I/Performa
nce.Data_Flow_I

/Register_File_I/Using_LUT6.All_RAM32M[6].ram32m_i_RAMD_D1_O>
is incomplete.
   The signal does not drive any load pins in the design.
WARNING:PhysDesignRules:2383 - Issue with pin connections
and/or configuration
   on

block:<uBlaze_i/axi_hwicap_0/axi_hwicap_0/HWICAP_CTRL_I/IPIC_I
F_I/STARTUP_INC
   LUDE.GEN_7Series_STARTUP.STARTUPE2_inst>:<STARTUP_STARTUP>.
 USRDONEO and/or
   USRDONETS are tied low. This will cause the DONE pin to go
low after
   configuration.  If this behavior is not intended, please
tie these inputs
   high.
WARNING:PhysDesignRules:2452 - The IOB LEDs_TRI_O[3] is either
not constrained
   (LOC) to a specific location and/or has an undefined I/O
Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB LEDs_TRI_O[4] is either
not constrained
   (LOC) to a specific location and/or has an undefined I/O
Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB LEDs_TRI_O[5] is either
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not constrained
   (LOC) to a specific location and/or has an undefined I/O
Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB LEDs_TRI_O[6] is either
not constrained
   (LOC) to a specific location and/or has an undefined I/O
Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB LEDs_TRI_O[0] is either
not constrained
   (LOC) to a specific location and/or has an undefined I/O
Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB LEDs_TRI_O[1] is either
not constrained
   (LOC) to a specific location and/or has an undefined I/O
Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB LEDs_TRI_O[2] is either
not constrained
   (LOC) to a specific location and/or has an undefined I/O
Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
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   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB Push_Buttons_TRI_I[3]
is either not
   constrained (LOC) to a specific location and/or has an
undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB Push_Buttons_TRI_I[4]
is either not
   constrained (LOC) to a specific location and/or has an
undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB Push_Buttons_TRI_I[1]
is either not
   constrained (LOC) to a specific location and/or has an
undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB Push_Buttons_TRI_I[2]
is either not
   constrained (LOC) to a specific location and/or has an
undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB Push_Buttons_TRI_I[0]
is either not
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   constrained (LOC) to a specific location and/or has an
undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the
device and will be an
   error in bitstream creation. It should be corrected by
properly specifying
   the pin location and I/O Standard.

Design Summary
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Design Summary:
Number of errors:      0
Number of warnings:   53
Slice Logic Utilization:
  Number of Slice Registers:                2,734 out of
407,600    1%
    Number used as Flip Flops:              2,696
    Number used as Latches:                     3
    Number used as Latch-thrus:                 0
    Number used as AND/OR logics:              35
  Number of Slice LUTs:                     3,020 out of
203,800    1%
    Number used as logic:                   2,572 out of
203,800    1%
      Number using O6 output only:          1,962
      Number using O5 output only:            114
      Number using O5 and O6:                 496
      Number used as ROM:                       0
    Number used as Memory:                    338 out of
64,000    1%
      Number used as Dual Port RAM:           160
        Number using O6 output only:           96
        Number using O5 output only:            0
        Number using O5 and O6:                64
      Number used as Single Port RAM:           0
      Number used as Shift Register:          178
        Number using O6 output only:          176
        Number using O5 output only:            1
        Number using O5 and O6:                 1
    Number used exclusively as route-thrus:   110
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      Number with same-slice register load:    103
      Number with same-slice carry load:         6
      Number with other load:                    1

Slice Logic Distribution:
  Number of occupied Slices:                 1,445 out of
50,950    2%
  Number of LUT Flip Flop pairs used:        3,851
    Number with an unused Flip Flop:         1,360 out of
3,851   35%
    Number with an unused LUT:                 831 out of
3,851   21%
    Number of fully used LUT-FF pairs:       1,660 out of
3,851   43%
    Number of unique control sets:             224
    Number of slice register sites lost
      to control set restrictions:             938 out of
407,600    1%

  A LUT Flip Flop pair for this architecture represents one
LUT paired with
  one Flip Flop within a slice.  A control set is a unique
combination of
  clock, reset, set, and enable signals for a registered
element.
  The Slice Logic Distribution report is not meaningful if the
design is
  over-mapped for a non-slice resource or if Placement fails.
  OVERMAPPING of BRAM resources should be ignored if the
design is
  over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:
  Number of bonded IOBs:                      27 out of
500    5%
    Number of LOCed IOBs:                     15 out of
27   55%
    IOB Flip Flops:                            3

Specific Feature Utilization:
  Number of RAMB36E1/FIFO36E1s:                32 out of
```

```
445    7%
    Number using RAMB36E1 only:                32
    Number using FIFO36E1 only:                 0
  Number of RAMB18E1/FIFO18E1s:                 2 out of
890    1%
    Number using RAMB18E1 only:                 2
    Number using FIFO18E1 only:                 0
  Number of BUFG/BUFGCTRLs:                     4 out of
32   12%
    Number used as BUFGs:                       3
    Number used as BUFGCTRLs:                   1
  Number of IDELAYE2/IDELAYE2_FINEDELAYs:       0 out of
500    0%
  Number of ILOGICE2/ILOGICE3/ISERDESE2s:       0 out of
500    0%
  Number of ODELAYE2/ODELAYE2_FINEDELAYs:       0 out of
150    0%
  Number of OLOGICE2/OLOGICE3/OSERDESE2s:       3 out of
500    1%
    Number used as OLOGICE2s:                   3
    Number used as OLOGICE3s:                   0
    Number used as OSERDESE2s:                  0
  Number of PHASER_IN/PHASER_IN_PHYs:           0 out of
40    0%
  Number of PHASER_OUT/PHASER_OUT_PHYs:         0 out of
40    0%
  Number of BSCANs:                             1 out of
 4   25%
  Number of BUFHCEs:                            0 out of
168    0%
  Number of BUFRs:                              0 out of
40    0%
  Number of CAPTUREs:                           0 out of
 1    0%
  Number of DNA_PORTs:                          0 out of
 1    0%
  Number of DSP48E1s:                           3 out of
840    1%
  Number of EFUSE_USRs:                         0 out of
 1    0%
  Number of FRAME_ECCs:                         0 out of
```

```
 1    0%
  Number of GTXE2_CHANNELs:                       0 out of
16    0%
  Number of GTXE2_COMMONs:                        0 out of
 4    0%
  Number of IBUFDS_GTE2s:                         0 out of
 8    0%
  Number of ICAPs:                                1 out of
 2   50%
  Number of IDELAYCTRLs:                          0 out of
10    0%
  Number of IN_FIFOs:                             0 out of
40    0%
  Number of MMCME2_ADVs:                          1 out of
10   10%
  Number of OUT_FIFOs:                            0 out of
40    0%
  Number of PCIE_2_1s:                            0 out of
 1    0%
  Number of PHASER_REFs:                          0 out of
10    0%
  Number of PHY_CONTROLs:                         0 out of
10    0%
  Number of PLLE2_ADVs:                           1 out of
10   10%
  Number of STARTUPs:                             1 out of
 1  100%
  Number of XADCs:                                0 out of
 1    0%

Average Fanout of Non-Clock Nets:                4.23

Peak Memory Usage:  1321 MB
Total REAL time to MAP completion:  9 mins 28 secs
Total CPU time to MAP completion:   9 mins 7 secs

Mapping completed.
See MAP report file "fsm.mrp" for details.
```