KC705 MultiBoot Design

July 2012

XTP104

Revision History

Date	Version	Description
07/25/12	3.0	Recompiled for 14.2. Added AR50886.
05/08/12	2.0	Recompiled for 14.1.
01/18/12	1.0	Initial version for 13.4.

Overview

- Kintex-7 MultiBoot Capability
- Overview of 7 Series Fallback MultiBoot
- Xilinx KC705 Board
- Software Requirements
- KC705 Setup
- Compiling the MultiBoot Design
- Run MultiBoot Design
- Kintex-7 MultiBoot Details
- References

Note: This presentation applies to the KC705

Kintex-7 MultiBoot Capability

- **What is MultiBoot?**
  - The MultiBoot feature allows the FPGA application to load two or more FPGA bitstreams under the control of the FPGA application. The FPGA application triggers a MultiBoot operation, causing the FPGA to reconfigure from a different configuration bitstream. After a MultiBoot operation is triggered, the FPGA restarts its configuration process as usual.
  - More details can be found in UG470
- **MultiBoot Capability**
  - FPGA application controlled configuration
  - Bitstream selection of multiple applications
- **Safe Update**
  - Golden bitstream
  - Upgradeable bitstream
  - Failure recovery
    - Possible Triggers (CRC error, IDCODE error, WDT timeout)

Note: Presentation applies to the KC705

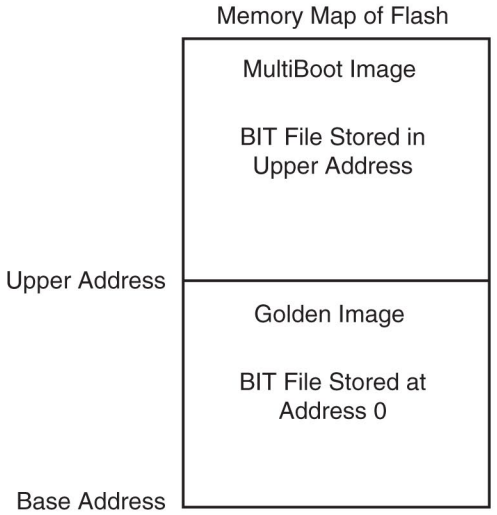
Kintex-7 MultiBoot Capability

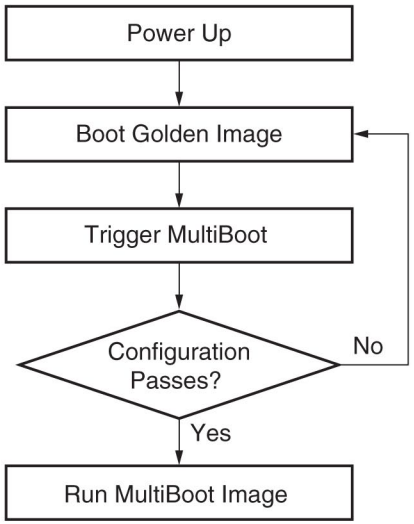
- **Overview of 7 Series Fallback MultiBoot**
  - The 7 series FPGAs MultiBoot and fallback features support updating systems in the field. Bitstream images can be upgraded dynamically in the field. The FPGA MultiBoot feature enables switching between images on the fly. When an error is detected during the MultiBoot configuration process, the FPGA can trigger a fallback feature that ensures a known good design can be loaded into the device.
  - The MultiBoot feature allows the FPGA application to load two or more FPGA bitstreams under the control of the FPGA application. The FPGA application triggers a MultiBoot operation, causing the FPGA to reconfigure from a different configuration bitstream. After a MultiBoot operation is triggered, the FPGA restarts its configuration process as usual.
- **Reference Design Source and Application**
  - rdf0104.zip
  - Available through http://www.xilinx.com/kc705

Note: Presentation applies to the KC705

KC705 MultiBoot Design Description

- **Description**
  - Design consists of three bitstreams, golden_iprog_spi.bit, multiboot.bit, and corrupted.bit loaded in the PROM at 0x0, 0x400000, and 0x800000
  - The golden_iprog_spi.bit has software to allow a reboot to the second or third bitstreams with certain switch settings
  - The multiboot.bit is compiled with “-g ConfigFallback:Enable” bitgen option
  - The corrupted.bit is the multiboot.bit with one byte changed to force a CRC error when loaded
- **This diagram shows the general process**
  - Since the corrupted.bit doesn’t pass configuration, the Golden Image is booted





Note: Presentation applies to the KC705

Upgrade Example

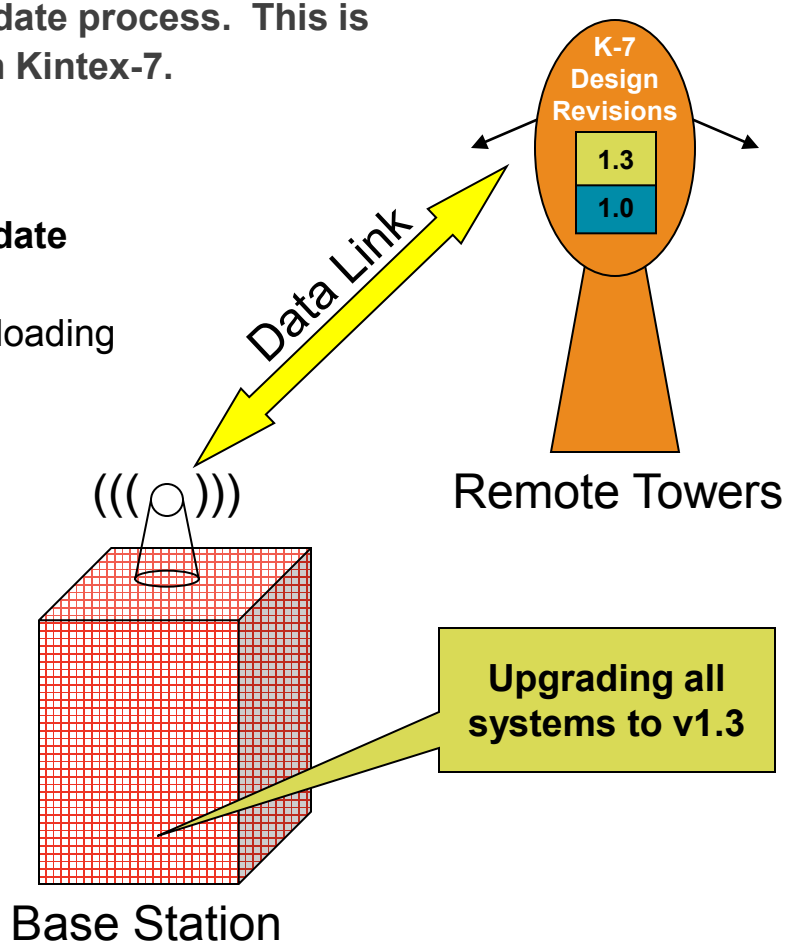
- **MultiBoot:** **Process by which the FPGA selectively reprograms and reloads its bitstream from an attached external memory.**
- **Safe update:** **Field updating bitstream storage with a new bitstream in such a manner to prevent any failure due to a failure in the update process. This is accomplished with the enhanced MultiBoot available in Kintex-7.**

Can a multi-boot system be implemented without safe update design considerations?

Yes – If there are no potential for disruptions during flash loading

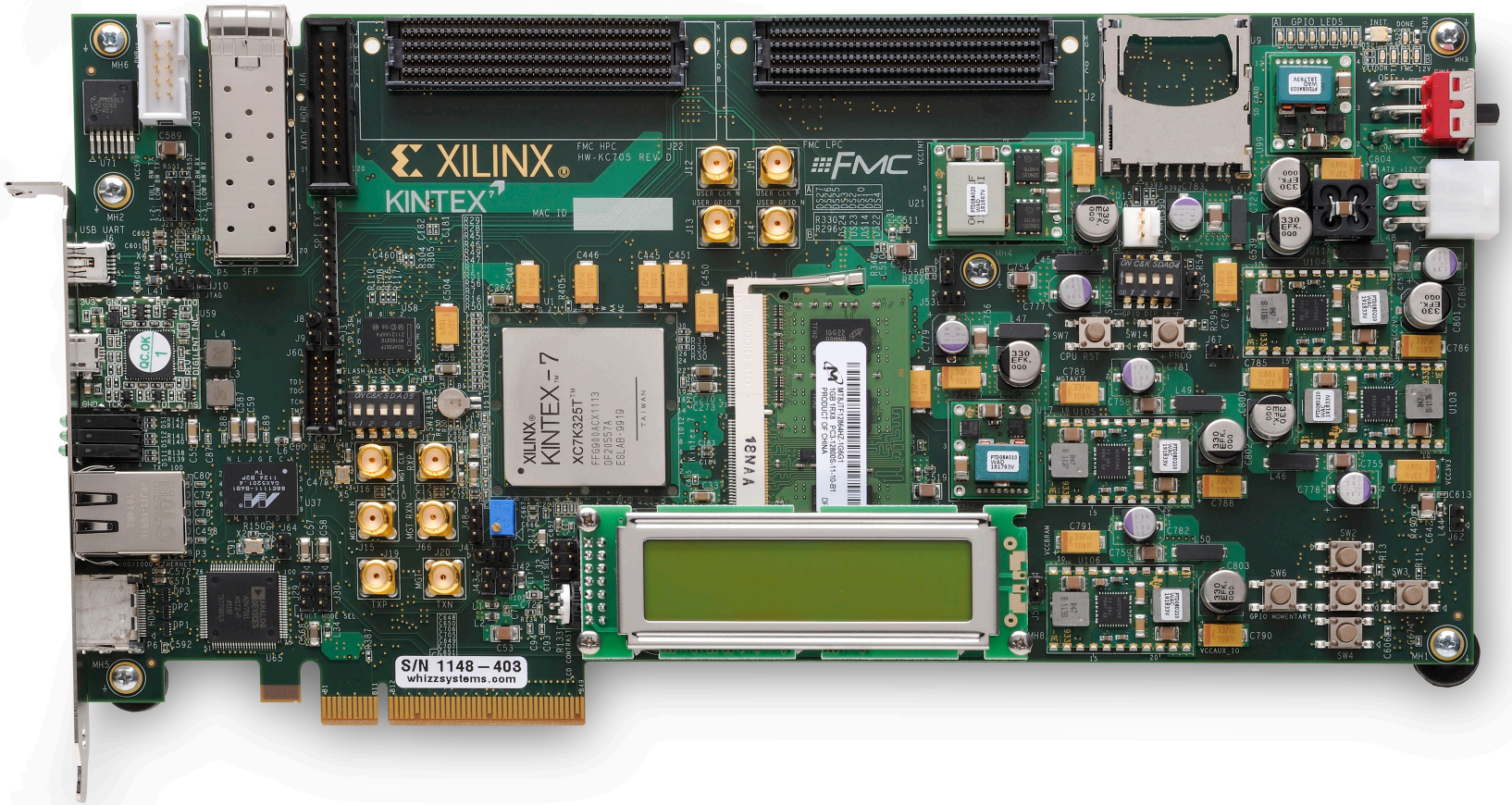
How is a system upgraded?

1. New multi-boot image is created
2. System setup to receive the new image
3. User application erases section of Flash
4. The new image is delivered into the system's Flash
5. User application resets system



Note: Presentation applies to the KC705

Xilinx KC705 Board



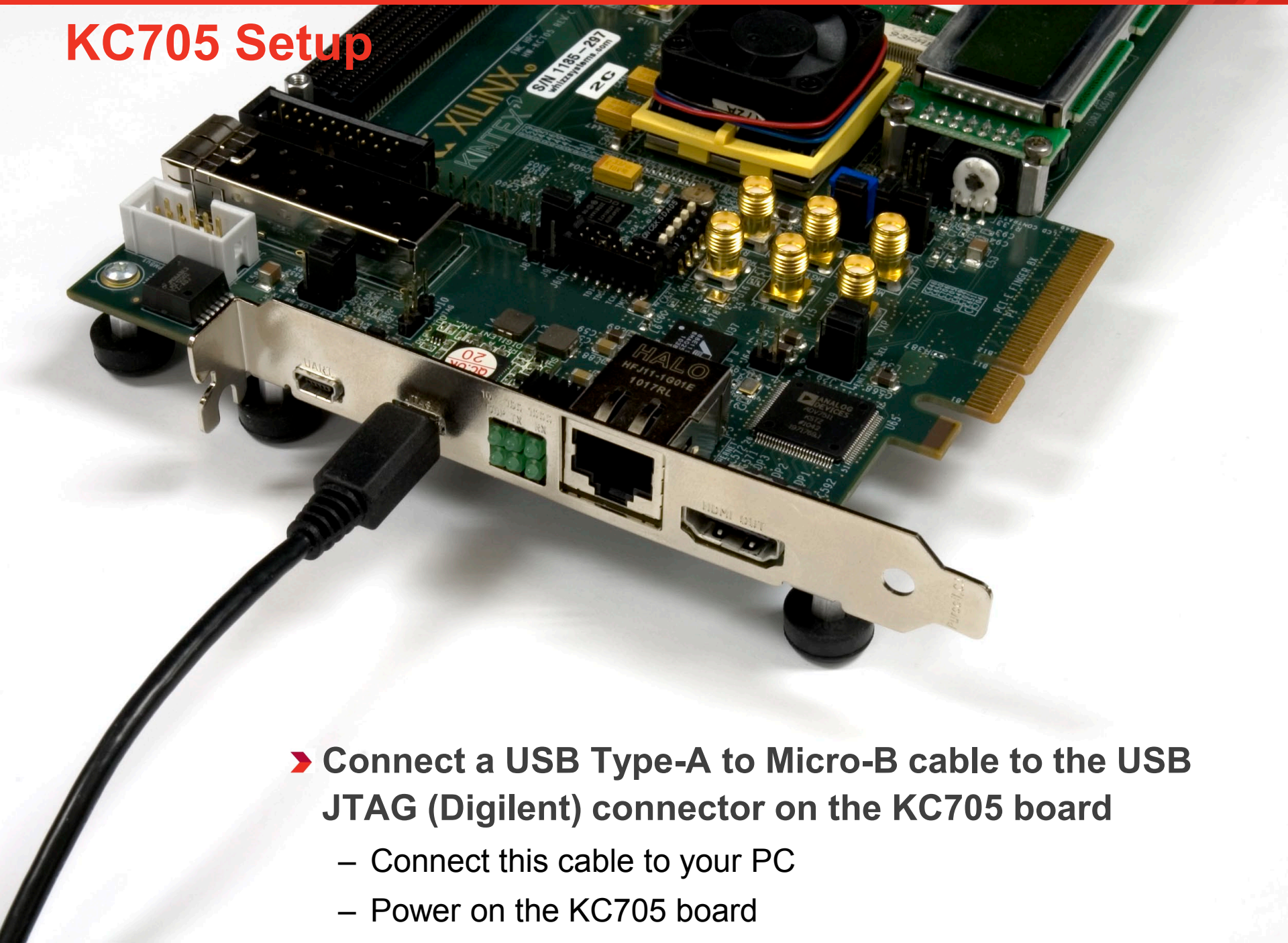
Note: Presentation applies to the KC705

ISE Software Requirement

- **Xilinx ISE 14.2 software**
  - Apply AR50886

Note: Presentation applies to the KC705

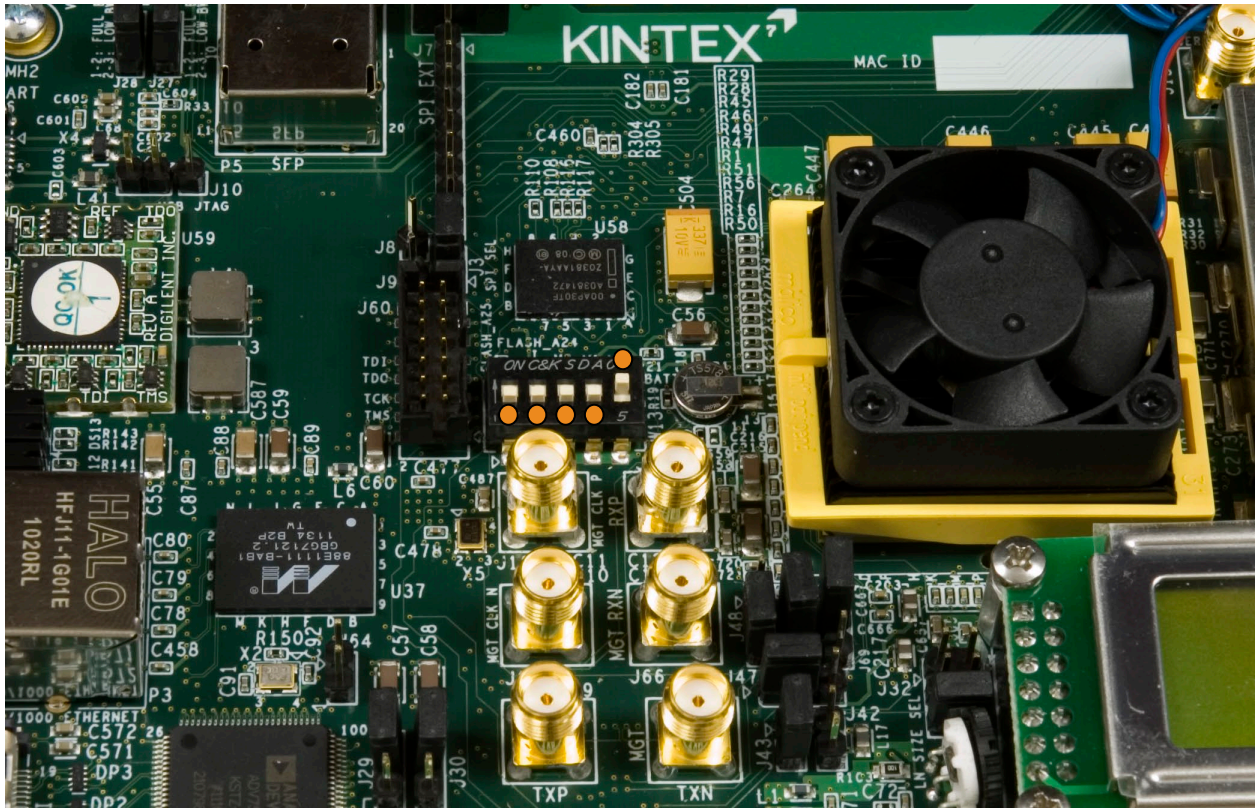
KC705 Setup



- Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board
  - Connect this cable to your PC
  - Power on the KC705 board

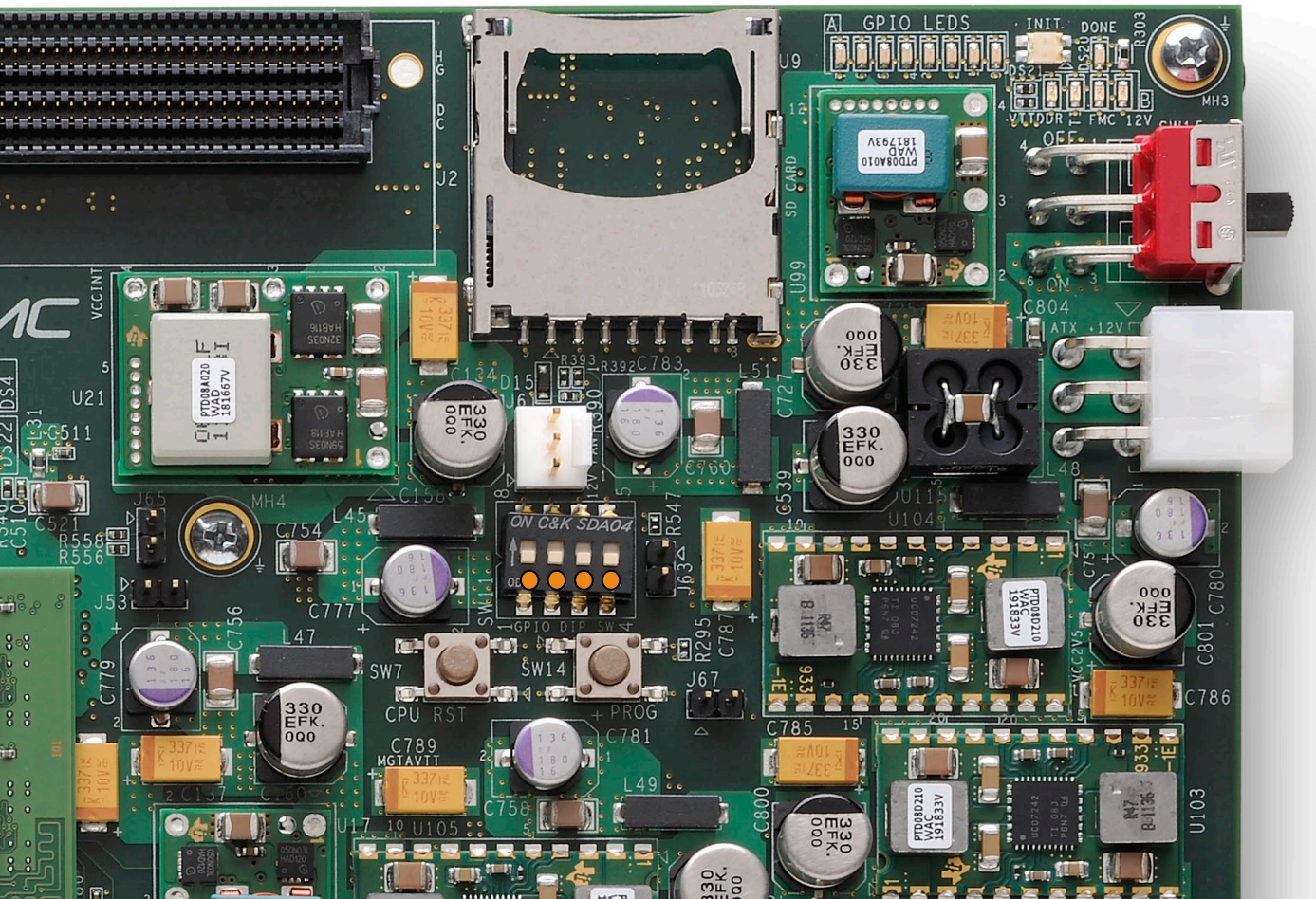
Hardware Setup

- **Set S13 to 00001 (1 = on, Position 1 → Position 5)**
  - This enables Master SPI configuration from the QSPI Flash
    - Flash A25, A24 = 00
    - FPGA mode pins M[2:0] = 001



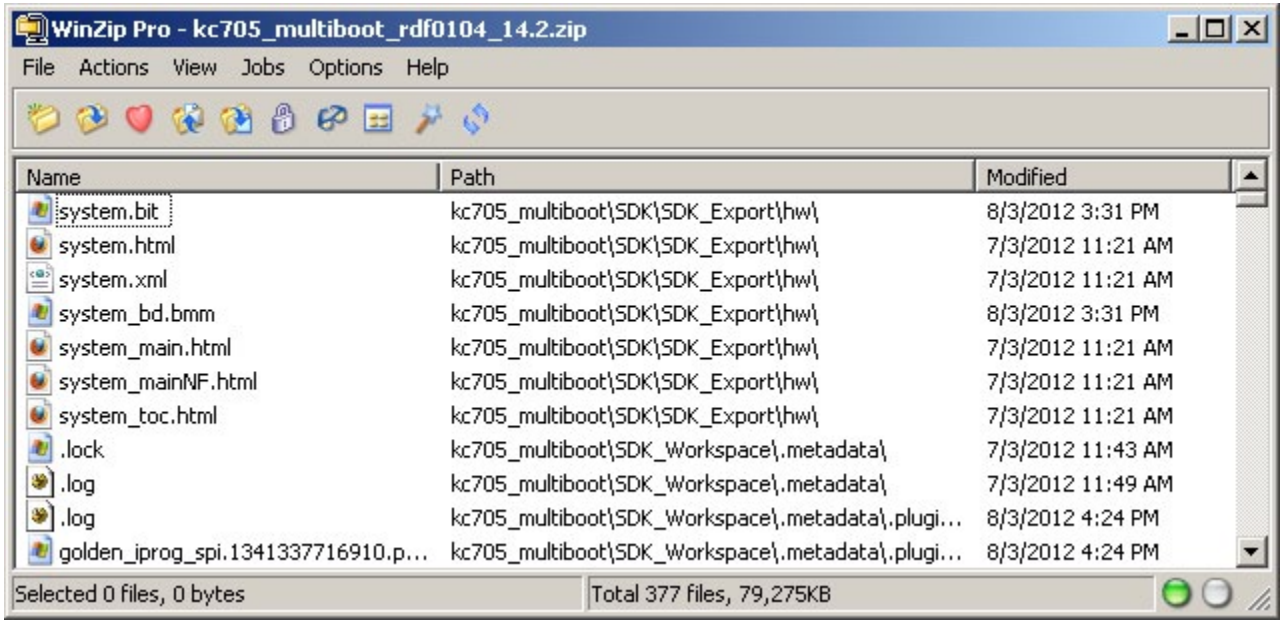
Hardware Setup

- **Set S11 to 0000 (1 = on, Position 1 → Position 4)**
  - This sets the MultiBoot functions to off



Program SPI MultiBoot Design

- **Unzip the KC705 Multiboot Design Files (14.2 CES)**
  - Available through http://www.xilinx.com/kc705



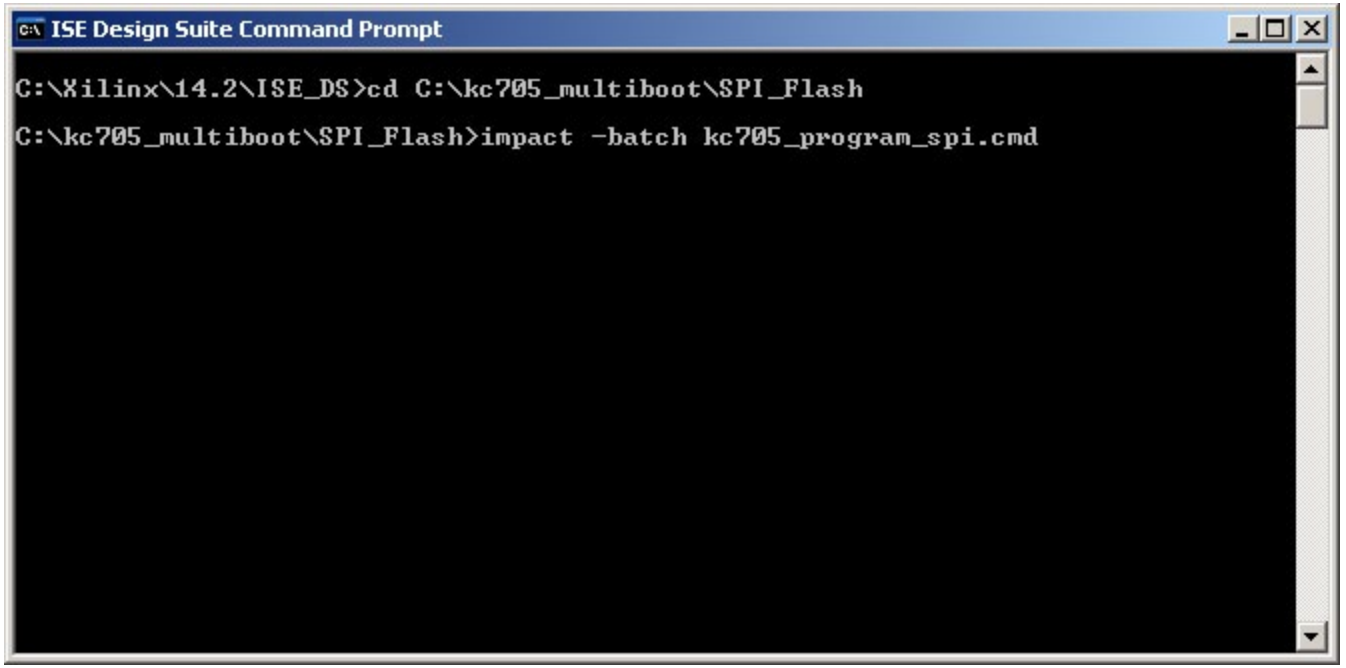
Note: Presentation applies to the KC705

Program SPI MultiBoot Design

- Open an ISE Design Suite Command Prompt and type:

  cd C:\kc705_multiboot\SPI_Flash

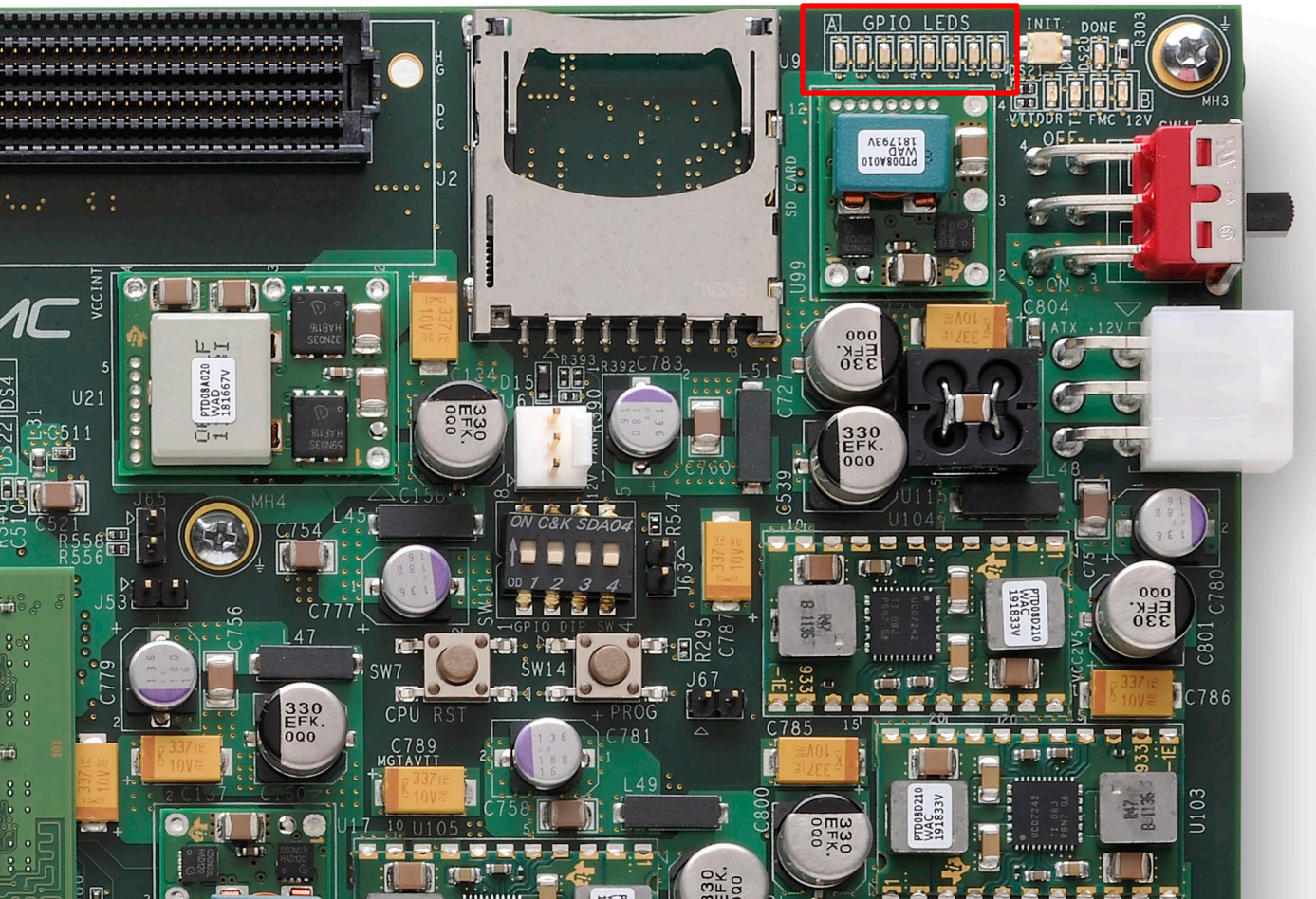
  impact -batch kc705_program_spi.cmd



Note: Takes about ten minutes

Run MultiBoot Design

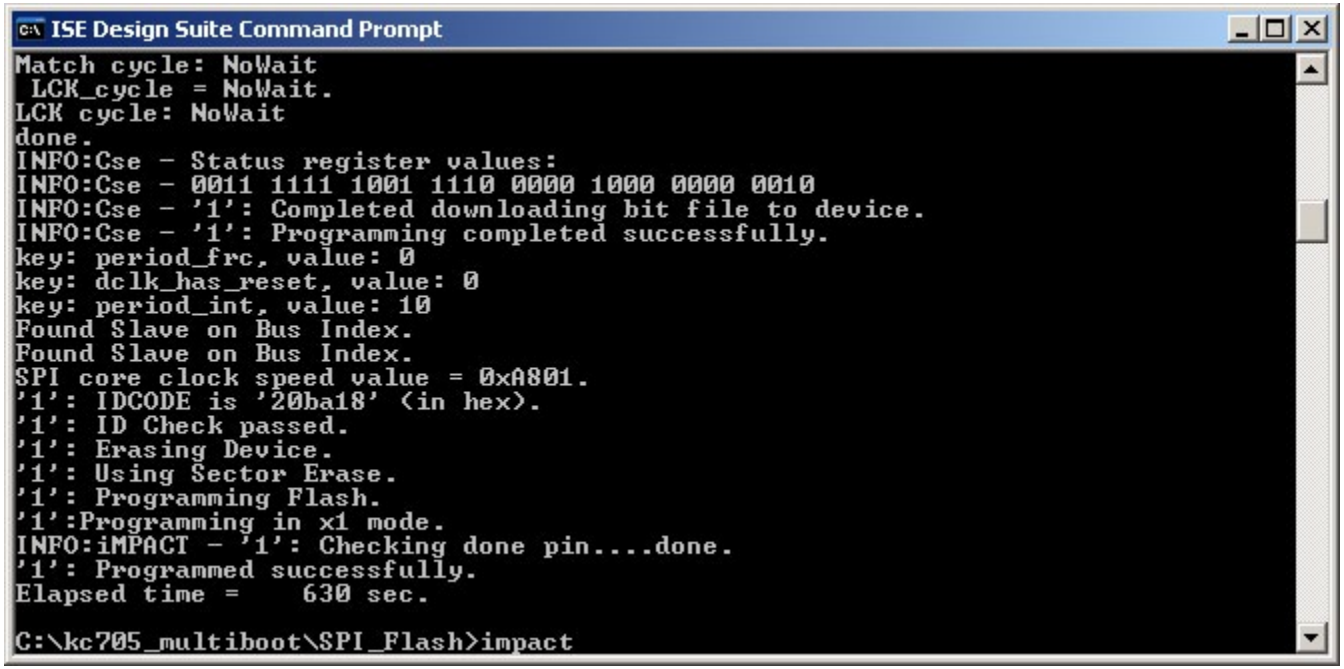
- The initial design, “golden_iprog_spi.bit”, shows a cycling LED pattern on the GPIO LEDs



Run MultiBoot Design

- Run iMPACT:

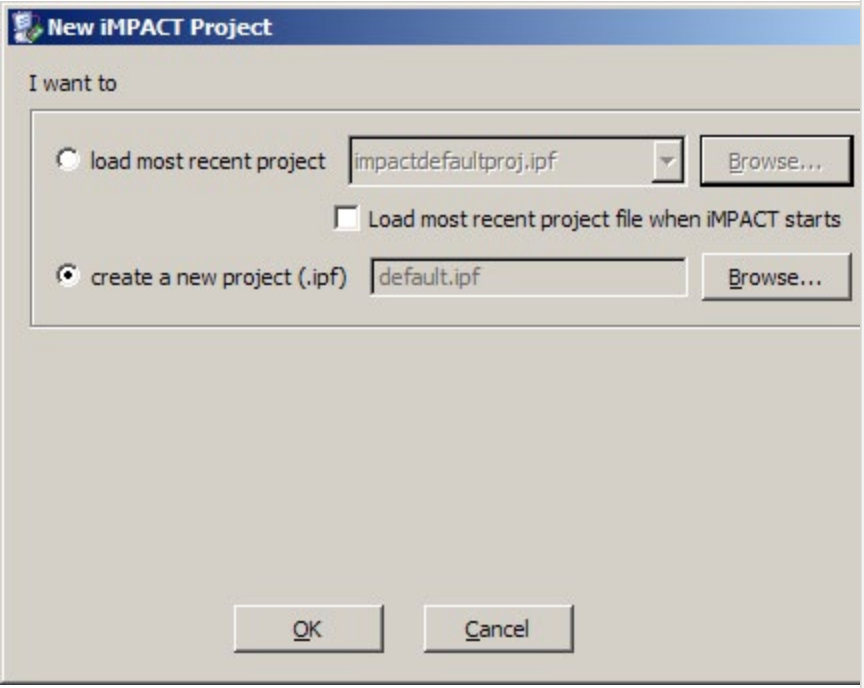
  impact

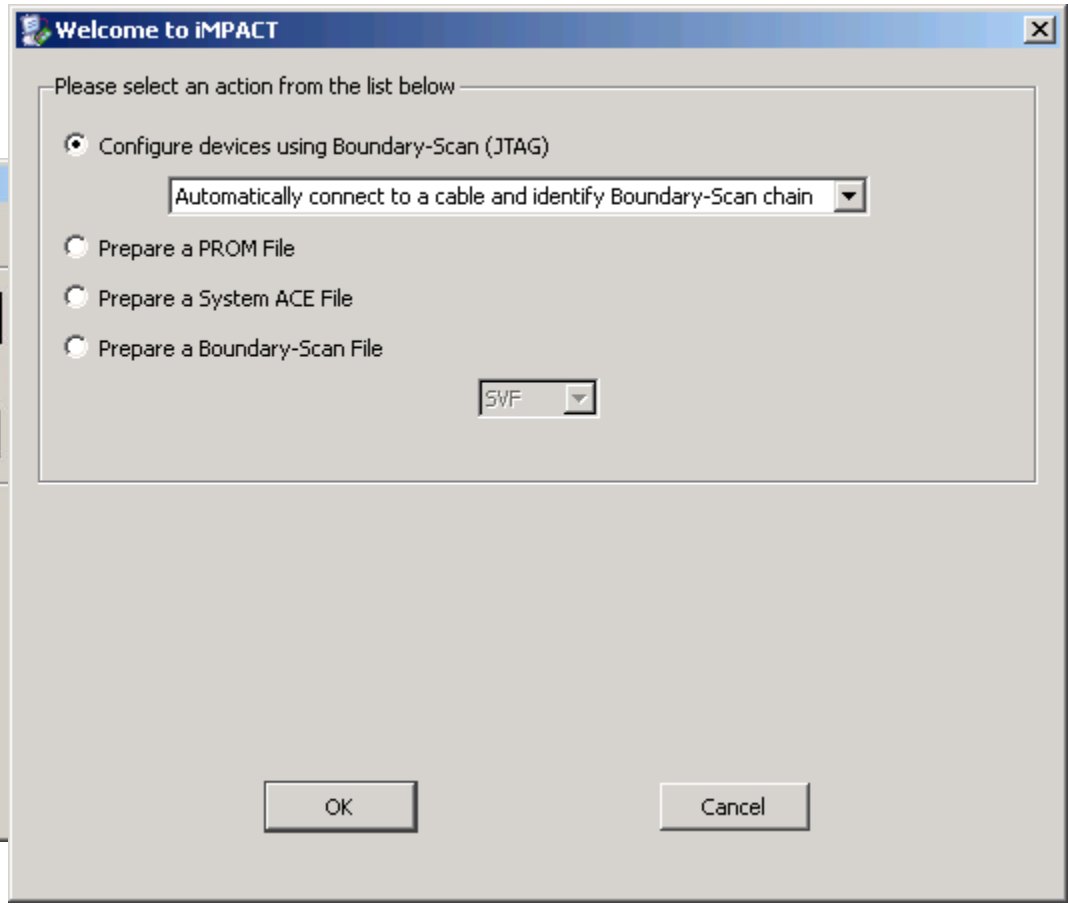


Note: Presentation applies to the KC705

Run MultiBoot Design

- **Select**
  - Create a new project
  - Configure devices using Boundary-Scan (JTAG)

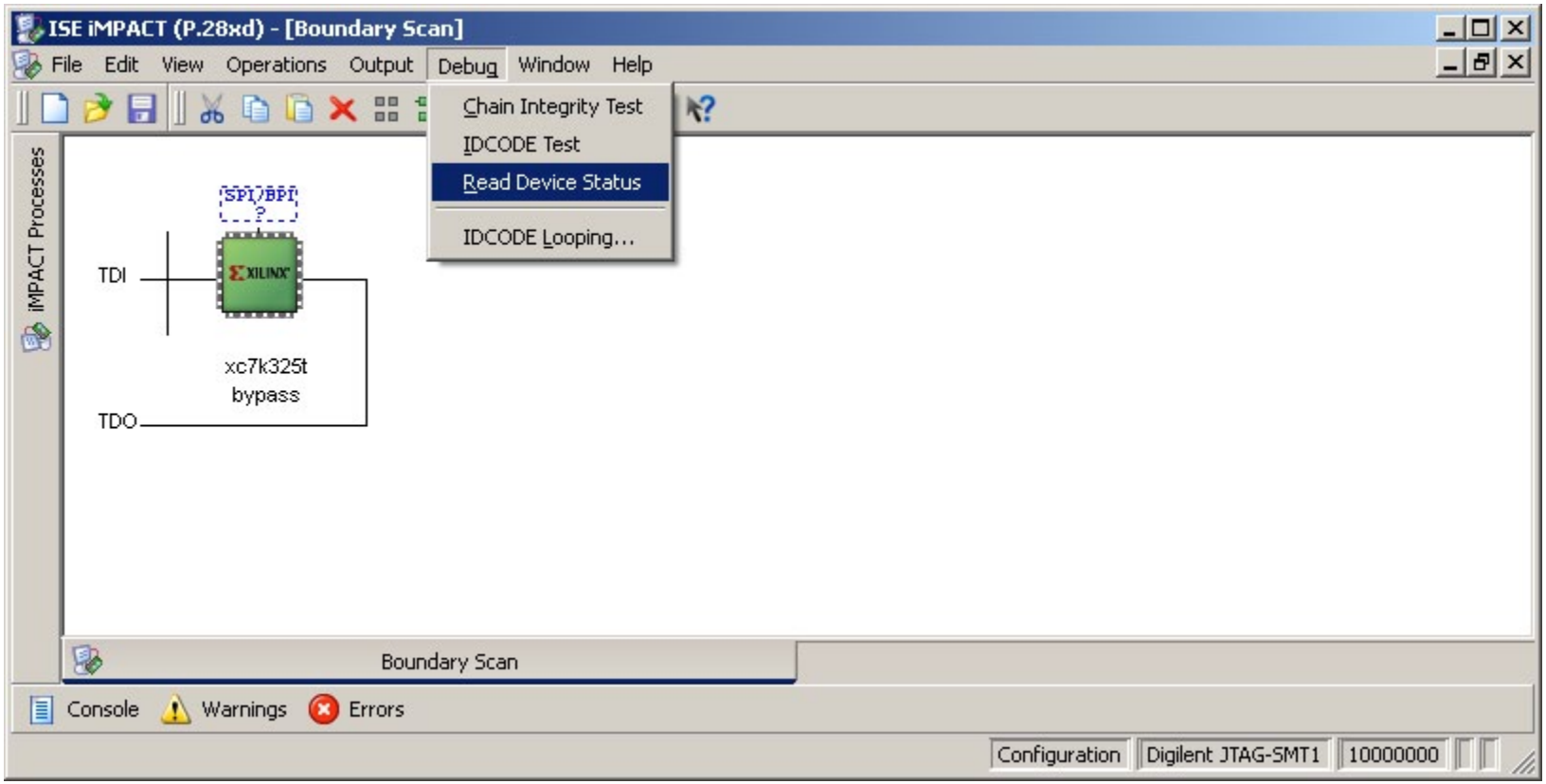




Note: Presentation applies to the KC705

Run MultiBoot Design

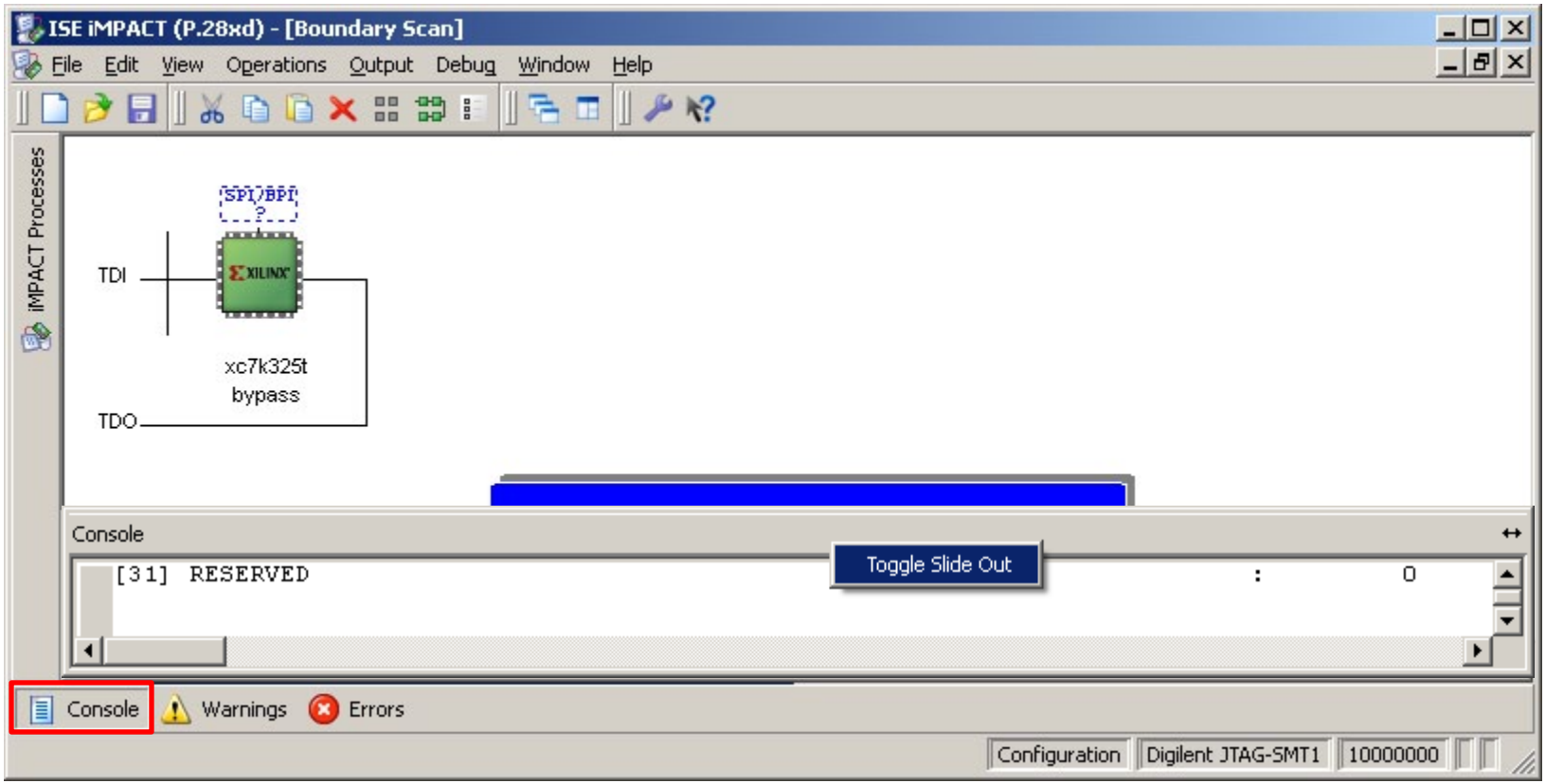
- Select the FPGA
- Select the menu item Debug → Read Device Status



Note: Presentation applies to the KC705

Run MultiBoot Design

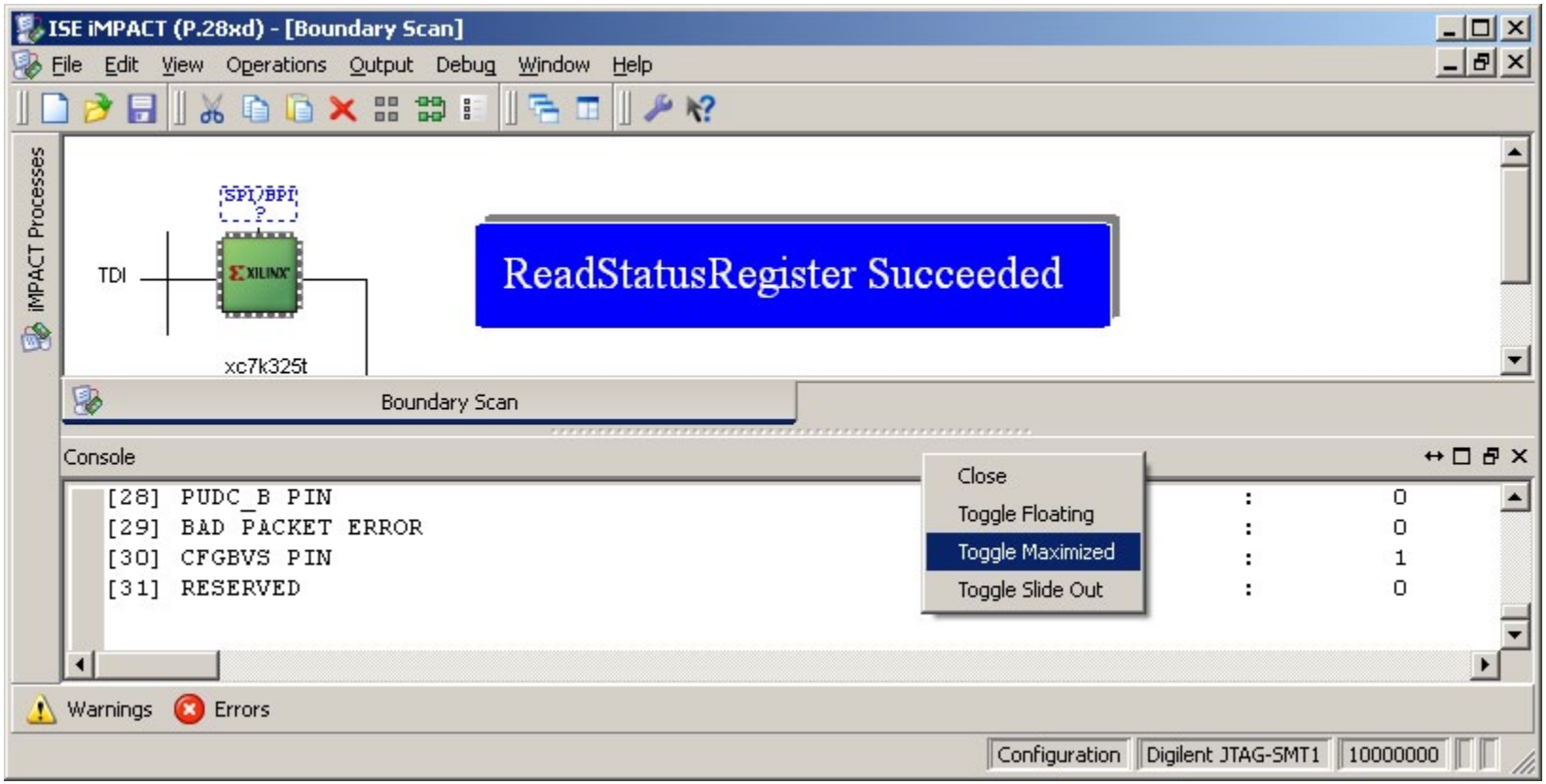
- Click console tab and then right click on the console panel and select “Toggle Slide Out”



Note: Presentation applies to the KC705

Run MultiBoot Design

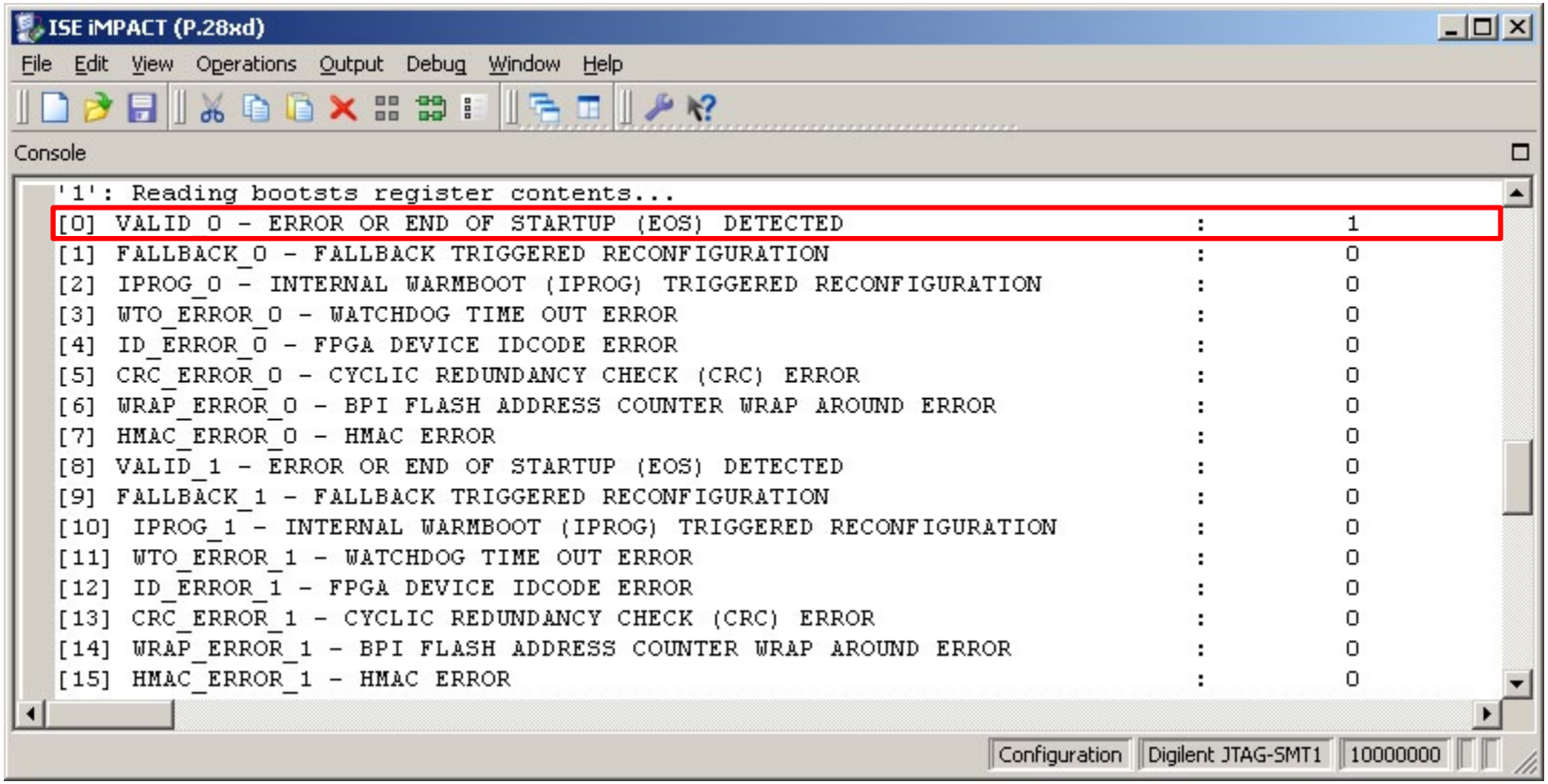
- Right click on the Console panel and select Toggle Maximized



Note: Presentation applies to the KC705

Run MultiBoot Design

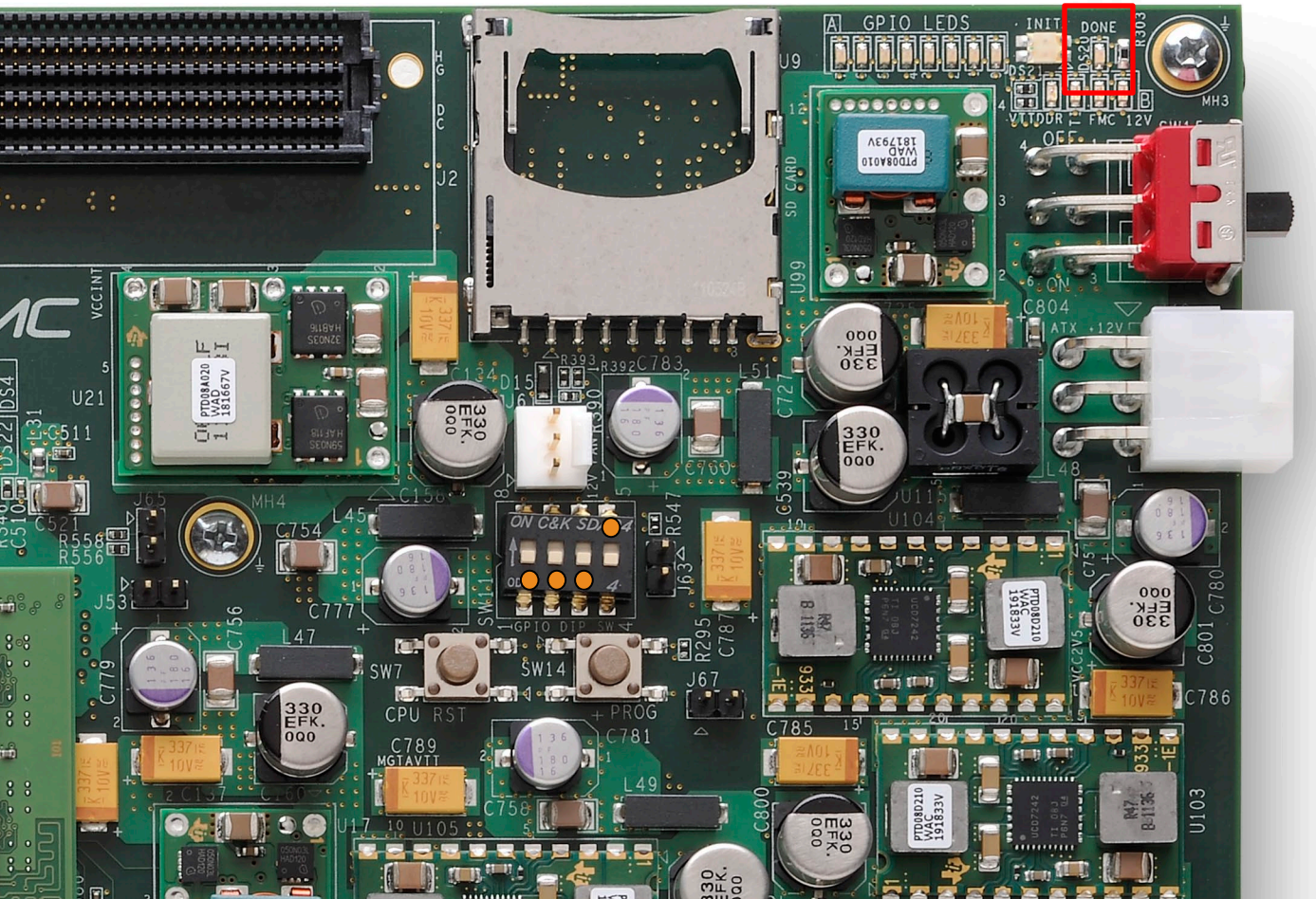
- Scroll to the “Reading bootsts register contents…” message
- Since this was a regular boot, only “VALID_0” is set



Note: Presentation applies to the KC705

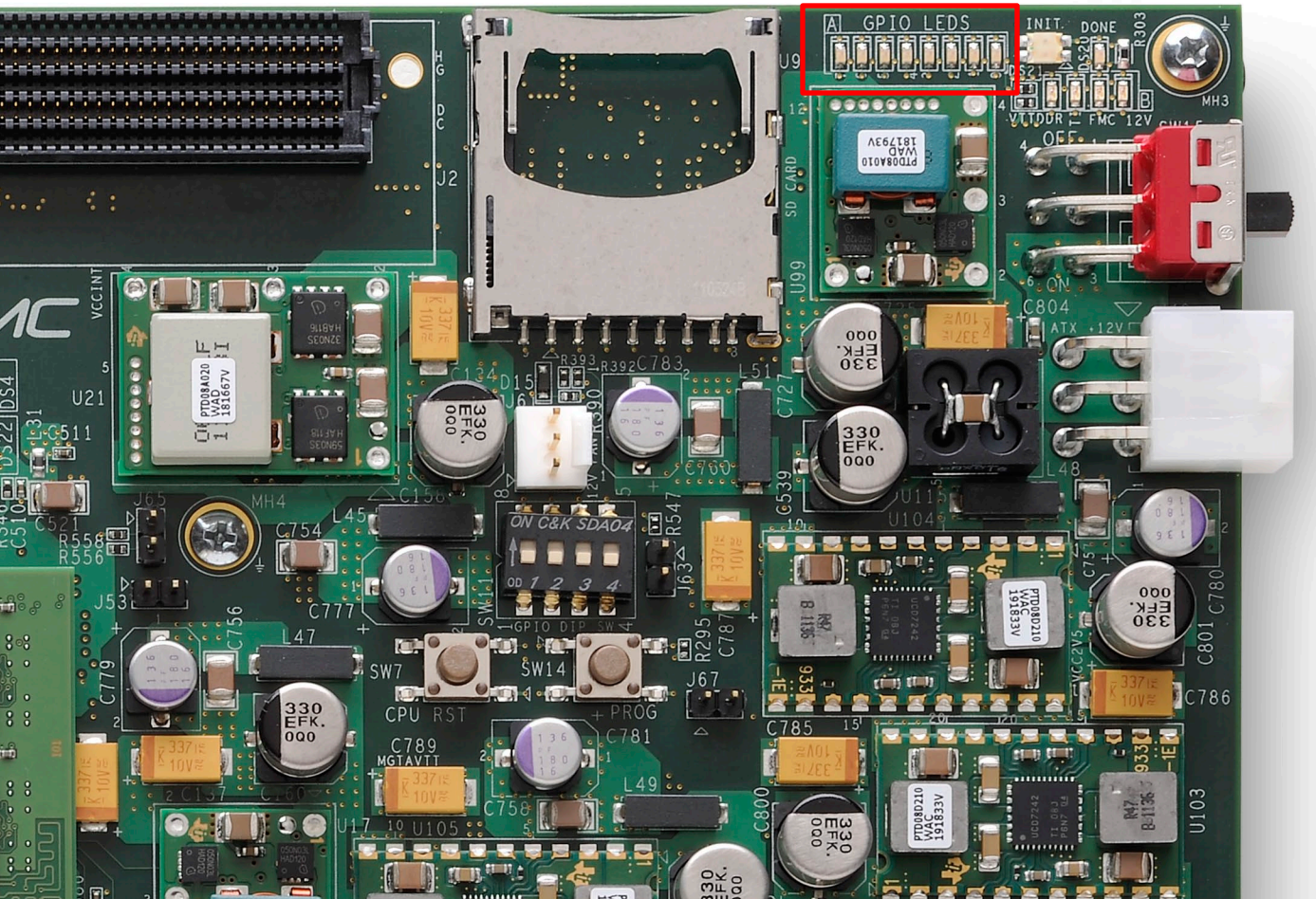
Run MultiBoot Design

- **Set S11 to 0001 (1 = on, Position 1 → Position 4)**
  - Issues an IPROG command to re-configure from a good MultiBoot bitstream
  - Set it back to 0000 when the DONE LED goes out



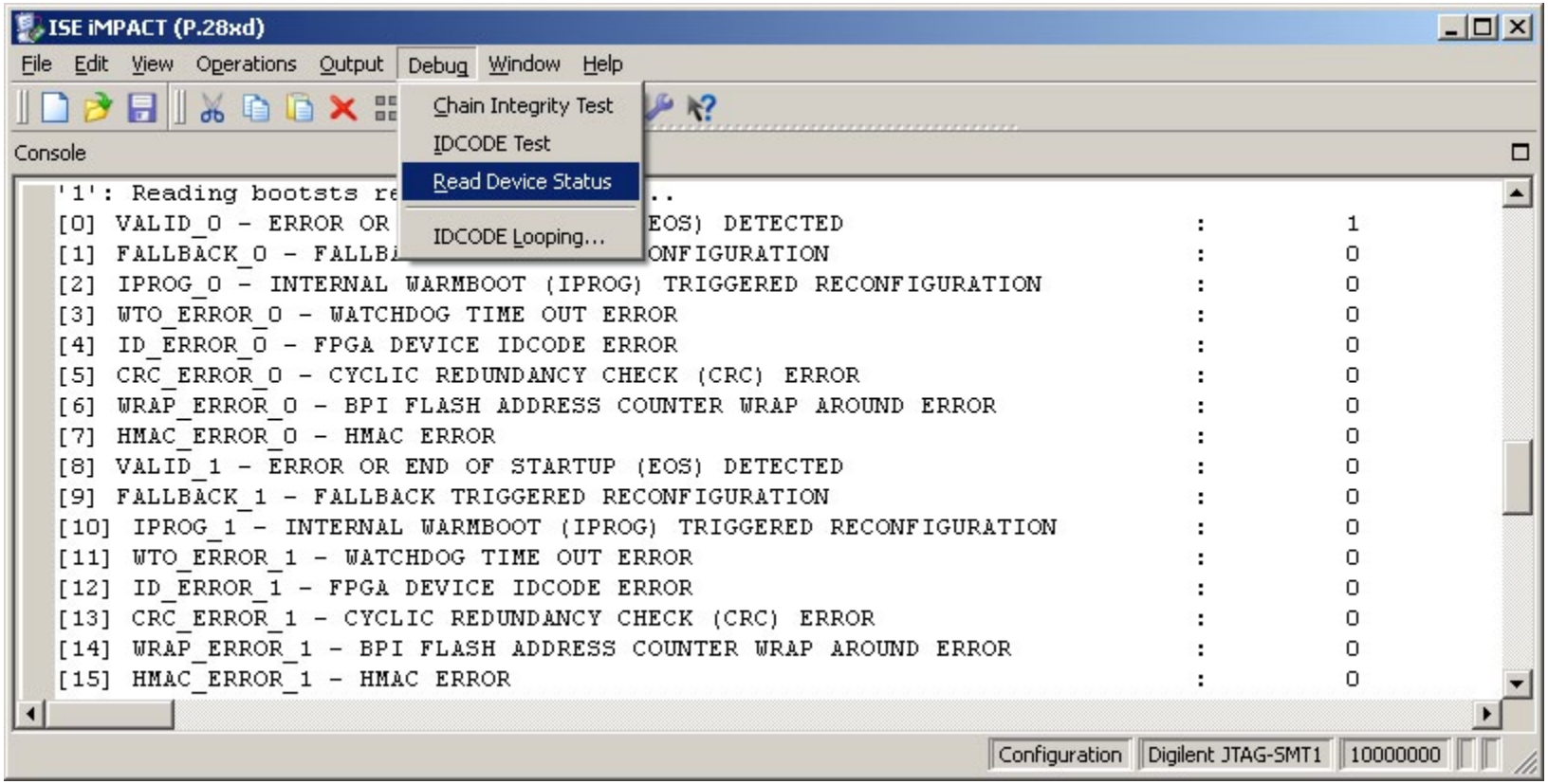
Run MultiBoot Design

- The MultiBoot design, “multiboot.bit”, shows a rapid blinking LED pattern on the GPIO LEDs



Run MultiBoot Design

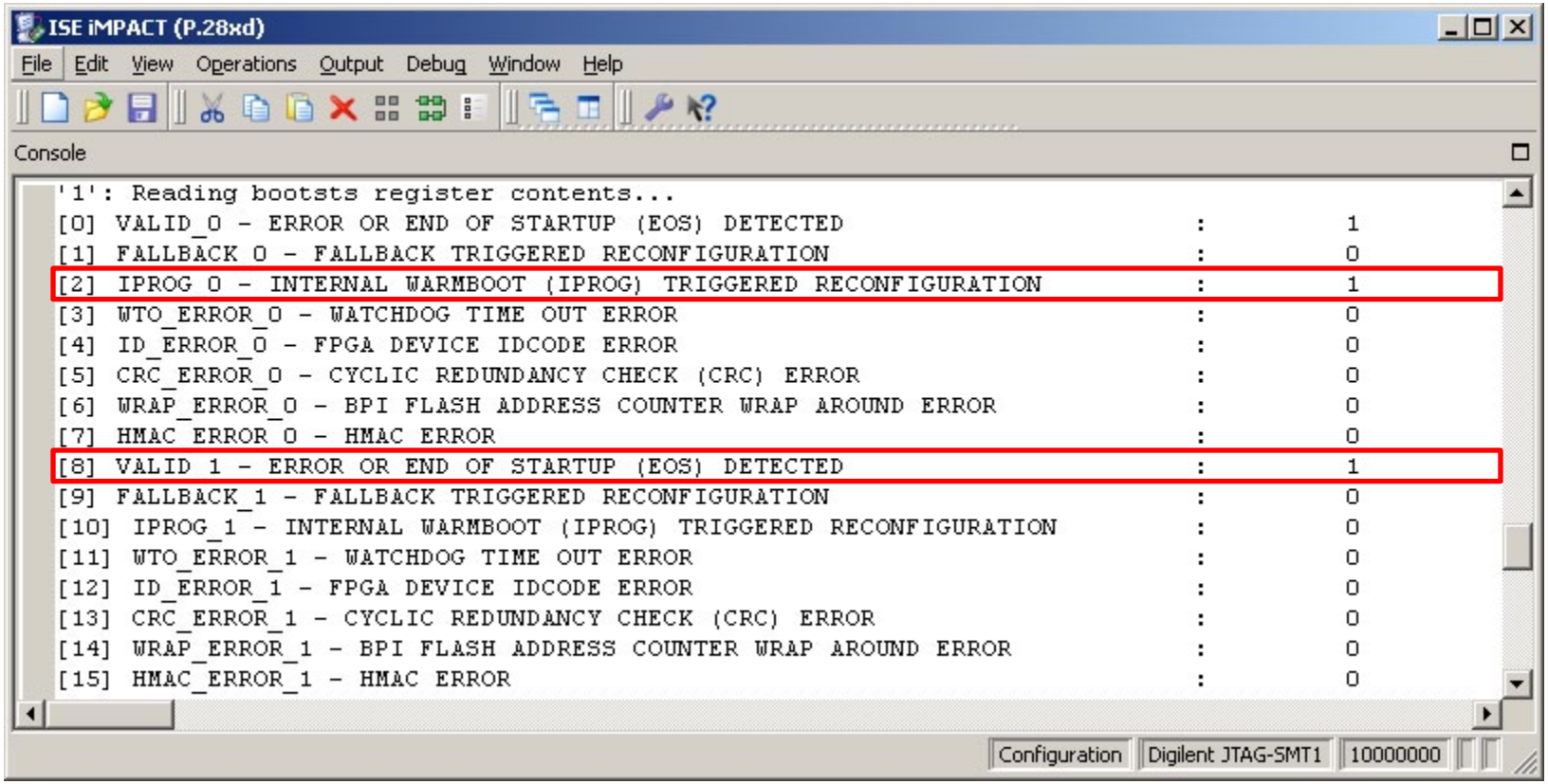
- Select the menu item Debug → Read Device Status
- Scroll down to the “Reading bootsts register contents…” message



Note: Presentation applies to the KC705

Run MultiBoot Design

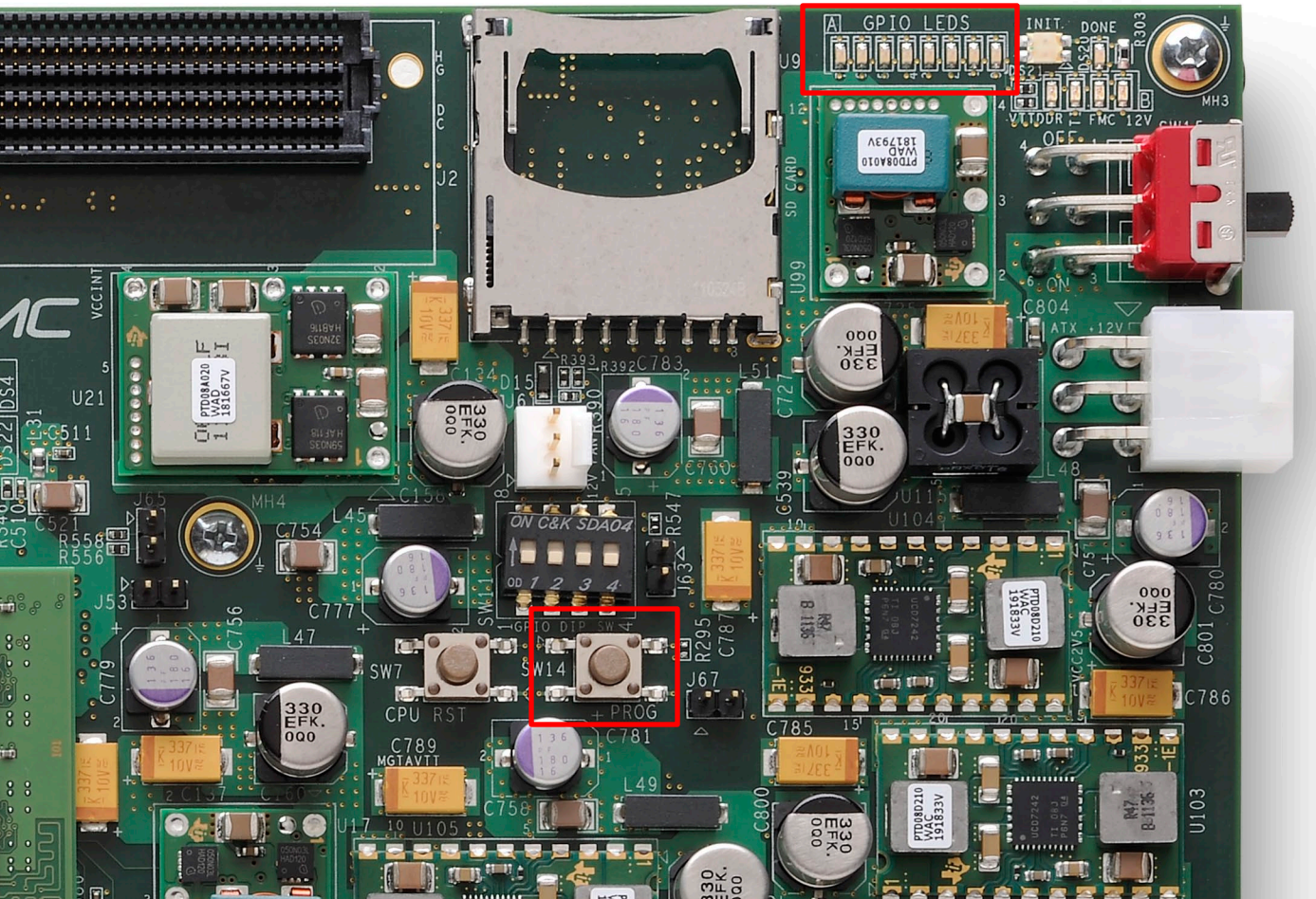
- The following status register messages are now set:
  - IPROG_0
  - VALID_1



Note: Presentation applies to the KC705

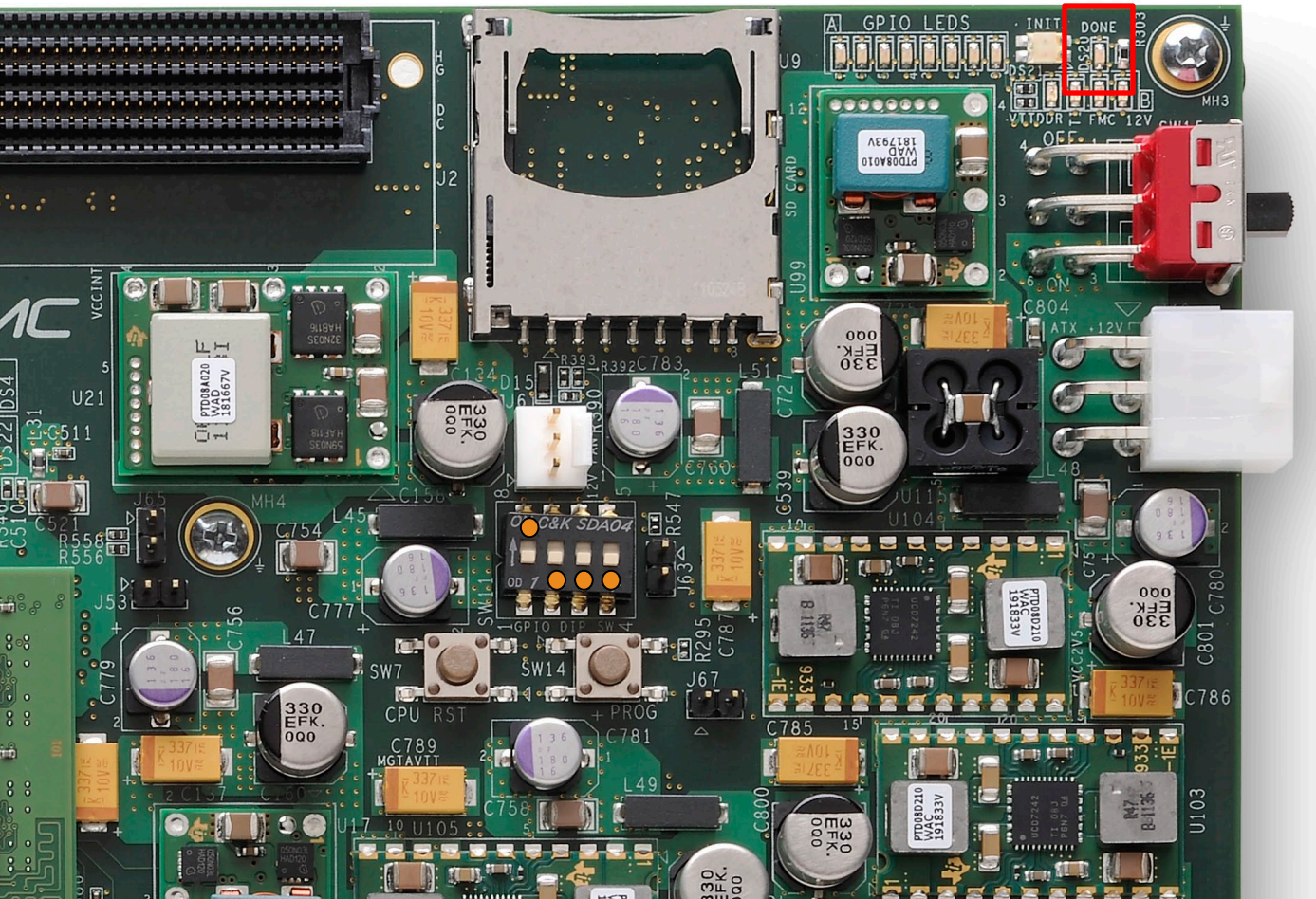
Run MultiBoot Design

- Press PROG to return to the golden bitstream
- Wait until you see the cycling pattern on the LEDs



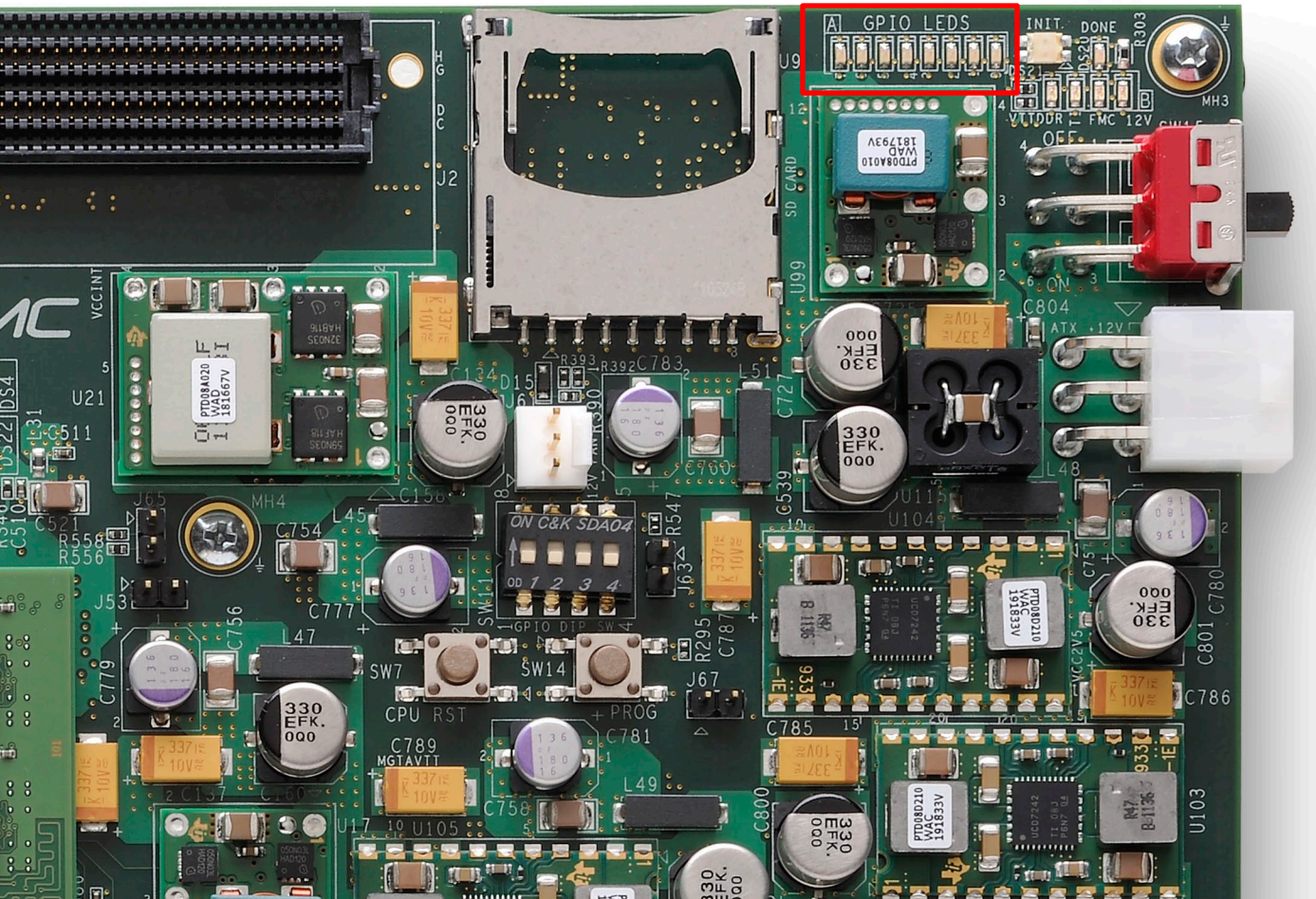
Run MultiBoot Design

- **Set S11 to 1000 (1 = on, Position 1 → Position 4)**
  - Issues an IPROG command to re-configure from a corrupted MultiBoot bitstream
  - Set it back to 0000 when the DONE LED goes out



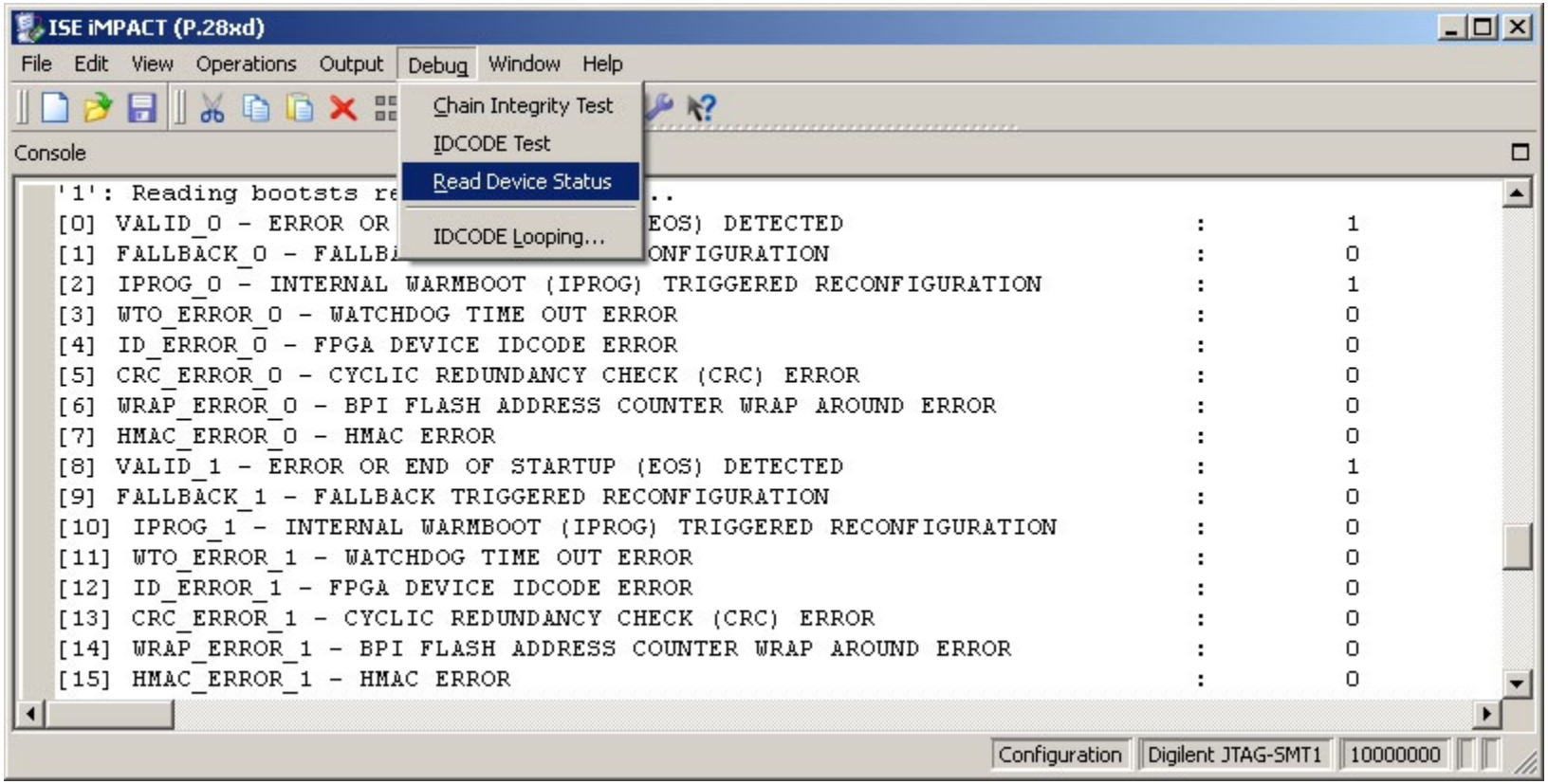
Run MultiBoot Design

- The corrupted.bit generates a CRC error and cannot load the FPGA
- The FPGA falls back to the golden bitstream with a cycling LED pattern



Run MultiBoot Design

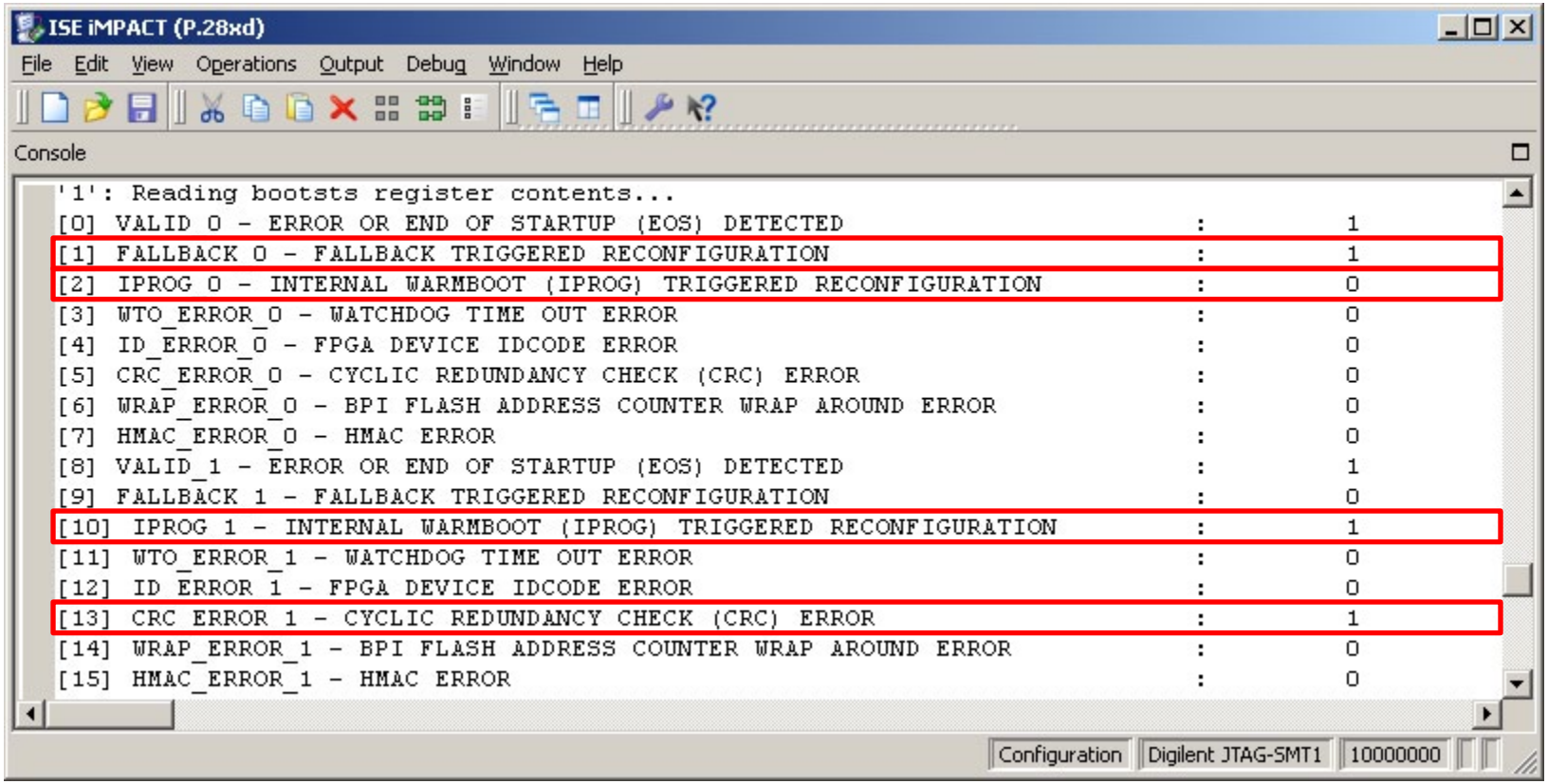
- Select the menu item Debug → Read Device Status
- Scroll down to the “Reading bootsts register contents…” message



Note: Presentation applies to the KC705

Run MultiBoot Design

- **The following status register messages are now seen:**
  - IPROG_0 is no longer active
  - FALLBACK_0, IPROG_1, and CRC_ERROR_1 are now active



Note: Presentation applies to the KC705

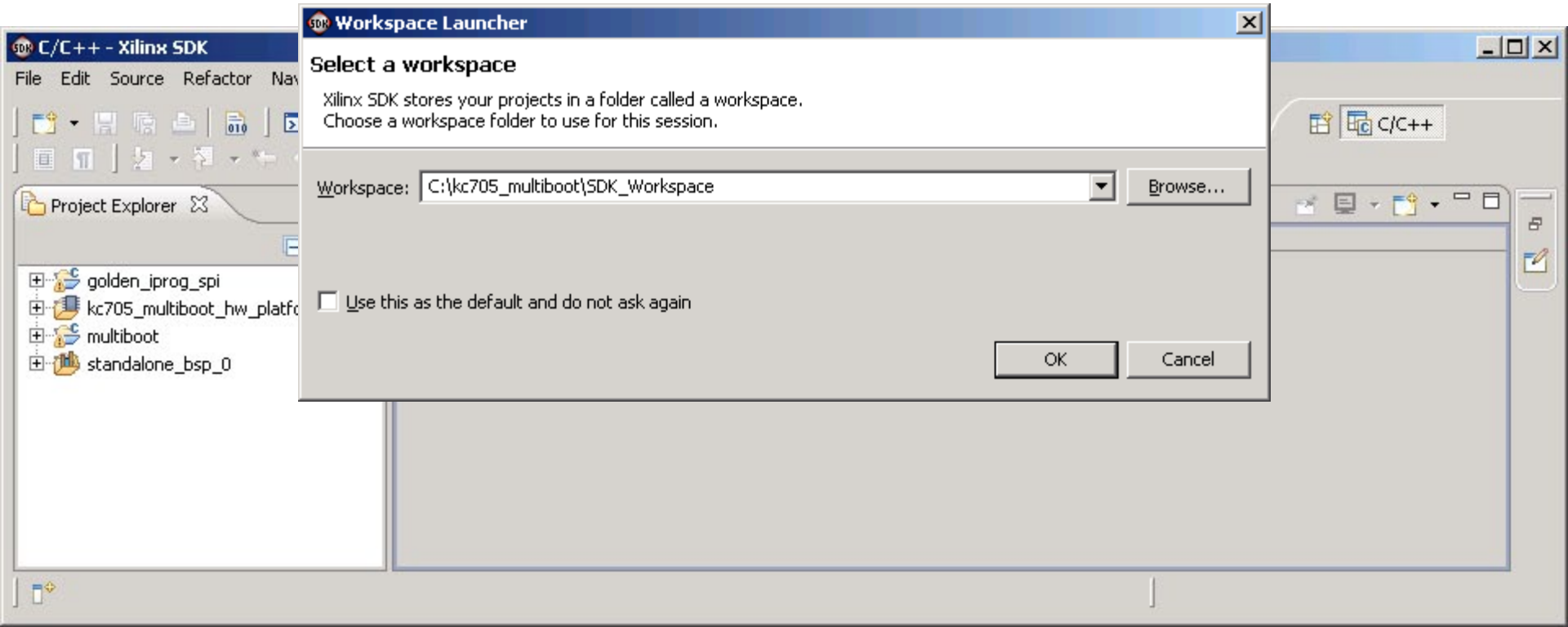
Compile KC705 MultiBoot Design

Compile KC705 MultiBoot Design

- If desired, FPGA compile can be skipped by opening SDK directly:

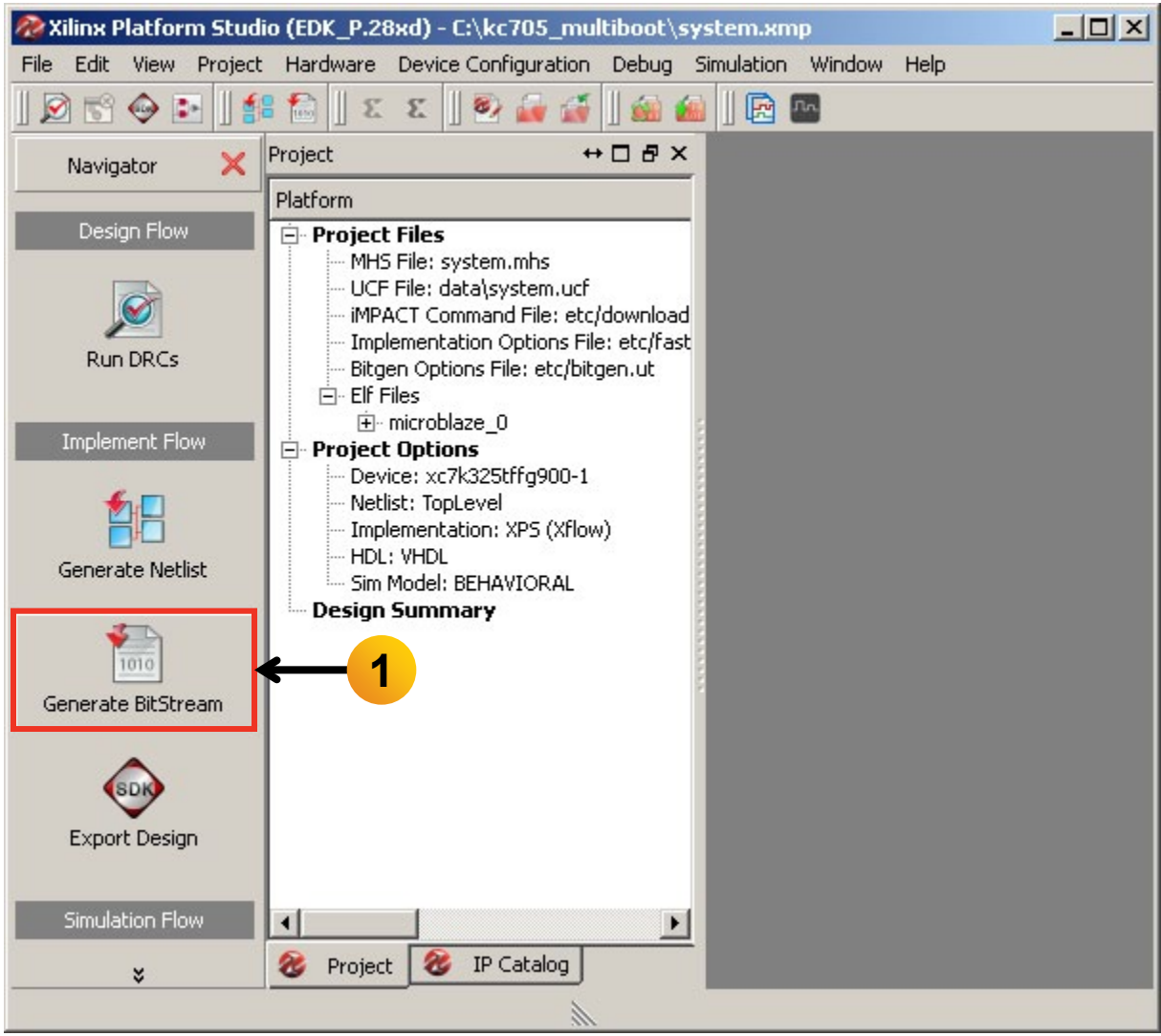
  Start → All Programs → Xilinx Design Tools → ISE Design Suite 14.2 → EDK → Xilinx Software Development Kit

- Select the workspace: <design files>\SW\SDK
- Go to SDK Software Compile



Compile KC705 MultiBoot Design

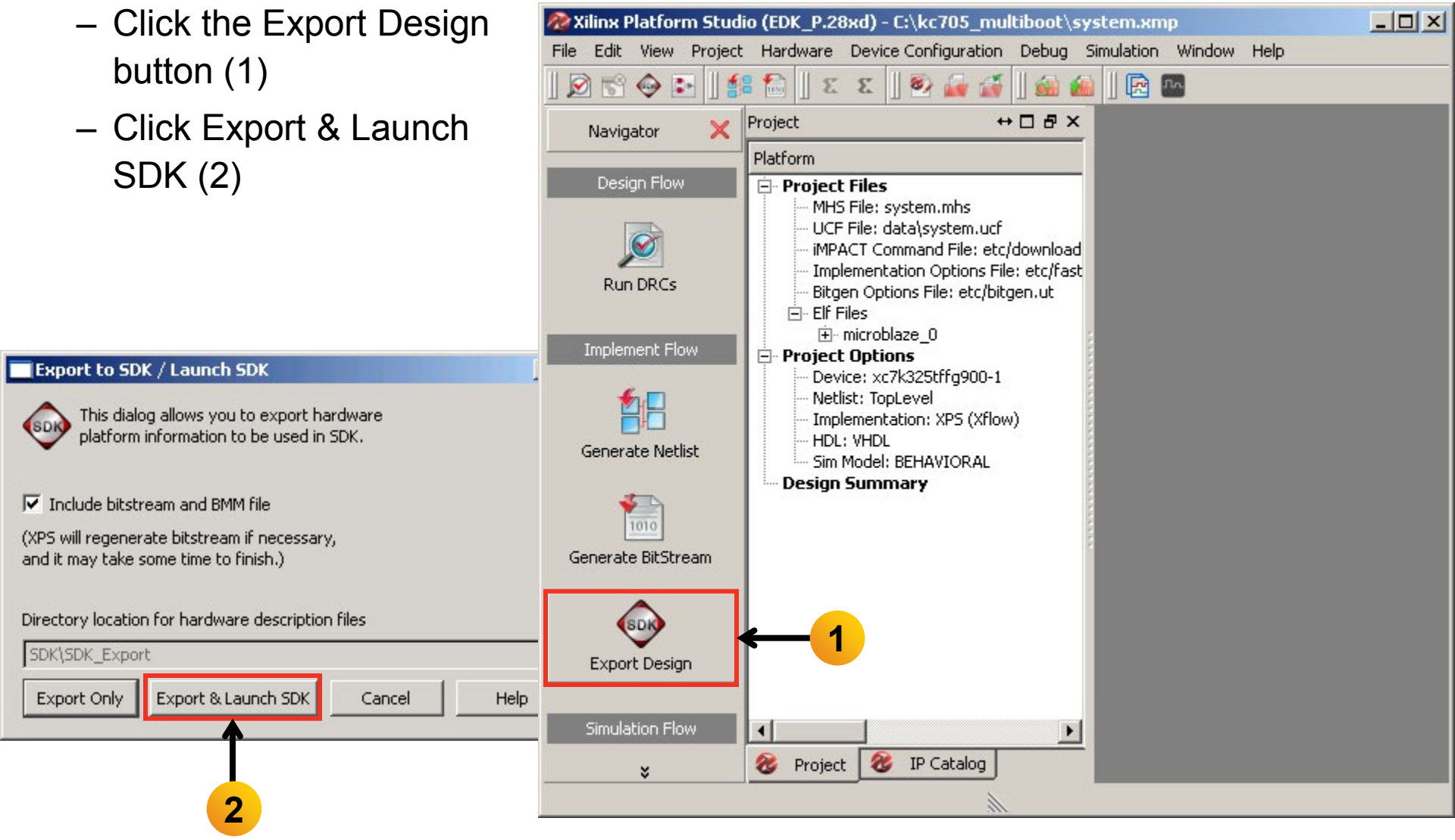
- Open XPS project <project directory>\system.xmp
- Create the hardware design, system.bit, located in <project directory>/implementation
  - Click the Generate Bitstream button (1)
  - Or from the menu, select Hardware → Generate Bitstream



Note: Presentation applies to the KC705

Launch KC705 Design in SDK

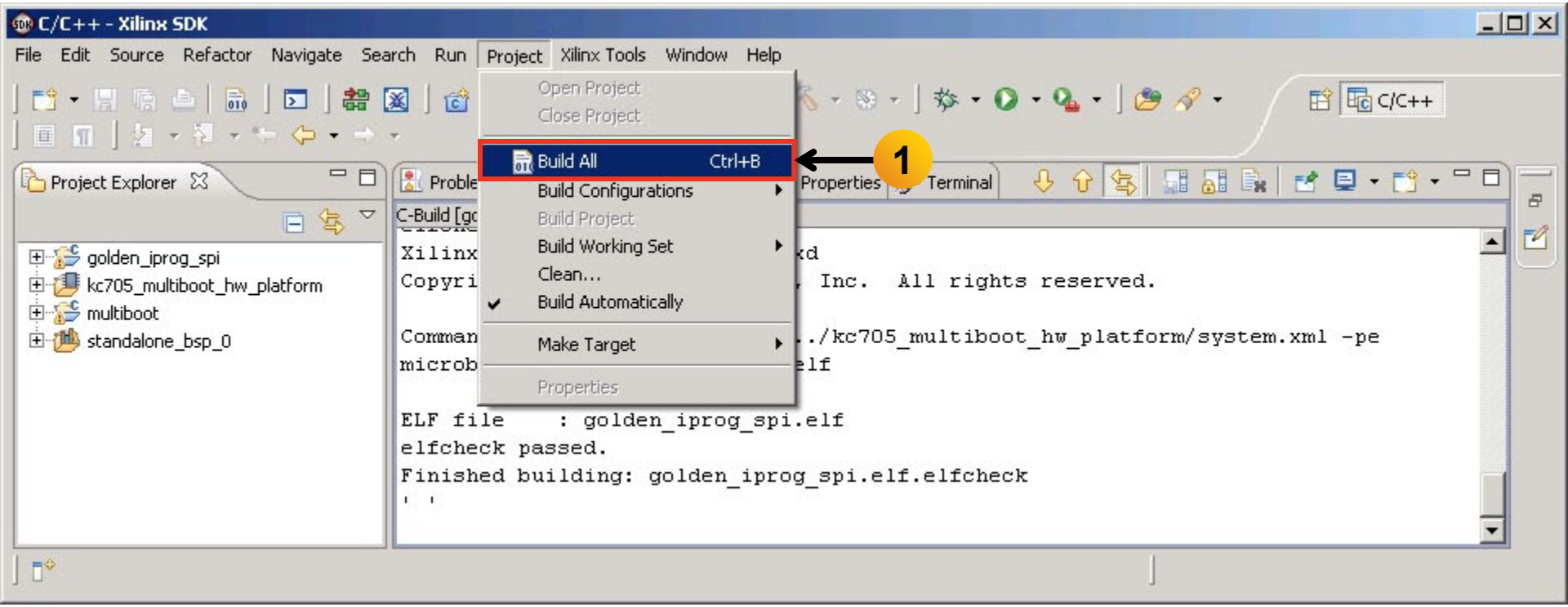
- **Open SDK**
  - Click the Export Design button (1)
  - Click Export & Launch SDK (2)



Note: Presentation applies to the KC705

Compile KC705 Software in SDK

- **SDK Software Compile - Build ELF files in SDK**
  - Project should build automatically; if not, select Project → Build All (1)
  - Note: If by-passing the FPGA compile, the ELF files are already built; if desired, the ELF files can be re-built by selecting Clean… followed by Build All



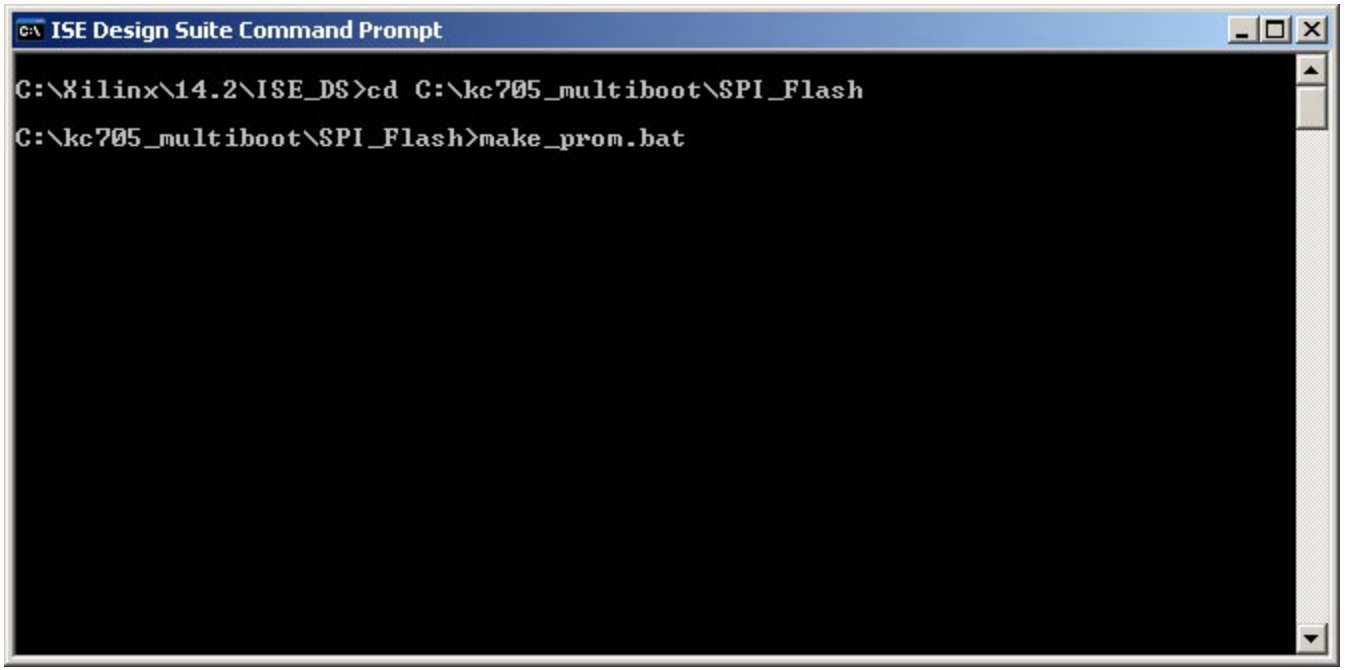
Note: Presentation applies to the KC705

Generate KC705 PROM File

- Start a ISE Design Suite Command Prompt and enter these commands:

  cd C:\kc705_multiboot\SPI_Flash

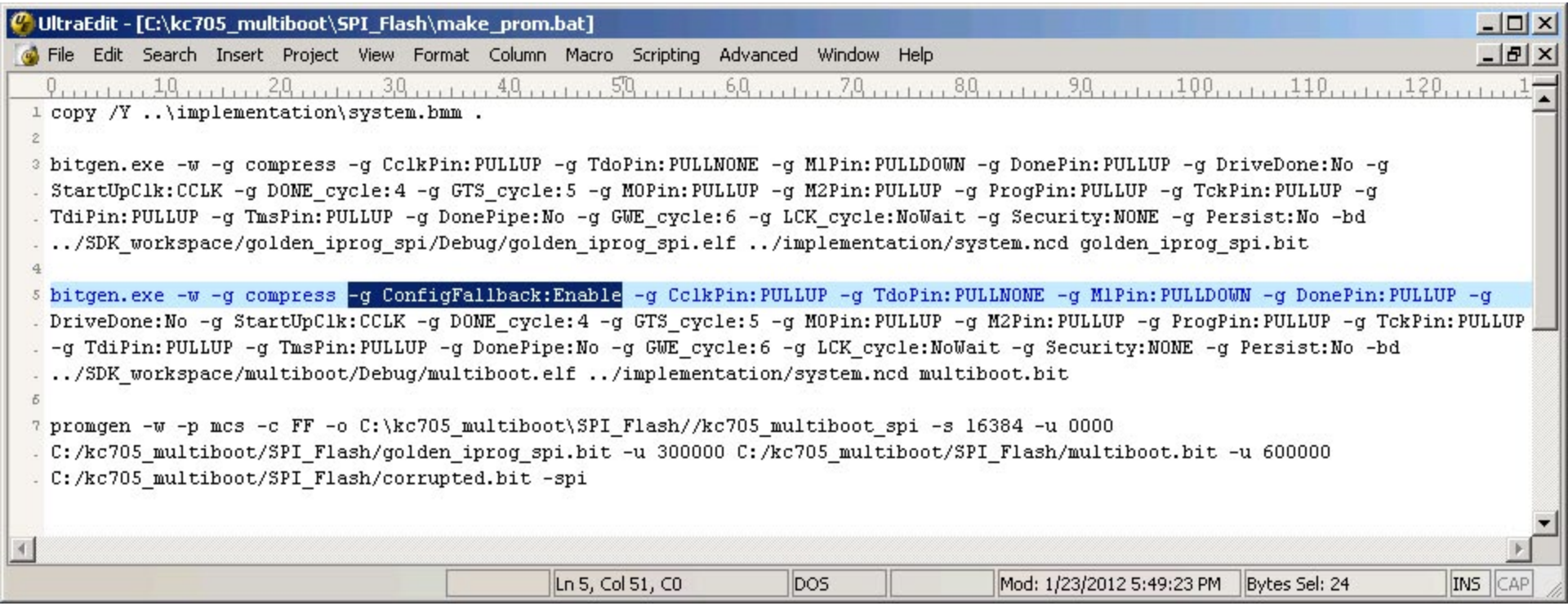
  make_prom.bat



Note: Presentation applies to the KC705

Generate KC705 PROM File

- The make_prom.bat generates compressed bitstreams with the ELF files in BRAM
- The MultiBoot bitstream uses the -g ConfigFallBack:Enable option
- “corrupted.bit” is a manually corrupted bitstream



Note: Presentation applies to the KC705

Kintex-7 MultiBoot Details

MultiBoot Register Setup & Command

- **Below are the values programmed into the ICAP via IPROG**
  - This table is from UG470, 7 Series FPGAs Configuration User Guide

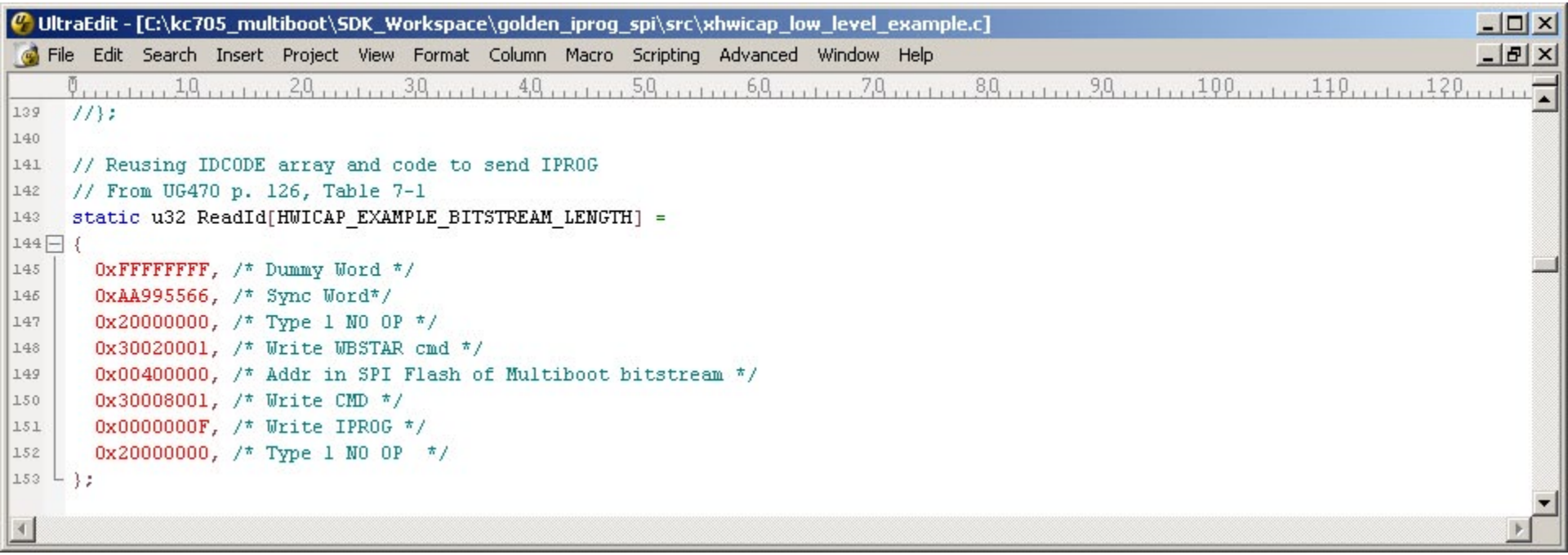
Table 7-1: **Example Bitstream for IPROG through ICAP**

Configuration Data (hex)	Explanation
FFFFFFFF	Dummy Word
AA995566	Sync Word
20000000	Type 1 NO OP
30020001	Type 1 Write 1 Words to WBSTAR
00000000	Warm Boot Start Address (Load the Desired Address)
30008001	Type 1 Write 1 Words to CMD
0000000F	IPROG Command
20000000	Type 1 NO OP

Note: Presentation applies to the KC705

MultiBoot Register Setup & Command

- IPROG command issued via the software in xhwicap_low_level_example.c



Note: Presentation applies to the KC705

References

References

- **7 Series Configuration**
  - 7 Series FPGAs Configuration User Guide
    - http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Documentation

Documentation

- **Kintex-7**
  - Kintex-7 FPGA Family
    - http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm
- **KC705 Documentation**
  - Kintex-7 FPGA KC705 Evaluation Kit
    - http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm
  - KC705 Getting Started Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ug883_K7_KC705_Eval_Kit.pdf
  - KC705 User Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ug810_KC705_Eval_Bd.pdf
  - KC705 Reference Design User Guide
    - http://www.xilinx.com/support/documentation/boards_and_kits/ug845_Ref_Design.pdf