Shiqing Li, Ph.D.

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Education

2019 – 2023 **Ph.D., Nanyang Technological University**
School of Computer Science and Engineering.
Advisor: Prof. Weichen Liu
Thesis title: *Accelerating Sparse Matrix Operations on FPGAs with On/Off-chip Memories.*

2016 – 2019 **M.S., Shandong University**
School of Computer Science and Technology
Advisor: Prof. Lei Ju

2012 – 2016 **B.S., Shandong University**
School of Computer Science and Technology

Research Interests

- Hardware Accelerators for Sparse Computation.
- Embedded Computer Architecture.
- High-level Synthesis.

Awards

2023 **Best Paper Candidate Award**, **Shiqing Li** and Weichen Liu, "Accelerating Gustavson-based SpMM on Embedded FPGAs with Element-wise Parallelism and Access Pattern-aware Caches", in *Design, Automation and Test in Europe (DATE'23).*

2022 **Best Paper Candidate Award**, Shien Zhu, **Shiqing Li**, and Weichen Liu, "iMAD: An In-Memory Accelerator for AdderNet with Efficient 8-bit Addition and Subtraction Operations", in *the 2022 Great Lakes Symposium on VLSI (GLSVLSI '22).*

Research Publications

- **Shiqing Li**, Di Liu, and Weichen Liu, "Optimized Data Reuse via Reordering for Sparse Matrix-Vector Multiplication on FPGAs", in *International Conference on Computer-Aided Design (ICCAD) 2021.*
- **Shiqing Li** and Weichen Liu, "Accelerating Gustavson-based SpMM on Embedded FPGAs with Element-wise Parallelism and Access Pattern-aware Caches", in *Design, Automation and Test in Europe (DATE'23).*
- **Shiqing Li**, Shien Zhu, Xiangzhong Luo, Tao Luo and Weichen Liu, "An Efficient Sparse LSTM Accelerator on Embedded FPGAs with Bandwidth-oriented Pruning", in *the 33rd edition of International Conference on Field-Programmable Logic and Applications (FPL 2023).*
- **Shiqing Li**, Di Liu, and Weichen Liu, "Efficient FPGA-based Sparse Matrix-Vector Multiplication with Data Reuse-aware Compression", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) 2023.*
- **Shiqing Li**, Shuo Huai, and Weichen Liu, "An Efficient Gustavson-based Sparse Matrix-matrix Multiplication Accelerator on Embedded FPGAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) 2023.*
- **Shiqing Li**, Yixun Wei, Lei Ju, "Automatic data placement for CPU-FPGA heterogeneous multiprocessor System-on-Chips", in *Design, Automation and Test in Europe (DATE'19).*

- Zelin Du, Qianling Zhang, Mao Lin, **Shiqing Li**, Xin Li, Lei Ju, "A Comprehensive Memory Management Framework for CPU-FPGA Heterogenous SoCs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) 2023.*
- Hui Chen, Di Liu, **Shiqing Li**, Shuo Huai, Xiangzhong Luo, Weichen Liu, "MUGNoC: A Software-Configured Multicast-Unicast-Gather NoC for Accelerating CNN Dataflows.", in *the 28th Asia and South Pacific Design Automation Conference (ASPDAC 2023).*
- Shien Zhu, **Shiqing Li**, and Weichen Liu, "iMAD: An In-Memory Accelerator for AdderNet with Efficient 8-bit Addition and Subtraction Operations", in *the 2022 Great Lakes Symposium on VLSI (GLSVLSI '22).*
- Hao Kong, Shuo Huai, Di Liu, Lei Zhang, Hui Chen, Shien Zhu, **Shiqing Li**, Weichen Liu, Manu Rastogi, Ravi Subramaniam, Madhu Athreya, M. Anthony Lewis, "EDLAB: A Benchmark for Edge Deep Learning Accelerators", in *IEEE Design & Test 2022.*
- Peng Chen, Weichen Liu, Hui Chen, **Shiqing Li**, Mengquan Li, Lei Yang, Nan Guan, "Reduced Worst-Case Communication Latency Using Single-Cycle Multihop Traversal Network-on-Chip", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) 2021.*
- Hui Chen, Zihao Zhang, Peng Chen, Xiangzhong Luo, **Shiqing Li**, Weichen Liu, "MARCO: A High-performance Task Mapping and Routing Co-optimization Framework for Point-to-Point NoC-based Heterogeneous Computing Systems", in *ACM Transactions on Embedded Computing Systems (TECS) 2021.*
- Peng Chen, Hui Chen, Jun Zhou, Di Liu, **Shiqing Li**, Weichen Liu, Wanli Chang, Nan Guan, "Partial order based non-preemptive communication scheduling towards real-time networks-on-chip", in *the 36th ACM/SIGAPP Symposium on Applied Computing (SAC), 2021.*
- Xiangzhong Luo, Di Liu, Hao Kong, Shuo Huai, Hui Chen, **Shiqing Li**, Guochu Xiong, Weichen Liu, "Pearls Hide Behind Linearity: Simplifying Deep Convolutional Networks for Embedded Hardware Systems via Linearity Grafting", in *the 29th Asia and South Pacific Design Automation Conference (ASP-DAC 2024).*
- Shuo Huai; Hao Kong; Xiangzhong Luo; **Shiqing Li**; Ravi Subramaniam; Christian Makaya; Qian Lin; Weichen Liu, "CRIMP: Compact & Reliable DNN Inference on In-Memory Processing via Crossbar-Aligned Compression and Non-ideality Adaptation", in *the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2023.*

Skills

Languages	Chinese, English.
Coding	C++, Python
Toolkit	Xilinx Vitis Toolkit, High-level Synthesis
Main Target Devices	Xilinx ZynqUltraScale ZCU106, Digilent PYNQ-Z1.

Research Plan

I mainly focus on accelerating sparse matrix operations on embedded FPGAs. Specifically, I have proposed accelerators for sparse matrix-vector multiplication (SpMV), sparse matrix-matrix multiplication (SpMM), and sparse LSTM (SpLSTM). In the future, I plan to accelerate more applications, e.g., graph processing and more types of neural networks. On the other side, I can target other architectures to extend my current research.