LSSDA Workshop – October 22, 2025

High-Rate Detectors: from data generation to data processing in real time

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SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

Outline

- Detector R&D and Applied Microelectronics Program Overview
- Program vision
- Example of upcoming detectors: ePixUHR for LCLS-II HE
- Data deluge
- SNL – SLAC Neural Network Library for FPGA ML model inference

SLAC long-term X-ray detector development plan

Bigger, Faster, Higher resolution and Higher Energies, Intelligent

With goals built into Projects progressively meeting Science priorities and requirements

LCLS-I

ePix (2013-2018)

- **In use at LCLS**

LCLS-II

ePixHR$_{5kHz}$ (2016-2025)

- **5kHz for LCLS-II first light**
- ePixHR10k for tender Imaging
- ePixHR250M for soft-ray Imaging

LCLS-II-HE

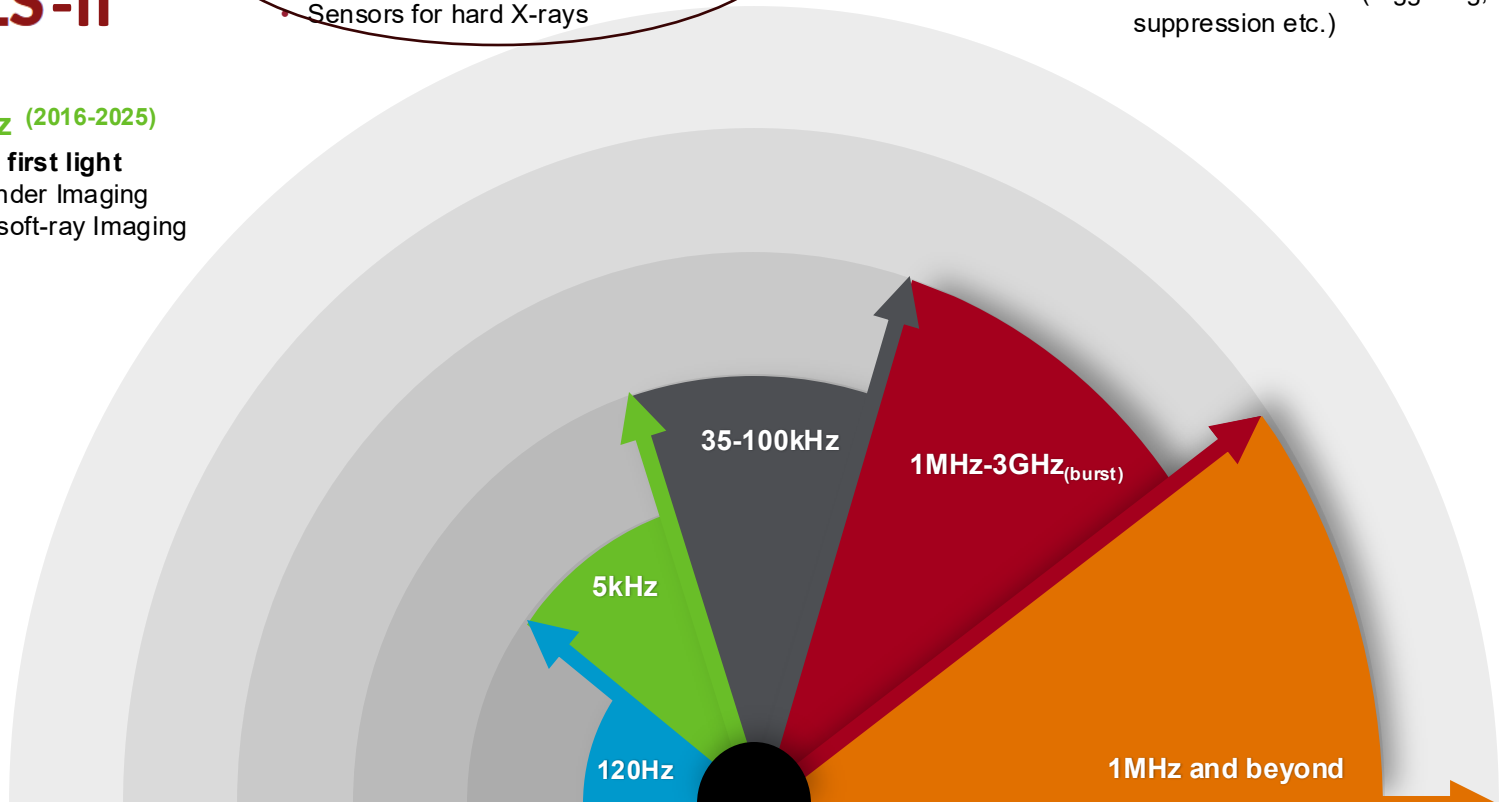
ePixUHR$_{35\text{-}100kHz}$ (2019-2028)

- **Full frame 35kHz-100kHz**
- "General purpose" cameras
- 35kHz for HE first light
- Sensors for hard X-rays

LCLS-II-HE (and beyond)

SparkPix (2020-2028)

- Revolutionary **E**xperiment **S**pecific **X**-ray **C**ameras
- **Information extraction at full rate (1MHz CW, 3GHz burst)**
- Advanced features (triggering, sparsification, zero suppression etc.)



BEYOND

Morpheus (2025-2032)

- **Data-driven intelligent Detector** with distributed real-time processing at the sensor
- Ultra-high frame rate (programmable patterns)
- Trainable Energy-efficient real-time information extraction
  - Advanced Calibration / Edge-AI/ML
  - Validated algorithms – no loss of information
- Adaptive resolution (spatial, energy, and time) for experimental steering

Our Vision for X-Ray Detectors and Research Goals over the years

Integrated — With the scientific needs and meet scheduled experiment priorities.

Scalable — In dimensions, performance (rate, resolution etc.) and functionalities.

Platform based — With standardized interfaces and communication protocols fully integrated with the facilities DAQs and their constrains.

Intelligent — Incrementally capable of advanced "smart" features reducing time-to-science and enabling novel modes of operation.

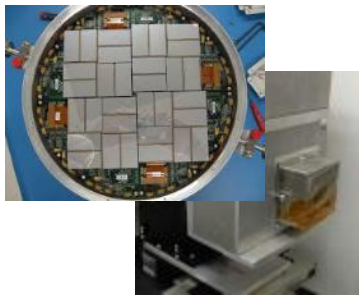
Experiment Specific — Experiment Specific X-ray Cameras (ESXC), co-designed with scientist and with architectures tweaked to fully exploit the machine potentials in each experiment.

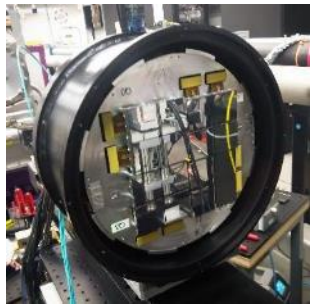
Innovative — Providing "Lego" blocks that can be mixed to develop novel innovative detectors with reduced risks and costs, sprouting ideas for novel cutting-edge experiments

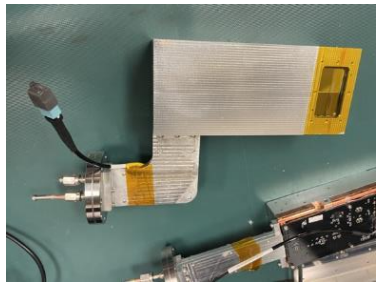
Support the mission of the Lab while advancing the state-of-the-art of technology for Radiation Detectors

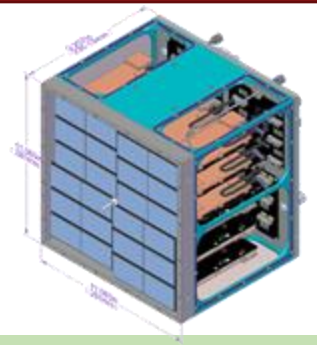
Performance and Architecture Versatility | Rate and Information Extraction | Intelligence and Efficiency

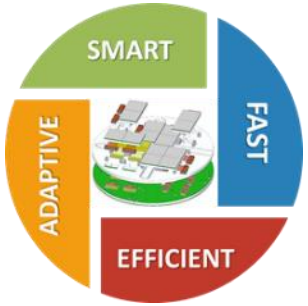
2006 — 2014 — 2019 — 2024 — 2026 — 2028 — beyond











LUSI Detectors and ePix | ePixHR, ePixUHR and SparkPix | Project Morpheus

ePixUHR for LCLS-II/HE

ePixUHR – 4M is in production
Delivery in FY26
Expected user exp. FY27

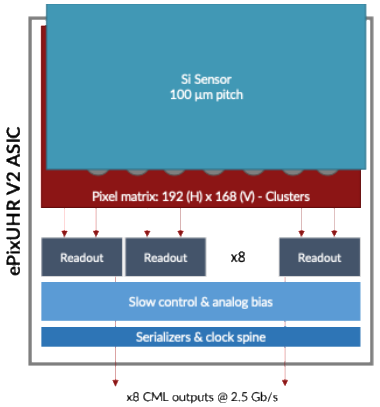
A one-of-a-kind Modular Detector

Modular approach with independent "SuperTiles" 1 Megapixel Detectors

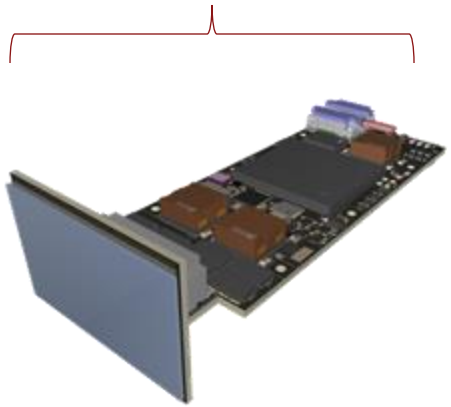
- Hybrid ASIC sensor module ePixUHR + 1mm Si Sensor
- Serviceable for metrology, calibration, repair
- Independent power, data and cooling lines per module
- All electronics behind the sensor modules
  - Minimizes dead space
- Beam pipe at the center of the detector
- Assembled in-air and in-vacuum

Detector	ePixUHR	
Mode	35 kHz	100 kHz
Pixel Pitch [um]	100	
Frame rate [kHz]	35	100
Matrix size	192 x 168	
Read Noise [e^- rms]	150	
Well depth [8keV photons]	10^4	
Power consumption [W/cm^2]	1.2	
Data rate [Gb/s]	16	44
CMOS tech node	TSMC 130 nm	

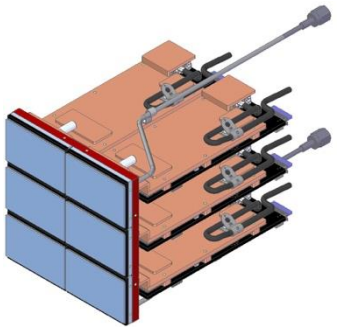
ePixUHR ASIC & Si Sensor



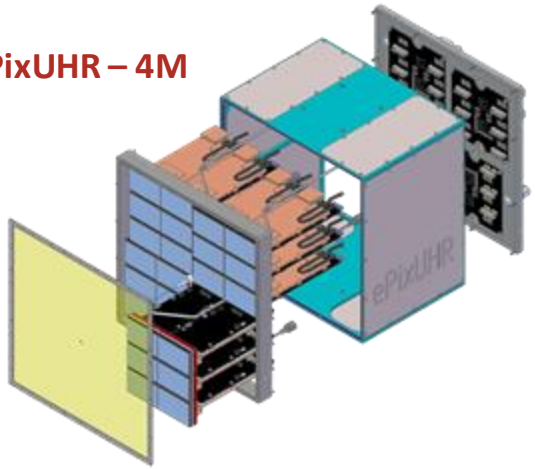
ePixUHR 2x3



ePixUHR – 1M



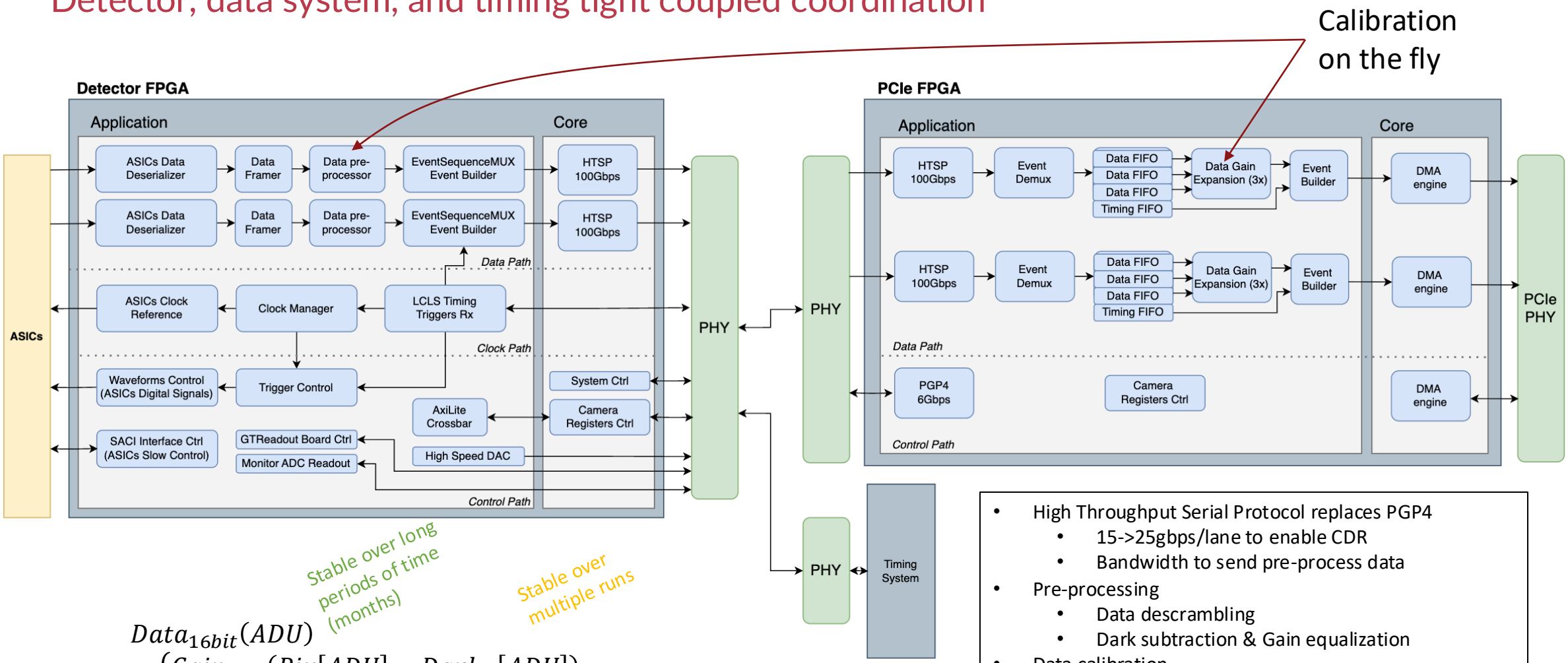
ePixUHR – 4M



System level data & controls

$$Data_{24bit}(ADU) = \begin{cases} 1 * (Pix[ADU]) \\ Gain_H/Gain_L * (Pix[ADU]) \end{cases} \quad \text{or} \quad Data_{16fp}(ADU) = \begin{cases} 1 * (Pix[ADU]) \\ Gain_H/Gain_L * (Pix[ADU]) \end{cases}$$

Detector, data system, and timing tight coupled coordination



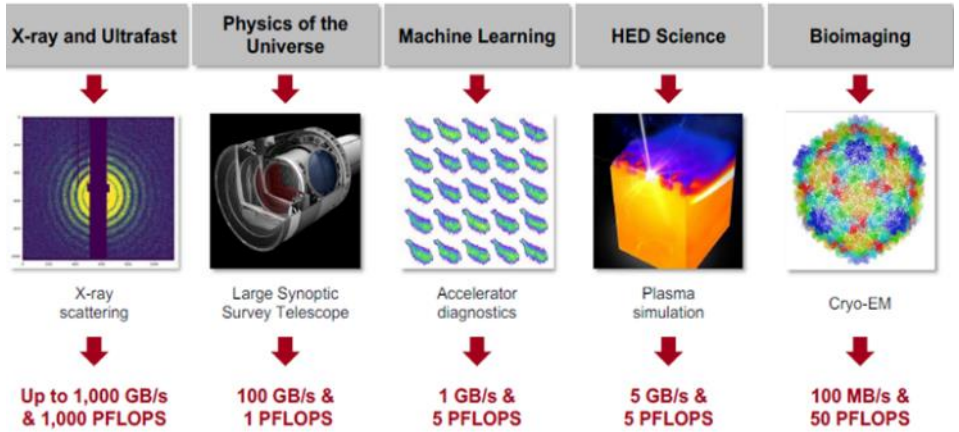
Stable over long periods of time (months)

Stable over multiple runs

$$Data_{16bit}(ADU) = \begin{cases} Gain_H * (Pix[ADU] - Dark_H[ADU]) \\ Gain_L * (Pix[ADU] - Dark_L[ADU]) \end{cases}$$

- High Throughput Serial Protocol replaces PGP4
  - 15->25gbps/lane to enable CDR
  - Bandwidth to send pre-process data
- Pre-processing
  - Data descrambling
  - Dark subtraction & Gain equalization
- Data calibration
  - Distributed process which includes PCIe firmware

The Data Deluge Problem in Scientific Experiments – a codesign distributed solution



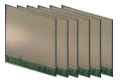
Super computers

Detectors = Network of high precision independent sensing units densely distributed with local and exa-scale computing

a 2Mpix MHz detector for LCLS would generate 5 Terabytes/s. Equivalent to ~1.2 Zettabytes/year (assuming 6 months operation per year)

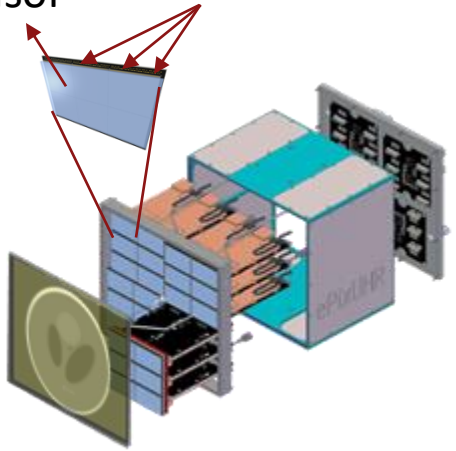
Detector ASIC Processing units (mixed signal)

PCIe FPGA Processing Units

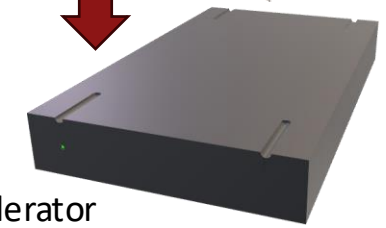


Sensor

ASICs



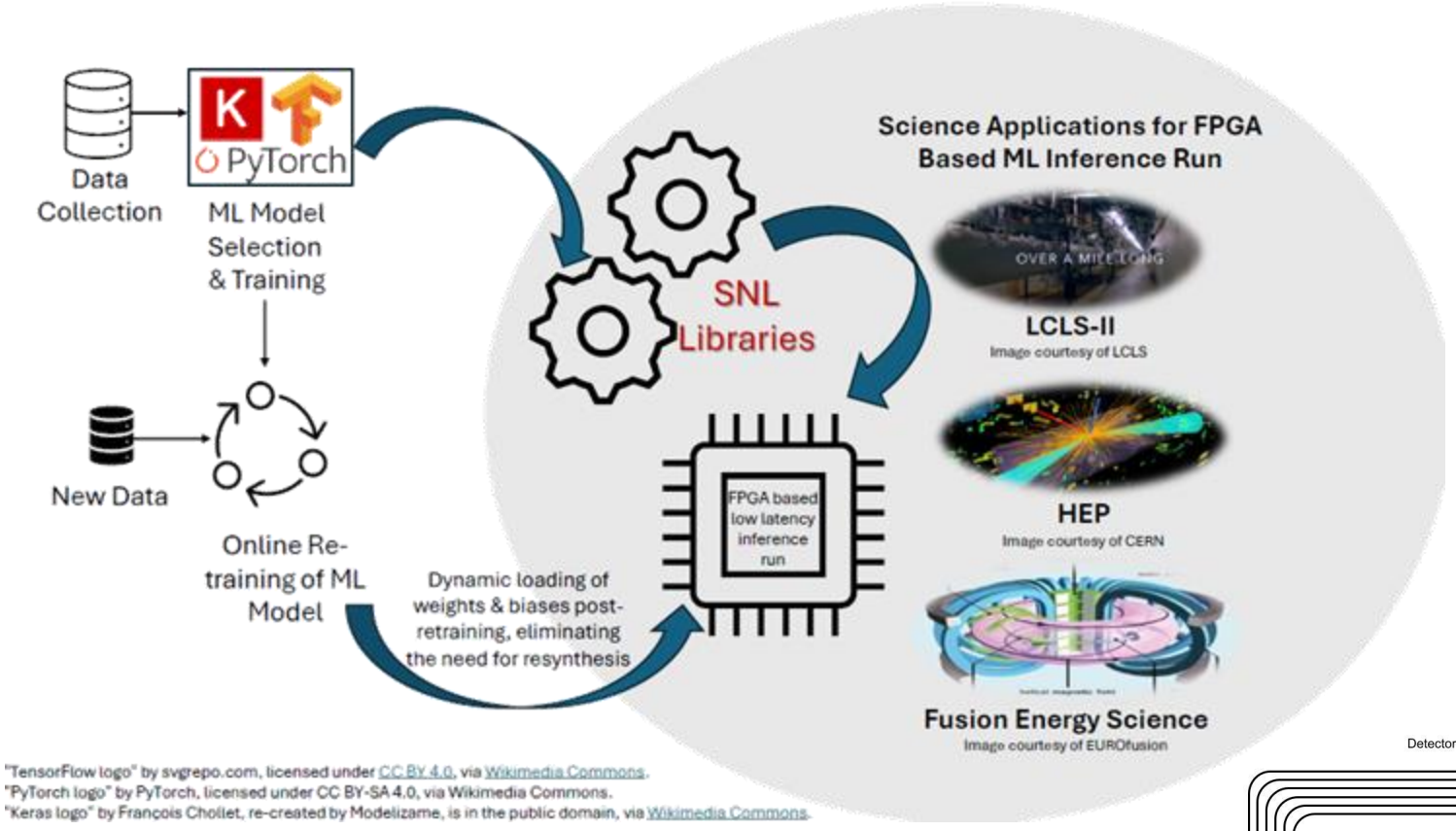
Detector (PU) (FPGA/ASIC/xPU) Processing units



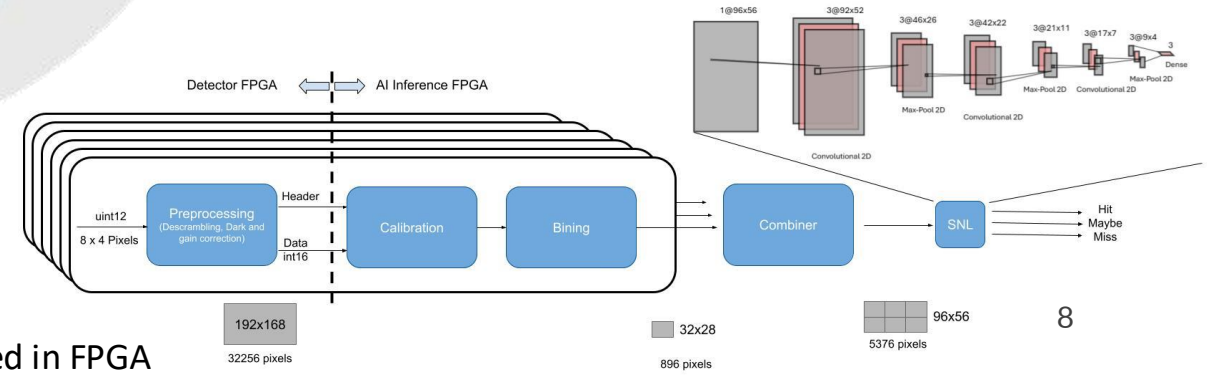
Accelerator (CPU, GPU GROQ,...) PROCESSING Units

ML in FPGA: SLAC Neural Network Library (SNL) Framework

Goal: Provide a set of libraries to synthesize AI inference networks into FPGAs



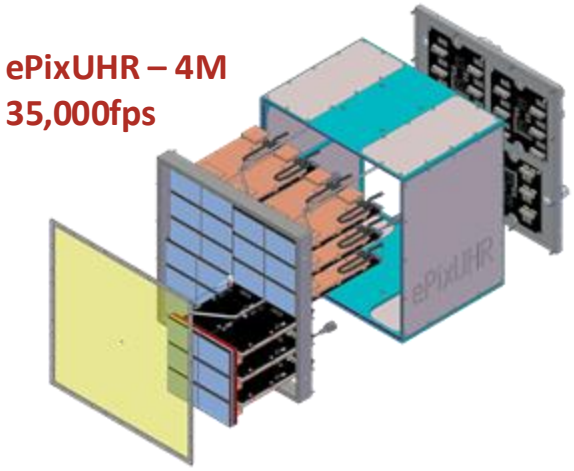
- Key Points
- Provides specialized set of libraries for deploying ML inference to FPGA
- Using High-Level-Synthesis (HSL): C++ programming of FPGA
- Supports Keras like API for layer definition
- **Dynamic reloading** of **weights** and **biases** to avoid re-synthesis
- Supports 10s of thousands of parameters or more depending on latency requirements for the inference model
- Total end to end latency of couple of **usec** to couple of **millisecond**.
- Streaming interface between layers.
- Allow for **pipeline** of the **data flow** for a **balance** of **latency vs frame rate**
- Library approach allows for user/application specific enhancements



Serial Crystallography Study Case:
Hit, Maybe, Miss ML model deployed in FPGA

Summary

- Priority X-ray detector development projects on track to deliver kHz to MHz detectors for LCLS-II & LCLS-II-HE.
- Data Deluge needs to be addressed at every PU level available in the data chain
- Detector can play a significant role
- Hardware Aware Algorithms are needed



Thank you!