

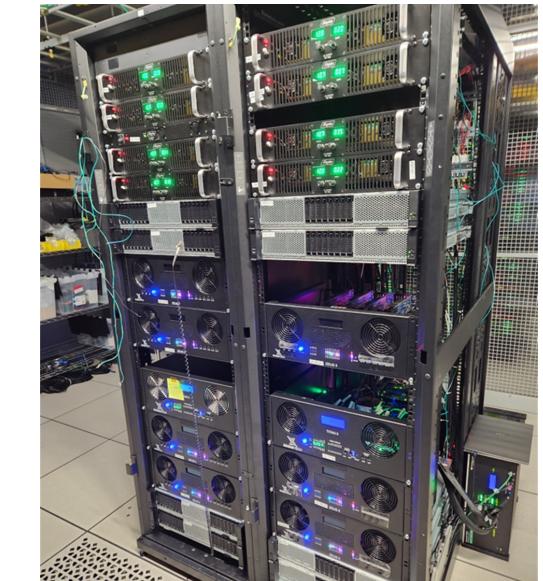
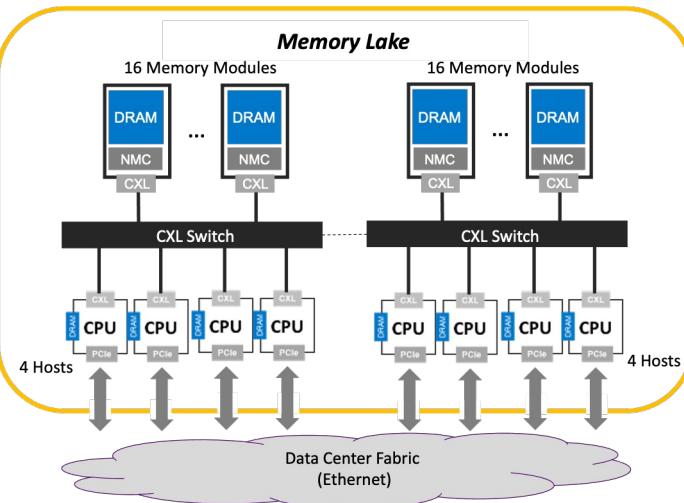
# Skyler Windh

Senior Systems Engineer

Storage and Memory Systems Pathfinding Group  
Richardson, Texas



- **Ph.D. In Computer Science from UC Riverside**
  - Thesis on Massive Multithreaded FPGA accelerators designed to hide memory latency
- Early projects at Micron focused on **programmability** and **API design** for custom accelerators
  - Latency hiding RISC-V barrel processor
  - Coarse-Grained Reconfigurable Array of RISC-V cores
    - Designed a custom assembly language and assembler in Rust
- Current Focus:
  - Leading the software development of Micron's CXL Memory Lake concept under the [PNNL AMAIS](#) project
    - Provides multi-host **shared memory** with **Near Memory Compute** cores in the memory modules
  - Emulating future NVMe drives and exploring performance trade-offs with [NVIDIA's StorageNext/SCADA initiative](#)
  - Advancing software development practices and leading a Rust workshop



# Interesting Areas of Discussion

## Disaggregation and Tiering

- New protocols enable Independent scaling of memory and compute
- Expanding tiers in the memory hierarchy:
  - Far memory/Fast storage
- Aligning GPU memory tiers with CPU tiers and disaggregated memory

## Near Memory Compute and Reducing Data Movement

- Orders of Magnitude more bandwidth in memory modules offers an attractive place to offload some compute
- Enable the specialized compute cores to focus on their optimal tasks

## Programmability of heterogeneous compute clusters

- What are the best ways to surface low level functionality to be usable across hardware vendors
- Shared memory and tracking ownership semantics