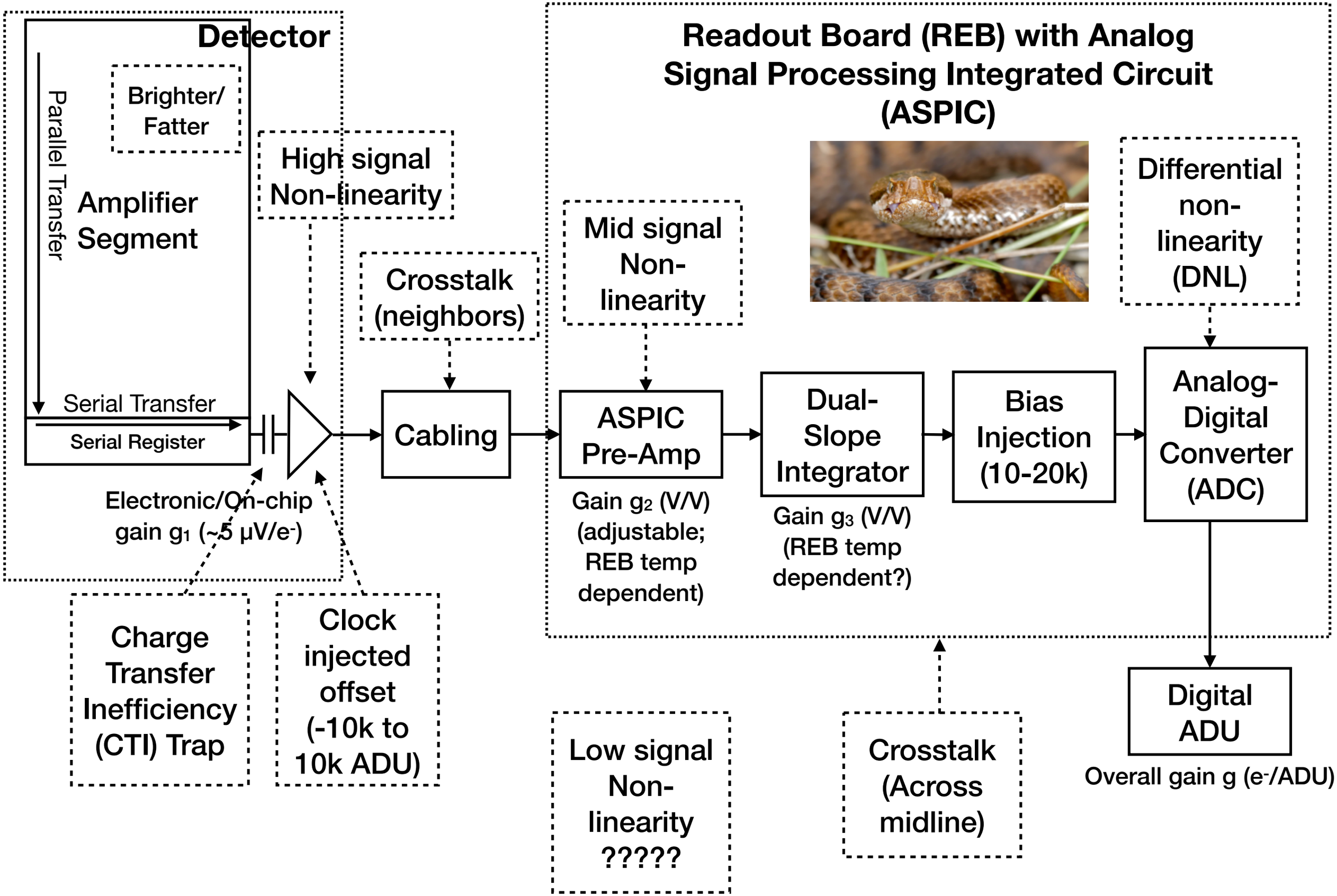
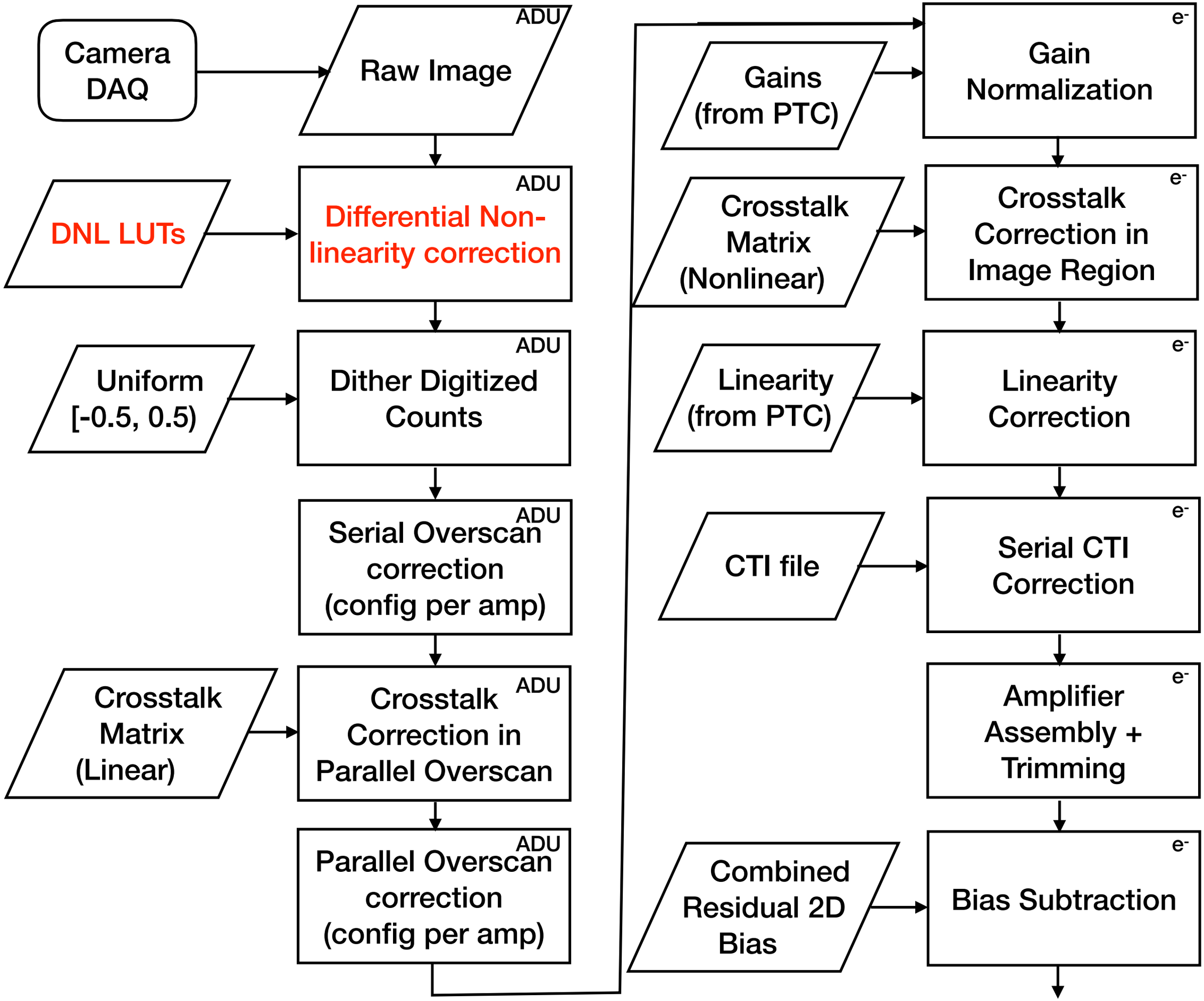
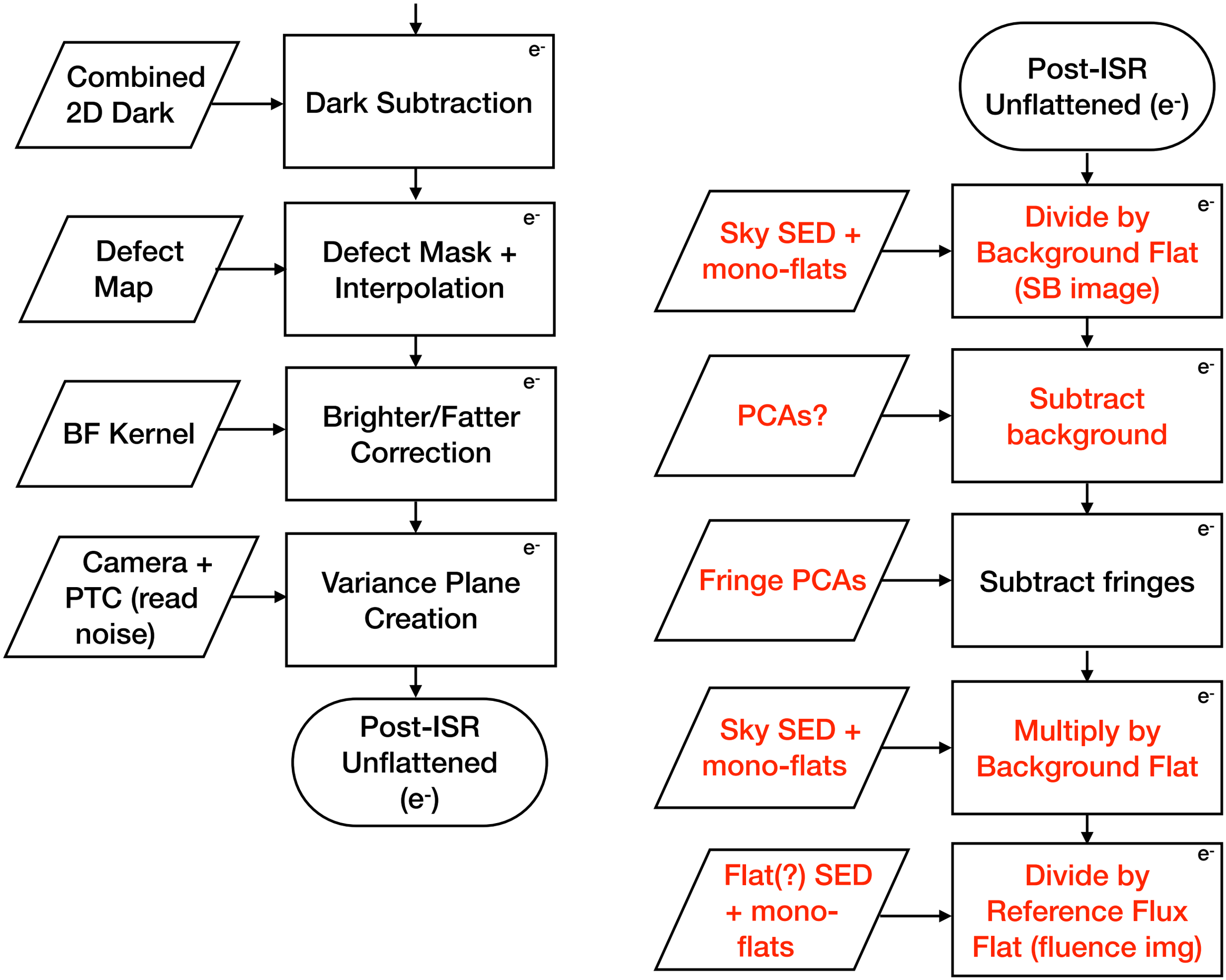

Detector
Parallel Transfer
Brighter/ Fatter
Amplifier Segment
Serial Transfer
Serial Register
Electronic/On-chip gain g_1 (~5 μV/e⁻)
Charge Transfer Inefficiency (CTI) Trap
Clock injected offset (-10k to 10k ADU)
High signal Non-linearity
Crosstalk (neighbors)
Cabling
Mid signal Non-linearity
Low signal Non-linearity ?????
Readout Board (REB) with Analog Signal Processing Integrated Circuit (ASPIC)
ASPIC Pre-Amp
Gain g_2 (V/V) (adjustable; REB temp dependent)
Dual-Slope Integrator
Gain g_3 (V/V) (REB temp dependent?)
Bias Injection (10-20k)
Differential non-linearity (DNL)
Analog-Digital Converter (ADC)
Crosstalk (Across midline)
Digital ADU
Overall gain g (e⁻/ADU)


Camera DAQ
Raw Image
ADU
DNL LUTs
Differential Non-linearity correction
ADU
Uniform [-0.5, 0.5)
Dither Digitized Counts
ADU
Serial Overscan correction (config per amp)
ADU
Crosstalk Matrix (Linear)
Crosstalk Correction in Parallel Overscan
ADU
Parallel Overscan correction (config per amp)
ADU
Gains (from PTC)
Gain Normalization
e-
Crosstalk Matrix (Nonlinear)
Crosstalk Correction in Image Region
e-
Linearity (from PTC)
Linearity Correction
e-
CTI file
Serial CTI Correction
e-
Amplifier Assembly + Trimming
e-
Combined Residual 2D Bias
Bias Subtraction
e-


Combined 2D Dark
Dark Subtraction
e-
Defect Map
Defect Mask + Interpolation
e-
BF Kernel
Brighter/Fatter Correction
e-
Camera + PTC (read noise)
Variance Plane Creation
e-
Post-ISR Unflattened (e-)
Post-ISR Unflattened (e-)
Sky SED + mono-flats
Divide by Background Flat (SB image)
e-
PCAs?
Subtract background
e-
Fringe PCAs
Subtract fringes
e-
Sky SED + mono-flats
Multiply by Background Flat
e-
Flat(?) SED + mono-flats
Divide by Reference Flux Flat (fluence img)
e-