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Recommended Usage of Microchip I²C™ Serial EEPROM Devices

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INTRODUCTION

The majority of embedded control systems require nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low-power consumption, and low cost, serial EEPROMs are a popular choice for nonvolatile storage. Microchip Technology has addressed this need by offering a full line of serial EEPROMs covering industry standard serial communication protocols for two-wire (I²C™), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges, and packaging options.

In order to achieve a highly robust application when utilizing serial EEPROMs, the designer must consider more than just the data sheet specifications.

There are a number of conditions which could potentially result in nonstandard operation. The details of such conditions depend greatly upon the serial protocol being used.

This application note provides assistance and guidance with the use of Microchip I²C serial EEPROMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design. The following topics are discussed:

• Chip Address Inputs
• Write-Protect Feature
• Power Supply
• Checking for Acknowledge
• Acknowledge Polling
• Increasing Data Throughput
• Bus Pull-up Resistors
• Software Reset Sequence

Figure 1 shows the suggested connections for using Microchip I²C serial EEPROMs. The basis for these connections will be explained in the sections which follow.

FIGURE 1:   RECOMMENDED CONNECTIONS FOR 24XXXX SERIES DEVICES
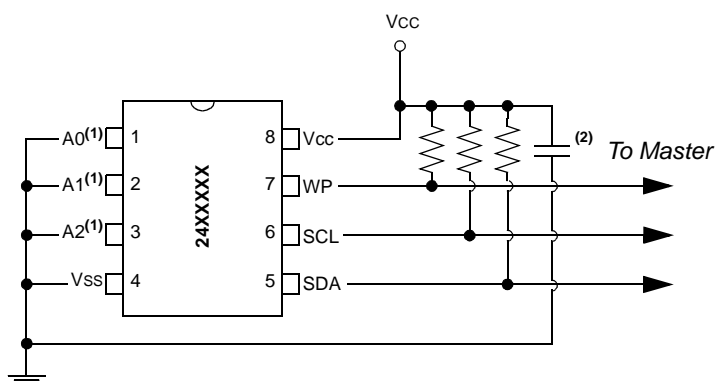
Note 1: Pins A0, A1 and A2 are not internally connected in some devices.
     2: A decoupling capacitor (typically 0.1 µF) should be used to help filter out small ripples on Vcc.

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CHIP ADDRESS INPUTS

The Chip Address input pins (A0, A1 and A2) are used on a number of devices to support multiple device operation. On devices with this feature, the levels on these inputs are compared with the corresponding bits in the slave address, and the device is selected if the comparison is true. Note that the Chip Address pins are not internally connected on some devices. Refer to the appropriate device data sheet for more details.

For devices with internally connected Chip Address pins, these inputs must be hard-wired to either logic '0' or logic '1'. That is, they cannot be left floating, otherwise the device will not operate correctly. Note that the 24XX515 and 24XX1025 devices require that the A2 pin always be held at logic '1' for proper operation.

In some applications, the Chip Address inputs are controlled by a microcontroller or other programmable device. In such instances, the inputs must be driven to either logic '0' or logic '1' before normal device operation can proceed.

WRITE-PROTECT FEATURE

For devices with write-protect functionality, the WP pin provides a hardware write-protect feature which allows the user to protect the entire array when the pin is tied to Vcc. If tied to Vss, the write protection is disabled.

A pull-up resistor connected to the WP pin can be used to ensure the device remains write-protected during power-up/power-down and any other time the pin is not being driven explicitly. This helps to guard against unwanted writes which may occur due to noise on the SDA/SCL lines or for other reasons. In order for a write cycle to be initiated, the WP pin must be driven to logic '0', otherwise the write cycle will not execute.

If the designer chooses not to control the WP pin, but rather to always disable write protection, the pin must be hard-wired to logic '0'. As with the Chip Address inputs, this pin cannot be left floating, otherwise the device will not operate correctly.

Note that some devices do not support write-protect functionality.

POWER SUPPLY

Microchip serial EEPROMs feature a high amount of protection from unintentional writes and data corruption while power is within normal operating levels. But certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

As shown in Figure 1, a decoupling capacitor (typically 0.1 μF) should be used to help filter out small ripples on Vcc.

Power-Up

On power-up, Vcc should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. Vcc should not linger at an ambiguous level (i.e., below the minimum operating voltage).

Brown-Out Conditions

For added protection, Microchip serial EEPROMs feature a Brown-out Reset circuit. However, if Vcc happens to fall below the minimum operating voltage for the serial EEPROM, it is recommended that Vcc be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial EEPROM, bringing Vcc down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the EEPROM keeps its current state. In this case, a software Reset sequence would be required before beginning further communication.

Power Failure During a Write Cycle

During a write cycle, Vcc must remain above the minimum operating voltage for the entire duration of the cycle (typically 5 ms max. for most devices). If Vcc falls below this minimum voltage at any point for any length of time, data integrity cannot be ensured. It will result in marginally programmed data that may or may not be correct. Furthermore, because the EEPROM cells were not able to be fully programmed, the device will have shorter data retention time than specified in the data sheet.

CHECKING FOR ACKNOWLEDGE

One of the many benefits of I²C communication is the Acknowledge bit transmitted after every byte is received. Except during write cycles, Microchip serial EEPROMs will always transmit this bit low after receiving each byte, assuming a valid Start bit and control byte were already received. Due to this, the master can monitor the ACK bit received throughout an operation to detect any errors that may occur. It is always good practice to check if a logic '1' is received for the ACK during transmission, which would indicate that the EEPROM did not respond. At that point, an error-handling routine would be required to determine why the device did not respond and, if necessary, to perform a software Reset sequence.

ACKNOWLEDGE POLLING

Write operations on serial EEPROMs require that a write cycle time be observed after initiating the write, allowing the device time to store the data. During this time, normal device operation is disabled, and any attempts by the master to access the device will be ignored. Therefore, it is important that the master wait for the write cycle to end before attempting to access the EEPROM again.

Each device has a specified worst-case write cycle time, typically listed as T_{WC}. A simple method for ensuring that the write cycle time is observed is to perform a delay for the amount of time specified before accessing the EEPROM again. However, it is not uncommon for a device to complete a write cycle in less than the maximum specified time. As such, using the previously shown delay method results in a period of time in which the EEPROM has finished writing, but the master is still waiting.

In order to eliminate this extra period of time, and therefore operate more efficiently, it is highly recommended to take advantage of the Acknowledge Polling feature. Since Microchip's I²C serial EEPROM devices will not acknowledge during a write cycle, the device can continuously be polled until an ACK bit is received, thus indicating that the write is complete. This is done after the Stop condition takes place to initiate the internal write cycle of the device.

Procedure

Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle, and ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be sent again. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 2 for details.

FIGURE 2:   **ACKNOWLEDGE POLLING FLOW**

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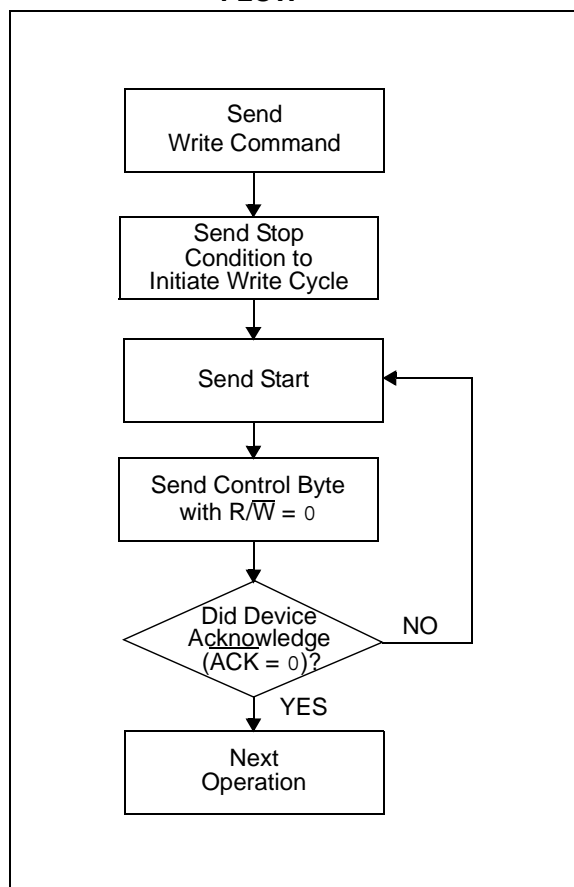
## INCREASING DATA THROUGHPUT

Page Writes

Most Microchip I^{2}C serial EEPROMs feature a page buffer for use during write operations. This allows the user to write any number of bytes from one to the maximum page size in a single operation. This can provide for a significant decrease in the total write time when writing a large number of bytes.

Page write operations are limited to writing within a single physical page, regardless of the number of bytes actually being written. This is because the memory array is physically stored as a two-dimensional array, as shown in Figure 3. When the word address is given at the beginning of a write operation, both the row and column Address Pointers are set. The row Address Pointer selects which row, or page, is accessed, whereas the column Address Pointer selects which byte from the chosen page is accessed first. Upon transmission of each data byte, the column Address Pointer is automatically incremented. However, during a write operation, the page Address Pointer is not incremented, which means that attempting to cross a page boundary during a page write operation will result in the data being looped back to the beginning of the page.

Note that physical page boundaries start at addresses that are multiples of the page size. For example, the 24XX512 features a 128-byte page size, which means that physical pages on the device begin at addresses 0x0000, 0x0080, 0x0100, and so on.

FIGURE 3:   PAGE BUFFER BLOCK DIAGRAM

Note: n is equal to the page size - 1
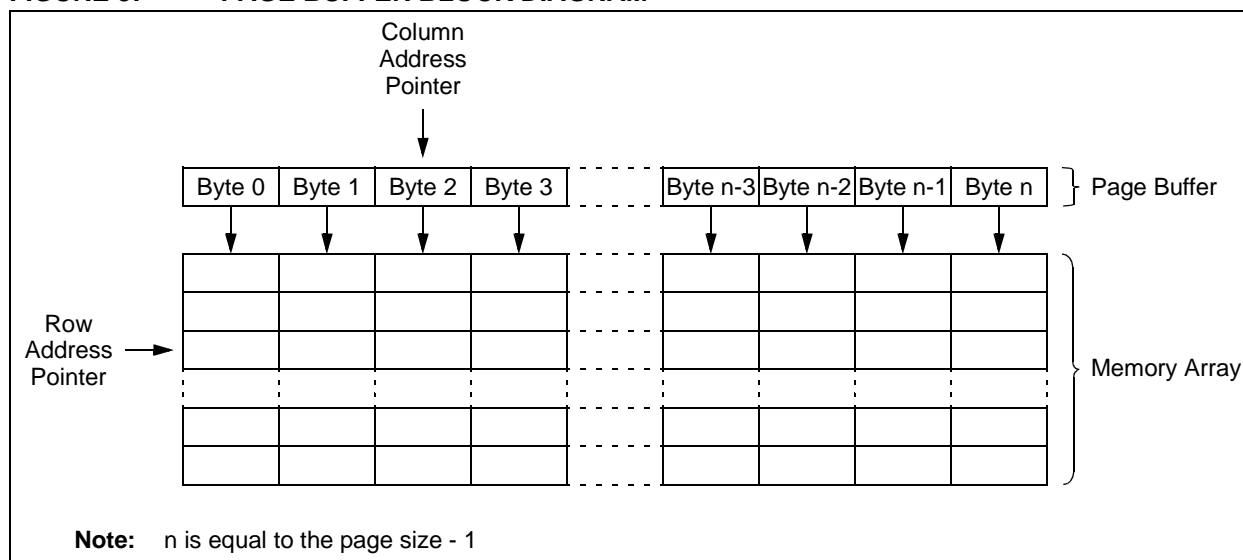
Procedure

The write control byte, word address, and the first data byte are transmitted to the device in the same way as in a byte write operation. But instead of generating a Stop condition, the master continues transmitting additional data bytes, which are temporarily stored in the on-chip page buffer, up to the maximum page size of the device. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin during which all bytes stored in the page buffer will be written.

Write Time Comparisons

In order to accurately calculate the full period of time required to write a particular amount of data to a device, two things must be considered.

- **Load time** is the amount of time needed to complete all bus operations. This includes generating Start and Stop conditions, as well as transmitting the control, address, and data bytes (including ACKs). This amount of time is dependent on the bus clock speed, the number of data bytes to be written, and the addressing scheme of the particular device (some devices utilize a 1-byte address, whereas others use a 2-byte address).

- **Write cycle time** is the time during which the device is executing its internal write cycle. As described in the previous section ("Acknowledge Polling"), there is a specified maximum write cycle time for each device. However, the internal write cycle typically completes in less time than specified. As such, both worst-case (5 ms) and typical (3 ms at T_{AMB} = 25 °C) calculations are provided in Table 1.

The following equations were used to calculate the values for Table 1:

EQUATION 1: WRITE TIME EQUATIONS

$$T_{LOAD} = \frac{9 \cdot (1 + \text{\# address bytes} + \text{\# data bytes}) + 1}{F_{CLK}}$$

$$T_{TOTAL} = (T_{LOAD} + T_{WC}) \cdot \text{\# write operations}$$

TABLE 1: WRITE TIME COMPARISONS

Device	Page Size (bytes)	# of Bytes to Write	Write Mode[1]	Clock Speed (kHz)	Load Time Per Operation (ms)	Total Time (ms) Worst-Case[2]	Total Time (ms) Typical[3]
24LC01B	8	1	Byte	100	0.28	5.28	3.28
		8	Byte	100	0.28	42.24	26.24
		8	Page	100	0.91	5.91	3.91
		1	Byte	400	0.07	5.07	3.07
		8	Byte	400	0.07	40.56	24.56
		8	Page	400	0.23	5.23	3.23
24LC16B	16	1	Byte	100	0.28	5.28	3.28
		16	Byte	100	0.28	84.48	52.48
		16	Page	100	1.63	6.63	4.63
		1	Byte	400	0.07	5.07	3.07
		16	Byte	400	0.07	81.12	49.12
		16	Page	400	0.41	5.41	3.41
24LC512	128	1	Byte	100	0.37	5.37	3.37
		128	Byte	100	0.37	687.36	431.36
		128	Page	100	11.80	16.80	14.80
		1	Byte	400	0.09	5.09	3.09
		128	Byte	400	0.09	651.84	395.84
		128	Page	400	2.95	7.95	5.95

Note 1: Byte Write mode signifies that only 1 byte is written during a single write operation.
Page Write mode signifies that a full page is written during a single write operation.

2: Worst-case calculations assume a 5 ms timed delay is used.

3: Typical calculations assume Acknowledge polling is used, with typical T_{WC} = 3 ms, T_{AMB} = 25 °C.

From these examples, it is clear that both page writes and Acknowledge polling can provide significant time savings. Writing 128 bytes to the 24LC512 via byte writes at 400 kHz requires roughly 652 ms worst-case. Switching to Acknowledge polling brings that down to roughly 396 ms (assuming typical conditions), nearly a 40% decrease. Additionally, changing to page writes further lowers the time to an impressive 5.95 ms, a decrease of over 98%. Overall, the two techniques provide a combined time savings of nearly 646 ms, increasing the total data throughput a staggering 109 times over.

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BUS PULL-UP RESISTORS

For proper operation, pull-up resistors are required for both SCL and SDA buses. However, the resistor value chosen can have a vast impact on the performance of the system. Specifically, three limiting factors must be considered when selecting pull-up resistor (R_P) values:

- Supply voltage (V_{CC})
- Total Bus Capacitance (C_{BUS})
- Total High-Level Input Current (I_{IH})

Supply Voltage (V_{CC})

Supply voltage limits the minimum R_P value due to maximum low-level output voltage (V_{OL}) specifications. Meaning that, for a given V_{CC} level, a smaller pull-up resistor will result in a higher output voltage. For Microchip I^2C devices, the V_{OL} specification is a maximum of 0.4V at 3 mA. In other words, if there is a voltage drop across R_P of V_{CC}-0.4V, it cannot be sourcing more than 3 mA. Applying Ohm's Law yields Equation 2.

EQUATION 2:   MINIMUM R_P VALUE

$$R_{PMIN} = \frac{V_{CC} - V_{OL}}{I_{OL}} = \frac{V_{CC} - 0.4V}{3\ mA}$$

Total Bus Capacitance (C_{BUS})

Bus capacitance includes all pin, connection, and wire capacitance on the bus. Due to the RC time constant, higher bus capacitance requires a smaller pull-up resistor to meet a particular rise time, and therefore, clock speed. This is an important consideration for designs consisting of many devices on a single bus.

Equation 3 is the general equation used to characterize charging of a capacitive load as a function of time. This allows for calculation of the amount of time required for the bus voltage to rise to a particular value for a specific pull-up resistance and bus capacitance.

EQUATION 3:   CAPACITOR CHARGING

$$V(t) = V_0(1 - e^{-t\, \S\, (RC)})$$

$$\Rightarrow -t = (RC)\ln\left(1 - \frac{V(t)}{V_0}\right)$$

Bus rise time (T_R) is defined as the amount of time required for the voltage to rise from V_{IL} to V_{IH}. Equation 3 is applied to calculate the bus rise time for V_{IL}=0.3*V_{CC} and V_{IH}=0.7*V_{CC}, and the result is shown in Equation 4. Note that because V_{IL} and V_{IH} are specified as functions of V_{CC}, the final equation is independent of V_{CC}, as long as the V_{IL} specification does not change.

EQUATION 4:   BUS RISE TIME

$$-T_1 = (RC)\ln\left(1 - \frac{V_{IL}}{V_{CC}}\right) = (RC)\ln(1 - 0.3)$$

$$\Rightarrow T_1 = 0.356675 \cdot RC$$

$$-T_2 = (RC)\ln\left(1 - \frac{V_{IH}}{V_{CC}}\right) = (RC)\ln(1 - 0.7)$$

$$\Rightarrow T_2 = 1.20397 \cdot RC$$

$$T_R = T_2 - T_1 = 0.847298 \cdot RC$$

Equation 4 can be quite useful in calculating bus rise time; however, such a parameter is already specified in the data sheet for different bus speeds. As such, the equation must be rearranged to be of any use in determining the maximum value of R_P as limited by bus rise time. This results in Equation 5.

EQUATION 5:   MAX. R_P DUE TO RISE TIME

$$R_{PMAX} = \frac{T_R}{0.847298 \cdot C_{BUS}}$$

Total High-Level Input Current (I_{IH})

The total high-level input current for a line is the total amount of current which will be flowing through the pull-up resistor when there are no contentions and the line is allowed to be pulled up by the resistor. This current consists of the sum of the input leakage currents for all devices connected to the bus, as well as any other current being sunk by the devices through the input pin.

Because some current will always exist through the pull-up resistor even without bus contention, the effective voltage seen at the pin will be lower than V_{CC} due to the voltage drop across the resistor. This voltage drop must be small enough that the voltage at the pin will still be considered a high by the device. That is, the voltage at the pin must be higher than V_{IH} combined with the high-level input noise margin (V_{HMAR}). Applying Ohm's Law once again results in Equation 6.

EQUATION 6:   MAX. R_P DUE TO CURRENT

$$R_{PMAX} = \frac{V_{CC} - (V_{IH} + V_{HMAR})}{I_{IH}}$$

Example Resistor Value Calculation

Here is an example of how to use the previous equations to select the appropriate pull-up resistor value. The following parameters will be used:

TABLE 2: **EXAMPLE PARAMETERS**

Parameter	Value	Units
V_{CC}	5.0	V
T_R	300[1]	ns
C_{BUS}	100	pF
V_{IH}	3.5[2]	V
V_{HMAR}	1.0[3]	V
I_{IH}	10	µA

Note 1: T_R based on desired clock speed of 400 kHz.

2: V_{IH} derived from 0.7*V_{CC} spec.

3: V_{HMAR} derived from 0.2*V_{CC} spec.

By applying Equation 2, Equation 5 and Equation 6, the following resistor value limits were calculated:

TABLE 3: **RESISTOR VALUE LIMITS**

Limit	Value	Limiting Factor
R_{PMIN}	1.533 kΩ	Supply Voltage
R_{PMAX}	3.541 kΩ	Bus Capacitance
R_{PMAX}	50 kΩ	Input Current

Although the input current is small enough that, at the specified V_{CC} level, a 50 kΩ resistor would not create too large of a voltage drop, such a large resistor would be far too slow for the specified bus capacitance. Therefore, the range of acceptable resistor values is from 1.533 kΩ to 3.541 kΩ. It is recommended to choose a value near the middle of the range to provide as much guard banding as possible. For this example, a 2.2 kΩ pull-up resistor would be ideal.

Bus Speed vs. Power Consumption

In order to reach a given bus speed, larger bus capacitance requires smaller pull-up resistors. For instance, in the above example, the calculated value for R_{PMAX} due to bus capacitance was 3.541 kΩ at 100 pF. However, if the bus capacitance were increased to roughly 231 pF, the new R_{PMAX} value would be 1.533 kΩ. This smaller resistor would, in turn, allow more current to be drawn when a device pulls down the bus. Specifically, a maximum of 3.26 mA at 1.533 kΩ versus 1.41 mA at 3.541 kΩ.

Larger currents due to smaller pull-up resistors can have a considerable effect on power consumption and battery life. As such, it is recommended that the slowest bus speed tolerable by the design be chosen. In the example above, simply decreasing to 100 kHz (1000 ns rise time) allows for a 5.109 kΩ pull-up resistor to be used, at 231 pF. This lowers the maximum current to 0.979 mA.

SOFTWARE RESET SEQUENCE

At times it may become necessary to perform a software Reset sequence to ensure the serial EEPROM is in a correct and known state. This could be useful, for example, if the EEPROM has powered up into an incorrect state (due to excessive bus noise, etc.), or if the microcontroller is reset during communication. The following sequence can be sent in order to ensure that the serial EEPROM device is properly reset:

- Start bit
- Clock in nine bits of '1'
- Start bit
- Stop bit

FIGURE 4: **SOFTWARE RESET SEQUENCE**
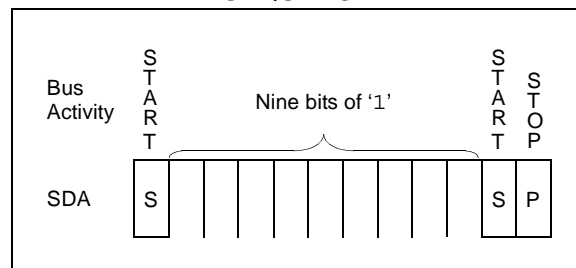
The first Start bit will cause the device to reset from a state in which it is expecting to receive data from the microcontroller. In this mode, the device is monitoring the data bus in Receive mode and can detect the Start bit which forces an internal Reset.

The nine bits of '1' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the device is in a mode where it is either driving an acknowledge on the bus (low), or is in an Output mode and is driving a data bit of '0' out on the bus. In both of these cases the previous Start bit (defined as SDA going low while SCL is high) could not be generated due to the device holding the bus low. By sending nine bits of '1' it is ensured that the device will see a NACK (i.e., the microcontroller does not drive the bus low to acknowledge data sent by the EEPROM), which also forces an internal Reset.

The second Start bit is sent to guard against the rare possibility of an erroneous write that could occur if the microcontroller was reset while sending a Write command to the EEPROM, and, the EEPROM was driving an ACK on the bus when the first Start bit was sent. In this special case, if this second Start bit was not sent, and instead the Stop bit was sent, the device could initiate a write cycle. This potential for an erroneous write occurs only in the event of the microcontroller being reset while sending a Write command to the EEPROM.

The final Stop bit terminates bus activity and puts the EEPROM in Standby mode.

This sequence does not affect any other I^2C devices which may be on the bus as they will simply disregard it as an invalid command.

In situations where the software Reset sequence is needed, a bus conflict is likely to occur. When using the MSSP module, this will cause the Bus Collision Flag (BCLIF) to be set and, therefore, will block any further bus transactions. In order to issue a software Reset, the module will need to be disabled and the software Reset sequence will need to be bit-banged. Once the software Reset sequence is complete, the module can be re-enabled, the Bus Collision Flag cleared, and the MSSP module will be ready for normal bus operations.

SUMMARY

This application note illustrates recommended techniques for increasing design robustness when using Microchip I^2C serial EEPROMs. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies, and tests its serial EEPROMs and will allow the devices to operate within the data sheet parameters. It is suggested that the concepts detailed in this application note be incorporated into any system which utilizes an I^2C serial EEPROM.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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