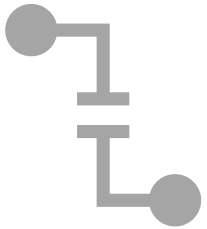
Advance Algorithm Summer Session project

Retiming of a graph

Retiming problem

Problem

Optimize the frequency of a circuit



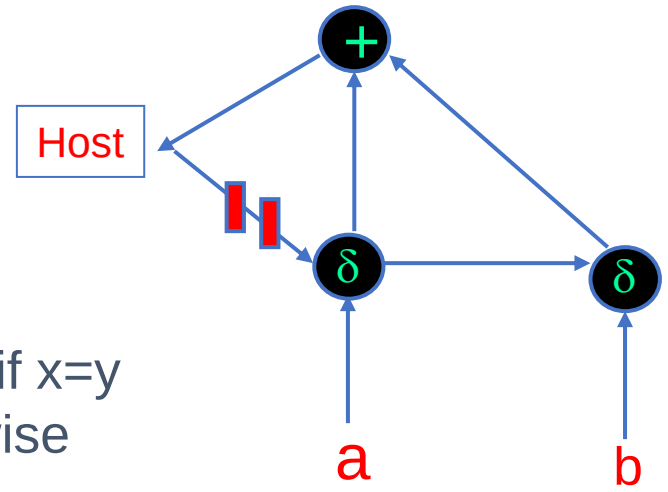
Solutions

Move register(s) so that

- clock cycle decreases, or number of registers decreases and
- input-output behavior is preserved

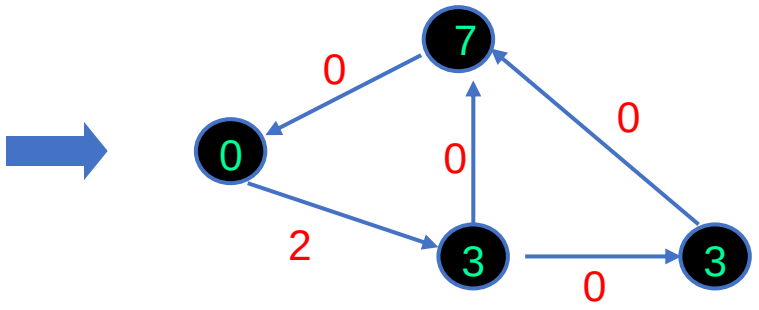
Circuit Representation

Example: Correlator (from Leiserson and Saxe) (simplified)



Circuit

δ(x, y) = 1 if x=y
0 otherwise



Retiming Graph (Directed)

Every cycle in Graph has at least one register i.e. no combinational loops.

Operation	delay
δ	3
+	7

Circuit Representation

Circuit represented as retiming graph G(V,E,d,w)

- V ↔ set of gates
- E ↔ set of connections
- d(v) = delay of gate/vertex v, (d(v)≥0)
- w(e) = number of registers on edge e, (w(e)≥0)

Clock Cycle

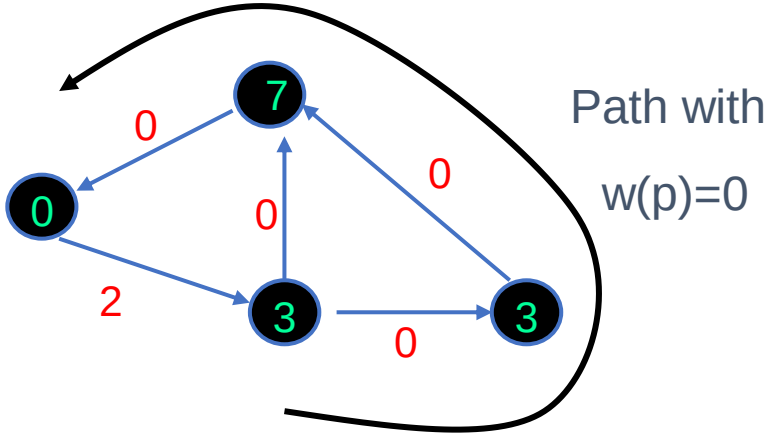
For a path p : $v_0 \xrightarrow{e_0} v_1 \xrightarrow{e_1} \cdots v_{k-1} \xrightarrow{e_{k-1}} v_k$

$$d(p) = \sum_{i=0}^{k} d(v_i) \quad \text{(includes endpoints)}$$

$$w(p) = \sum_{i=0}^{k-1} w(e_i)$$

Clock cycle

$$c = \max_{p:\, w(p)=0} \{d(p)\}$$



Path with w(p)=0

For correlator c = 13

Retiming for Minimum Clock Cycle

Problem Statement: (minimum cycle time)

Given G (V, E, d, w), find a legal retiming so that

$$c = \max_{p:\, w_r(p)=0} \{d(p)\}$$

is minimized

Implementation details

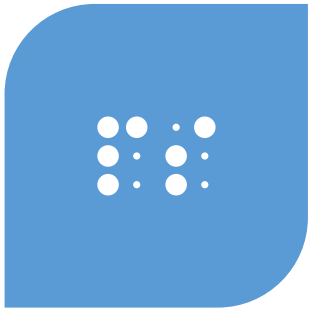
- Reference paper:
  - C. E. Leiserson and J. B. Saxe, "Retiming Synchronous Circuitry", Digital Systems Research Center, Report 18, August 20, 1986.
  - Implement Algorithms: WD, OPT1, FEAS and OPT2
- Use BGL – Boost Graph Library to describe the Retiming Graph
  - https://www.boost.org/doc/libs/1_67_0/libs/graph/doc/index.html
- Testcases: random generated retiming graph
- Python vs C++
- Anti plagiarism software – Honor code
- Share a GitHub repo. Private repo are free for students

Evaluation

HOW IT IS PRESENTED

HOW IT IS DOCUMENTED

HOW IT IS TESTED



HOW IT IS ASSESSED

AAPP exam

- From the exam rules:
- It is possible to integrate or to partially skip the written exam with either a programming project or a report on further readings
  - Project on parallelization -> skip II part
  - Project on advanced algorithms -> skip I part

- In case you pass this take-home project, you will skip the I part of the exam