Project 1

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COMPE 572: VSLI Circuit Design

Dr. Ying-Khai Teh

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# Diversity Bonus

We claim \_\_\_\_\_ as our “Diversity Hire.” They are \_\_\_\_\_

# The M.V.P. Award

\_\_\_\_\_ was the most important person for our team. They really \_\_\_\_\_\_

# Project 1: MOS SPICE modeling IV extraction and Inverter Design

This project involves the comprehensive simulation of Metal-Oxide-Semiconductor (MOS) devices using SPICE models. The primary objectives include performing I-V (current-voltage) characteristic extraction for both NMOS and PMOS transistors, analyzing their behavior in various conditions, and designing a minimal-sized CMOS inverter circuit.

The project begins with selecting either the AMI 06 or TSMC 04\_4M\_2P technology model to extract transistor parameters such as minimal channel length and standard supply voltage. Subsequently, DC analysis is conducted to obtain drain current-drain voltage curves for minimally sized NMOS and PMOS transistors across a range of gate voltages. The threshold voltage and circuit parameter k(μCOX​) are determined by comparing the simulated curves with theoretical saturation current equations.

Additionally, the impact of body bias (V\_BS) on the transistor's performance is explored by adjusting V\_BS to -0.3V and 0.3V. This analysis helps in understanding how variations in body voltage affect the threshold voltages of NMOS and PMOS transistors.

Finally, a minimally sized CMOS inverter circuit is designed, and its transfer characteristics (V\_OUT-V\_IN) are analyzed to determine the mid-supply voltage (VM​). The project concludes with designing a matched inverter where VM​=0.5VDD​, optimizing transistor widths-to-lengths ratios accordingly.

Overall, this project aims to provide a detailed understanding of MOS device behavior and CMOS inverter design through SPICE simulation tools.

# Method (Heading Level 1)

## Participants (Heading Level 2)

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## Assessments and Measures

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### Heading Level 3

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# Results

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## Outcome 1

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## Outcome 2

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# Discussion

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# References

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