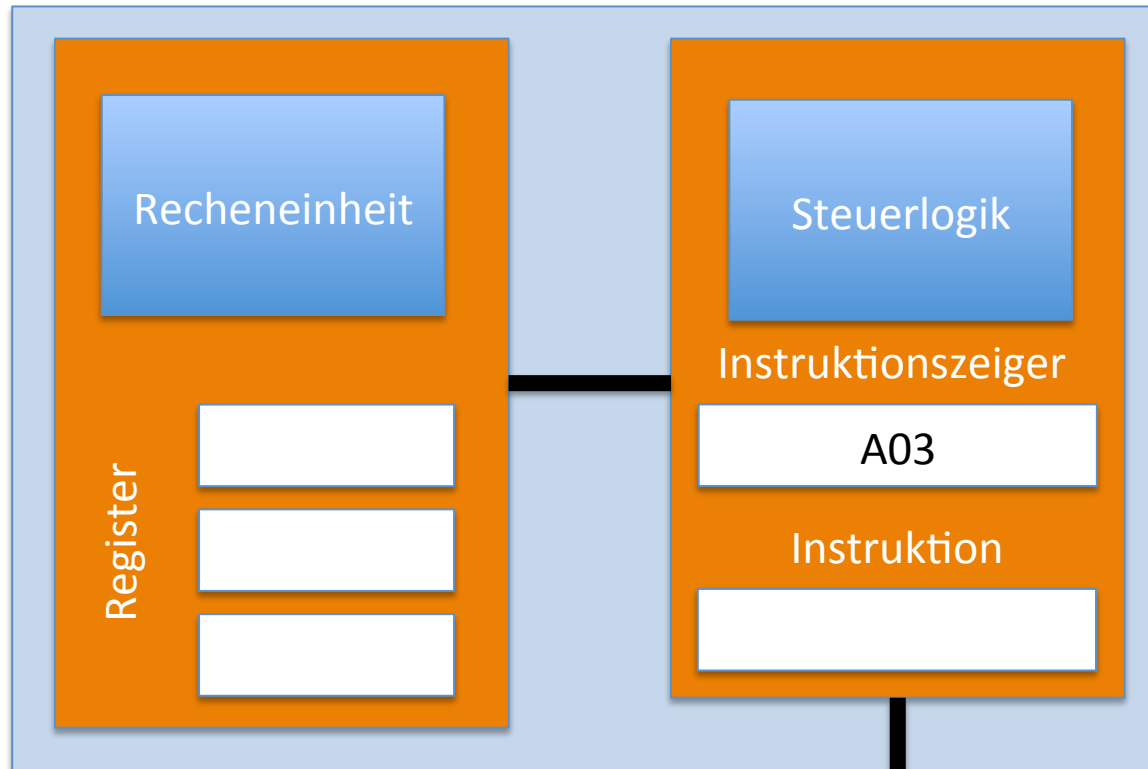
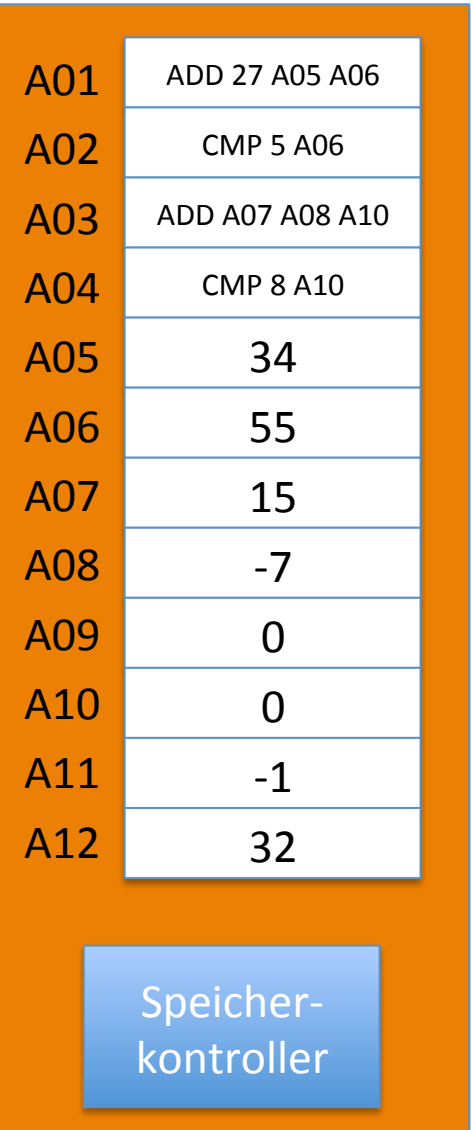


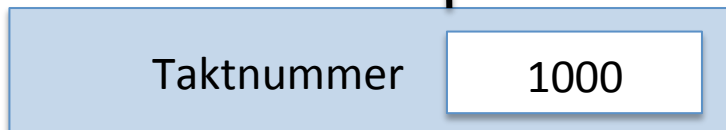
# CPU



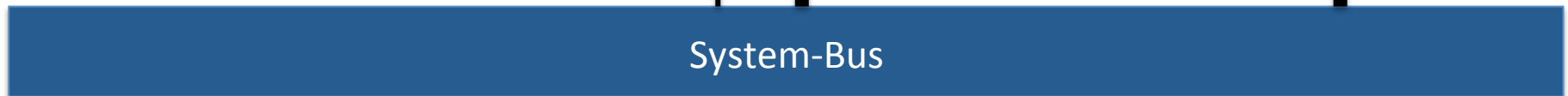
# Hauptspeicher



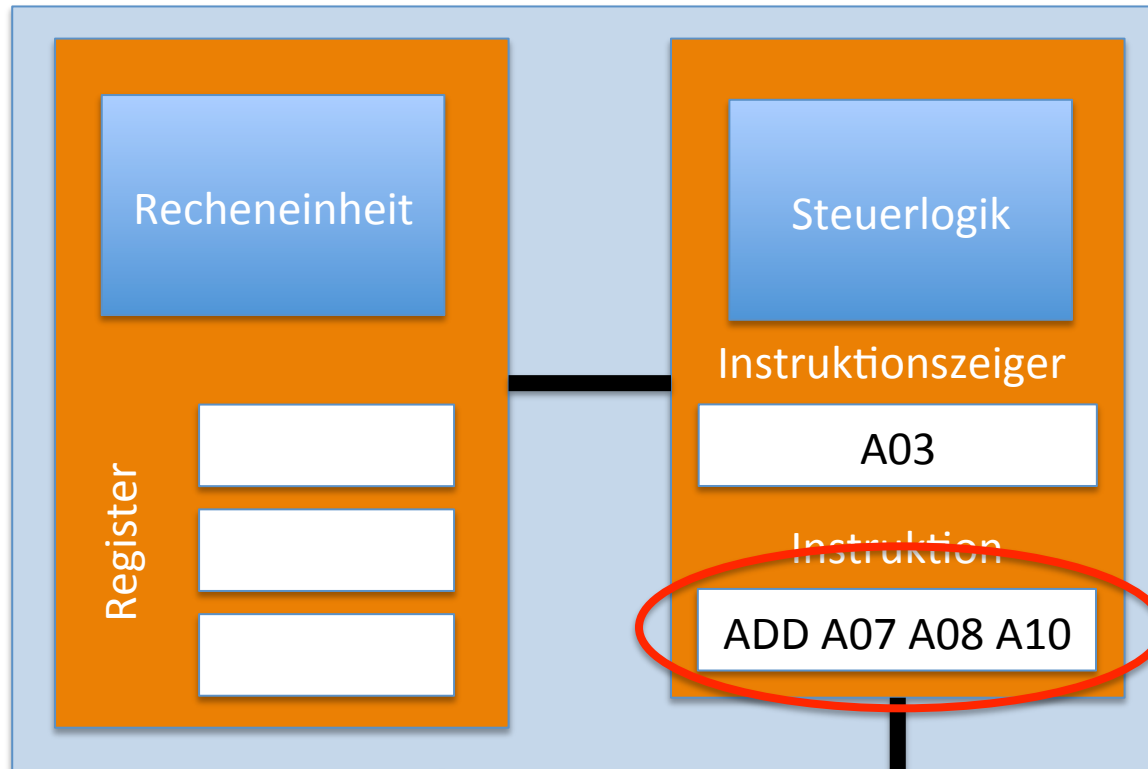
# Taktgeber



# System-Bus



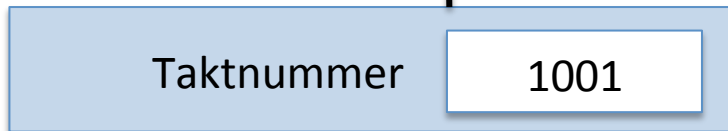
# CPU



# Hauptspeicher

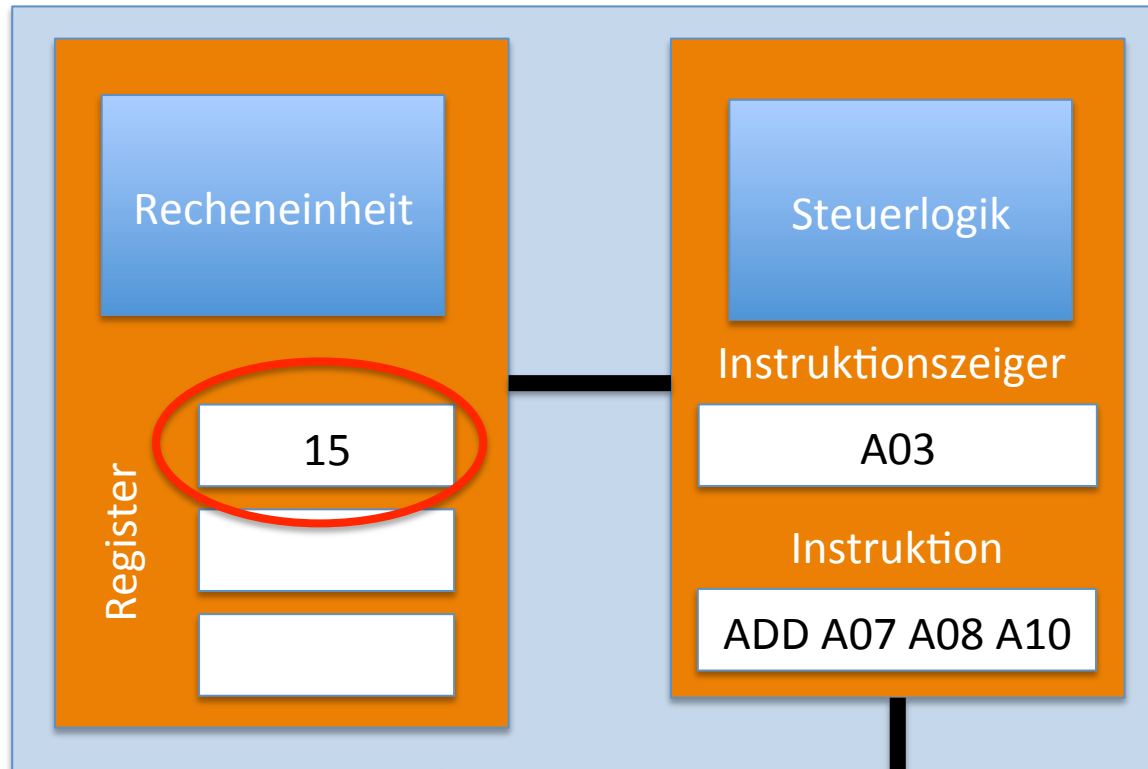
A01	ADD 27 A05 A06
A02	CMP 5 A06
A03	ADD A07 A08 A10
A04	CMP 8 A10
A05	34
A06	55
A07	15
A08	-7
A09	0
A10	0
A11	-1
A12	32

# Taktgeber

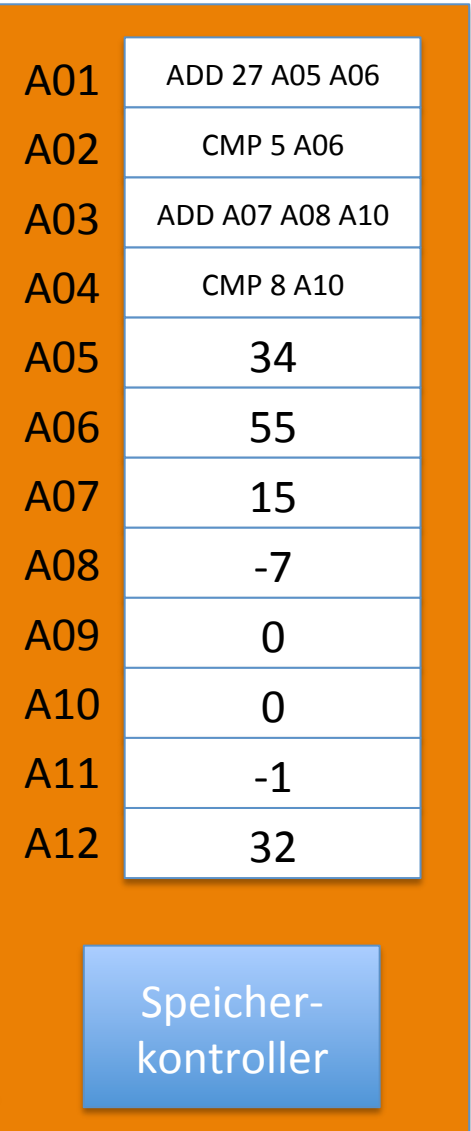


# System-Bus

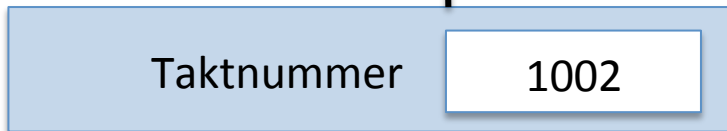
# CPU



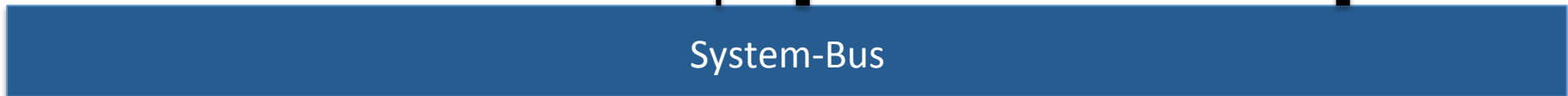
# Hauptspeicher



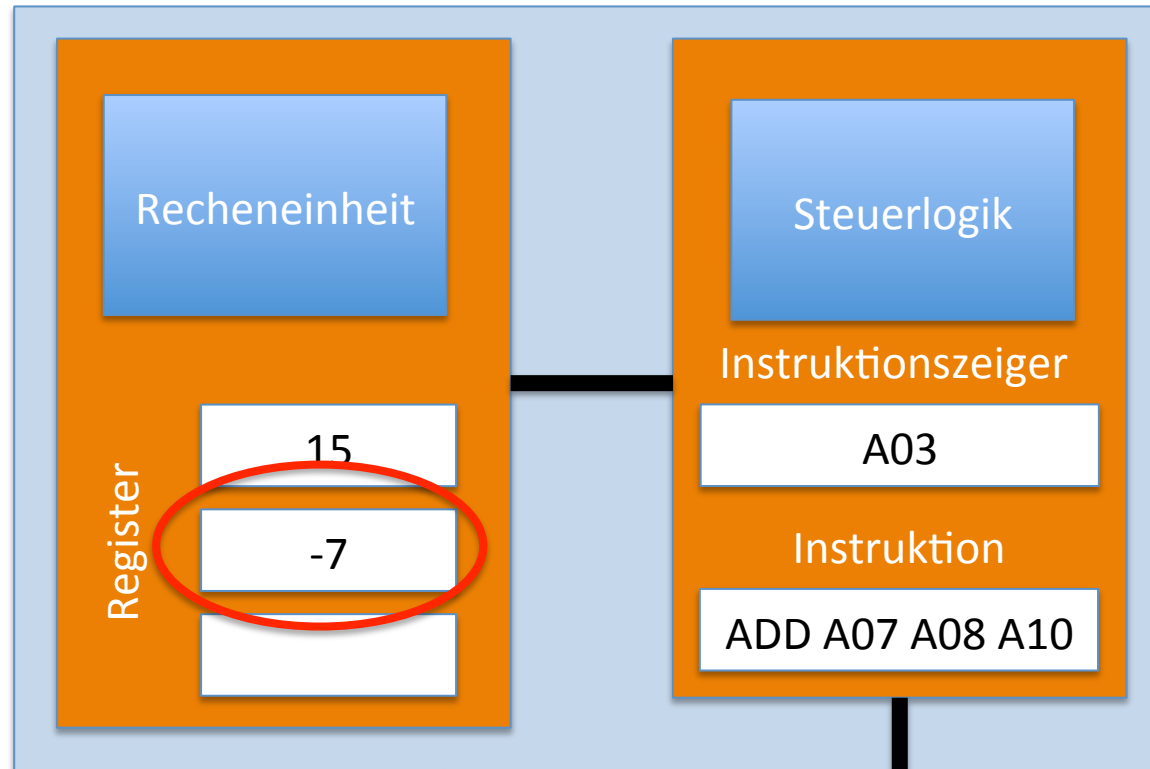
# Taktgeber



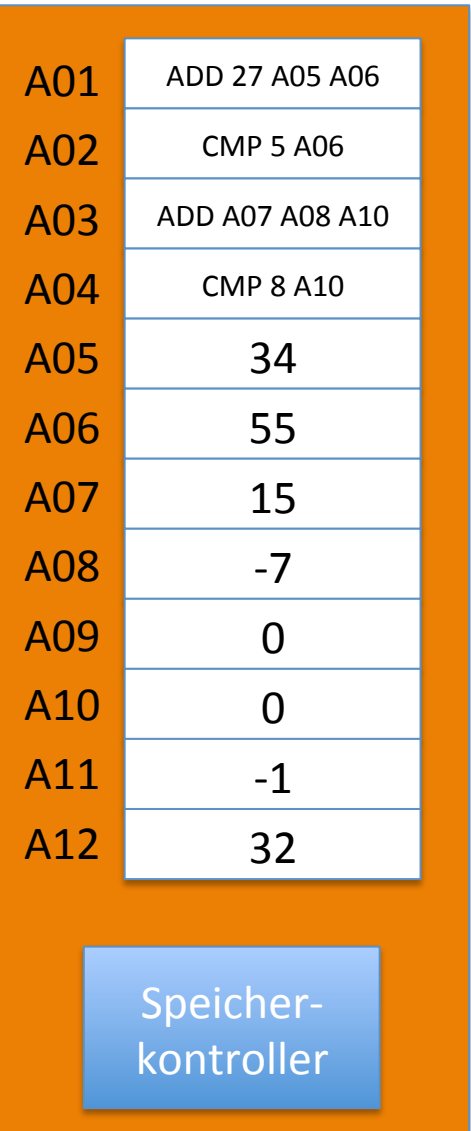
# System-Bus



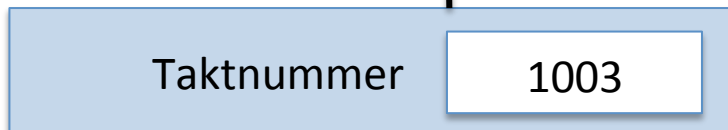
# CPU



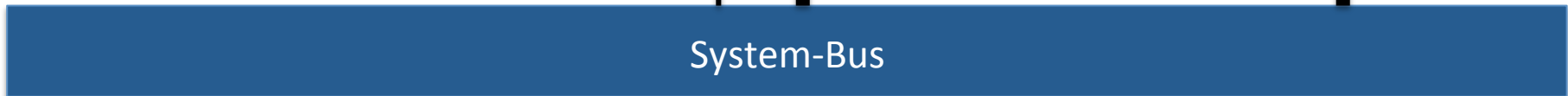
# Hauptspeicher



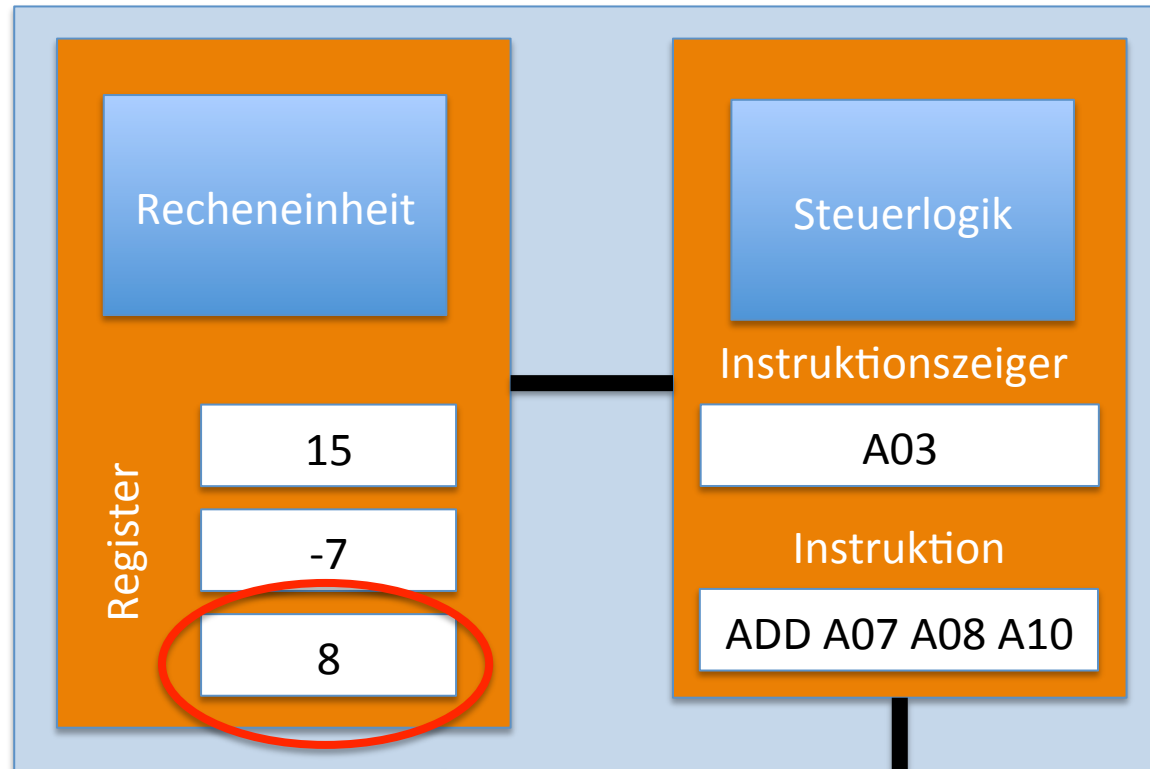
# Taktgeber



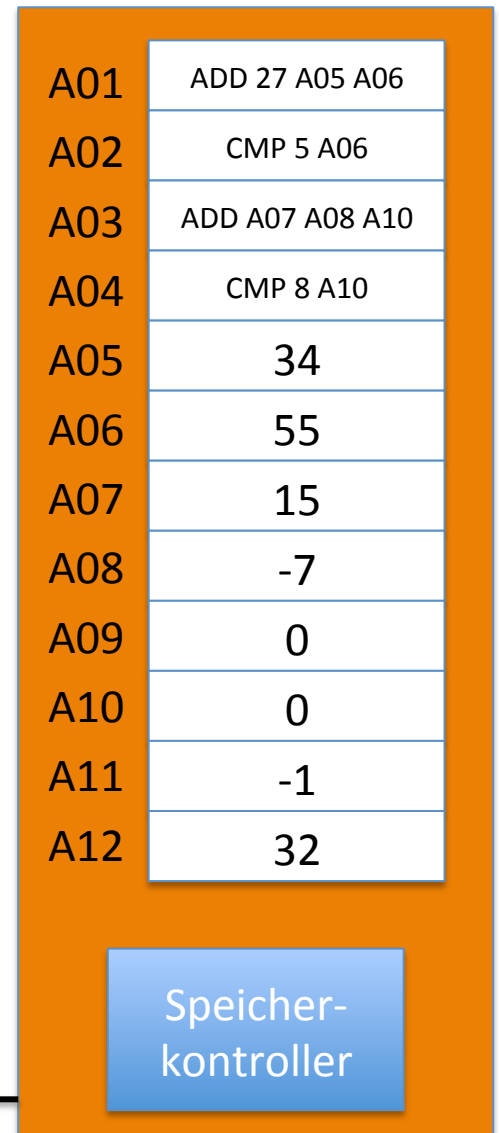
# System-Bus



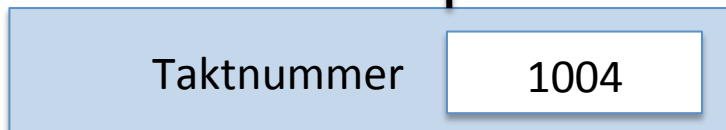
# CPU



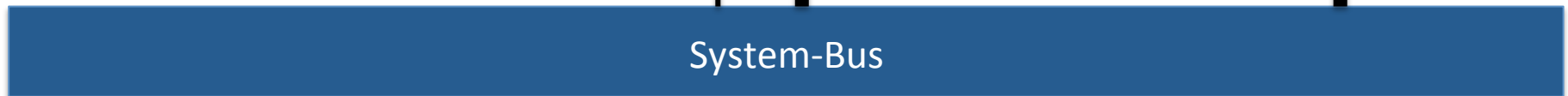
# Hauptspeicher



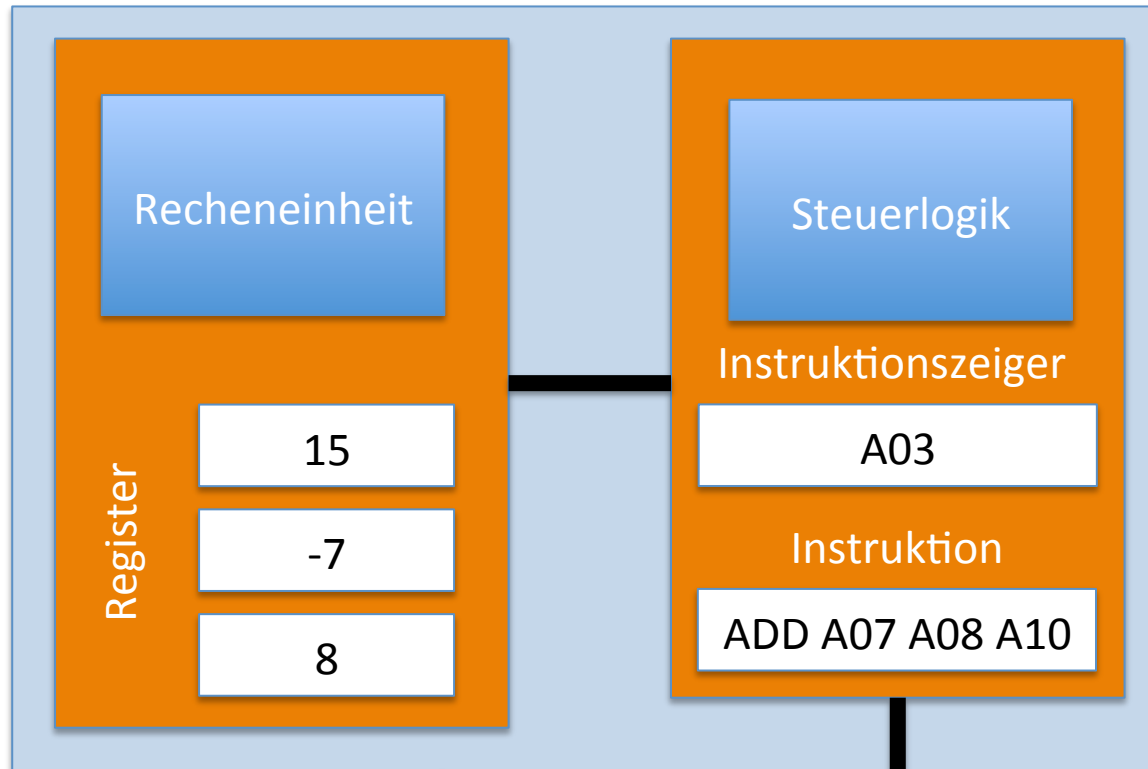
# Taktgeber



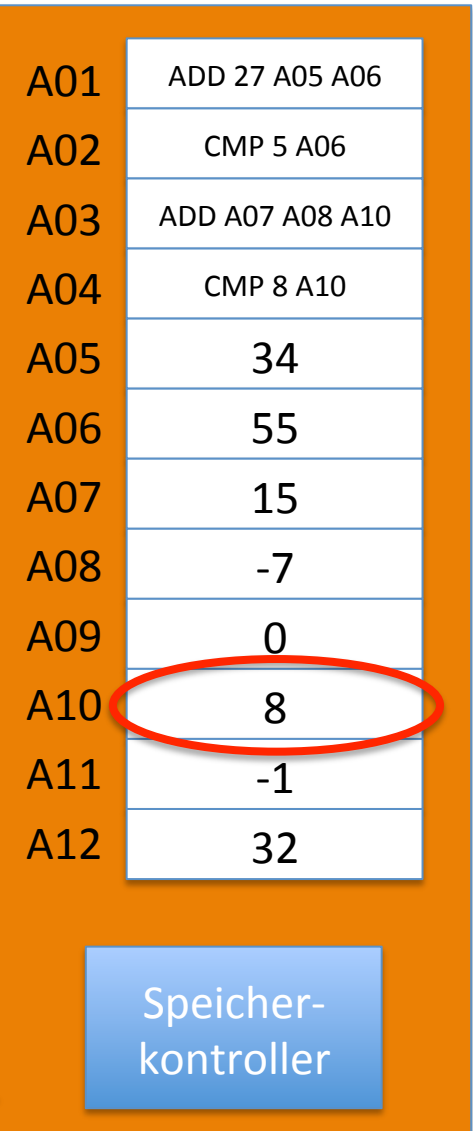
# System-Bus



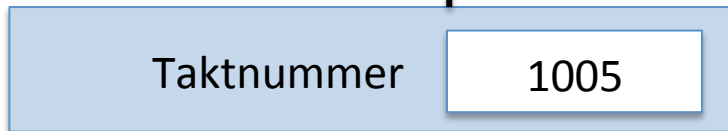
# CPU



# Hauptspeicher

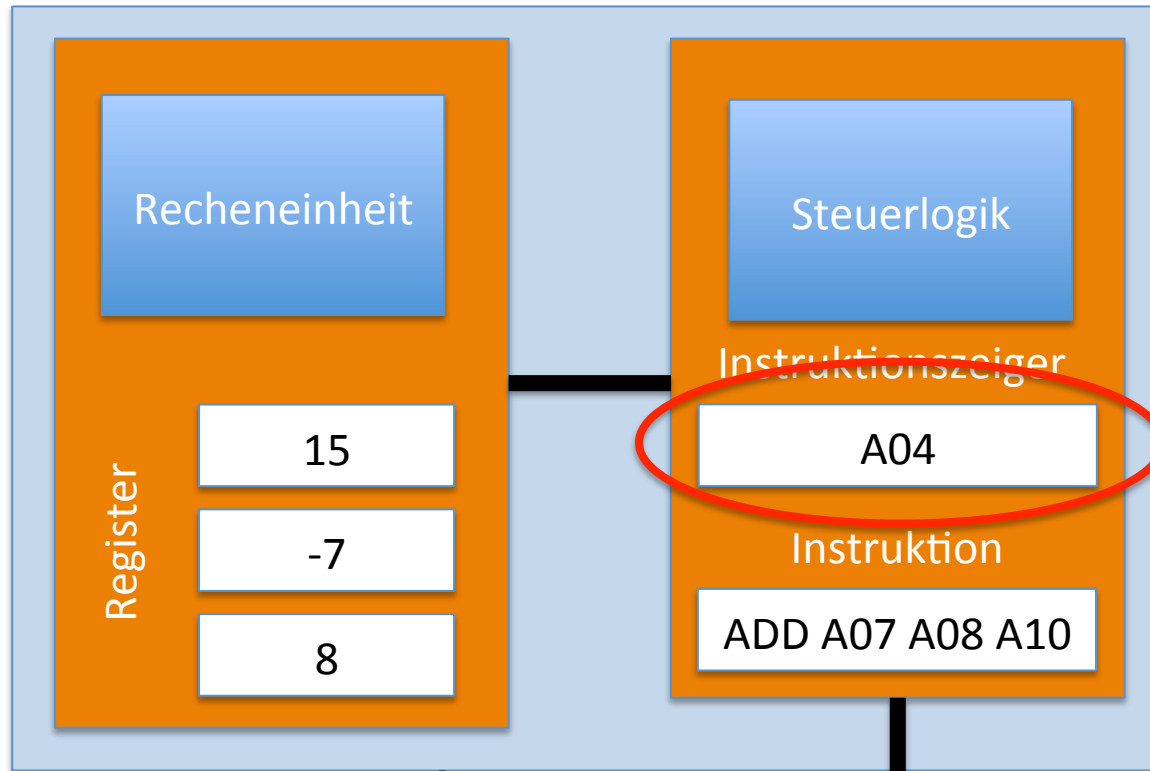


# Taktgeber

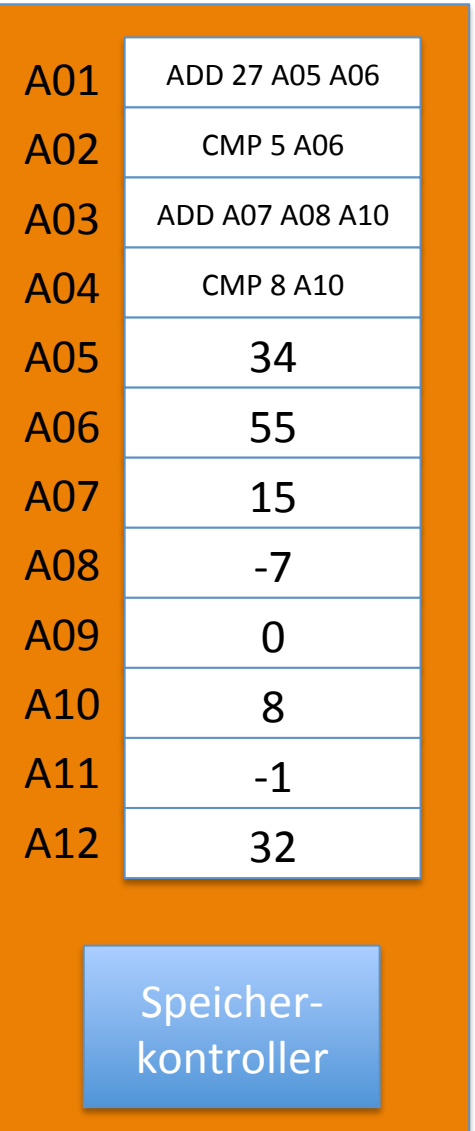


System-Bus

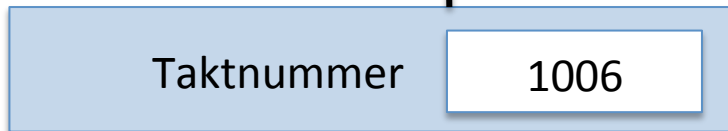
# CPU



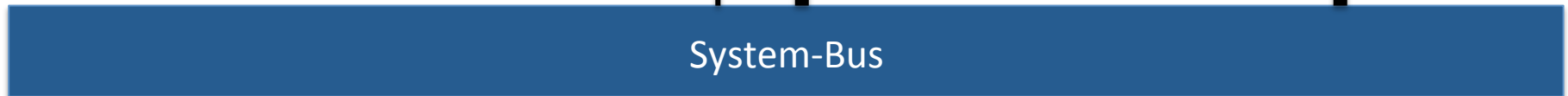
# Hauptspeicher



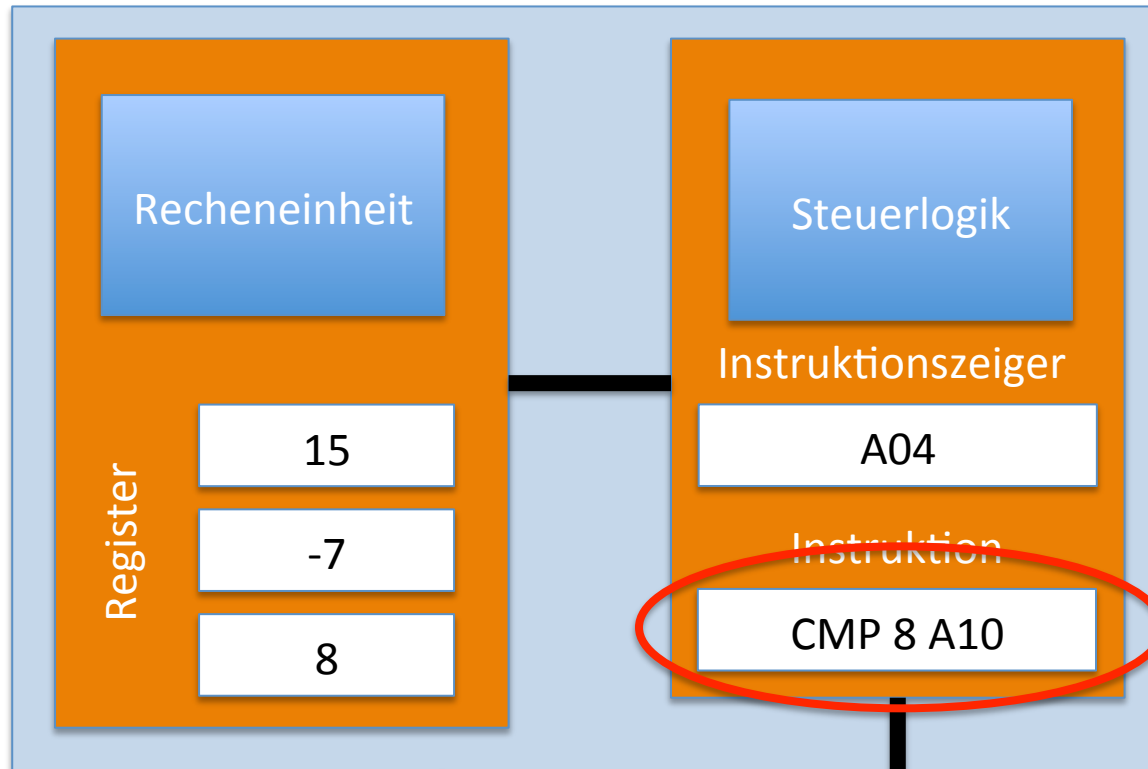
# Taktgeber



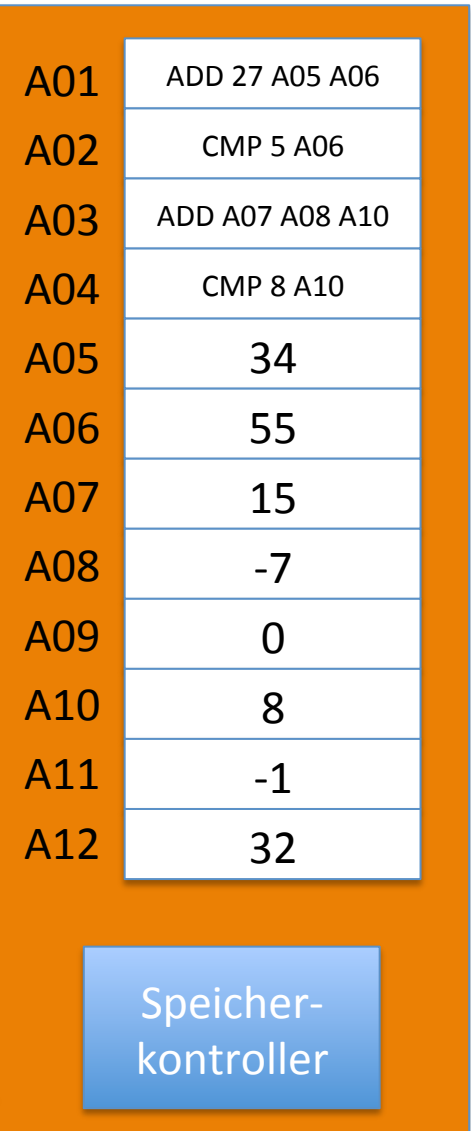
# System-Bus



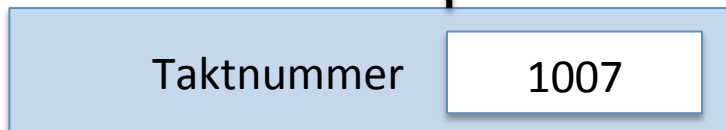
# CPU



# Hauptspeicher



# Taktgeber



# System-Bus

