3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 8 Kbyte SRAM2 in Standby with SRAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L412xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The V_{CORE} can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L412xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.

Table 4. STM32L412xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Run	MR range 1	Yes	ON[4]	ON	Any	All	N/A	91 µA/MHz	N/A
	SMPS range 2 high							34 µA/MHz	
	MR range2					All except USB_FS, RNG		79 µA/MHz	
	SMPS range 2 low							28 µA/MHz	
LPRun	LPR	Yes	ON[4]	ON	Any except PLL	All except USB_FS, RNG	N/A	83 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	MR range 1	No	ON[4]	ON[5]	Any	All	Any interrupt or event	21 µA/MHz	6 cycles
	SMPS range 2 high							7.5 µA/MHz	
	MR range2					All except USB_FS, RNG		20 µA/MHz	
	SMPS range 2 low							7 µA/MHz	
LPSleep	LPR	No	ON[4]	ON[5]	Any except PLL	All except USB_FS, RNG	Any interrupt or event	83 µA/MHz	6 cycles
Stop 0	MR Range 1	No	OFF	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMP1, OPAMP1 USARTx (x=1...3)[6] LPUART1[6] I2Cx (x=1...3)[7] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMP1 USARTx (x=1...3)[6] LPUART1[6] I2Cx (x=1...3)[7] LPTIMx (x=1,2) USB_FS[8]	105 µA	2.47 µs in SRAM 4.1 µs in Flash
	MR Range 2								

Table 4. STM32L412xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMP1, OPAMP1 USARTx (x=1...3)[6] LPUART1[6] I2Cx (x=1...3)[7] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMP1 USARTx (x=1,..3)[6] LPUART1[6] I2Cx (x=1...3)[7] LPTIMx (x=1,2) USB_FS[8]	3.25 µA w/o RTC 3.65 µA w RTC	5.7 µs in SRAM 7 µs in Flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMP1 I2C3[7] LPUART1[6] LPTIMx (x = 1, 2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMP1 I2C3[7] LPUART1[6] LPTIMx (x = 1, 2)	710 nA w/o RTC 950 nA w RTC	5.8 µs in SRAM 8.3 µs in Flash

Table 4. STM32L412xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Standby	LPR	Powered Off	Off	SRAM 2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)[9] BOR, RTC, IWDG	195 nA	16.1 µs
	OFF			Powered Off				105 nA	
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down[10]	Reset pin 5 I/Os (WKUPx)[9] RTC	18 nA	256 µs

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at V_{DD} = 1.8 V, 25°C. Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
5. The SRAM1 and SRAM2 clocks can be gated on or off independently.
6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. USB_FS wakeup by resume from suspend and attach detection protocol event.
9. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PA2, PC5.
10. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.