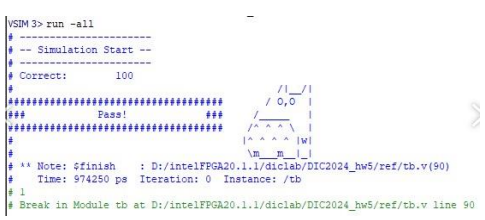
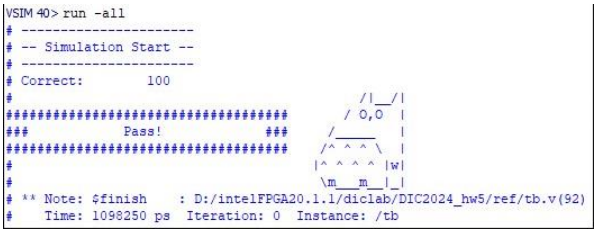
2024 Digital IC Design Homework 5

NAME	盧尚毅
Student ID	N26124264
Score = area*timing (ps)	50058235000
Cycle time (ns)	9.5

Simulation Result

Functional simulation	Completed	Gate-level simulation	Completed





Flow Status	Successful - Wed Jun 19 20:37:48 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AES
Top-level Entity Name	AES
Family	Cyclone IV E
Device	EP4CE75F29C8
Timing Models	Final
Total logic elements	45,580 / 75,408 (60 %)
Total registers	2720
Total pins	387 / 427 (91 %)
Total virtual pins	0
Total memory bits	0 / 2,810,880 (0 %)
Embedded Multiplier 9-bit elements	0 / 400 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

在此次的設計中，我先利用組合電路完成每一 round 所需要的動作，並複製 10 組，再新增一組電路用於將一開始輸入的 K 與 P 進行 XOR 動作，並寫出十個 key expansion 的電路，最後在一個 flip-flop 中將每一次的輸入與輸出，送至下一個 register，達成 pipeline 的硬體設計。

The scoring standard: (The smaller, the better)

Scoring =

*Area cost * Timing cost*

Area cost =

*Total logic elements + total memory bits + 9*embedded multiplier 9-bit elements*

Timing cost =

Simulation time

Flow Summary

<<Filter>>

Flow Status	Successful - Mon May 20 14:38:37 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AES
Top-level Entity Name	AES
Family	Cyclone IV E
Device	EP4CE75F29C8
Timing Models	Final
Total logic elements	45,971
Total registers	2954
Total pins	387
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

```
# Correct:        100
#                                          /|__/|
####################################      / 0,0  |
###            Pass!              ###    /_____   |
####################################    /^ ^ ^ \  |
#                                       |^ ^ ^ ^ |w|
#                                        \m___m__|_|
# ** Note: $finish    : C:/Users/diclab/Desktop/DIC2024/HW5_/tb.v(99)
#    Time: 991250 ps  Iteration: 0  Instance: /tb
```