Lab 5 Report (ECE558)
Further Usage of Automated Processes in VLSI

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***Purpose & Introduction* — This lab primarily focusses on the potential of synthesis that could be used to maximize number of tiles can be fit into a 1mm x 1mm (1 mm^2) floorplan. In short, a semi continuation of where lab 4 was.**

I. Problem Statement and Objectives (Section 1):

A. Problem Statement and Goal

As we have seen in the last step of lab 4, the synthesis and encounter automated generation of the layout is not necessarily desirable. As a continuation of lab 4, this lab will primarily focus on ways that a person can optimize encounter's simulation to better fit a 1mm x 1mm area with the below tile's characteristics:

Table 1. *Tile's characteristic from CompileAnalyzer*

Max Time (ns)	Cells	Area (um^2)
20	30577	58951.45

Our goal is trying to find a tile's layout area that allows us to fit the most number of tiles within a 1 mm^2 chip area. As learned in lab 3 and 4, the tile's layout could be greatly influenced by the aspect ratio, density configuration and the position of constrain pins. ***Doing this will attempt to reduce wasted space within the encounter's layout simulation.***

B. Objectives and Reasons for Picking

As we have learned in class, VLSI industry works with microscopic items, as such, even with only 100 um^2 wasted, it is a huge downside as ***wasted space correlates to wasted money and unproductivity (since so many things can still be fitted into the design with that wasted space).***

This problem is intriguing to me ***because when working for VLSI field, we must get used to optimizing our design, in other words, making our design (be it tiles, gates, or chip) to work correctly and as small as possible***, has always been one of the most sought-after criteria of VLSI industry. In addition, once we begin to pursue this field, it will be more and more obvious to see that it is impossible to design an entire chip from scratch, therefore, ***we need to learn how to use powerful simulation tools to approach more complex designs***.

II. Experimental Plan (Section 2):

A. Design and Format

The tile design that I will be using are completely the same with what we had in lab 4, which means that all the associated files and simulations steps prior to the encounter's simulation can be found within my lab 4 report. This is primarily because I intended for ***this lab to be an extension of lab 4.***

To reduce the amount of wasted space within encounter's simulation, I would try ***changing aspect ratio and the density of encounter's configuration***. The aspect ratio and density are very important in minimizing the wasted space, due to the fact that, ***in layout, metals need to be a certain distance apart from each other, otherwise this will cause DRC violations*** (as per described in my lab 4, section 5 step EXTRA). DRC violations are important as we can't simply shrink the size alone and ignore the functionality of the layout.

B. Tools and Usage

The tools, associated files, and their purposes are as follow:

Table 2. *Tools and Files needed*

Tools/Files	Purpose
Synthesis	Construction of the initial Tile's design
Encounter (p&r)	Layout simulation of Tile's design
Lab 4 Files	RTL, specifications, etc. Serve as the foundation to kickstart lab 5's analysis

Below is the figure of the initial tile's layout with aspect ratio of 1 and density of 0.9:

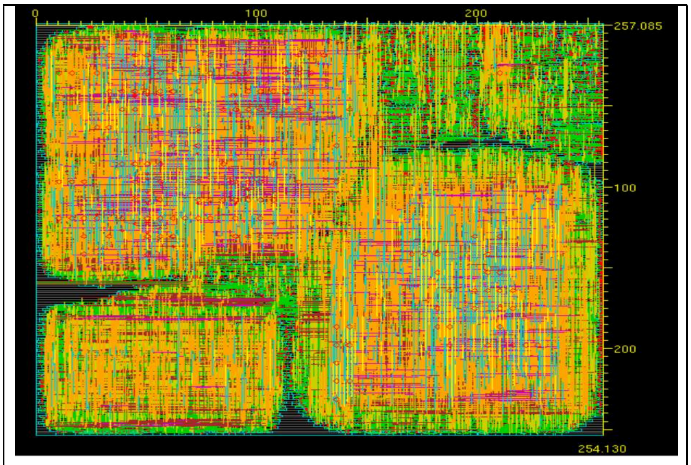

Figure 1. *Encounter – Tile's physical view wires and vias*

Table 3. *Encounter's simulation of initial Tile*

Aspect ratio	Density	Cells	Area (um^2)	DRC
1	0.9	30577	65501	0

C. What data and information am I looking for?

To answer how many tiles can be fitted into a 1 mm^2 chip, I am looking for the encounter's simulation output, and specifically that of layout and DRC violation from encounter's place and route process. ***From here on out, I will refer to aspect ratio as "ar" and density as "d".***

As observe in Fig. 1, we see some empty (wasted) space, and this lab seeks to reduce the amount of wasted space while keeping the simulation free of DRC violations.

III. Result and Analysis (Section III):

A. *Encounter simulation with ar = 0.5 and d = 0.9*

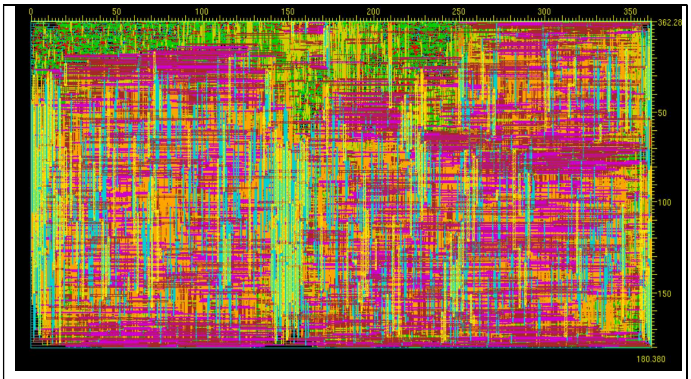

Figure 2. *Tile's physical view: wires & vias with nano routing*

Table 4. *Encounter's simulation of modified Tile*

Aspect ratio	Density	Cells	Area (um^2)	DRC
0.5	0.9	30577	65348.0664	0

We see that the encounter area is not quite the same with what specified in the CompileAnalyzer simulation. Which means that we have around 7000 um^2 area difference between encounter's result when compared with that of CompileAnalyzer. This is largely due to a parameter called density within encounter's configuration, and in order to better match the area between CA and Encounter, we have to get the density to be as close to 1 as possible while still maintaining 0 DRC violations.

B. *Encounter simulation with ar = 0.5 and d = 0.95*

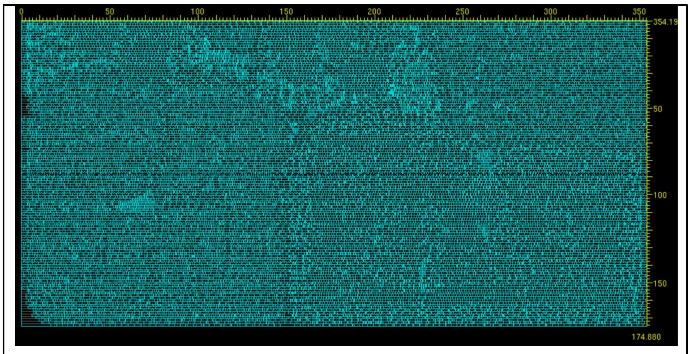

Figure 3. *Encounter's nano route – physical view no wires*

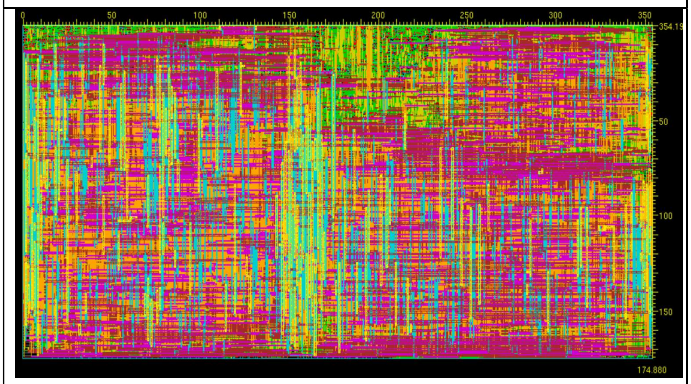

Figure 4. *Encounter's nano route – physical view with wires*

Table 5. *Encounter's simulation of modified Tile*

Aspect ratio	Density	Cells	Area (um^2)	DRC
0.5	0.95	30577	61940.7472	0

In Fig. 3, we can almost cover up every wasted space, as the figure barely has any area that is not covered with cell instances, but we can do better.

C. *Encounter simulation with ar = 0.5 and d = 0.97*

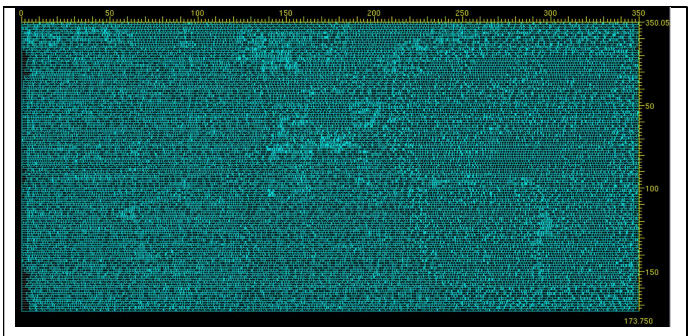

Figure 5. *Encounter's nano route – physical view no wires*

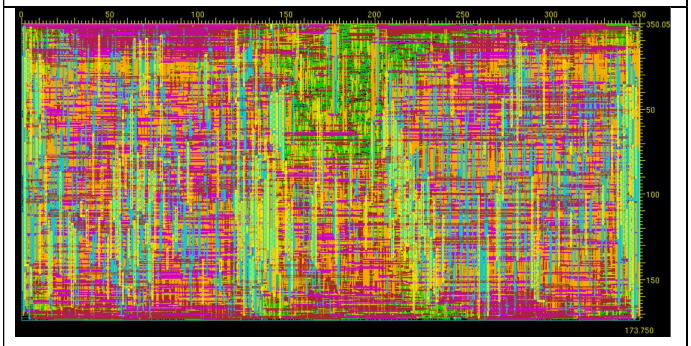

Figure 6. *Encounter's nano route – physical view with wires*

Table 6. *Encounter's simulation of modified Tile*

Aspect ratio	Density	Cells	Area (um^2)	DRC
0.5	0.97	30577	60757	0

Now we can see the trend that the area is getting smaller and smaller (as well as approaching the standard cell area stated in table 1), ***but some wasted spaces can be observed on the left edge of the figure***, thus, increasing the density by another notch.

D. *Encounter simulation with ar = 0.5 and d = 0.985*

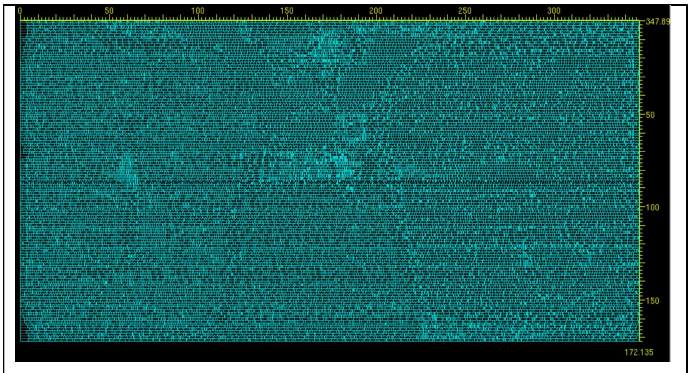

Figure 7. *Encounter's nano route – physical view no wires*

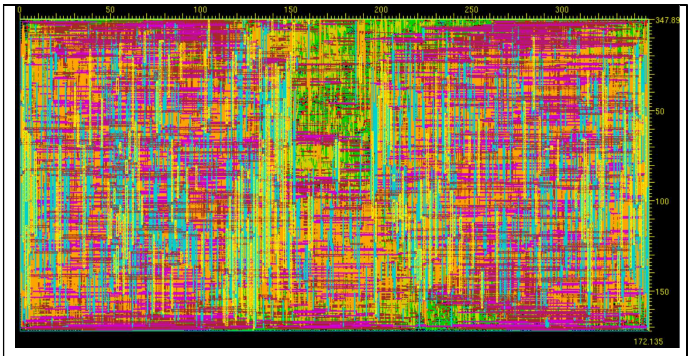

Figure 8. *Encounter's nano route – physical view with wires*

Table 7. *Encounter's simulation of modified Tile*

Aspect ratio	Density	Cells	Area (um^2)	DRC
0.5	0.985	30577	59841	0

From Fig. 7 and 8, it is safe to say that the layout is reasonably fitted as tightly as possible, since it is almost impossible to detect any wasted space within the encounter simulation.

E. Conclusion and what I have learned

In conclusion, with ar = 0.5 and d = 0.985, we have achieved the desired optimization (i.e: minimizing the tile's area). The reason is because the resulting area from optimization is very close to that of the actual CompileAnalyzer's output, where:

Table 8. *Area Comparison*

CompileAnalyzer	Encounter	Actual Density
58951.45 um^2	59841 um^2	0.9851

Since we know that the area from CA is optimized – due to the area constraints set to 0 during the Tile setup – this means that the smallest we can hope to make this tile is 58951 um^2. My attempt was able to shrink the tile (while maintaining its functionality through 0 DRC violations) with 0.9851 density when compared to the analysis from synthesis and CA steps. This means that, we can use the following formula to find the number of tiles can be fitted to a given chip area:

$$\#\ \text{tiles} = \text{total\_chip\_area} / \text{single\_tile\_area} \qquad (1)$$

Thus, we have the following table:

Table 9. *How many tiles on can be fitted on chip?*

Encounter		
Tile's area (mm^2)	Chip's area (mm^2)	How many can be fitted on chip?
0.059841	1	16.7
CompileAnalyzer		
Tile's area (mm^2)	Chip's area (mm^2)	How many can be fitted on chip?
0.058951	1	16.96

From the above table, ideally, we should manage to fit 17 tiles in a 1 mm^2 chip. While my area optimization is very close to 17, but only 16 or so tiles can be fitted with my optimization (since it is pointless to fit 0.7 of a tile). While this is not ideal, in my opinion, this is reasonable enough. Since I only actively changing the floorplan and layout dimension of encounter simulation, more optimizations could be done with pins and wires – but given the knowledge that I learned about synthesis and encounter from lab 3 and 4, this is the best that I could do.

However, this difference is what I had hoped to show throughout this lab. As we see, even with a 0.9851 density, those wasted space could add up and eventually, such ineffective use of space will only be more and more visible. At one point the difference will be so large that it will not only harm the performance, but also bring losses to the company's chip production line. Observe the graph below:

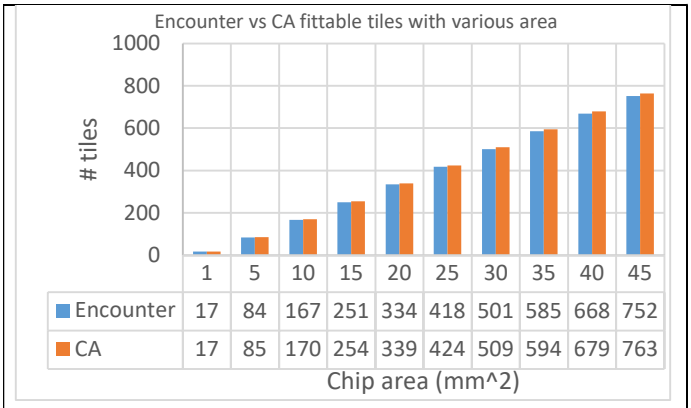

Figure 9. *Number of Tiles projection and comparison*

From Fig. 9, we can see that the disparity between encounter and CA number of tiles becomes more and more visible as the chip area becomes larger and larger. For example, at 45mm^2, the difference in number of tiles is approximately 11 tiles. ***Ultimately, this is to stress the fact that even with 0.9851 density, on a larger manufacturing scale, this is still not desirable due to the projection in Fig. 9, but for the purpose of this lab, it would suffice***. Furthermore, as stated previously, ***to fabricate a large network or layout, we have to depend on these tools, which is why it is important for students to understand how to correctly utilize these powerful software to their utmost capability*** – as it will make the process of design and optimization a lot less strenuous.

IV. Appendix and Notes:

The reason why I chose aspect ratio to be 0.5 is because it is the most even out of all the ratios. Since the area is a square, if our tile cannot be optimized by using the square ratio, then we have to turn to the most evenly distributed rectangular shape.

All files that are needed to recreate this lab report can be found within "Lab_5_Vo (30553600)" zip file. Encounter's simulations are named appropriately and can be found within pr folder of the zip file, and log name is formatted as: "density_d DRC Yes/No". So, for example, section 3 part A simulation's log can be found in: density_0.9 DRC No. Files that are generically named are my trial simulations (e.g: encounter.log1)