ES8156

High Performance Stereo Audio DAC

FEATURES

- High performance and low power multi-bit delta-sigma audio DAC
- 110 dB signal to noise ratio, -80 dB THD+N
- 24-bit, 8 to 96 kHz sampling frequency
- Integrated headphone driver with capless option
- Differential output for higher SNR and CMRR
- I^2S/PCM master or slave serial data port
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- I^2C interface
- 7-band fully adjustable EQ
- Dynamic range compression
- Playback signal feedback
- Pop and click noise suppression
- 1.8V to 3.3V operation

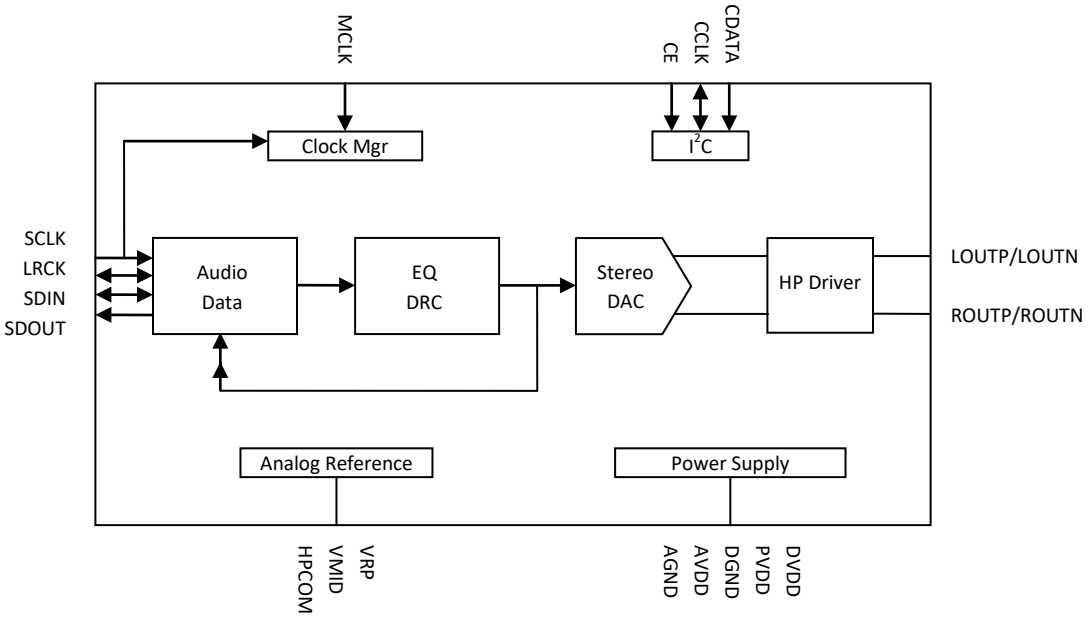
APPLICATIONS

- Headphone
- Speaker
- TV
- Portable audio devices

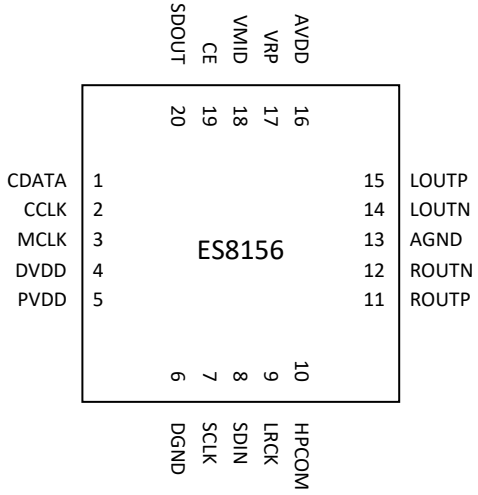
ORDERING INFORMATION

ES8156 -40°C ~ +85°C
QFN-20

1. BLOCK DIAGRAM

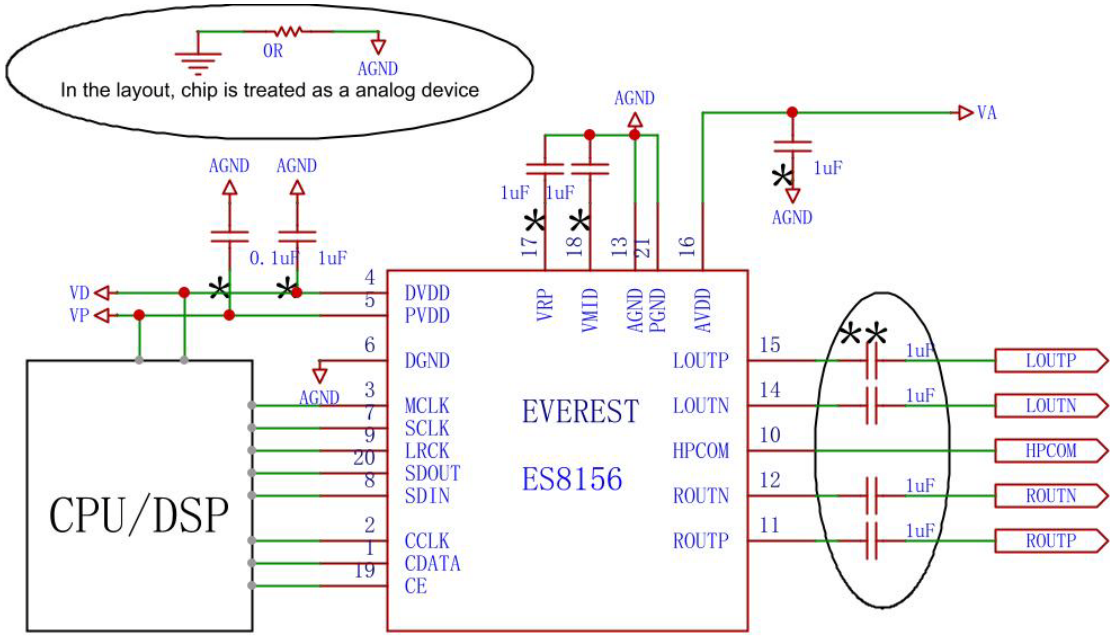


2. PIN OUT AND DESCRIPTION

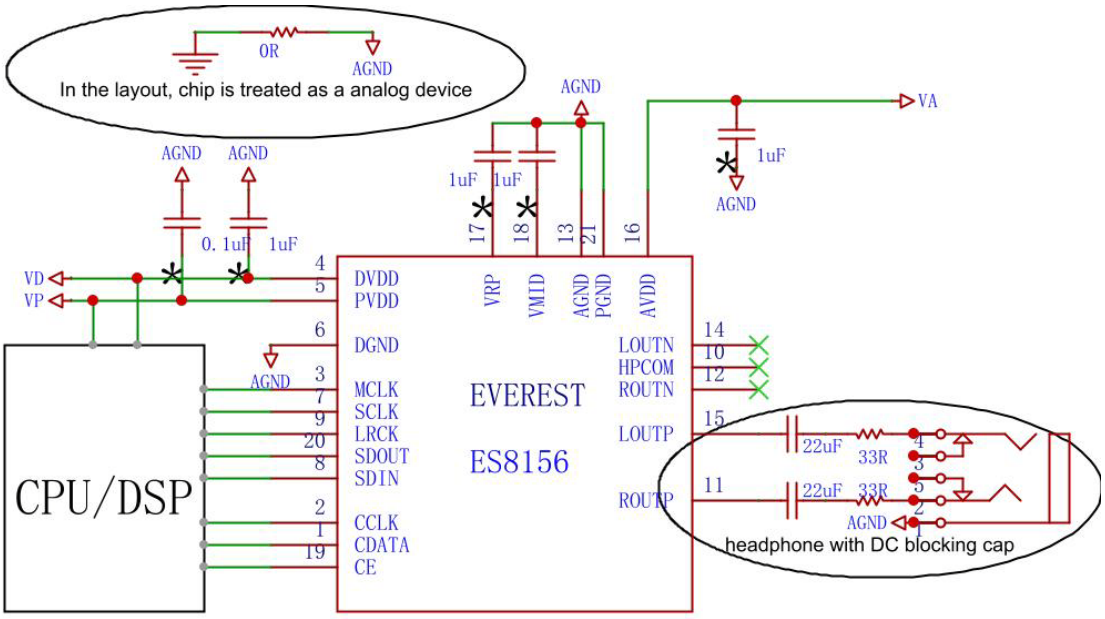


Pin Name	Pin number	Input or Output	Pin Description
CDATA, CCLK, CE	1, 2, 19	I/O, I, I	I^2C clock, data, address
MCLK	3	I	Master clock
SCLK	7	I/O	Serial data bit clock/DMIC bit clock
SDIN	8	I	DAC serial data input
LRCK	9	I/O	Serial data left and right channel frame clock
SDOUT	20	O	Playback signal feedback
LOUTP, LOUTN ROUTP, ROUTN	15, 14 11, 12	O O	Left channel differential analog output Right channel differential analog output
HPCOM	10	Analog	Virtual ground for capless headphone (Only available in software mode)
PVDD	5	Analog	Power supply for the digital input and output
DVDD, DGND	4, 6	Analog	Digital power supply
AVDD, AGND	16, 13	Analog	Analog power supply
VMID	18	Analog	Filtering capacitor connection
VRP	17	Analog	Filtering capacitor connection

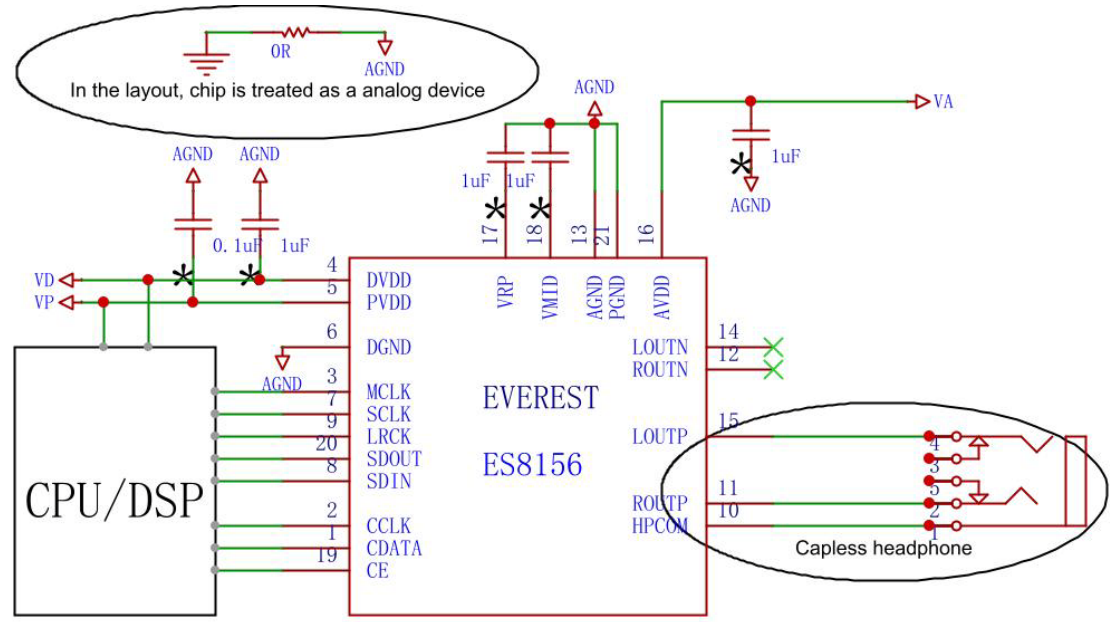
3. TYPICAL APPLICATION CIRCUIT



*For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible
** Capacitances should be used for the AC couple connection which on the gound
and removed for the DC couple connection which used the HPCOM instead of ground



*For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible



* For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible

4. HARDWARE MODE

The device works either in hardware mode (HW mode) or software mode (I^2C mode). The default is hardware mode. Software mode is enabled by setting bit 2 of configuration register 0x02.

In HW mode, LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with some specific rates. The device can auto detect MCLK/LRCK ratio according to Table 1. The device only supports the MCLK/LRCK ratios listed in Table 1. The SCLK/LRCK ratio is normally 64.

Table 1 Slave Mode Sampling Frequencies and MCLK/LRCK Ratio

Speed Mode	Sampling Frequency	MCLK/LRCK Ratio
Single Speed	8kHz – 50kHz	32, 64, 96, 128, 192, 256, 384, 512, 640, 768, 1024, 1152, 1280, 1536

5. CLOCK MODES AND SAMPLING FREQUENCIES

In software mode, the device supports standard audio clocks (32Fs, 64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (16 MHz, 25 MHz, 26 MHz, etc).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

6. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a "start" signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0001 00x, where x equals CE. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a "stop" signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 2 and Table 3. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 2 Write Data to Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0001 00 CE	0	ACK	RAM	ACK	DATA	ACK	Stop

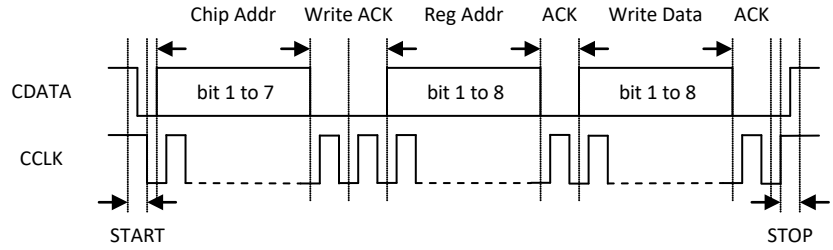


Figure 1a I^2C Write Timing

Table 3 Read Data from Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		
Start	0001 00 CE	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0001 00 CE	1	ACK	Data	NACK	Stop

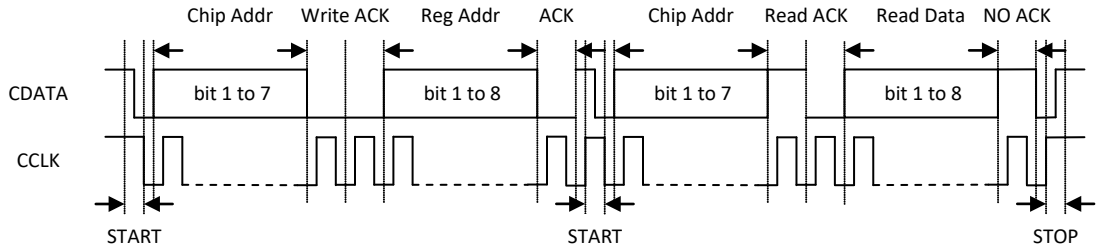


Figure 1b I^2C Read Timing

7. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input or output through LRCK, SCLK and SDIN or SDOUT pins. These formats are I^2S, left justified, right justified and DSP/PCM. SDIN is sampled by the device on the rising edge of SCLK. SDOUT is out on the falling edge of SCLK. The relationship of SDATA (SDIN or SDOUT), SCLK and LRCK with these formats are shown through Figure 2a to Figure 2d.

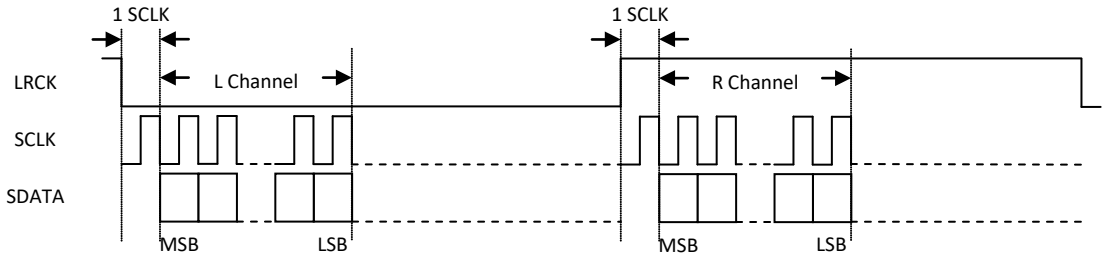


Figure 2a I^2S Serial Audio Data Format

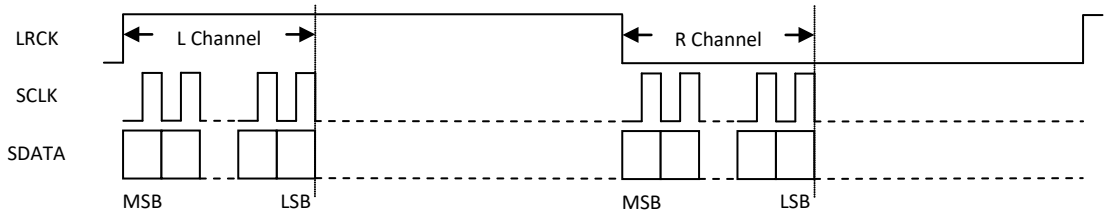


Figure 2b Left Justified Serial Audio Data Format

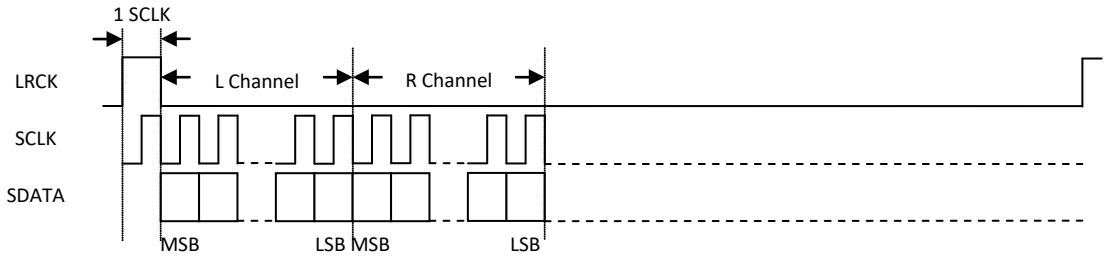


Figure 2c DSP/PCM Mode A Serial Audio Data Format

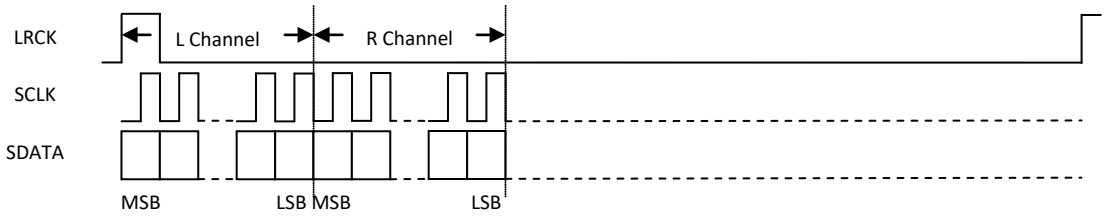


Figure 2d DSP/PCM Mode B Serial Audio Data Format

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
DVDD (Note 1)	1.6	1.8/3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V
AVDD (Note 2)	1.7	1.8/3.3	3.6	V

Note 1: if SCLK is input to clock manager, and is less than 1 MHz, DVDD must be lower than 2V.

Note 2: in hardware mode, AVDD must be higher than 3V.

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	105	110	115	dB
THD+N	-85	-80	-78	dB
Channel Separation (1KHz)	105	110	115	dB
Interchannel Gain Mismatch		0.2	1	dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	56			dB
Analog Output				
Full Scale Output (differential P and N)	1.71*AVDD/3.3	2*0.9*AVDD/3.3	1.89*AVDD/3.3	Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V (Note 3a) DVDD=1.8V, PVDD=1.8V, AVDD=1.8V		19 6		mW
Power Down Mode (Note 3b)				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

Note 3a: recommend VDDP and VDDD power supply turn on or off within 10 ms of each other; VDDD must be on when VDDA is on.

Note 3b: recommend all power supply on, entering low power through control register setting, then stopping input clock.

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

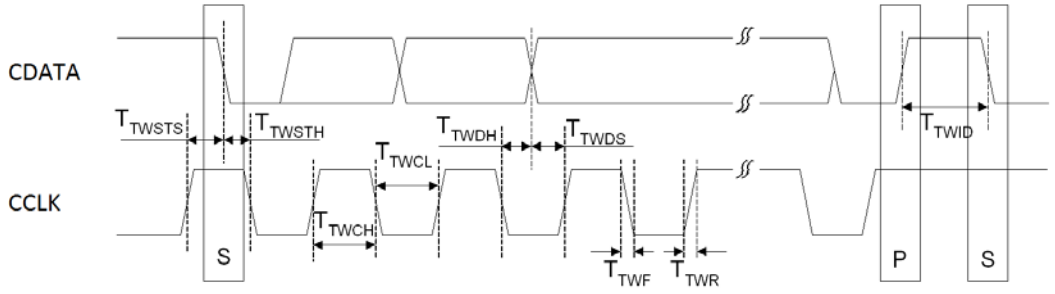


Figure 3 I²C Timing

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			100	KHz
LRCK duty cycle (Note 4)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid VDDD=3.3V VDDD=1.8V	T_{SDO}		16 39	ns
LRCK edge to SDOUT valid (Note 5) VDDD=3.3V VDDD=1.8V	T_{LDO}		11 25	ns
SDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to SDIN hold time	T_{SDIH}	10		ns

Note 4: one SCLK period of high time in DSP/PCM modes.

Note 5: only apply to MSB of Left Justified or DSP/PCM mode B.

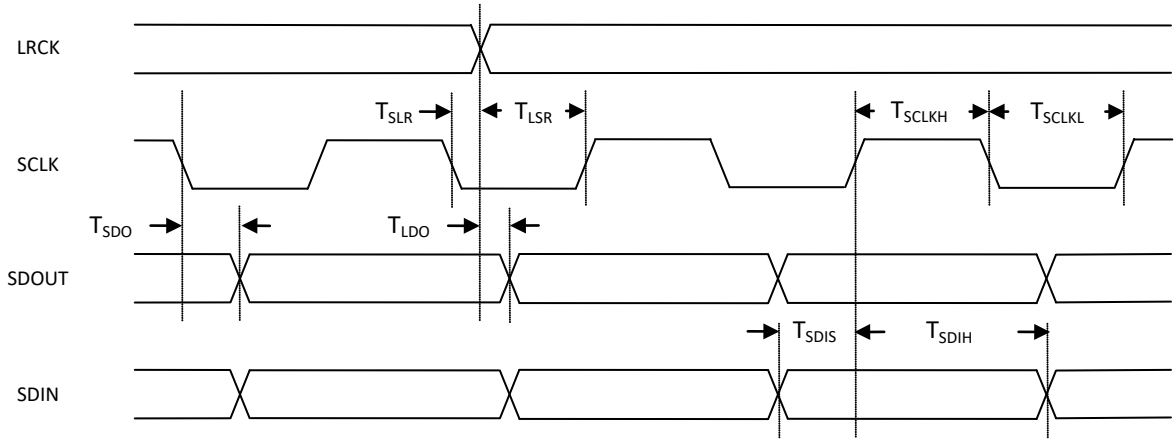


Figure 4 Serial Audio Port Timing

9. CONFIGURATION REGISTER DEFINITION

Registers reside in two pages. Page 1 is dedicated to EQ coefficients. All other registers are in page 0. Page select is in register 0xFC.

REGISTER 0X00 – RESET CONTROL, DEFAULT 00011100

Bit Name	Bit	Description
Reserved	7:6	Reserved
RST_REGS	5	0 – normal 1 – reset control registers
RST_MSTGEN	4	0 – normal 1 – reset master mode LRCK and SCLK
RST_DAC_DIG	3	0 – normal 1 – reset DAC
RST_DIG	2	0 – normal 1 – reset digital
SEQ_DIS	1	Auto power sequence 0 – enable 1 – disable
CSM_ON	0	Chip state machine power down 0 – disable 1 – enable

REGISTER 0X01 – MAIN CLOCK CONTROL, DEFAULT 00100000

Bit Name	Bit	Description
MULTP_FACTOR	7:6	Master clock multiplier 00 – multiply by 1 01 – multiply by 2 10 – multiply by 4 11 – multiply by 8
OSR128_SEL	5	1 – 128 OSR 0 – 64 OSR
CLK_DAC_DIV	4:0	DAC clock divide 0/1 – no divide 2 – divide by 2 ….. 31 – divide by 31

REGISTER 0X02 – MODE CONFIG 1, DEFAULT 00000000

Bit Name	Bit	Description
SCLK_AS_MCLK	7	0 – MCLK is as MCLK 1 – SCLK is as MCLK
ISCLKLRCK_SEL	6	0 – according to M/S mode 1 – master mode's LRCK/SCLK as internal LRCK/SCLK for speedy start up
SCLKLRCK_TRI	5	0 – original data 1 – SCLK/LRCK is tri state output
SCLK_INV_MODE	4	SCLK invert 0 – normal 1 – SCLK invert

EQ_HIGH_MODE	3	0 – 1x frequency 1 – 2x frequency
SOFT_MODE_SEL	2	software mode/hardware mode select 0 – hardware mode 1 – software mode
SPEED_MODE	1	0 – single speed 1 – double speed
MS_MODE	0	LRCK/SCLK clock mode 0 – slave mode 1 – master mode

REGISTER 0X03 – MASTER LRCK DIVIDER 1, DEFAULT 00000001

Bit Name	Bit	Description
Reserved	7:4	Reserved
M_LRCK_DIV_HIGH4	3:0	M_LRCK_DIV[11:8]

REGISTER 0X04 – MASTER LRCK DIVIDER 0, DEFAULT 00000000

Bit Name	Bit	Description
M_LRCK_DIV_LOW8	7:0	M_LRCK_DIV[7:0]

REGISTER 0X05 – MASTER CLOCK CONTROL, DEFAULT 00000100

Bit Name	Bit	Description
M_SCLK_MODE	7	0 – normal 1 – reserved
M_SCLK_DIV	6:0	SCLK divide (use with MSTCLK_SRCSEL) 0/1 – no divide 2 – divide by 2 .... 127 – divide by 127

REGISTER 0X06 – NFS CONFIG, DEFAULT 00010001

Bit Name	Bit	Description
LRCK_CNT_RV	7:4	Use for debug, Read Only
LRCK_RATE_MODE	3:0	1 – 2 channels, normal mode 2 – 4 channels 3 – 6 channels 4 – 8 channels 5 – 10 channels 6 – 12 channels 7 – 14 channels 8 – 16 channels Other – reserved

REGISTER 0X07 – MISC CONTROL 1, DEFAULT 00000000

Bit Name	Bit	Description
MCLK_INV	7	0 – normal 1 – invert MCLK
CLK_DAC_DIV0	6:4	DAC clock divide 0/1 – no divide 2 – divide by 2

		….. 7 – divide by 7
CLKDBL_PW_SEL	3:2	0/1 – normal clock doubler duty cycle 2 – clock doubler duty cycle1 3 – clock doubler duty cycle2
CLKDBL_PATH_SEL	1	Clock doubler path select (internal use)
LRCK_EXTEND	0	0 – normal internal LRCK pulse width 1 – extended internal LRCK pulse width

REGISTER 0X08 – CLOCK OFF, DEFAULT 00000110

Bit Name	Bit	Description
Reserved	7:6	Reserved
P2S_CLK_ON	5	0 – turn off P2S master clock 1 – turn on P2S master clock
MASTER_CLK_ON	4	0 – turn off master mode SCLK and LRCK 1 – turn on master mode SCLK and LRCK
EXT_SCLKLRCK_ON	3	0 – turn off slave mode SCLK and LRCK 1 – turn on slave mode SCLK and LRCK
ANA_CLK_ON	2	0 – turn off DAC analog clock 1 – turn on DAC analog clock
DAC_MCLK_ON	1	0 – turn off DAC master clock 1 – turn on DAC master clock
MCLK_ON	0	0 – turn off master clock 1 – turn on master clock

REGISTER 0X09 – MISC CONTROL 2, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:6	Reserved
MSTCLK_SRCSEL	5	0 – source clock of master mode from pad 1 – source clock of master mode from internal clock
CSM_CNTSEL	4	0 – slave LRCK used for CSM counter 1 – master LRCK used for CSM counter
Reserved	3:2	Reserved
DLL_ON	1	1 – normal 0 – power down DLL
PUPDN_OFF	0	Pin internal pull up 1 – off 0 – on

REGISTER 0X0A – TIME CONTROL 1, DEFAULT 01010000

Bit Name	Bit	Description
V_T1	7:0	Timer1 For LRCK=48KHz: 0 - NA 1 - 80us(default) 2 – 2.5ms … 63 - 675ms(max)

REGISTER 0X0B – TIME CONTROL 2, DEFAULT 01010000

Bit Name	Bit	Description
V_T2	7:0	Timer2 For LRCK=48KHz: 0 - NA 1 - 80us(default) 2 – 2.5ms … 63 - 675ms(max)

REGISTER 0X0C – CHIP STATUS, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved
CSM_STATE	6:4	Chip state machine state, Read Only 000 – S0 001 – S1 010 – S2 011 – S3 110 – S6 Other – NA
Reserved	3	Reserved
FORCE_CSM	2:0	Force chip state machine 100 – force to S0 101 – force to S1 110 – force to S2 111 – force to S3 110 – force to S6 Other – no force

REGISTER 0X0D – P2S CONTRL, DEFAULT 00010000

Bit Name	Bit	Description
LRCK_1STCNT	7:4	Reserved
P2S_NFS_FLAGOFF	3	0 – include flag in P2S data 1 – don't include flag in P2S data
P2S_SDOUT_MUTEB	2	0 – mute P2S output 1 – output P2S data
P2S_SDOUT_SEL	1	0 – normal 1 – only use under test mode
P2S_SDOUT_TRI	0	SDOUT tri-state control 0 – normal output 1 – high z output

REGISTER 0X10 – DAC COUNTER PARAMETER, DEFAULT 01000000

Bit Name	Bit	Description
Reserved	7	Reserved
DAC_NS	6:0	OSR parameter selection >=64

REGISTER 0X11 – SDP INTERFACE CONFIG 1, DEFAULT 00000000

Bit Name	Bit	Description

Reserved	7	Reserved
SP_WL	6:4	000 – 24-bit 001 – 20-bit 010 – 18-bit 011 – 16-bit 100 – 32-bit
SP_MUTE	3	Software mute control 0 – normal 1 – mute DAC input data to 0
SP_LRP	2	I^2S/Left Justified: 0 – L/R normal polarity Left/Right=High/Low (Left Justified) Left/Right=Low/High (I^2S) 1 – L/R invert polarity Left/Right=Low/High (Left Justified) Left/Right=High/Low (I^2S) DSP/PCM mode: 0 – mode A 1 – mode B
SP_PROTOCAL	1:0	00 – I^2S 01 – Left Justified 10 – Reserved 11 – DSP mode

REGISTER 0X12 – AUTOMUTE CONTROL, DEFAULT 00000100

Bit Name	Bit	Description
AUTOMUTE_NG	7:4	DAC auto mute noise gate 0000 – -96dB 0001 – -90dB 0010 – -84dB 0011 – -78dB 0100 – -72dB 0101 – -66dB 0110 – -60dB 0111 – -54dB 1000 – -51dB 1001 – -48dB 1010 – -45dB 1011 – -42dB 1100 – -39dB 1101 – -36dB 1110 – -33dB 1111 – -30dB
AUTOMUTE_SIZE	3:0	Auto mute window size 0 – 2048 other – 2048 * AUTOMUTE_SIZE

REGISTER 0X13 – MUTE CONTROL, DEFAULT 00010001

Bit Name	Bit	Description
INTOUT_CLIPEN	7	DSP clip out control 0 – normal

		1 – clip out
AM_ATTENU6_ENA	6	DSP clip out control 0 – normal 1 – enable attenuation
AM_ACLKOFF_ENA	5	0 – normal 1 – disable analog clock
AM_DSMMUTE_ENA	4	0 – normal 1 – mute DSM output
AM_MUTE_FLAG	3	Reserved
RCH_DSM_SMUTE	2	0 – normal 1 – mute DSM output of right channel
LCH_DSM_SMUTE	1	0 – normal 1 – mute DSM output of left channel
AM_ENA	0	0 – automute off 1 – automute on

REGISTER 0X14 – VOLUME CONTROL, DEFAULT 10111111

Bit Name	Bit	Description
DAC_VOLUME_DB	7:0	0x00 - '-95.5dB' (default) 0x01 - '-95.0dB' ⋯ 0.5dB/step 0xBE - '-0.5dB' 0xBF - '0dB' 0xC0 - '+0.5dB' ⋯ 0xFF - '+32dB'

REGISTER 0X15 – ALC CONFIG 1, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
ALC_MUTE_GAIN	3:1	ALC gain control when automute 000 – 0dB 001 – -4dB 010 – -8dB 011 – -12dB 100 – -16dB 101 – -20dB 110 – -24dB 111 – -28dB
DAC_ALC_EN	0	0 – ALC off 1 – ALC on

REGISTER 0X16 – ALC CONFIG 2, DEFAULT 00000000

Bit Name	Bit	Description
ALC_RAMP_RATE	7:4	DAC ALC ramp rate For LRCK=48KHz: 1 - 0.25dB/80us 2 - 0.25dB /160us 3 - 0.25dB /320us 4 - 0.25dB /640us

		5 - 0.25dB /1.28ms 6 - 0.25dB /2.56ms 7 - 0.25dB /5.12ms 8 - 0.25dB /10.24ms 9 - 0.25dB /20.48ms 10 - 0.25dB /40.96ms 11 - 0.25dB /81.92ms 12 - 0.25dB /163.84ms 13 - 0.25dB /327.68ms 14 - 0.25dB /655.36ms 15 - 0.25dB /1.3s
ALC_WIN_SIZE	3:0	DAC ALC window size For LRCK=48KHz: 1 - 0.25dB/40us 2 - 0.25dB /80us 3 - 0.25dB /160us 4 - 0.25dB /320us 5 - 0.25dB /640us 6 - 0.25dB / 1.28ms 7 - 0.25dB / 2.56ms 8 - 0.25dB /5.12ms 9 - 0.25dB /10.24ms 10 - 0.25dB /20.48ms 11 - 0.25dB /40.96ms 12 - 0.25dB /81.92ms 13 - 0.25dB /163.84ms 14 - 0.25dB /327.68ms 15 - 0.25dB /655.36ms

REGISTER 0X17 – ALC LEVEL, DEFAULT 11110111

Bit Name	Bit	Description
ALC_MAXLEVEL	7:4	ALC max level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB 12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB 1 – -24.1dB 0 – -30.1dB
ALC_MINLEVEL	3:0	ALC min level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB

		12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB 1 – -24.1dB 0 – -30.1dB

REGISTER 0X18 – MISC CONTROL 3, DEFAULT 00000000

Bit Name	Bit	Description
P2S_DATA_BITNUM	7	DSP clip out control 0 – 24 bit 1 – 26 bit
P2S_DPATH_SEL	6	DSP clip out control 0 – EQ output 1 – DSP output
CHN_CROSS	5:4	00 – normal 01 – left channel to both left and right channels 10 – right channel to both left and right channels 11 – left and right channel output switch
LCH_INV	3	0 – normal 1 – invert left channel output
RCH_INV	2	0 – normal 1 – invert right channel output
DSM_DITHERON	1	0 – normal 1 – open dither of DSM
DAC_RAM_CLR	0	0 – normal 1 – clear DSP ram

REGISTER 0X19 – EQ CONTROL 1, DEFAULT 00100000

Bit Name	Bit	Description
Reserved	7	Reserved
EQ_BAND_NUM	6:4	000 – 1 left and right band 001 – 2 left and right band 010 – 3 left and right band (3.3V DVDD required for 48 kHz Fs) 011 – 4 left and right band 100 – 5 left and right band (3.3V DVDD for 48 kHz Fs) 101 – 6 left and right band (3.3V DVDD for 48 kHz Fs) 110 – 7 left and right band (3.3V DVDD for 48 kHz Fs) 111 – NA
EQ_RST	3	0 – normal 1 – reset EQ logic
EQ_CFG_RD	2	0 – EQ RAM read controlled by internal logic 1 – EQ RAM read controlled by I^2C

EQ_CFG_WR	1	0 – EQ RAM write controlled by internal logic 1 – EQ RAM write controlled by I^2C
EQ_ON	0	0 – EQ off 1 – EQ on

REGISTER 0X1A – EQ CONFIG 2, DEFAULT 00000000

Bit Name	Bit	Description
EQ_1STCNT_VLD	7	0 – the parameter of EQ_RUN_1STCNT is invalid 1 – the parameter of EQ_RUN_1STCNT is valid
EQ_RUN_1STCNT	6:0	Internal

REGISTER 0X20 – ANALOG SYSTEM, DEFAULT 00010110

Bit Name	Bit	Description
Reserved	7:6	Reserved
S3_SEL	5:4	SEL S3 00 – NA 01 – default 10 – state2 11 – state3
S2_SEL	3:2	SEL S2 00 – NA 01 – default 10 – state2 11 – state3
S6_SEL	1:0	SEL S6 00 – NA 01 – default 10 – state2 11 – state3

REGISTER 0X21 – ANALOG SYSTEM, DEFAULT 01111111

Bit Name	Bit	Description
Reserved	7	Reserved
VREF_RMPDN2	6	0 – normal 1 – fast option
VREF_RMPDN1	5	0 – normal 1 – slow option
VSEL	4:0	Select bias 001 - 25% 010 - 50% 011 - 75% 100 – 100% 101 - 120% 110 - 150% 111 - 175%

REGISTER 0X22 – ANALOG SYSTEM, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
HPSW	3	0 – line out

		1 – enable HP driver for headphone output
Reserved	2	
SWRMPSEL	1	0 – disable 1 – enable
OUT_MUTE	0	0 – normal 1 – mute output

REGISTER 0X23 – ANALOG SYSTEM, DEFAULT 10000110

Bit Name	Bit	Description
IBIAS_SW	7:6	0 –bias setting level0（lowest） 1 –bias setting level1 2 –bias setting level2 3 –bias setting level3
VMIDLVL	5:4	0 –'vdda/2' (default) 1 – vmid level1 2 – vmid level2 3 – vmid level3
DAC_IBIAS_SW	3	0 – normal DAC bias setting 1 – higher DAC bias setting
VROI	2	0 – normal impedance 1 – low impedance
HPCOM_REF2	1	0 – normal HPCOM output bias 1 – high level HPCOM bias
HPCOM_REF1	0	0 – normal output bias 1 – low level HPCOM bias

REGISTER 0X24 – ANALOG SYSTEM, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
LPDAC	3	0 – normal mode 1 – low power mode for DAC
LPDACVRP	2	0 – normal mode 1 – low power mode for DAC reference
LPHPCOM	1	0 – normal mode 1 – low power mode for HP output reference
LPVREFBUF	0	0 – normal mode 1 – low power mode for internal reference

REGISTER 0X25 – ANALOG SYSTEM, DEFAULT 00000111

Bit Name	Bit	Description
PDN_ANA	7	0 – enable analog circuits 1 – power down analog circuits
ENREFR	6	0 – disable reference circuits for output 1 – enable reference circuits for DAC output
VMIDSEL	5:4	0 – VMID power down 1 – VMID speed charge1 2 – normal VMID operation 3 – VMID speed charge3
ENHPCOM	3	0 – disable HPCOM 1 – enable HPCOM

PDN_DACVREFGEN	2	0 – enable analog DAC reference circuits 1 – power down analog DAC reference circuits
PDN_VREFBUF	1	0 – disable internal reference circuits 1 – enable reference circuits
PDN_DAC	0	0 – enable DAC 1 – power down DAC

REGISTER 0X40~0X5E – EQ DATA RAM CLEAR, DEFAULT 00000000

Bit Name	Bit	Description
EQ_RAM_WDATA	7:0	Software write 0 data during these address space.

REGISTER 0XFC – PAGE SELECT, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:1	Reserved
PAGE_SEL	0	0 – I^2C work at the address space of page 0 1 – I^2C work at the address space of page 1

REGISTER 0XFD – CHIP ID1, DEFAULT 10000001

Bit Name	Bit	Description
Chip_number_id1	7:0	Chip ID

REGISTER 0XFE – CHIP ID0, DEFAULT 01010101

Bit Name	Bit	Description
Chip_number_id0	7:0	Chip ID

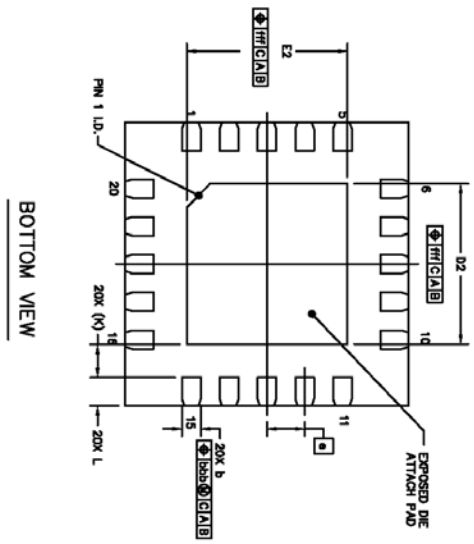
REGISTER 0XFF – CHIP VERSION, DEFAULT 00010000

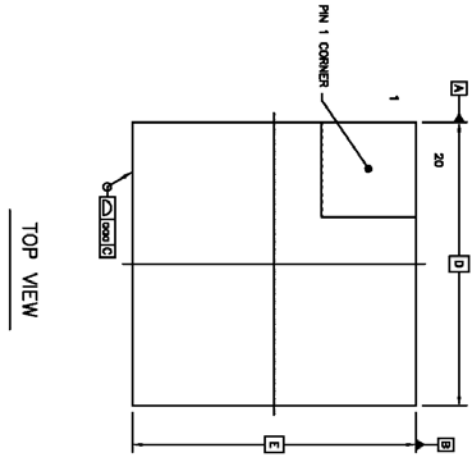
Bit Name	Bit	Description
Chip_version_id1	7:4	Version ID
Chip_version_id0	3:0	Version ID

REGISTER 0X00~0XD1(PAGE 1) – EQ COEFFICENT

Bit Name	Bit	Description
Reserved	7:5	Reserved
EQ_COEF	4:0	EQ coefficient

10.PACKAGE (UNIT: MM)





	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	----	0.4	----
L/F THICKNESS	A3		0.152 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		3 BSC	
BODY SIZE Y	E		3 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	1.6	1.7	1.8
EP SIZE Y	E2	1.6	1.7	1.8
LEAD LENGTH	L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE	K		0.35 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

11.CORPORATE INFORMATION

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