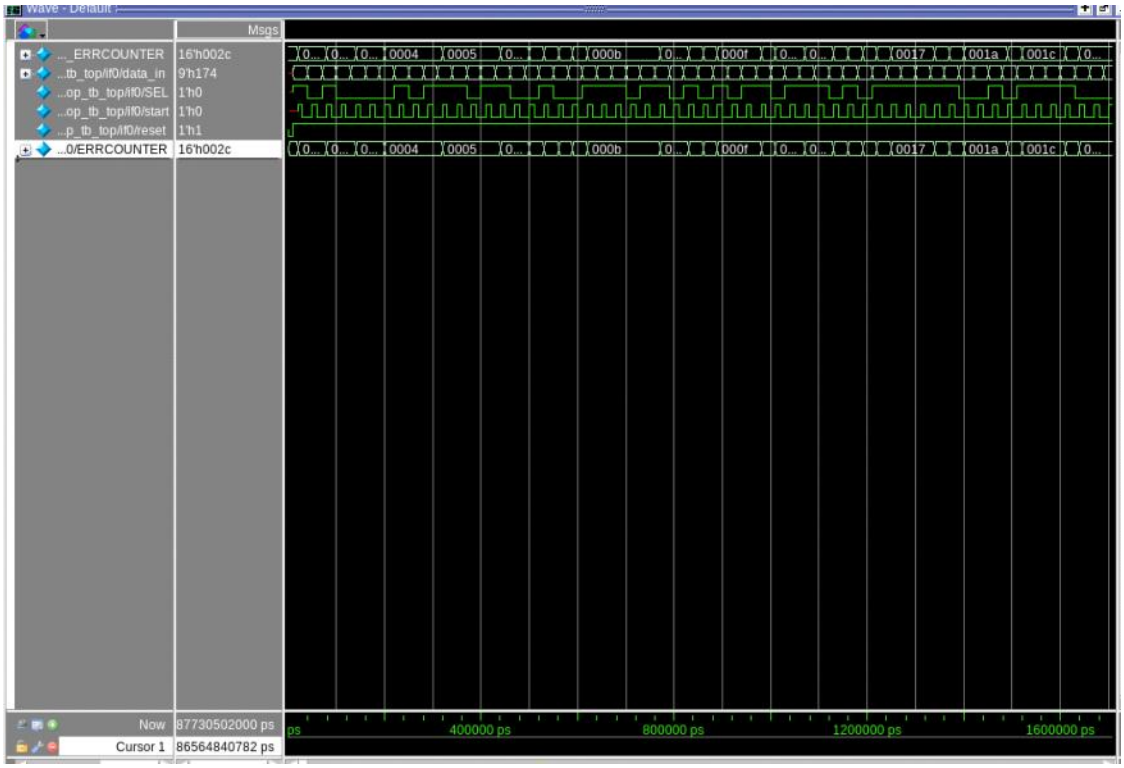
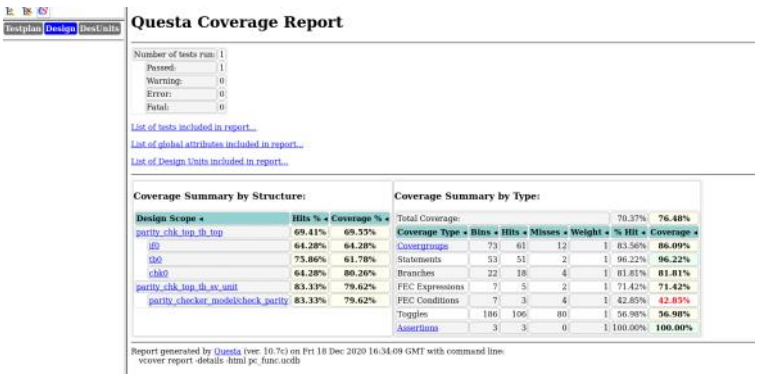
Functional and Code Verification

18 December 2020 15:53

Parity_Checker




```
Total Node Count     =         11
Toggled Node Count   =         11
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (22 of 22 bins)

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------
Covergroup                                              Metric       Goal    Status

----------------------------------------------------------------------------------------------------
 TYPE /parity_top/tb1/cover_a_value                   100.00%        100    Covered
    covered/total bins:                                     7          7
    missing/total bins:                                     0          7
    % Hit:                                           100.00%        100
    Coverpoint cover_a_value::#coverpoint__0#        100.00%        100    Covered
        covered/total bins:                                 5          5
        missing/total bins:                                 0          5
        % Hit:                                       100.00%        100
    Coverpoint cover_a_value::#coverpoint__1#        100.00%        100    Covered
        covered/total bins:                                 2          2
        missing/total bins:                                 0          2
        % Hit:                                       100.00%        100
 Covergroup instance \/parity_top/tb1/cav0           100.00%        100    Covered
    covered/total bins:                                     7          7
    missing/total bins:                                     0          7
    % Hit:                                           100.00%        100
    Coverpoint #coverpoint__0#                       100.00%        100    Covered
        covered/total bins:                                 5          5
        missing/total bins:                                 0          5
        % Hit:                                       100.00%        100
        bin zero                                            4          1    Covered
        bin lo                                              7          1    Covered
        bin med                                             8          1    Covered
        bin hi                                              8          1    Covered
        bin max                                             4          1    Covered
    Coverpoint #coverpoint__1#                       100.00%        100    Covered
        covered/total bins:                                 2          2
        missing/total bins:                                 0          2
        % Hit:                                       100.00%        100
        bin even                                          513          1    Covered
        bin odd                                           486          1    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

ASSERTION RESULTS:
---------------------------------------------------------------------
Name                File(Line)                   Failure      Pass
                                                 Count        Count
---------------------------------------------------------------------
/parity_top/genl/assert_check_parity
                    parity_generator/parity_gen.sv(24)
                                                       0          1

Total Coverage By File (code coverage only, filtered view): 87.14%
```



Testplan Design DesUnits

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

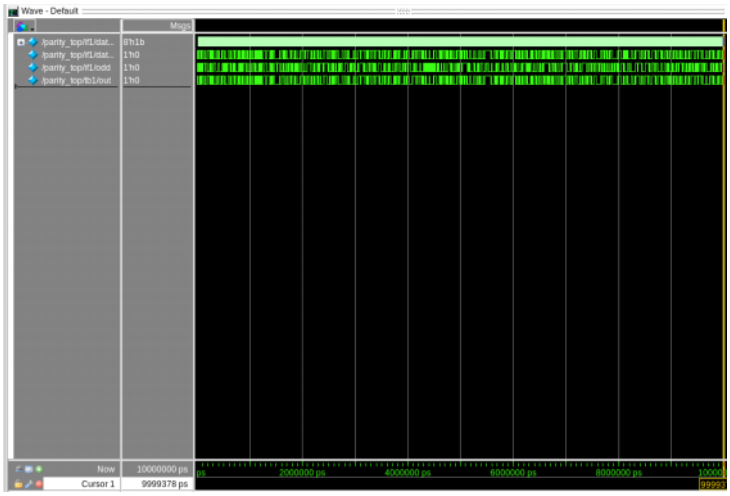
Design Scope	Hits %	Coverage %
parity_chk_top_tb_top	69.41%	69.55%
if0	64.28%	64.28%
tb0	75.86%	61.78%
chk0	64.28%	80.26%
parity_chk_top_tb_sv_unit	83.33%	79.62%
parity_checker_model/check_parity	83.33%	79.62%

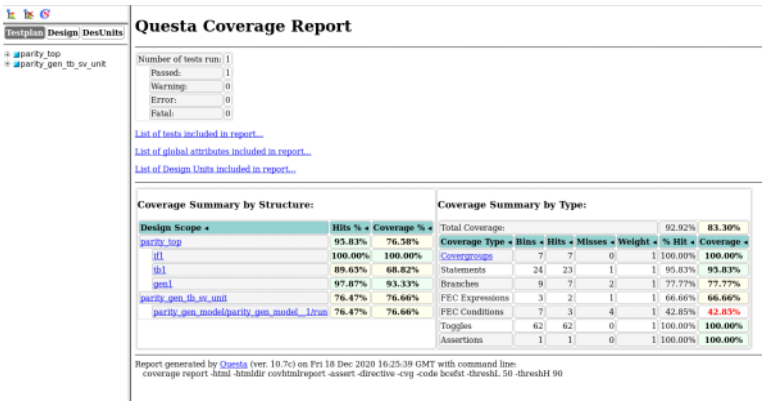
Coverage Summary by Type:

Total Coverage:					70.37%	76.48%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	73	61	12	1	83.56%	86.09%
Statements	53	51	2	1	96.22%	96.22%
Branches	22	18	4	1	81.81%	81.81%
FEC Expressions	7	5	2	1	71.42%	71.42%
FEC Conditions	7	3	4	1	42.85%	42.85%
Toggles	186	106	80	1	56.98%	56.98%
Assertions	3	3	0	1	100.00%	100.00%

Report generated by Questa (ver. 10.7c) on Fri 18 Dec 2020 16:34:09 GMT with command line:
vcover report -details -html pc_func.ucdb

Parity_Generator





Testplan Design DesUnits

parity_top

parity_gen_tb_sv_unit

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
parity_top	93.83%	76.58%
if1	100.00%	100.00%
tb1	89.65%	68.82%
gen1	97.87%	93.33%
parity_gen_tb_sv_unit	76.47%	76.66%
parity_gen_model/parity_gen_model__1/run	76.47%	76.66%

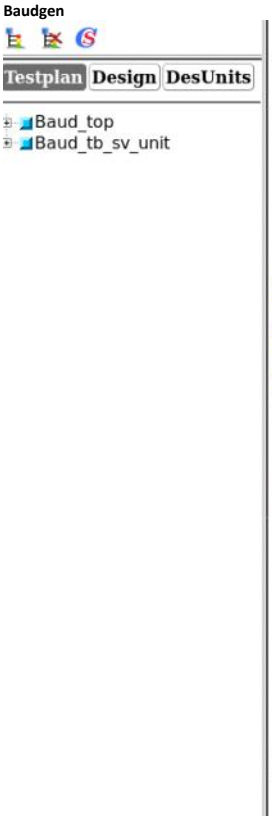
Coverage Summary by Type:

Total Coverage:					92.92%	83.30%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	7	7	0	1	100.00%	100.00%
Statements	24	23	1	1	95.83%	95.83%
Branches	9	7	2	1	77.77%	77.77%
FEC Expressions	3	2	1	1	66.66%	66.66%
FEC Conditions	7	3	4	1	42.85%	42.85%
Toggles	62	62	0	1	100.00%	100.00%
Assertions	1	1	0	1	100.00%	100.00%

Report generated by Questa (ver. 10.7c) on Fri 18 Dec 2020 16:25:39 GMT with command line:
coverage report -html -htmldir covhtmlreport -assert -directive -cvg -code bcefst -threshL 50 -threshH 90

```
Toggle Coverage for File parity_generator/parity_gen_tb.sv --

       Line                                  Node      1H->0L      0L->1H  "Coverage"
--------------------------------------------------------------------------------

Total Node Count     =         11
Toggled Node Count   =         11
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (22 of 22 bins)

COVERGROUP COVERAGE:
--------------------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal    Status
--------------------------------------------------------------------------------------------------------------
 TYPE /parity_top/tb1/cover_a_value                100.00%        100    Covered
    covered/total bins:                                  7          7
    missing/total bins:                                  0          7
    % Hit:                                          100.00%        100
    Coverpoint cover_a_value::#coverpoint__0#       100.00%        100    Covered
        covered/total bins:                              5          5
        missing/total bins:                              0          5
        % Hit:                                      100.00%        100
    Coverpoint cover_a_value::#coverpoint__1#       100.00%        100    Covered
        covered/total bins:                              2          2
        missing/total bins:                              0          2
        % Hit:                                      100.00%        100
 Covergroup instance \/parity_top/tb1/cav0          100.00%        100    Covered
    covered/total bins:                                  7          7
    missing/total bins:                                  0          7
    % Hit:                                          100.00%        100
    Coverpoint #coverpoint__0#                      100.00%        100    Covered
        covered/total bins:                              5          5
        missing/total bins:                              0          5
        % Hit:                                      100.00%        100
        bin zero                                         4          1    Covered
        bin lo                                           7          1    Covered
        bin med                                          8          1    Covered
        bin hi                                           8          1    Covered
        bin max                                          4          1    Covered
    Coverpoint #coverpoint__1#                      100.00%        100    Covered
        covered/total bins:                              2          2
        missing/total bins:                              0          2
        % Hit:                                      100.00%        100
        bin even                                       513          1    Covered
        bin odd                                        486          1    Covered

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

ASSERTION RESULTS:
--------------------------------------------------------------------
Name                File(Line)                   Failure      Pass
                                                 Count        Count
--------------------------------------------------------------------
/parity_top/gen1/assert_check_parity
                    parity_generator/parity_gen.sv(25)
                                                   0          1

Total Coverage By File (code coverage only, filtered view): 76.62%
```

Baudgen



Questa Coverage Report

Number of tests run:	1
Passed:	0
Warning:	0
Error:	1
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
Baud_top	84.59%	76.78%
if0	100.00%	100.00%
bg0	82.82%	80.26%
tb0	85.00%	69.48%
Baud_tb_sv_unit	97.67%	98.24%
baudgen_model/Setbaudrate	96.55%	96.66%
baudgen_model/run	100.00%	100.00%

Coverage Summary by Type:

Total Coverage:					86.14%	79.82%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	20	18	2	1	90.00%	93.75%
Statements	72	71	1	1	98.61%	98.61%
Branches	28	26	2	1	92.85%	92.85%
FEC Expressions	2	1	1	1	50.00%	50.00%
FEC Conditions	3	2	1	1	66.66%	66.66%
Toggles	232	190	42	1	81.89%	81.89%
Assertions	4	3	1	1	75.00%	75.00%

Report generated by Questa (ver. 10.7c) on Fri 18 Dec 2020 22:54:32 GMT with command line:
coverage report -html -htmldir covhtmlreport -assert -directive -cvg -code bcefst -threshL 50 -threshH 90

UART_tx


```
vcover report -details uart_tx_CC_rep.ucdb

ASSERTION RESULTS:
---------------------------------------------------------------------
Name                File(Line)                  Failure      Pass
                                                Count        Count
---------------------------------------------------------------------
/uart_tx_tb_top/uart0/assert_check_tx
                    uart_tx.sv(207)                    0          1
/uart_tx_tb_top/uart0/gen1/assert_check_parity
                    parity_gen.sv(25)                  0          1
End time: 21:08:51 on Dec 18,2020, Elapsed time: 0:00:00
```