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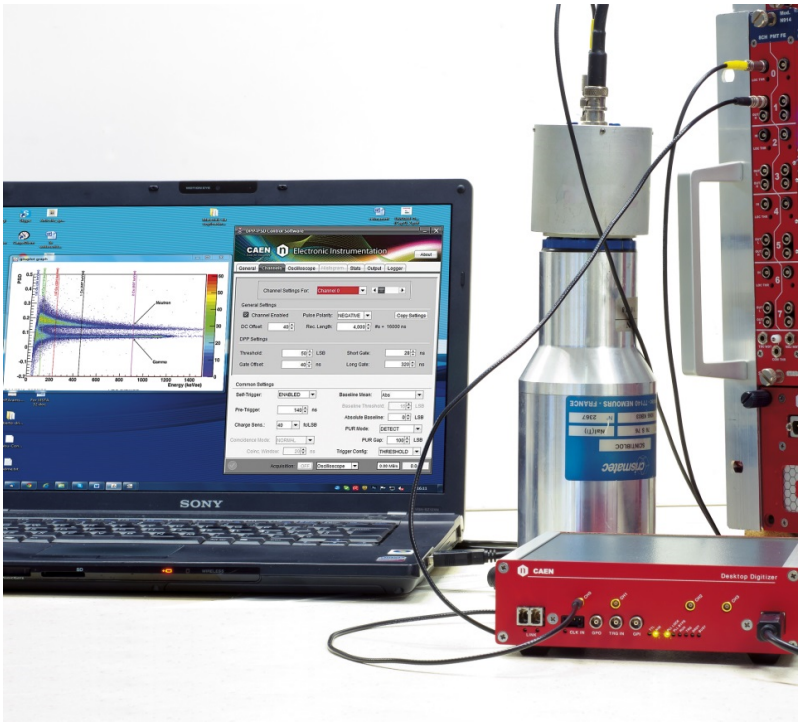

User Manual UM4380

725-730 DPP-PSD Registers

Register Description for 725 and 730 DPP-PSD

Rev. 1 - 02 October 2015

Purpose of this Manual

The User Manual contains the full description of the DPP-PSD firmware registers for 725 and 730 family series. The description is compliant with the DPP-PSD firmware revision **4.7_136.6** for 725 series, and DPP-PSD firmware revision **4.7_136.5** for 730 series. For future release compatibility check in the firmware history files.

Change Document Record

Date	Revision	Changes
01 September 2015	00	Initial Release
02 October 2015	01	Added support to 725 series

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
DAQ	Data Acquisition
DPP	Digital Pulse Processing
DPP-CI	DPP for Charge Integration
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
MCA	Multi-Channel Analyzer
OS	Operating System
PC	Personal Computer
PMT	Photo Multiplier Tube
QDC	Charge-to-Digital Converter
TDC	Time-to-Digital Converter
USB	Universal Serial Bus

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1 Registers and Data Format

All registers described in the User Manual can be accessed via **D32**. In case of VME access, **A24** and **A32** addressing mode can be used.

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R	**Read only**. The register can be accessed in read only mode.
W	**Write only**. The register can be accessed in write only mode.
R/W	**Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the access mode can be done in the following ways:

I **Individual access**. The register can be read/write in single channel mode. The register address is 0x1nXY, where n is the channel number. *Broadcast write* is also possible at the address 0x80XY. For example:

- to read/write register 0x1n70 for channel 5, access to address 0x1570;
- to write the same value for all channels in the board, access to 0x8070 (broadcast write only). To read the corresponding value, access to the individual address 0x1n70.

G **Group access**. In case of 740, 742, and 743 digitizer families, some registers manage groups of channels. In this case the group access can be handled at the address 0x1nXY, where the n index identifies the n^{th} group. *Broadcast write* is also possible at the address 0x80XY. For example:

- to read/write register 0x1n70 for group 3 of the board, access to address 0x1370. In case of 740 and 742 board, group 3 corresponds to channels from 24 to 31 (8 channels per group). In case of 743, group 3 corresponds to channels 6-7. The same value is applied for all channels in the same group.
- to write the same value for all groups in the board, access to 0x8070 (broadcast write only). To read the corresponding value, access to the individual address 0x1n70.

In case of 725 and 730 digitizer family, some registers are common between couples of channels. The group access can be handled at the address 0x1nXY, where the n index identifies the first channel of the couple. *Broadcast write* is also possible at the address 0x80XY. For example:

- to read/write register 0x1n70 for couple 3 of the board (i.e. channel 6 and channel 7), access to address 0x1670. The same value is applied also to channel 7.
- to write the same value for all couples in the board, access to 0x8070 (broadcast write only). To read the corresponding value, access to the individual address 0x1n70.

C **Common access**. Register with this attribute can be accessed in common mode. Only one address is available both in read and write mode, according to the ”Mode” option.

Register Name	Address	Mode	Attribute
Record Length	0x1n20, 0x8020	R/W	G
Input Dynamic Range	0x1n28, 0x8028	R/W	I
Number of Events per Aggregate	0x1n34, 0x8034	R/W	G
Pre Trigger	0x1n38, 0x8038	R/W	I
CFD settings	0x1n3C, 0x803C	R/W	I
Forced Data Flush	0x1n40, 0x8040	R/W	I
Short Gate Width	0x1n54, 0x8054	R/W	I
Long Gate Width	0x1n58, 0x8058	R/W	I
Gate Offset	0x1n5C, 0x805C	R/W	I
Trigger Threshold	0x1n60, 0x8060	R/W	I
Fixed Baseline	0x1n64, 0x8064	r/w	I
Shaped Trigger Width	0x1n70, 0x8070	R/W	I
Trigger Hold-Off Width	0x1n74, 0x8074	R/W	I
Threshold for the PSD cut	0x1n78, 0x8078	R/W	I
DPP Algorithm Control	0x1n80, 0x8080	R/W	I
Local Trigger Management	0x1n84, 0x8084	R/W	G
Channel n Status	0x1n88	R	I
AMC Firmware Revision	0x1n8C	R	I
DC Offset	0x1n98, 0x8098	R/W	I
ADC Temperature	0x1nA8, 0x80A8	R	I
Individual Software Trigger	0x1nC0, 0x80C0	R/W	I
Veto Duration Extention	0x1nD4, 0x80D4	R/W	I
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Aggregate Organization	0x800C	R/W	C
Channel Calibration	0x809C	R	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT Enable Mask	0x8110	R/W	C
LVDS Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Channel Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Set Monitor DAC	0x8138	R/W	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Monitor DAC Mode	0x8144	R/W	C
Event Size	0x814C	R	C
Time Bomb Downcounter	0x8158	R	C
Fan Speed Control	0x8168	R/W	C
Memory Buffer Almost Full Level	0x816C	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Disable External Trigger	0x817C	R/W	C
Trigger Validation Mask	0x8180+(4n)	R/W	G
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Channel Shutdown	0x81C0	R/W	C
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Interrupt Status ID	0xEF14	R/W	C
Interrupt Event Number	0xEF18	R/W	C

Aggregate Number per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length2	0xF004	R	C
Configuration ROM Checksum Length1	0xF008	R	C
Configuration ROM Checksum Length0	0xF00C	R	C
Configuration ROM Constant2	0xF010	R	C
Configuration ROM Constant1	0xF014	R	C
Configuration ROM Constant0	0xF018	R	C
Configuration ROM c Code	0xF01C	R	C
Configuration ROM r Code	0xF020	R	C
Configuration ROM Manufacter Identifier OUI2	0xF024	R	C
Configuration ROM Manufacter Identifier OUI1	0xF028	R	C
Configuration ROM Manufacter Identifier OUI0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board Number ID1	0xF038	R	C
Configuration ROM Board Number ID0	0xF03C	R	C
Configuration ROM Revis3	0xF040	R	C
Configuration ROM Revis2	0xF044	R	C
Configuration ROM Revis1	0xF048	R	C
Configuration ROM PCB Revision	0xF04C	R	C
Configuration ROM Flash Type	0xF050	R	C
Configuration ROM Board Serial Number1	0xF080	R	C
Configuration ROM Board Serial Number0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

Record Length

Sets the record length for the acquisition acquisition

Address	0x1n20, 0x8020
Mode	R/W
Attribute	G

Bit	Description
[15:0]	Number of samples (Ns) for the waveform acquisition, where the Record Length = Ns*8 (e.g.: write Ns = 3 to acquire 24 samples). Multiply this value by the sampling rate (4 ns for 725 series, and 2 ns for 730 series) to get the record length value in ns.
[31:16]	Reserved

Input Dynamic Range

Sets the Input Dynamic Range of the digitizer

Address	0x1n28, 0x8028
Mode	R/W
Attribute	I

Bit	Description
[0]	Options for the input dynamic range of the digitizer are: 0 : 2 Vpp 1 : 0.5 Vpp
[31:1]	Reserved

Number of Events per Aggregate

Each couple of channels has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffer, called ”aggregates”, whose number of events can be programmed by this register.

Address	0x1n34, 0x8034
Mode	R/W
Attribute	G

Bit	Description
[9:0]	Number of events per aggregate. Maximum value is 1023.
[31:10]	Reserved

Pre Trigger

Sets the Pre Trigger for the waveform acquisition. Once the event triggers, the digital samples are delayed by the pre trigger number of samples, to ensure that the waveform is completely acquired.

Address	0x1n38, 0x8038
Mode	R/W
Attribute	I

Bit	Description
[8:0]	Number of samples Ns for the Pre Trigger width, where Pre Trigger = Ns * 4. The value is expressed in steps of sampling frequency, 4 ns for 725 series, and 2 ns for 730 series. NOTE: the Pre Trigger value must be greater than the Gate Offset value by at least 38 ns.
[31:9]	Reserved

CFD settings

Sets the Constant Fraction Discrimination (CFD) delay and fraction parameters

Address	0x1n3C, 0x803C
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Set the CFD delay in time sample unit (4 ns for 725 series, and 2 ns for 730 series).
[9:8]	Set the CFD fraction. Options are: 00 : fraction = 25%; 01 : fraction = 50%; 10 : fraction = 75%; 11 : fraction = 100%.
[31:10]	Reserved

Forced Data Flush

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Address	0x1n40, 0x8040
Mode	R/W
Attribute	I

Bit	Description
[31:0]	A write access to this register forces the data flush.

Short Gate Width

Sets the Short Gate width for the charge integration of the fast component in the Pulse Shape Discrimination

Address	0x1n54, 0x8054
Mode	R/W
Attribute	I

Bit	Description
[11:0]	Number of samples for the Short Gate width. Each sample corresponds to 4 ns for 725 series, and 2 ns for 730 series.
[31:12]	Reserved

Long Gate Width

Sets the Long Gate width for the charge integration of the slow component in the Pulse Shape Discrimination. The Long integration Gate is also used for the energy spectra calculation

Address	0x1n58, 0x8058
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Number of samples for the Long Gate width. Each sample corresponds to 4 ns for 725 series, and 2 ns for 730 series.
[31:16]	Reserved

Gate Offset

Corresponds to the shift in time of the integration gate position with respect to the trigger

Address	0x1n5C, 0x805C
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Number of samples for the Gate Offset width. Each sample corresponds to 4 ns for 725 series, and 2 ns for 730 series.
[31:8]	Reserved

Trigger Threshold

Sets the Trigger Threshold value for the Leading Edge discrimination, and to arm the digital Constant Fraction Discrimination (725 and 730 only)

Address	0x1n60, 0x8060
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Set the number of LSB counts for the Trigger Threshold, where 1 LSB = 0.12 mV for 725 and 730 series with 2 Vpp input range, and 1 LSB = 0.03 mV for 725 and 730 series with 0.5 Vpp input range.. The threshold is referred to the baseline level.
[31:14]	Reserved

Fixed Baseline

Sets a fixed value for the baseline, which remains constant for the whole acquisition. The user must also disable the automatic baseline calculation, by setting Baseline Mean = 0.

Address	0x1n64, 0x8064
Mode	r/w
Attribute	I

Bit	Description
[13:0]	Value of Fixed Baseline in LSB counts, where 1 LSB = 0.12 mV for 725 and 730 series with 2 Vpp input range, and 1 LSB = 0.03 mV for 725 and 730 series with 0.5 Vpp input range. To set Baseline Mean = 0 refer to bits[22:20] of register 0x1n80 (0x8080).
[31:14]	Reserved

Shaped Trigger Width

The Shaped Trigger is a logic signal of programmable width generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic.

Address	0x1n70, 0x8070
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Set the number of samples for the Shaped Trigger width in trigger clock cycles (8 ns step)
[31:10]	Reserved

Trigger Hold-Off Width

The Trigger Hold-Off is a logic signal of programmable width generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold- Off duration

Address	0x1n74, 0x8074
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Set the Trigger Hold-Off width in steps of 8 ns.
[31:16]	Reserved

Threshold for the PSD cut

Sets the PSD threshold to online select events according to their PSD value.

Address	0x1n78, 0x8078
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Set the PSD threshold value. The desired value has to be multiplied by 1024 and converted into a hex number. Set bits[28:27] of register 0x1n80 to enable the cut on gamma or neutron respectively.
[31:10]	Reserved

DPP Algorithm Control

Management of the DPP algorithm features

Address	0x1n80, 0x8080
Mode	R/W
Attribute	I

Bit	Description
[2:0]	Charge Sensitivity: defines how many fC of charge corresponds to one channel of the energy spectrum. Options for Input Range = 2 Vpp are: 000: 5 fC; 001: 20 fC; 010: 80 fC; 011: 320 fC; 100: 1.28 pC. Options for Input Range = 0.5 Vpp are: 000: 1.25 fC; 001: 5 fC; 010: 20 fC; 011: 80 fC; 100: 320 fC.
[3]	Reserved
[4]	Charge Pedestal: when enabled a fixed value of 1024 is added to the charge. This feature is quite useful in case of energies close to zero.
[5]	Trigger Counting. Options are: 0 (default value): the shaped trigger used for TRG-OUT and coincidences reflects only the accepted self-triggers, i.e. the real events saved into memory; 1: the shaped trigger used for TRG-OUT and coincidences reflects all the self-triggers, even those of rejected events (for example consecutive events on the same gate, or events occurring during the board busy condition).
[6]	Discrimination mode for the event selection. Options are: 0 (default value): leading edge discrimination (LED); 1: digital constant fraction discrimination (CFD).
[7]	Reserved
[8]	Internal Test Pulse. It is possible to enable an internal test pulse for debugging purposes. The ADC counts are replaced with the built-in pulse emulator. Options are: 0: disabled. 1: enabled.
[10:9]	Test Pulse Rate. Set the rate of the built-in test pulse emulator. Options are: 00: 1 kHz; 01: 10 kHz; 10: 100 kHz; 11: 1 MHz.
[15:11]	Reserved
[16]	Pulse Polarity. Options are: 0: positive pulse; 1: negative pulse.
[17]	Reserved
[19:18]	Trigger Mode. Options are: 00: Normal mode. Each channel can self-trigger independently from the other channels. 01: Coincidence mode. Each channel saves the event only when a validation signal occurs inside the shaped trigger coincidence window. 10: Reserved. 11: Anti-coincidence mode. Each channel saves the event only when no validation signal occurs inside the shaped trigger coincidence window.

[22:20]	Baseline Mean. Sets the number of events for the baseline mean calculation. Options are: 000: Fixed: the baseline value is fixed to the value set in register 0x1n64; 001: 16 samples; 010: 64 samples; 011: 256 samples; 100: 1024 samples.
[23]	Reserved
[24]	Disable Self Trigger. If disabled the self-trigger is still propagated to the mother board for coincidence logic and TRG-OUT front panel connector, though it is not used by the channel to acquire the event. Options are: 0: self-trigger enabled; 1: self-trigger disabled.
[25]	Reserved
[26]	Pile-Up Rejection. Not yet implemented.
[27]	Enable PSD cut below threshold (to cut on gammas)
[28]	Enable PSD cut above threshold (to cut on neutrons).
[29]	Over-range Rejection. Reject the event when the ADC sample value is over/under the dynamic range during the long gate integration. Options are: 0: disabled; 1: enabled.
[30]	Trigger Hysteresis. The trigger can be inhibited during the trailing edge of a pulse, to avoid re-triggering on the pulse itself. Options are: 0 (default value): enabled; 1: disabled.
[31]	Reserved

Local Trigger Management

Manages the local shaped trigger and local trigger validation inside couples of channels, i.e. between channel 0 and channel 1, channel 2 and channel 3, and so on. This register is also used to configure the readout data format.

Address	0x1n84, 0x8084
Mode	R/W
Attribute	G

Bit	Description
[1:0]	Local Shaped Trigger mode. Sets how to combine the self-triggers of the channels inside each couple to generate a trigger request to the mother board. Enable Local Shaped Trigger mode by setting bit[2] of this register. Options are: 00: AND 01: even channel of the couple only 10: odd channel of the couple only 11: OR
[2]	Enable Local Shaped Trigger mode. Options are: 0: disabled; 1: enabled
[3]	Reserved
[5:4]	Local Trigger Validation mode. Sets how the trigger validation signal is generated for the two channels inside a couple. Enable the Local Trigger Validation mode by setting bit[6] of this register. Options are: 00: AND 01: trigger validation from mother board only (trigger validation is a combination of the other channels shaped triggers) 10: trigger validation comes from the other channel in the couple (coincidence inside the couple) 11: OR
[6]	Enable Local Trigger Validation mode. Options are: 0: disabled; 1: enabled.
[7]	Local Trigger Validation used as Veto. When enabled, the Local Trigger Validation coming from mother board is used to veto the event acquisition in the couple. Set the veto duration extension from register 0x1nD4. Options are: 0: disabled; 1: enabled.
[10:8]	Extras Word options. The channel aggregate data format has a 32 bit word, called EXTRAS word which can be configured to have the following information (firmware release greater than 136.2): 000: bits[31:16] = Extended Time Stamp, bits[15:0] = Baseline * 4; 001: bits[31:16] = Extended Time Stamp, bits[15:0] = Flags; 010: bits[31:16] = Extended Time Stamp, bits[15:10] = Flags, bits[9:0] = Fine Time Stamp; 011: Reserved; 100: Reserved; 101: bits[31:16] = Positive Zero Crossing, bits[15:0] = Negative Zero Crossing; 110: Reserved; 111: Fixed value = 0x12345678 (debug use only). ”Flags” correspond to: bit[15]: Trigger Lost (the first event after a trigger lost has this flag set); bit[14]: Over-range (the first event after a saturation has this flag set);
[11]	Use smoothed signal (see bits[15:12]) for charge integration. Options are: 0: disabled; 1: enabled.

[15:12]	Input smoothing factor. Sets the number of average samples for smoothing the input pulse. The smoothed input can be used both for CFD and LED triggering. Options are: 0000: disabled; 0001: 2 samples; 0010: 4 samples; 0011: 8 samples.
[31:16]	Reserved

Channel n Status

Read the status of channel n

Address	0x1n88
Mode	R
Attribute	I

Bit	Description
[1:0]	Reserved
[2]	If 1, the SPI bus is not available, therefore it is not possible to access registers 0x1nB4 and 0x1nB8
[3]	If 1, the ADC calibration has been done.
[7:4]	Reserved
[8]	ADC Power Down. The ADC of channel n has been shut down due to an over-temperature condition.
[31:9]	Reserved

AMC Firmware Revision

Returns the DPP firmware revision (mezzanine level).
To control the mother board firmware revision see register 0x8124.
For example: if the register value is 0xC3218303:
- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.

Address	0x1n8C
Mode	R
Attribute	I

Bit	Description
[7:0]	Firmware revision number
[15:8]	Firmware DPP code. Each DPP firmware has a unique code.
[19:16]	Build Day (lower digit)
[23:20]	Build Day (upper digit)
[27:24]	Build Month. For example: 3 means March, 12 is December.
[31:28]	Build Year. For example: 0 means 2000, 12 means 2012

DC Offset

Adjust the DC Offset level to exploit the full input dynamic range of the digitizer.

Address	0x1n98, 0x8098
Mode	R/W
Attribute	I

Bit	Description
[15:0]	DC Offset value in DAC LSB unit. Since the DAC ranges over 16 bits, while the ADC is over 14 bits, write the desired value multiplied by 4.
[31:16]	Reserved

ADC Temperature

Monitors the temperature of the ADC chips

Address	0x1nA8, 0x80A8
Mode	R
Attribute	I

Bit	Description
[7:0]	ADC chip temperature in °C.
[31:8]	Reserved

Individual Software Trigger

Sends Software Trigger to individual channel n. This is not affected by the Trigger Validation, i.e. the Individual Software Trigger can be issued also when coincidences are enabled without being affected.

Address	0x1nC0, 0x80C0
Mode	R/W
Attribute	I

Bit	Description
[31:0]	A write access to this register enables a software trigger for channel n.

Veto Duration Extention

When the Veto from Local Trigger Validation is enabled, the user can choose to extend its duration writing the corresponding value in this register.

Address	0x1nD4, 0x80D4
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Value for the veto extension.
[31:16]	Reserved

Board Configuration

General settings for the board configuration

Address	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Mode	R/W
Attribute	C

Bit	Description
[0]	Enable Automatic Data Flush: in case of very slow rate, this command forces the automatic data readout in a time window of 16-32 ms, even if the buffer is not completed. This is valid from AMC firmware revision greater than 136.2. Options are: 0: disabled (default value); 1: enabled.
[1]	Reserved: must be 0
[2]	Trigger Propagation: enables the propagation of the individual trigger from mother board individual trigger logic to the mezzanine. This is required in case of coincidence trigger mode
[3]	Reserved: must be 0
[4]	Reserved: must be 1
[7:5]	Reserved: must be 0
[8]	Individual trigger: must be 1
[10:9]	Reserved: must be 0
[11]	Dual Trace: in oscilloscope or mixed mode, it is possible to plot two different waveforms. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. According to the Analog Probe selection (see bits[13:12]) the following selections are available. Dual Trace = 0, Analog Probe = 0 => Trace 1 = Input, Trace 2 = N/A; Dual Trace = 0, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = N/A; Dual Trace = 1, Analog Probe = 0 => Trace 1 = Input, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 2 => Trace 1 = Input, Trace 2 = CFD.
[13:12]	Analog Probe selection: select which signal is associated to the analog probes. According to the Dual Trace value (see bit[11]) the following selections are available. Dual Trace = 0, Analog Probe = 0 => Trace 1 = Input, Trace 2 = N/A; Dual Trace = 0, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = N/A; Dual Trace = 1, Analog Probe = 0 => Trace 1 = Input, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 2 => Trace 1 = Input, Trace 2 = CFD.
[15:14]	Reserved: must be 0
[16]	Waveform Recording: enables the data recording of the waveform. The user must define the number of samples to be saved in the Record Length 0x1n20 register. According to the Analog Probe option one or two waveforms are saved. Options are: 0: disabled; 1: enabled.
[17]	Extras Recording: when enabled the EXTRAS word is saved into the event data. Refer to the ”Channel Aggregate Data Format” chapter of the DPP User Manual for more details about the EXTRAS word. Options are: 0: disabled; 1: enabled.
[18]	Time Stamp Recording: must be 1
[19]	Charge Recording: must be 1
[20:22]	Reserved: must be 0

[25:23]	Digital Virtual Probe 1: when the mixed mode is enabled, the following digital virtual probes can be selected: 000 = ”Long Gate”; 001 = ”Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold; 010 = ”Shaped TRG”, logic signal of programmable width generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic; 011 = ”TRG Val. Acceptance Win.”, logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory; 100 = ”Pile Up”, logic pulse set to 1 when a pile up event occurred (not implemented); 101 = ”Coincidence”, logic pulse set to 1 when a coincidence occurred; 110 = Reserved; 111 = ”Trigger”
[28:26]	Digital Virtual Probe 2: when the mixed mode is enabled, the following digital virtual probes can be selected: 000 = ”Short Gate”; 001 = ”Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold; 010 = ”TRG Validation”, logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory; 011 = ”TRG HoldOff”, logic signal of programmable width generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration; 100 = ”Pile Up”, logic pulse set to 1 when a pile up event occurred (to be implemented); 101 = ”Coincidence”, logic pulse set to 1 when a coincidence occurred; 110 = Reserved; 111 = ”Trigger”.
[31:29]	Reserved: must be 0

Aggregate Organization

Number of digital memory segmentation per aggregate (i.e. channel buffers).
Note: this register must not be modified while the acquisition is running.

Address	0x800C
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Buffer Organization Nb: the digitizer memory can be divided into N_aggr channel aggregates (buffers), where N_aggr = 2^{Nb}. Options for Nb ranges from 0x4 to 0xA. The corresponding values of N_aggr are: 0x0 - 0x1: Not used 0x2 : 4 0x3 : 8 0x4 : 16 0x5 : 32 0x6 : 64 0x7 : 128 0x8 : 256 0x9 : 512 0xA : 1024
[31:4]	Reserved: must be 0

Channel Calibration

Performs the automatic calibration of the ADC for all channels of the board. The calibration status can be monitored through bit[3] of the Channel n Status register 0x1n88.
NOTE: before writing this register, it is necessary to check that the ”SPI Bus Busy” flag of the Channel n Status register is equal to ”0” (i.e. (bit[2]) = 0), otherwise the writing process cannot run properly. After writing, the user is recommended to wait few seconds before a new RUN, to let the calibration get stabilized.

Address	0x809C
Mode	R
Attribute	C

Bit	Description
[31:0]	Write any value in this register to enable the ADC calibration.

Acquisition Control

-

Address	0x8100
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Start/Stop Mode. Options are: 00 = SW CONTROLLED, start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM), if the acquisition is armed (i.e. bit[2] = 1), then the acquisition starts when S-IN/GPI is asserted and stops when S-IN/GPI returns inactive. If bit[2] = 0, the acquisition is always off. 10 = FIRST TRIGGER CONTROLLED, if the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0). 11 = LVDS CONTROLLED (VME only), is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using register ”Front Panel I/O Control” 0x811C, and register ”Front Panel LVDS I/O New Features” 0x81A0.
[2]	Acquisition Start/Arm. When bits[1:0] = 00, this bit acts as a Run Start/Stop (0 = stopped; 1 = running). When bits[1:0] = 01, 10, 11, this bit arms the acquisition (0 = disarmed; 1 = armed); the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others) 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others)
[3]	Trigger Counting Mode. Options are: 0: only accepted triggers are counted; 1: all triggers are counted.
[4]	Reserved
[5]	Memory Full Mode. Options are: 0: the board is full whenever all buffers are full; 1: the board is full whenever N-1 buffers are full, where N is the number of blocks.
[6]	PLL Reference Clock source (Desktop/NIM only). Options are: 0: Internal Oscillator; 1: External clock from front panel CLK-IN connector.
[7]	Reserved
[8]	LVDS I/O Busy Enable mode. The LVDS I/O (VME only) can be programmed to accept a Busy signal as input, or to transfer it as output. Register 0x81A0 should be enabled. Options are: 0: disabled; 1: enabled.
[9]	LVDS I/O Veto Enable mode. The LVDS I/O (VME only) can be programmed to accept a Veto signal as input, or to transfer it as output. Register 0x81A0 should be enabled. Options are: 0: disabled; 1: enabled.
[10]	Reserved
[11]	LVDS I/O RunIn Enable mode. The LVDS I/O (VME only) can be programmed to accept a RunIn signal as input, or to transfer it as output. Register 0x81A0 should be enabled. Options are: 0: starts on RunIn level; 1: starts on RunIn rising edge.
[31:12]	Reserved

Acquisition Status

Monitors the status of the acquisition.

Address	0x8104
Mode	R
Attribute	C

Bit	Description
[1:0]	Reserved
[2]	Acquisition Status. Options are: 0: Acquisition is stopped; 1: Acquisition is running.
[3]	Event Ready. Options are: 0: no event is available for readout; 1: at least one event is available for readout.
[4]	Event full. Options are: 0: No channel has reached the full status condition; 1: the maximum number of events to be read is reached.
[5]	Clock Source. Options are: 0: internal (PLL uses the internal 50 MHz oscillator as reference); 1: external (PLL uses the external clock as reference).
[6]	PLL Bypass Mode. Options are: 0: PLL bypass mode is not active; 1: PLL bypass mode is active and the VCXO frequency directly drives the clock distribution tree.
[7]	PLL Unlock Detect: this flag shows a PLL unlock condition. Options are: 0: PLL has had an unlock condition since the last register read access; 1: PLL hasn't had any unlock condition since the last register read access. Note: flag can be restored to 1 via read access to VME Status register.
[8]	Board Ready: the board is ready for acquisition (PLL and ADCs are correctly synchronised). Options are: 0: Board is not ready to start the acquisition; 1: Board is ready to start the acquisition. This bit should be checked after software reset to ensure that the board will enter immediately run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved
[15]	S-IN (GPI) Status: read the current logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status: read the current logical level on TRG-IN front panel connector.
[18:17]	Reserved
[19]	Channels Shutdown Status. This bit is related to the Channel Shutdown register (0x81C0). Options are: 0: shutdown is OFF 1: shutdown is ON

[23:20]	Bits[23:20] (bits[21:20] in case of 8-channel versions) monitor the temperature status of the board channels. Each bit refers to a 4-channel mezzanine, i.e. bit[20] refers to channels 3-0, bit[21] to channels 7-4, etc. When at least one of the channels in the mezzanine exceeds the 70°C limit, the relevant bit is set automatically to ”1”. As soon as at least one of these bits becomes ”1”, the board enters the temperature protection condition which causes the automatic channel turning off and the acquisition RUN stop (if it was on): 1. Bit[19] becomes ”1”. 2. Bit[2] of the Acquisition Control register is automatically set to ”0”. Data possibly stored at the moment can be readout in any case. When all the bits[23:20] (bits[21:20] in case of 8-channel versions) become ”0”, the board exits the temperature protection condition. This means that the channel temperature reached at least 61°C. The user has then to turn on the board channels and the acquisition RUN (if necessary): 1. Bit[0] of the Channels Shutdown 0x81C0 must be set to ”0” (bit[19] of the Acquisition Status register becomes ”0”). 2. Bit[2] of of the Acquisition Control 0x8100 register must be set to ”1”.
[31:24]	Reserved

Software Trigger

-

Address	0x8108
Mode	W
Attribute	C

Bit	Description
[31:0]	A write access (whatever value) to this location generates a software trigger to all enabled channels of the board.

Global Trigger Mask

Sets which signal can contribute to the global trigger generation.

Address	0x810C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Bit n corresponds to which trigger request from couple of channels n (n=0,...,7) participates to the global trigger generation. Couple n corresponds to the two consecutive channels 2n and 2n+1, i.e. couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, etc. The trigger request from the couple can be programmed as the local shaped trigger from register 0x1n84, choosing among the options: AND/OR/one of the channels.
[19:8]	Reserved
[23:20]	Coincidence window: sets the time window (in mother board clock unit) for the majority coincidence. Set the majority level through bits [26:24].
[26:24]	Majority level. Sets the majority level for the global trigger generation. For a level m the trigger fires when at least m+1 of the enabled trigger requests (bits [7:0]) are over-threshold inside the coincidence window (bits [23:20]).
[28:27]	Reserved
[29]	LVDS Trigger: when enabled the trigger from LVDS (VME form factor only) participates to the global trigger generation (in logic OR). Options are: 0: disabled; 1: enabled.
[30]	External Trigger: when enabled the external trigger on TRG-IN participates to the global trigger generation (in logic OR). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger participates to the global trigger generation (in logic OR). Options are: 0: disabled; 1: enabled.

Front Panel TRG-OUT Enable Mask

Sets which signal can contibute to the TRG-OUT signal generation.

Address	0x8110
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Bit n corresponds to the trigger request from couple of channels n (n=0,...,7) which participates to the TRG-OUT signal. Couple n corresponds to the two consecutive channels 2n and 2n+1, i.e. couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, etc. The trigger request from the couple can be programmed as the local shaped trigger from register 0x1n84, choosing among the options: AND/OR/one of the channels.
[9:8]	TRG-OUT generation logic: the enabled trigger requests (bits [7:0]) can be combined to generate of the TRG-OUT signal. Options are: 00: OR; 01: AND; 10: Majority; 11: Reserved.
[12:10]	Majority level. Sets the majority level for the TRG-OUT signal generation. For a level m the majority fires when at least m+1 of the enabled trigger requests (bits [7:0]) are over-threshold.
[28:13]	Reserved
[29]	LVDS Trigger enable: if the LVDS (VME form factor only) are programmed as output, they can participate to the TRG-OUT signal generation. They are in logic OR with the other enabled signals. Options are: 0: disabled; 1: enabled.
[30]	External Trigger: when enabled the external trigger on TRG-IN can participate to the TRG-OUT signal generation (in logic OR with the other enabled signals). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger can participate to the TRG-OUT signal generation (in logic OR with the other enabled signals). Options are: 0: disabled; 1: enabled.

LVDS Data

Allows to read/write from LVDS I/O connectors.

Address	0x8118
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Front Panel I/O Data (VME form factor only). Allows to read/write from the corresponding nth LVDS I/O according to its configuration (see register Front Panel I/O Control 0x811C). A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input.
[31:16]	Reserved

Front Panel I/O Control

Manages the front panel I/O connectors

Address	0x811C
Mode	R/W
Attribute	C

Bit	Description
[0]	LEMO I/O (TRG-IN, S-IN/GPI, TRG-OUT) electrical level. Options are: 0: NIM I/O levels; 1: TTL I/O levels.
[1]	LVDS I/O enable. Options are: 0: enabled; 1: high impedance.
[2]	LVDS I/O [3:0] direction. Options are: 0: input; 1: output.
[3]	LVDS I/O [7:4] direction. Options are: 0: input; 1: output.
[4]	LVDS I/O [11:8] direction. Options are: 0: input; 1: output.
[5]	LVDS I/O [15:12] direction. Options are: 0: input; 1: output.
[7:6]	LVDS I/O signal configuration (old features). This configuration must been enabled through bit[8] sets to 0. Options are: 00: general purpose I/O; 01: programmed I/O; 10: pattern mode. LVDS signals are input and their value is written into the header PATTERN field; 11: reserved.
[8]	LVDS I/O new features selection. Options are: 0: LVDS old features; 1: LVDS new features. The new features options can be configured through register 0x81A0. Refer to the User Manual for all details. Note: this option is valid from mother board firmware revision greater than 3.8.
[9]	LVDS I/Os Pattern Latch Mode. Options are: 0: Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post-trigger settings and input latching delays. 1: Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives.
[10]	TRG-IN signal edge disable. Options are: 0: the trigger logic is active at the edge of the TRG-IN signal; 1: the trigger logic is active for the whole duration of the TRG-IN signal.
[11]	TRG-IN to mezzanines (channels). Options are: 0: Standard operating mode, the TRG-IN signal is processed by the mother board and sent to mezzanine as global trigger; 1: TRG-IN is directly sent to the mezzanines as global trigger. This can be useful when the TRG-IN is used to veto the acquisition in conjunction with bit[10] of this register.
[13:12]	Reserved
[14]	Force TRG-OUT. Options are: 0: Force TRG-OUT to 0; 1: Force TRG-OUT to 1. Sets TRG-OUT test logical level if bit[15] = 1.

[15]	TRG-OUT Mode. Options are: 0 = TRG-OUT is an internal signal (according to bits[17:16]) 1= TRG-OUT is a test logic level set via bit[14]
[17:16]	TRG-OUT Mode selection. Options are: 00: Trigger (TRG-OUT propagates the internal trigger sources according to the Front Panel TRG-OUT Enable Mask register 0x8110); 01: Motherboard probes (TRG-OUT is used to propagate signals of the motherboards, according to bits[19:18]); 10: Channel probes (TRG-OUT is used to propagate signals of the mezzanines (Channel Signal Virtual Probe)); 11: S-IN propagation.
[19:18]	Motherboard Virtual Probe selection (to be propagated on TRG- OUT). Options are: 00: RUN: the signal is active when the acquisition is running. This option can be used to synchronize the start/stop of the acquisition through the TRG- OUT->TR-IN or TRG-OUT->S-IN daisy chain; 01: CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10: CLK Phase; 11: Board BUSY or PLL Lock Loss. This probe can be selected according to bit[20].
[20]	Select between Board BUSY and PLL Lock Loss of bits[19:18]. Options are: 0: Board BUSY; 1: PLL Lock Loss.
[31:21]	Reserved

Channel Enable Mask

Enable/disable selected channels to participate to the event readout.
Note: this register must not be modified while the acquisition is running.

Address	0x8120
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Bit n can enable/disable selected channel n to participate to the event readout. Options are: 0: disabled; 1: enabled.
[31:16]	Reserved

ROC FPGA Firmware Revision

Reads the mother board (ROC FPGA) firmware revision in the format X.Y.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	Firmware revision (Y)
[15:8]	Firmware revision (X).
[31:16]	Revision Date in the format Y/M/DD

Set Monitor DAC

Sets the DAC value when the Voltage Level Mode is enabled (see register 0x8144). 1 LSB = 0.244 mV, terminated on 50 Ohm.
Note: VME form factor only.

Address	0x8138
Mode	R/W
Attribute	C

Bit	Description
[11:0]	DAC Voltage Setting (12 bit). The corresponding output value is multiplied by 0.244 mV
[31:12]	Reserved

Software Clock Sync

A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock. In case of Daisy chain clock distribution among boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.
Note: the command must be issued starting from the first to the last board in the clock chain.

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Software Sync command.

Board Info

Retrieves the specific information of the board.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[7:0]	Digitizer Family Code: 0xE = 725 digitizer family; 0xB = 730 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 1: each channel is equipped with 640 kS acquisition memory; 8: each channel is equipped with 5.12 MS acquisition memory.
[23:16]	Equipped Channels Number. If this number is lower than the physical channel number, there could be a communication problem with some of the channel mezzanines.
[31:17]	Reserved

Monitor DAC Mode

Sets the Monitor DAC output connector mode.
Note: VME form factor only.

Address	0x8144
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Analog Monitor Output mode (VME form factor only). Options are: 000: Trigger Majority mode; 001: Test mode; 010: reserved; 011: Buffer Occupancy mode; 100: Voltage Level mode; 101: reserved; 110: reserved; 111: reserved.
[31:3]	Reserved

Event Size

Represents the current available event in 32-bit words. The value is updated after the complete readout of each event.

Address	0x814C
Mode	R
Attribute	C

Bit	Description
[31:0]	Event size (in 32-bit word)

Time Bomb Downcounter

This is a down counter value. If the value is constant, the firmware license is enabled and the current firmware can be used without any time limitation. If the value decreases with time, the firmware will stop working (no possibility to enter RUN mode) after 30 minutes after module power- on. If the value is 0, the time bomb has expired, and module is not allowed to enter in RUN mode without power cycling the module.

Address	0x8158
Mode	R
Attribute	C

Bit	Description
[31:0]	Down counter value. If this value is constant the DPP firmware is licensed

Fan Speed Control

Manages the fan speed control (DT form factor only) to automatically control the fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.
This functionality is available from revision 4 of the hardware, and ROC FPGA firmware revision greater than 4.4.
The hardware revision can be read at the 0xF04C address in the Configuration ROM.
Independently of the revision, the user can set the fan speed "high" by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for rev. 4 or higher, or the low fan speed in case of revisions less than 4.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved, must be 0.
[3]	Fan Speed. Options are: 0: slow speed or automatic speed tuning; 1: high speed.
[5:4]	Reserved, must be 1
[31:6]	Reserved, must be 0

Memory Buffer Almost Full Level

Allows to set the level for the Almost Full generation. If this register is set to 0, the Almost Full is a Full. Refer to the User Manual for further details.

Address	0x816C
Mode	R/W
Attribute	C

Bit	Description
[10:0]	LEVEL
[31:11]	Reserved

Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay, expressed in trigger clock cycles (i.e. 8 ns for x725 and x730 models) between the arrival of the Start signal at the input of the board (either on S-IN or TRG-IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backward along the chain.

Address	0x8170
Mode	R/W
Attribute	C

Bit	Description
[31:0]	RUN/START/STOP Delay (expressed in trigger clock cycles).

Board Failure Status

Monitors whether a failure occurred in the board. In case of error, bit[26] of the second work of the data header is set to 1 during the data readout. Read this register to check the exact error occurred.
Note: In case of problems with the board, the user can monitor this register and contact CAEN for support (see the User Manual or visit CAEN website for contacts).

Address	0x8178
Mode	R
Attribute	C

Bit	Description
[3:0]	Internal Communication Timeout. Options are: 0000: No Error; Any other value means that a timeout error occurred.
[4]	PLL Lock Loss. Options are: 0: No error; 1: A PLL lock loss occurred.
[5]	Temperature failure. Options are: 0: No error; 1: A temperature failure occurred, and at least one channel is in over- temperature condition.
[6]	ADC Power Down. Options are: 0: No error; 1: At least one channel is in power down mode due to an automatic over- temperature protection.
[31:7]	Reserved

Disable External Trigger

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Address	0x817C
Mode	R/W
Attribute	C

Bit	Description
[0]	External Trigger on TRG-IN connector can be disabled through this bit. Options are: 0: external trigger enabled; 1: external trigger disabled.
[31:1]	Reserved

Trigger Validation Mask

Sets the trigger validation logic

Address	0x8180+(4n)
Mode	R/W
Attribute	G

Bit	Description
[7:0]	Bit n corresponds to the trigger request from couple of channels n (n=0,...,7) which participates to the generation of the trigger validation signal. Couple n corresponds to the two consecutive channels 2n and 2n+1, i.e. couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, etc. The trigger request from the couple can be programmed as the local shaped trigger from register 0x1n84, choosing among the options: AND/OR/one of the channels.
[9:8]	Operation Mask. Sets the logic operation among the enabled trigger request signals. Options are: 00: OR; 01: AND; 10: majority; 11: reserved.
[12:10]	Sets the majority level. For a level m the majority fires when at least m+1 trigger requests are high.
[27:13]	Reserved
[28]	LVDS I/O Global Trigger: when enabled (VME form factor only) the global trigger from LVDS I/O participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[29]	LVDS I/O Individual Trigger: when enabled (VME form factor only) the individual trigger from LVDS I/O participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[30]	External Trigger: when enabled the external trigger from TRG-IN front panel connector participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.

Front Panel LVDS I/O New Features

Configures the new features of the LVDS I/O (VME form factor only). It is possible to configure four LVDS at a time. Possible configurations are:
0000 = Register, where the four LVDS act as register (read/write according to the configured input/output option);
0001 = Trigger (each four LVDS can be configured to receive a input trigger for each channel, or to propagate the shaped trigger in output);
0010 = nBUSY/nVETO (the four LVDS of the group can be configured as: 0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In in case of input LVDS setting, while they can be configured as 0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun Out in case of output LVDS setting);
0011 = Legacy (where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting). Refer to the User Manual for additional details.
Note: this functionality is supported from revision 3.8 of the ROC FPGA firmware on.

Address	0x81A0
Mode	R/W
Attribute	C

Bit	Description
[3:0]	LVDS I/O [3:0] pin configuration
[7:4]	LVDS I/O [7:4] pin configuration
[11:8]	LVDS I/O [11:8] pin configuration
[15:12]	LVDS I/O [15:12] pin configuration
[31:16]	Reserved

Channel Shutdown

Performs the shutdown of all the board's channels. This register is automatically set to "1" when the board enters the temperature protection condition (see register Acquisition Status 0x8104). It has to be set to "0" by the user only after the board exits the temperature protection condition.
Note: bit[0] is forced to "1" while the board is in the temperature protection condition.
Note: it is not recommended to set bit[0] = 1 when the board is not in temperature protection condition.

Address	0x81C0
Mode	R/W
Attribute	C

Bit	Description
[0]	Channels Shutdown. Options are: 0: no shutdown command is issued; 1: a shutdown command is issued.
[31:1]	Reserved

Readout Control

This register is mainly intended for VME form factor models. Anyway some bits are applicable also for non-VME boards.

Address	0xEF00
Mode	R/W
Attribute	C

Bit	Description
[2:0]	VME Interrupt level. Options are: 0: VME interrupts are disabled; 1-7: set the VME interrupt level.
[3]	Optical Link Interrupt Enable. Options are: 0: Optikal Link interrupts are disabled; 1: Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout enable. Options are: 0: VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1: VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer read out in D32).
[5]	VME Align64 Mode. Options are: 0: 64-bit aligned readout mode disabled; 1: 64-bit aligned readout mode disabled enabled.
[6]	VME Base Address Relocation. Options are: 0: Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1: Address Relocation enabled (VME Base Address is set by the Relocation Address register 0xEF0C).
[7]	Interrupt Release mode. Options are: 0: Release On Register Access (RORA). This is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable = 0. 1: Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). Note: ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link.
[8]	Extended Block Transfer enable, selects the Memory Interval allocated for Block Transfers. Options are: 0: Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1: Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFFC interval. In Extended mode, the board VME Base Address is only set via the on-board [31:28] rotary switches or the bits[31:28] of Relocation Address register.
[31:9]	Reserved

Readout Status

-

Address	0xEF04
Mode	R
Attribute	C

Bit	Description
[0]	Event Ready. Options are: 0: No Data Ready; 1: Event Ready.
[1]	Reserved
[2]	Bus error flag. Options are: 0: BERR FLAG: no Bus Error has occurred; 1: BERR FLAG: a Bus Error has occurred (this bit is reset after a status register read out).
[31:3]	Reserved

Board ID

The Meaning of the register depends on which VME crate it is inserted in.
For VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
For other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address
[31:5]	Reserved

MCST Base Address and Control

Configures the board for the VME Multicast Cycles

Address	0xEF0C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00: Board disabled; 01: Last board; 10: First board; 11: Intermediate board.
[31:10]	Reserved

Relocation Address

If address relocation is enabled through register 0xEF00, this register sets the VME Base Address of the module.

Address	0xEF10
Mode	R/W
Attribute	C

Bit	Description
[15:0]	These bits contain the A31÷A16 bits of the address of the module. If address relocation is enabled through register 0xEF00, this register sets the VME Base Address of the module.
[31:16]	Reserved

Interrupt Status ID

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

Address	0xEF14
Mode	R/W
Attribute	C

Bit	Description
[31:0]	STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

Interrupt Event Number

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER.

Address	0xEF18
Mode	R/W
Attribute	C

Bit	Description
[9:0]	INTERRUPT EVENT NUMBER
[31:10]	Reserved

Aggregate Number per BLT

This register sets the maximum number of complete aggregates which has to be transferred for each block transfer (via VME BLT/CBLT cycles or block readout through Optical Link).

Address	0xEF1C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Number of complete aggregates to be transferred for each block transfer (BLT).
[31:8]	Reserved

Scratch

This register can be used to write/read words for VME test purposes.

Address	0xEF20
Mode	R/W
Attribute	C

Bit	Description
[31:0]	Scratch

Software Reset

A write access to this location of any value, allows to perform a software reset. All registers are set to default values (i.e. actual settings are lost).

Address	0xEF24
Mode	W
Attribute	C

Bit	Description
[31:0]	Access write to perform a software reset.

Software Clear

A write access to this location of any value, clears all the internal memories. Registers value are not changed.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Write access to clear the internal memories.

Configuration Reload

A write access to this register of any value, causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write access to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

-

Address	0xF000
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Checksum
[31:8]	Reserved

Configuration ROM Checksum Length2

-

Address	0xF004
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Checksum Length [23:16]
[31:8]	Reserved

Configuration ROM Checksum Length1

-

Address	0xF008
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Checksum Length [15:8]
[31:8]	Reserved

Configuration ROM Checksum Length0

-

Address	0xF00C
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Checksum Length [7:0]
[31:8]	Reserved

Configuration ROM Constant2

-

Address	0xF010
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Constant2 fixed value.
[31:8]	Reserved

Configuration ROM Constant1

-

Address	0xF014
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Constant1 fixed value
[31:8]	Reserved

Configuration ROM Constant0

-

Address	0xF018
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Constant0 fixed value
[31:8]	Reserved

Configuration ROM c Code

-

Address	0xF01C
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'c' character code
[31:8]	Reserved

Configuration ROM r Code

-

Address	0xF020
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'r' character code.
[31:8]	Reserved

Configuration ROM Manufacter Identifier OUI2

-

Address	0xF024
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Manufacter Identifier OUI2 value
[31:8]	Reserved

Configuration ROM Manufacter Identifier OUI1

-

Address	0xF028
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Manufacter Identifier OUI1 value
[31:8]	Reserved

Configuration ROM Manufacter Identifier OUI0

-

Address	0xF02C
Mode	R
Attribute	C

Bit	Description
[7:0]	Configuration ROM Manufacter Identifier OUI0 value
[31:8]	Reserved

Configuration ROM Board Version

-

Address	0xF030
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Version Code. Options for VME form factor are: V1725: F0; V1725B: F1; V1725C: F2; V1725D: F3. V1730: C0; V1730B: C1; V1730C: C2; V1730D: C3. Options for Desktop/NIM form factor are: DT5725/N6725: F0; DT5725B/N6725B: F1. DT5730/N6730: C0; DT5730B/N6730B: C1.
[31:8]	Reserved

Configuration ROM Board Form Factor

-

Address	0xF034
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Form Factor CAEN Code. 0: VME64. 1: VME64X. 2: Desktop. 3: NIM.
[31:8]	Reserved

Configuration ROM Board Number ID1

-

Address	0xF038
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID 1 (bit[15:8])
[31:8]	Reserved

Configuration ROM Board Number ID0

-

Address	0xF03C
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID0 (bit[7:0])
[31:8]	Reserved

Configuration ROM Revis3

-

Address	0xF040
Mode	R
Attribute	C

Bit	Description
[31:0]	Reserved

Configuration ROM Revis2

-

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[31:0]	Reserved

Configuration ROM Revis1

-

Address	0xF048
Mode	R
Attribute	C

Bit	Description
[31:0]	Reserved

Configuration ROM PCB Revision

-

Address	0xF04C
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision
[31:8]	Reserved

Configuration ROM Flash Type

-

Address	0xF050
Mode	R
Attribute	C

Bit	Description
[7:0]	Flash Type
[31:8]	Reserved

Configuration ROM Board Serial Number1

-

Address	0xF080
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number1 (bit[15:8])
[31:8]	Reserved

Configuration ROM Board Serial Number0

-

Address	0xF084
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number0 (bit[7:0])
[31:8]	Reserved

Configuration ROM VCXO Type

-

Address	0xF088
Mode	R
Attribute	C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0: AD9510 with 1 GHz. 1: AD9510 with 500 MHz (not programmable). 2: AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: 0: AD9520-3.

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