





DPSD Register Description5 June 2013

Purpose of this Manual

This User Manual contains the full description of Digital Pulse Shape Discrimination registers.



Important Note:

The content of this document has been extracted from UM2588 DPSD User Manual - rev 2 - 10 October 2012

FOR RELEASES OF THE ROC FPGA FIRMWARE HIGHER THAN 3.8 THE CONTENT OF THIS DOCUMENT MAY RESULT NOT FULLY COMPLIANT.

IT IS INTENDED TO BE REPLACED BY A NEW DOCUMENT UNIFYING THE REGISTERS DESCRIPTIONS OF CAEN DIGITIZERS CURRENTLY IN PROGRESS.

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1 Registers and Data Format

This chapter describes the accessible registers of a DPSD board and the format of the readout data.

If not expressly written, the description has to be intended common to 720 and 751 series.

Registers

In the table below, registers referred as *Reserved* in the field "Register name" are not supported by the DPP-PSD Firmware and their description is not included in this context.

Register name	Address	Mode
CONFIG	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W
BUFF_ORG	0x800C	R/W
Reserved	0x8010-0x801C	-
RECORD LENGTH	0x1n20 (channel n), 0x8020 (all channels)	R/W
NEV AGGREGATE	0x1n34 (channel n), 0x8034 (all channels)	R/W
PRE TRG	0x1n38 (channel n), 0x8038 (all channels)	R/W
 Reserved	0x803C-0x8050	-
SHORT_GATE	0x1n54 (channel n), 0x8054 (all channels)	R/W
LONG GATE	0x1n58 (channel n), 0x8058 (all channels)	R/W
PRE GATE	0x1n5C (channel n), 0x805C (all channels)	R/W
DPP TRG THRESHOLD (thr)	0x1n60 (channel n), 0x8060 (all channels)	R/W
BASELINE THRESHOLD (bithr)	0x1n64 (channel n), 0x8064 (all channels)	R/W
BASELINE_TIME_OUT (bito)	0x1n68 (channel n), 0x8068 (alla channels)	R/W
Reserved	0x806C	-
Reserved	0x8070	_
Reserved	0x8074	_
Reserved	0x8074 0x8078-0x807C	-
	0x1n80 (channel n), 0x8080 (all channels)	R/W
DPP_CTRL Reserved	0x1080 (channel n), 0x8080 (all channels) 0x8088	ry vv
		- D
AMC_FIRMWARE_REVISION	0x1n8C	R
Reserved	0x8090-0x8094	-
DC_OFFSET	0x1n98 (channel n), 0x8098 (all channels)	R/W
Reserved	0x809C	-
ACQUISITION_CONTROL	0x8100	R/W
ACQUISITION_STATUS	0x8104	R
SOFTWARE_TRIGGER	0x8108	W
GLOBAL_TRIGGER_MASK	0x810C	R/W
TRIGGER_OUT_MASK	0x8110	R/W
Reserved	0x8114	-
LVDS_DATA	0x8118	R/W
FRONT_PANEL_CONTROL	0x811C	R/W
CHANNEL_ENABLE_MASK	0x8120	R/W
ROC_FIRMWARE_REVISION	0x8124	R
Reserved	0x812C	-
Reserved	0x8130	-
Reserved	0x8134	-
MONITOR_DAC_CONTROL	0x8138	R/W
SW_CLOCK_SYNC	0x813C	W
BOARD_INFO	0x8140	R
MONITOR DAC MODE	0x8144	R/W
Reserved	0x8148	-
EVENT SIZE	0x814C	R/W
	0x8150	-
Reserved	0x8154	-
TIME BOMB DOWNCOUNTER	0x8158	R
Reserved	0x815C	-
Reserved	0x8160	_
Reserved	0x8164	-
Reserved	0x816C	-
RUN_START_STOP_DELAY	0x8170	R/W
Reserved	0x8174	-
Reserved	0x8174	-
VETO	0x8178 0x817C	R/W
	0x8180-0x819C	-
Reserved	00200 00250	
Reserved RESERVED CONTROL	0x8200-0x83FC 0xEF00	- R/W

VME_MULTICAST_CONTROL 0xEF0C R/W VME_ADDRESS_RELOCATION 0xEF10 R/W VME_INTERRUPT_ID 0xEF14 R/W READOUT_INTERRUPT_CONDITION (EVENT NUMBER) 0xEF18 R/W READOUT_BLT_AGGREGATE_NUMBER 0xEF1C R/W DUMMY 0xEF20 R/W SOFTWARE_RESET 0xEF24 W SOFTWARE_CLEAR 0xEF28 W BOARD_CONFIGURATION_RELOAD 0xEF34 R/W CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CONSTANT2 0xF001 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_OUI2	VME GEO ADDRESS	0xEF08	R/W
VME_INTERRUPT_ID 0xEF14 R/W READOUT_INTERRUPT_CONDITION (EVENT NUMBER) 0xEF18 R/W READOUT_BLT_AGGREGATE_NUMBER 0xEF10 R/W DUMMY 0xEF20 R/W SOFTWARE_RESET 0xEF24 W SOFTWARE_CLEAR 0xEF28 W BOARD_CONFIGURATION_RELOAD 0xEF34 R/W CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF000 R CONFIGURATION_ROM_CONSTANT2 0xF0010 R CONFIGURATION_ROM_CONSTANT2 0xF0010 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_OUI1 0xF024 R CONFIGURATION_ROM	VME MULTICAST CONTROL	0xEF0C	R/W
READOUT_INTERRUPT_CONDITION (EVENT NUMBER) 0xEF18 R/W READOUT_BLT_AGGREGATE_NUMBER 0xEF1C R/W DUMMY 0xEF20 R/W SOFTWARE_RESET 0xEF24 W SOFTWARE_CLEAR 0xEF28 W BOARD_CONFIGURATION_RELOAD 0xEF34 R/W CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM 0xF0004 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF0004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF0008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF000 R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF010 R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_OUI1 0xF024 R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURAT	VME_ADDRESS_RELOCATION	0xEF10	R/W
READOUT_BLT_AGGREGATE_NUMBER 0xEF1C R/W DUMMY 0xEF20 R/W SOFTWARE_RESET 0xEF24 W SOFTWARE_CLEAR 0xEF28 W BOARD_CONFIGURATION_RELOAD 0xEF34 R/W CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF000 R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF016 R CONFIGURATION_ROM_CODE 0xF016 R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI3 0xF036 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_FORM_FACTO	VME_INTERRUPT_ID	0xEF14	R/W
DUMMY 0xEF20 R/W SOFTWARE_RESET 0xEF24 W SOFTWARE_CLEAR 0xEF28 W BOARD_CONFIGURATION_RELOAD 0xEF34 R/W CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF000 R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF01C R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI0 0xF028 R CONFIGURATION_ROM_OUI0 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0	READOUT_INTERRUPT_CONDITION (EVENT NUMBER)	0xEF18	R/W
SOFTWARE_RESET	READOUT_BLT_AGGREGATE_NUMBER	0xEF1C	R/W
SOFTWARE_CLEAR 0xEF28 W BOARD_CONFIGURATION_RELOAD 0xEF34 R/W CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF00C R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF00C R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CC_CODE 0xF01C R CONFIGURATION_ROM_CC_CODE 0xF020 R CONFIGURATION_ROM_COULD 0xF020 R CONFIGURATION_ROM_OULD 0xF028 R CONFIGURATION_ROM_OULD 0xF028 R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_IDD 0xF038 R CONFIGURATION_ROM_BOARD_IDD 0xF036 R	DUMMY	0xEF20	R/W
BOARD_CONFIGURATION_RELOAD 0xEF34 R/W CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF0004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF0008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF000C R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF010 R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF016 R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_VERSION 0xF02C R CONFIGURATION_ROM_FERSION 0xF030 R CONFIGURATION_ROM_BOARD_ID1 0xF034 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS1 0xF048 R	SOFTWARE_RESET	0xEF24	W
CONFIGURATION_ROM_CHECKSUM 0xF000 R CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF00C R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF01C R CONFIGURATION_ROM_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI0 0xF028 R CONFIGURATION_ROM_OUI0 0xF028 R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF04C R C	SOFTWARE_CLEAR	0xEF28	W
CONFIGURATION_ROM_CHECKSUM_LENGTH2 0xF004 R CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF00C R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CODE 0xF01C R CONFIGURATION_ROM_CODE 0xF01C R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF028 R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS2 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R	BOARD_CONFIGURATION_RELOAD	0xEF34	R/W
CONFIGURATION_ROM_CHECKSUM_LENGTH1 0xF008 R CONFIGURATION_ROM_CHECKSUM_LENGTH0 0xF00C R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_CCODE 0xF01C R CONFIGURATION_ROM_R CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATIO	CONFIGURATION_ROM_CHECKSUM	0xF000	R
CONFIGURATION_ROM_CHECKSUM_LENGTHO 0xF00C R CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_C_CODE 0xF01C R CONFIGURATION_ROM_R_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF080 R	CONFIGURATION_ROM_CHECKSUM_LENGTH2	0xF004	R
CONFIGURATION_ROM_CONSTANT2 0xF010 R CONFIGURATION_ROM_CONSTANT1 0xF014 R CONFIGURATION_ROM_CONSTANT0 0xF018 R CONFIGURATION_ROM_C_CODE 0xF01C R CONFIGURATION_ROM_R_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS1 0xF044 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_CHECKSUM_LENGTH1	0xF008	R
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CONFIGURATION_ROM_C_CODE 0xF01C R CONFIGURATION_ROM_R_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_CONSTANT1	0xF014	R
CONFIGURATION_ROM_R_CODE 0xF020 R CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_CONSTANT0	0xF018	R
CONFIGURATION_ROM_OUI2 0xF024 R CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_C_CODE	0xF01C	R
CONFIGURATION_ROM_OUI1 0xF028 R CONFIGURATION_ROM_OUI0 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_R_CODE	0xF020	R
CONFIGURATION_ROM_OUIO 0xF02C R CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_OUI2	0xF024	R
CONFIGURATION_ROM_VERSION 0xF030 R CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_OUI1	0xF028	R
CONFIGURATION_ROM_FORM_FACTOR 0xF034 R CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_OUIO	0xF02C	R
CONFIGURATION_ROM_BOARD_ID1 0xF038 R CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_VERSION	0xF030	R
CONFIGURATION_ROM_BOARD_ID0 0xF03C R CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_FORM_FACTOR	0xF034	R
CONFIGURATION_ROM_REVIS3 0xF040 R CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_BOARD_ID1	0xF038	R
CONFIGURATION_ROM_REVIS2 0xF044 R CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_BOARD_ID0	0xF03C	R
CONFIGURATION_ROM_REVIS1 0xF048 R CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_REVIS3	0xF040	R
CONFIGURATION_ROM_PCB_REVISION 0xF04C R CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_REVIS2	0xF044	R
CONFIGURATION_ROM_SERNUM1 0xF080 R CONFIGURATION_ROM_SERNUM0 0xF084 R	CONFIGURATION_ROM_REVIS1	0xF048	R
CONFIGURATION_ROM_SERNUMO 0xF084 R	CONFIGURATION_ROM_PCB_REVISION	0xF04C	R
	CONFIGURATION_ROM_SERNUM1	0xF080	R
CONFIGURATION_ROM_VCXO_TYPE 0xF088 R	CONFIGURATION_ROM_SERNUM0	0xF084	R
	CONFIGURATION_ROM_VCXO_TYPE	0xF088	R

Tab. 1.1: Register address map

Tab. 1.2 shows the default values of the DPSD registers related to the DPP-PSD algorithm:

Register name	x720	x751
CONFIG	0x40F0010	0x10
BUFF_ORG	0x07	0x0A
RECORD_LENGTH	0x80	0x00
NEV_AGGREGATE	0x28	0x00
PRE_TRG	0x64	0x00
SHORT_GATE	0x0A	0x00
LONG_GATE	0x50	0x00
PRE_GATE	0x15	0x00
DPP_TRG_THRESHOLD (thr)	0x1E	0x00
BASELINE_THRESHOLD (blthr)	0x03	0x00
DPP_CTRL	0x0000084	0x00

Tab. 1.2: DPP-PSD registers default values

CONFIG

For 720 series:

Address: 0x8000, 0x8004 (BitSet), 0x8008 (BitClear)

Bits: [28:0] Access Mode: Read and Write

Bit(s) Info	Bit(s) Description		
[0]	Reserved: must be 0		
[3:1]	Reserved: must be 0		
[4]	Reserved: must be 1		
[7:5]	Reserved: must be 0		
[8]	Individual trigger: must be 1		
[9]	Reserved: must be 0		
[10]	Reserved: must be 0		
[11]	Dual Trace: when the oscilloscope mode is enabled (readout of waveforms), it is possible to read two different		
Default: 0	waveforms from the FPGA (for example the input signal and the baseline). When the dual trace is enabled, the		
	samples of two signals are interleaved, thus each waveform is recorded at half the ADC frequency.		
	0: Dual Trace disabled (record one waveform at 250 MSps)		
	1: Dual Trace enabled (record two waveforms at 125 MSps)		
[13:12]	Virtual Probe 1: Select which signal is associated to the trace 2 in the readout data (only in dual trace mode).		
Default: 0	00: Baseline (input baseline)		
	01: Baseline Threshold		
[1 [. 1]			
[15:14]	Reserved: must be 0		
[16]	Oscilloscope Mode: enables the saving of a certain number of samples in the event data. The number of samples		
Default: 1	depends on the CUST_SIZE setting in the RECORD_LENGTH register and they belong to one or two signals,		
	according to the Dual Trace and Virtual Probe settings.		
	0: Oscilloscope Mode disabled		
	1: Oscilloscope Mode enabled		
[17]	Baseline Mode: when enabled, the baseline (used as reference for the pulse integration) is saved into the event		
Default: 1	data (last word of the event).		
Delaar. 1	0: Baseline Mode disabled		
	1: Baseline Mode enabled		
[18] Default: 1	Time Tag Mode: when enabled, the time tag (i.e. time of the threshold crossing) is saved into the event data (first word of the event).		
	0: Time Tag Mode disabled		
	1: Time Tag Mode enabled		
[19]	Charge Mode: when enabled, the Qshort and Qlong, is saved into the event data (third word of the event).		
Default: 1	0: Charge Mode disabled		
	1: Charge Mode enabled		
[21:20]	Trigger Mode:		
Default: 0	00: Normal		
	10: Coincidence		
[22]	Enable Pile Up Rejection (PUR): when enabled, these pulse with the relative information are rejected.		
Default: 0	0: PUR disabled		
	1: PUR enabled		
[25:23]	Digital Virtual Probe 1: when the oscilloscope mode is enabled, each 32-bit word contains two samples (12 bits)		
Default: 0	plus four digital values (digital virtual probes). The third bit is selected by these 3 bits among the following options:		
	000: Armed		
	001: Trigger		
	010: Charge ready		
	011: Pile Up		
	100: Baseline out of safe band		
	101: Baseline timeout		
	110: Coincidence meet		
	111: Time validation acquisition window		
[20, 20]	The first 2 bits are always the gate short and the gate long digital signal.		
[28:26]	Digital Virtual Probe 2: when the oscilloscope mode is enabled, each 32-bit word contains two samples (12 bits)		
Default: 1	plus four digital values (digital virtual probes). The fourth bit is selected by these 3 bits among the following		
	options: 000: Armed		
	010: Charge ready		
	100: Pile Up Baseline out of safe band		
	101: Baseline timeout		

	110: Coincidence meet
	111: Time validation acquisition window
	The first 2 bits are always the gate short and the gate long digital signal.
[31:29]	Reserved: must be 0

Tab. 1.3: CONFIG for 720 series

For 751 series:

Address: 0x8000, 0x8004 (bitSet), 0x8008 (BitClear)

Bits: [24:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description	
[0]	Reserved: must be 0	
[1]	Reserved: must be 0	
[2]	Reserved	
[3]	Test Mode: when the test pattern is enabled, the input signal samples are replaced by a sawtooth test signal.	
	0: Test Mode disabled	
	1: Test Mode enabled	
[4]	Reserved: must be 1	
[7:5]	Reserved: must be 0	
[8]	Individual trigger: must be 1	
[9]	Reserved: must be 0	
[10]	Reserved: must be 0	
[11]	Dual Trace: when the oscilloscope mode is enabled (readout of waveforms), it is possible to read two different	
	waveforms from the FPGA (for example the input signal and the baseline). When the dual trace is enabled, the	
	samples of two signals are interleaved, thus each waveform is recorded at half the ADC frequency.	
	0: Dual Trace disabled (record one waveform at 1 GSps)	
	1: Dual Trace enabled (record two waveforms at 500 MSps)	
[15:12]	Reserved: must be 0	
[16]	Oscilloscope Mode: enables the saving of a certain number of samples in the event data. The number of samples	
	depends on the CUST.SIZE setting in the RECORD_LENGTH register and they belong to one or two signals, according	
	to the Dual Trace and Virtual Probe settings.	
	0: Oscilloscope Mode disabled	
[17]	1: Oscilloscope Mode enabled Receling Mode, when anabled the baseline (used as reference for the pulse integration) is sound into the quart	
[17]	Baseline Mode: when enabled, the baseline (used as reference for the pulse integration) is saved into the event data.	
	0: Baseline Mode disabled	
	1: Baseline Mode enabled	
[18]	Time Tag Mode: when enabled, the time tag (i.e. time of the threshold crossing) is saved into the event data (the	
[10]	first word of the event).	
	0: Time Tag Mode disabled	
	1: Time Tag Mode enabled	
[19]	Charge Mode: when enabled, the Qshort and Qlong, is saved into the event data the (the last word of the event).	
[]	0: Charge Mode disabled	
	1: Charge Mode enabled	
[22:20]	Reserved	
[24:23]	Digital Virtual Probes: when the Oscilloscope Mode is enabled, each 32-bit word contains three samples (10 bits)	
	plus a trigger coding (2 bits). If the digital probes are enabled, each input sample is represented on 8 bits (input/4)	
	and 2 MSB are used for selecting digital signals. In Dual Trace, only the samples related to input signal contain	
	digital probes, while the samples related to the baseline are unchanged.	
	00: No digital probes	
	01: OverThr and GateShot	
	10: OverThr and GateLong	
	11: GateShort and GateLong	
	The OverThreshold signal sets high as the trigger is issued (when the input signal crosses the threshold	
	remains high till the input goes under the threshold.	
[31:25]	Reserved	

Tab. 1.4: CONFIG for 751 series

BUFF_ORG

Address: 0x800C Bits: [3:0]

Access Mode: Read and Write

Bit(s) Info Bit(s) Description	
[3:0]	BUFFER ORGANIZATION (Nb): each part of the channel memory is divided into buffers that contain Ne events. The single buffer size is equal to Ne times the event size. Each event can contains the time stamp information, charges +baseline information or the waveform samples (according to what is set in the CONFIG register)
	This register sets the number of buffers (according to the table below) that can be written in the channel space memory before it goes full and the acquisition is suspended. When developing a customized software, It is up to the user to set the correct number of buffers according to their data size and the on-board memory size, otherwise the DPP-PSD Control Software provided by CAEN calculates it automatically.)
	$num.buffers = 2^{Nb}$, where Nb is the value written in the register.
	Note: memory organization is described in the DPSD User Manual.
[31:4] Reserved	

Tab. 1.5: BUFF_ORG

Settable Values in the BUFF_ORG for each channel	Number of buffers
0	reserved
1	reserved
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
Α	1024

Tab. 1.6: Buffer organization table

RECORD_LENGTH

For 720 series:

Address: 0x1n20 (channel n), 0x8020 (all channels)

Bits: [11:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description	
[11:0]	CUST. SIZE: through this value the user can set the record length, that is the number of samples (Ns) in the	
Default: 0x80	waveform, according to the formula: CUST. SIZE = Ns/8 (e.g.: if 24 samples are intended to be saved, then the value	
(1024 smpls)	3 must be written in the register).	
[31:12]	Reserved	

Tab. 1.7: RECORD _LENGTH for 720 series

For 751 series:

Address: 0x1n20 (channel n), 0x8020 (all channels)

Bits: [15:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[15:0]	CUST. SIZE: through this value the user can set the record length, that is the number of samples (<i>Ns</i>) in the waveform, according to the formula: CUST. SIZE = <i>Ns</i> /12 (e.g.: if 24 samples are intended to be saved, then the
	value 2 must be written in the register).
[31:16]	Reserved

Tab. 1.8: RECORD _LENGTH for 751 series

NEV_AGGREGATE

Address: 0x1n34 (channel n), 0x8034 (all channels)

Bits: [9:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[9:0]	NR. OF EVENTS PER AGGREGATE (Ne): sets the number of events contained in one buffer (i.e. aggregate).
	Minimum value = 2.
[31:10]	Reserved

Tab. 1.9: NEV_AGGREGATE

PRE_TRG

For 720 series:

Address: 0x1n38 (channel n), 0x8038 (all channels)

Bits: [8:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[8:0]	PRE-TRIGGER: through this value the user can can set the number of samples of the pre-trigger. Since the buffer
Default: 0x64	itself is not managed as a circular buffer, it doesn't make sense to set a post-trigger as in the standard firmware. In
(400 ns)	this case, there is a delay line (FIFO) to allow for a pre-trigger.
	WARNING: $NS_{pre_trg} \ge NS_{pre_gate} + 4$; this equation must be always true.
[31:9]	Reserved

Tab. 1.10: PRE_TRG for 720 series

For 751 series:

Address: 0x1n38 (channel n), 0x8038 (all channels)

Bits: [10:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[10:0]	PRE-TRIGGER: through this value the user can set the number of samples of the pre-trigger, according to the formula: pre-trigger = PRE-TRIGGER*8 (e.g.: if a pre-trigger of 24 samples is intended to be set, then the value 3 must be written in the register). Since the buffer itself is not managed as a circular buffer, it doesn't make sense to set a post-trigger as in the standard firmware. In this case, there is a delay line (FIFO) to allow for a pre-trigger. This parameter is an integer with sign (10 bit + 1bit sign), which means that even negative pre-triggers are allowed. In this case the waveform is saved starting from a PRE-TRIGGER number of samples after the pre-trigger signal.
	NOTE: Negative pre-triggers are not managed by the DPP-PSD Control Software.
[31:11]	Reserved

Tab. 1.11: PRE_TRG for 751 series

SHORT_GATE

For 720 series:

Address: 0x1n54 (channel n), 0x8054 (all channels)

Bits: [11:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[11:0]	SHORT GATE WIDTH: sets the number of samples for the short gate integration. The gate position is referred to the
	trigger signal.
[31:12]	Reserved

Tab. 1.12: SHORT_GATE for 720 series

For 751 series:

Address: 0x1n54 (channel n), 0x8054 (all channels)

Bits: [9:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[9:0]	SHORT GATE WIDTH: sets the number of samples for the short gate integration. The gate position is referred to the
	trigger signal.
[31:10]	Reserved

Tab. 1.13: SHORT_GATE for 751 series

LONG_GATE

For 720 series:

Address: 0x1n58 (channel n), 0x8058 (all channels)

Bits: [11:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[11:0]	LONG GATE WIDTH: sets the number of samples for the long gate integration. The gate position is referred to the
	trigger signal.
[31:12]	Reserved

Tab. 1.14: LONG_GATE for 720 series

For 751 series:

Address: 0x1n58 (channel n), 0x8058 (all channels)

Bits: [9:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[9:0]	LONG GATE WIDTH: sets the number of samples for the long gate integration. The gate position is referred to the
	trigger signal.
[31:10]	Reserved

Tab. 1.15: LONG_GATE for 751 series

PRE_GATE

Address: 0x1n5C (channel n), 0x805C (all channels)

Bits: [7:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[7:0]	PRE GATE: the instant when the integration starts (also referred to as GATE OFFSET). It is expressed as number of
	samples before the trigger.
[31:8]	Reserved

Tab. 1.16: PRE_GATE

DPP_TRG_THRESHOLD (thr)

For 720 series:

Address: 0x1n60 (channel n), 0x8060 (all channels)

Bits: [11:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[11:0]	TRIGGER THRESHOLD: when the TRIGGER CONFIG in DPP_CTRL register is set to "Peak Pulse Detection" and the
Default: 0x1E	input signal crosses the TRIGGER THRESHOLD, the trigger logic gets armed; the actual trigger is then issued on the
	detected peak pulse.
	If the TRIGGER CONFIG is set to "Threshold Crossing" and the input signal crosses the TRIGGER THRESHOLD, the
	trigger logic gets armed and, at the same time, the trigger signal is issued.
[31:12]	Reserved

Tab. 1.17: DPP_TRG_THRESHOLD for 720 series

For 751 series:

Address: 0x1n60 (channel n), 0x8060 (all channels)

Bits: [9:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[9:0]	TRIGGER THRESHOLD: when the input signal crosses the TRIGGER THRESHOLD, the trigger logic gets armed and, at
	the same time, the trigger signal is issued.
[31:10]	Reserved

Tab. 1.18: DPP_TRG_THRESHOLD for 751 series

BASELINE_THRESHOLD (blthr)

For 720 series:

Address: 0x1n64 (channel n), 0x8064 (all channels)

Bits: [11:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[11:0]	BASELINE THRESHOLD: when the PEAK AVERAGING WINDOW in the DPP_CTRL register is "0", it defines the
Default: 0x03	absolute baseline value. In other cases, defines the acceptance band: when the input signal goes outside the \pm blthr
	interval, the correspondent samples are not included in the input signal baseline mean calculation. In other words,
	when {abs(baseline – signal) < blthr}, the baseline mean is calculated.
[31:12]	Reserved

Tab. 1.19: BASELINE_THRESHOLD for 720 series

For 751 series:

Address: 0x1n64 (channel n), 0x8064 (all channels)

Bits: [9:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[9:0]	BASELINE THRESHOLD: when the PEAK AVERAGING WINDOW in the DPP_CTRL register is "0", it defines the
	absolute baseline value. Otherwise, according to the numeric value set into the DPP_CTRL register, it defines the
	acceptance band: when the input signal goes outside the \pm blthr interval, the correspondent samples are not
	included in the input signal baseline mean calculation. In other words, when {abs(baseline - signal) < blthr}, the
	baseline mean is calculated.
[31:10]	Reserved

Tab. 1.20: BASELINE_THRESHOLD for 751 series

BASELINE_TIME_OUT (blTo)

Address: 0x1n68 (channel n), 0x8068 (all channels)

Bits: [7:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[7:0]	BASELINE TIME-OUT: this parameter is set to its maximum value by the firmware.
Default: 0x03	WARNING: it is recommended to the user not to modify this parameter. Please, contact support.frontend@caen.it for more details.
	support.irontend@caen.it.ror more details.
[31:8]	Reserved

Tab. 1.21: BASELINE_TIME_OUT (bITo)

DPP_CTRL

For 720 series:

Address: 0x1n80 (channel n), 0x8080 (all channels)

Bits: [24:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[1:0]	CHARGE SENSITIVITY: this parameter defines how many LSB are thrown away (i.e. right shift) before the charge is
0x00000003	saved into the memory buffer; this corresponds to a division by $N = 2^n$, where n is the charge sensitivity:
Default: 0	00: 40 fC/LSB (N = 1)
	01 : 160 fC/LSB (N = 2)
	10 : 640 fC/LSB (N = 3)
	11: 2.5 pC/LSB (N = 4)
[15:2]	Reserved
[16]	PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be
0x00010000	digitally inverted inside the FPGA before to apply the DPP algorithms:
Default: 1	0: The digital signal is inverted (analog signals are positive)
	1: The digital signal is not inverted (analog signals are negative)
[17]	TRIGGER CONFIG.: sets the trigger issuing mode once the input signals crosses the trigger threshold (THRESHOLD):
0x00020000	0: Peak pulse detection (the trigger is issued when the peak pulse is detected)
Default: 0	1: Threshold crossing (the trigger is issued when the input pulse crosses the trigger threshold)
[19:18]	Reserved
[22:20]	PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter:
0x00700000	000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the
Default: 2	BASELINE_THRESHOLD (bithr) register).
	001: 4 samples
	010: 8 samples
	011: 16 samples
	100: 32 samples
	101: 64 samples
	110: 128 samples
[23]	Reserved
[24]	SELF-TRIGGER: enables/disables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is
Default: 0	still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the
	TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external
	trigger (input on the front panel TRG IN) is sent to the digitizer.
	WARNING: this is an active low bit.
	0: Self-trigger enabled
	1: Self-trigger disabled
[31:25]	Reserved

Tab. 1.22: DPP_CTRL for 720 series

For 751 series:

Address: 0x1n80 (channel n), 0x8080 (all channels)

Bits: [24:0]

Access Mode: Read and Write

CHARGE SENSITIVITY: this parameter defines how many LSB are thrown away (i.e. right shift) before the charge is saved into the memory buffer; this corresponds to a division by N = 2°, where n is the charge sensitivity: O00: 20 fc/LSB (N = 1) O01: 40 fc/LSB (N = 2) O10: 80 fc/LSB (N = 3) O11: 160 fc/LSB (N = 4) 100: 320 fc/LSB (N = 5) O11: 640 fc/LSB (N = 6) (I5:3] Reserved O15: PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: O: The digital signal is inverted (analog signals are positive) 1: The digital signal is inverted (analog signals are negative) O16: Reserved O22: O20 PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: dos (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (bithr) register). O01: 8 samples O10: 16 samples O11: 32 samples O10: 64 samples O11: 128 samples O10: 256 samples O11: 128 samples O10: 256 samples O11: 128 samples O12: 351 samples O13: 351 samples O14: 352 samples O15: 4 samples O16: 512 samples O17: 512 samples O18: 512 samples O19: 64 samples O19: 64 samples O19: 70: 70: 70: 70: 70: 70: 70: 70: 70: 70	Bit(s) Info	Bit(s) Description
000: 20 fC/LSB (N = 1) 001: 40 fC/LSB (N = 2) 010: 80 fC/LSB (N = 3) 011: 160 fC/LSB (N = 4) 100: 320 fC/LSB (N = 5) 101: 640 fC/LSB (N = 5) 101: 640 fC/LSB (N = 5) 101: 640 fC/LSB (N = 6) [15:3] Reserved [16] PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: 0: The digital signal is inverted (analog signals are positive) 1: The digital signal is not inverted (analog signals are negative) [19:17] Reserved [22:20] PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD blithr) register). 001: 8 samples 010: 16 samples 010: 16 samples 101: 128 samples 100: 64 samples 101: 128 samples 110: 256 samples 111: 512 samples 123] Reserved [23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.	[2:0]	CHARGE SENSITIVITY: this parameter defines how many LSB are thrown away (i.e. right shift) before the charge is
001: 40 fC/LSB (N = 2) 010: 80 fC/LSB (N = 3) 011: 160 fC/LSB (N = 4) 100: 320 fC/LSB (N = 5) 101: 640 fC/LSB (N = 6) [15:3] Reserved [16] PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: 0: The digital signal is inverted (analog signals are positive) 1: The digital signal is inverted (analog signals are negative) [19:17] Reserved [22:20] PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (blthr) register). 001: 8 samples 010: 16 samples 010: 16 samples 110: 256 samples 110: 256 samples 110: 256 samples 111: 512 samples 123] Reserved [23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		saved into the memory buffer; this corresponds to a division by $N = 2^n$, where n is the charge sensitivity:
o10: 80 fC/LSB (N = 3) o11: 160 fC/LSB (N = 4) 100: 320 fC/LSB (N = 5) 101: 640 fC/LSB (N = 6) [15:3] Reserved [16] PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: 0: The digital signal is inverted (analog signals are positive) 1: The digital signal is not inverted (analog signals are negative) [19:17] Reserved [22:20] PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 00: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (bithr) register). 001: 8 samples 010: 16 samples 010: 16 samples 110: 256 samples 110: 256 samples 111: 512 samples 123] Reserved [23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		000: 20 fc/LSB (N = 1)
o11: 160 fC/LSB (N = 4) 100: 320 fC/LSB (N = 5) 101: 640 fC/LSB (N = 6) [15:3] Reserved [16] PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: 0: The digital signal is inverted (analog signals are positive) 1: The digital signal is not inverted (analog signals are negative) [19:17] Reserved [22:20] PFAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (bithr) register). 001: 8 samples 010: 16 samples 010: 48 samples 110: 42 samples 110: 42 samples 110: 456 samples 110: 456 samples 111: 512 samples 123] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger abled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		001: 40 fC/LSB (N = 2)
100: 320 fC/LSB (N = 5) 101: 640 fC/LSB (N = 6) 15:3 Reserved PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: 0: The digital signal is inverted (analog signals are positive) 1: The digital signal is not inverted (analog signals are negative) 1: The digital signal is not inverted (analog signals are negative) 1: The digital signal is not inverted (analog signals are negative) 1: The digital signal is not inverted (analog signals are negative) 1: The digital signal is not inverted (analog signals are negative) 1: The digital signal is not inverted (analog signals are negative) 1: The digital signal is not inverted (analog signals are negative) 1: The digital signal is not inverted (analog signals are negative) 1: The digital baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (bithr) register).		010 : 80 fC/LSB (N = 3)
101: 640 fC/LSB (N = 6) Reserved		011: 160 fC/LSB (N = 4)
[15:3] Reserved PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: 0:		100: 320 fC/LSB (N = 5)
PULSE POLARITY: the DPP-PSD algorithm is designed to work with negative pulses. The input signal polarity can be digitally inverted inside the FPGA before to apply the DPP algorithms: 0: The digital signal is inverted (analog signals are positive) 1: The digital signal is not inverted (analog signals are negative) 19:17 Reserved PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (bithr) register). 001: 8 samples 010: 16 samples 010: 16 samples 110: 22 samples 110: 22 samples 110: 128 samples 111: 512 samples 112: 512 samples 113: 512 samples 114: 512 samples 115: 512 samples 116: 356 samples 117: 512 samples 118: 512 samples 119: 512 samples 119: 512 samples 110: 256 samples 111: 512 samples 111: 512 samples 112: 512 samples 113: 512 samples 114: 512 samples 115: 512 samples 116: 512 samples 117: 512 samples 118: 512 samples 119: 512 samples 119: 512 samples 110: 256 samples 111: 512 samples 111: 512 samples 112: 512 samples 113: 512 samples 114: 512 samples 115: 512 samples 116: 512 samples 117: 512 samples 118: 512 samples 119: 512 samples 119: 512 samples 110: 512 samples 110: 512 samples 110: 512 samples 111: 512 samples 112: 512 samples 113: 512 samples 114: 512 samples 115: 512 samples 116: 512 samples 117: 512 samples 118: 512 samples 119: 512 samples 119: 512 samples 110: 5		101: 640 fC/LSB (N = 6)
digitally inverted inside the FPGA before to apply the DPP algorithms: 0: The digital signal is inverted (analog signals are positive) 1: The digital signal is inverted (analog signals are positive) [19:17] Reserved [22:20] PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (blthr) register). 001: 8 samples 010: 16 samples 011: 32 samples 100: 64 samples 101: 128 samples 101: 128 samples 102: 256 samples 111: 512 samples [23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.	[15:3]	Reserved
19:17 Reserved PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (bithr) register).	[16]	
1: The digital signal is not inverted (analog signals are negative) [19:17] Reserved [22:20] PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (blthr) register). 001: 8 samples 010: 16 samples 010: 64 samples 100: 64 samples 101: 128 samples 101: 128 samples 102: 256 samples 111: 512 samples [23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		
[19:17] Reserved [22:20] PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (blthr) register). 001: 8 samples 010: 16 samples 011: 32 samples 100: 64 samples 101: 128 samples 110: 256 samples 111: 512 samples 123] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		
PEAK AVERAGING WINDOW: defines the number of samples to calculate the input signal baseline by a mean filter: 000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (blthr) register). 001: 8 samples 010: 16 samples 011: 32 samples 100: 64 samples 101: 128 samples 110: 256 samples 111: 512 samples 123] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		
000: abs (in this case the mean filter is disabled and a fixed baseline value can be set in the BASELINE_THRESHOLD (blthr) register). 001: 8 samples 010: 16 samples 101: 32 samples 100: 64 samples 110: 256 samples 111: 512 samples 123] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		
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101: 128 samples 110: 256 samples 111: 512 samples [23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		·
110: 256 samples 111: 512 samples [23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		
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[23] Reserved [24] SELF-TRIGGER DISABLE: disables/enables the self-trigger (i.e. auto trigger) inside the DPP. If the self-trigger is disabled, it is still generated, but the channels doesn't acquire the input signal. The generated trigger is provided out through the TRG OUT output port on the digitizer front panel. The channel can acquire the input signal only in case an external trigger (input on the front panel TRG IN) is sent to the digitizer. WARNING: this is an active high bit. 1: Self-trigger disabled 0: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		
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O: Self-trigger enabled NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		WARNING: this is an active high bit.
NOTE: in the DPP-PSD Control Software the self-trigger configuration is not managed: the Self-Trigger is always enabled.		1: Self-trigger disabled
enabled.		
		55 5 5
	[31:25]	

Tab. 1.23: DPP_CTRL for 751 series

AMC_FIRMWARE_REVISION

Address: 0x1n8C (channel n)

Bits: [31:0] Access Mode: Read Only

Firmware revision and build date of the AMC FPGA (i.e. the channel FPGA).

Bit(s) Info	Bit(s) Description
[7:0]	Firmware minor revision: This field is the firmware minor revision number.
0x000000FF	
[15:0]	Firmware major revision: This field is the firmware major revision number.
0x0000FF00	
[19:16]	Build Day (lower digit).
[23:20]	Build Day (upper digit).
[27:24]	Build Month. Es.: 3: March; 10: October.
[31:28]	Build Year. Es.: 0: 2000; 12: 2012.
0xFFFF0000	

Tab. 1.24: AMC_FIRMWARE_REVISION

Example:

0xC3218303 firmware revision must be interpreted as follows:

- Firmware revision is 131.3
- Build Year is 2012
- Build Month is March
- Build Day is 21

DC_OFFSET

Address: 0x1n98 (channel n), 0x8098 (all channels)

Bits: [15:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[15:0]	DAC data configuration: This field is the fixed value (in LSB) to add to the input signal for the input channel DC
0x0000FFFF	Offset adjustment.
Default: 0x8000	
[31:15]	Reserved.

Tab. 1.25: DC_OFFSET

ACQUISITION_CONTROL

Address: 0x8100 Bits: [5:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[1:0]	Start/Stop Mode.
0x00000003	00: SW controlled. Start and Stop of Run take place on SW command, that is by setting/resetting bit[2].
Default: 0	01: S-IN controlled. If the acquisition is armed (bit 2 = 1), the run starts when S-IN is asserted and stops when
	SIN returns inactive. If bit[2] = 0, the acquisition is always off.
	10: First Trigger. If the acquisition is armed (bit[2] = 1), the run starts on the first trigger pulse (rising edge on
	TRGIN); this pulse is not used as trigger, actual triggers start from the second pulse. The stop of run must be SW
	controlled (reset of Bit[2]).
	11: Reserved.
[2]	Acquisition Start or Arm: When bits[1:0] = 00, this bit acts as a run start/stop (0=stopped, 1=running);
0x00000004	when bits[1:0] = 01, 10, 11, this bit arms the acquisition (0=disarmed, 1=armed); the actual start/stop is controlled
Default: 0	by an external signal, as described above.
[5:3]	Reserved
[6]	PLL reference clock source (only in Desktop and NIM modules).
	0: Internal Oscillator.
	1: External clock on front panel CLK-IN.
	Note: In VME modules this settings is made through a hardware switch on the board.
[31 7]	Reserved.

Tab. 1.26: ACQUISITION_CONTROL

ACQUISITION_STATUS

Address: 0x8104
Bits: [31:0]
Access Mode: Read Only

[0] Reserved.	Bit(s) Info	Bit(s) Description
[2] 0x00000004 0: Acquisition is stopped. 1: Acquisition is running. [3] Event Ready: It indicates availability of events from one of the channels. 0x00000008 0: There are no events stored in one of the acquisition buffers of any of the board channels. 1: There are re events stored in one of the acquisition buffers of any of the board channels. 1: There are no events stored in one of the acquisition buffers of any of the board channels. 1: There are re events stored in one of the acquisition buffers of any of the board channels. 1: There are no events stored in one of the acquisition buffers of any of the board channels. 1: There are events stored in one of the acquisition buffers of any of the board channels. 1: Acquisition Full: Acquisition memory full condition. 1: At least one channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. PLL Reference: PLL reference frequency. 0: PLL uses the internal oscillator (50 MHz) as a reference. 1: PLL uses the external clock as a reference. 1: PLL bypass: PLL Bypass state. 0: PLL is not bypassed. 1: PLL into bypassed. 1: PLL into bypassed. 1: PLL bypassed: the VCXO frequency directly drive the clock distribution tree. 1: PLL unlock flag. 0: PLL unlock flag. 0: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since th	[0]	Reserved.
Ox00000004 O: Acquisition is stopped. 1: Acquisition is running.	[1]	Reserved.
1: Acquisition is running. 3 Symmo Ready: It indicates availability of events from one of the channels. 0: There are no events stored in one of the acquisition buffers of any of the board channels. 1: There are events stored in one of the acquisition buffers of any of the board channels. 1: There are events stored in one of the acquisition buffers of any of the board channels. 1: There are events stored in one of the acquisition buffers of any of the board channels. 1: No channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. 1: PLL Reference: PLL reference frequency. 0: PLL uses the internal oscillator (50 MHz) as a reference. 1: PLL bypass: PLL Bypass state. 0: PLL bypassed: the VCXO frequency directly drive the clock distribution tree. 1: PLL bypassed: the VCXO frequency directly drive the clock distribution tree. 1: PLL bash ad an unlock condition since the last register read access. 1: PLL hash't had any unlock condition since the last register read access. 1: PLL hash't had any unlock condition since the last register read access. 1: PLL hash't had any unlock condition since the last register read access. 1: PLL bypass't had any unlock condition since the last register read access. 1: PLL bypas't had any unlock condition since the last register read access. 1: PLL bypas't had any unlock condition since the last register read access. 1: PLL bypas't had any unlock condition since the last register read access. 1: PLL bypas't had any unlock condition since the last register read access. 1: PLL bypas't had any unlock condition since the last register read access. 1: PLL bypas't had any unlock condition since the last register read access. 1: PLL bypas't had any unlock condition since the last register read access. 1: PLL bypas't had any unl	[2]	Acquisition status: It reflects the status of the acquisition.
[3] Event Ready: It indicates availability of events from one of the channels. 0: There are no events stored in one of the acquisition buffers of any of the board channels. 1: There are events stored in one of the acquisition buffers of any of the board channels. Acquisition Full: Acquisition memory full state. 0: No channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. [5] PLL Reference: PLL reference frequency. 0: PLL uses the internal oscillator (50 MHz) as a reference. 1: PLL uses the external clock as a reference. [6] PLL Bypass: PLL Bypass state. 0: PLL is not bypassed. 1: PLL has had an unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Ox00001000 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. 1: Board is ready to start acquisition. 1: Board is ready to start acquisition. 0: Channel firmware is licensed. Time bomb is not active. 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [15] Ox00000000 [16] Reserved. TRG-IN Status: Read current logical level on S-IN input.	0x00000004	0: Acquisition is stopped.
Ox00000008 C.		1: Acquisition is running.
1: There are events stored in one of the acquisition buffers of any of the board channels. [4] Acquisition Full: Acquisition memory full state. 0: No channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. [5] PLL Reference: PLL reference frequency. 0: PLL uses the internal oscillator (50 MHz) as a reference. 1: PLL uses the external clock as a reference. [6] Ox00000040 0: PLL Bypass: PLL Bypass state. 0: PLL is not bypassed. 1: PLL us bypassed: the VCXO frequency directly drive the clock distribution tree. [7] PLL Unlock Detect: PLL unlock flag. 0x00000080 0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0x00000100 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. 0x00000200 0x00000200 0x00000200 0x00000000	[3]	Event Ready: It indicates availability of events from one of the channels.
[4] Acquisition Full: Acquisition memory full state. 0: No channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. [5] PLL Reference: PLL reference frequency. 0: PLL uses the internal oscillator (50 MHz) as a reference. 1: PLL uses the external clock as a reference. 0: PLL bypass: PLL Bypass state. 0: PLL is bypassed. 1: PLL is bypassed. 1: PLL is bypassed: the VCXO frequency directly drive the clock distribution tree. [7] PLL Unlock Detect: PLL unlock flag. 0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. 1: Board is ready to start acquisition. 1: Board is ready to start acquisition. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] Ox00000000 [16] TRG-IN Status: Read current logical level on TRG-IN input.	0x00000008	0: There are no events stored in one of the acquisition buffers of any of the board channels.
O: No channel has reached a memory full condition. 1: At least one channel has reached a memory full condition. 5 PLL Reference: PLL reference frequency. Ox000000200 O: PLL uses the internal oscillator (50 MHz) as a reference. 1: PLL uses the external clock as a reference. Ox00000040 O: PLL is not bypassed. 1: PLL is bypassed: the VCXO frequency directly drive the clock distribution tree. 7 PLL Unlock Detect: PLL unlock flag. Ox00000080 O: PLL hasn't had any unlock condition since the last register read access. Ox00000080 O: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. 8 Board Ready: Board readiness for acquisition. O: Board is not ready to start acquisition. O: Board is ready to start acquisition. Ox00000200 O: Channel firmware is licensed. Time bomb is not active. Default: O		1: There are events stored in one of the acquisition buffers of any of the board channels.
Seeved Status: Read current logical level on TRG-IN input.	[4]	Acquisition Full: Acquisition memory full state.
S Ox00000020 O: PLL uses the internal oscillator (50 MHz) as a reference.		0: No channel has reached a memory full condition.
0: PLL uses the internal oscillator (50 MHz) as a reference. [6] PLL Bypass: PLL Bypass state. 0x00000040 0: PLL is not bypassed. 1: PLL is bypassed: the VCXO frequency directly drive the clock distribution tree. [7] PLL Unlock Detect: PLL unlock flag. 0x00000080 0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. 5-IN Status: Read current logical level on S-IN input. 7-RG-IN Status: Read current logical level on TRG-IN input.		1: At least one channel has reached a memory full condition.
Seerved. 1: PLL uses the external clock as a reference.	[5]	PLL Reference: PLL reference frequency.
[6] PLL Bypass: PLL Bypass state. 0: PLL is not bypassed. 1: PLL is bypassed: the VCXO frequency directly drive the clock distribution tree. [7] PLL Unlock Detect: PLL unlock flag. 0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0x00000200 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. 5-IN Status: Read current logical level on S-IN input. Reserved.	0x00000020	0: PLL uses the internal oscillator (50 MHz) as a reference.
0: PLL is not bypassed. 1: PLL is bypassed: the VCXO frequency directly drive the clock distribution tree. [7] PLL Unlock Detect: PLL unlock flag. 0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. 1: Board is ready to start acquisition. 0: Channel firmware is licensed. Time bomb is not active. 0-Efault: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. S-IN Status: Read current logical level on S-IN input. TRG-IN Status: Read current logical level on TRG-IN input.		1: PLL uses the external clock as a reference.
1: PLL is bypassed: the VCXO frequency directly drive the clock distribution tree. [7] PLL Unlock Detect: PLL unlock flag. 0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. S-IN Status: Read current logical level on S-IN input. TRG-IN Status: Read current logical level on TRG-IN input.	[6]	PLL Bypass: PLL Bypass state.
[7] PLL Unlock Detect: PLL unlock flag. 0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. S-IN Status: Read current logical level on S-IN input. TRG-IN Status: Read current logical level on TRG-IN input.	0x00000040	0: PLL is not bypassed.
0: PLL has had an unlock condition since the last register read access. 1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. TRG-IN Status: Read current logical level on TRG-IN input.		1: PLL is bypassed: the VCXO frequency directly drive the clock distribution tree.
1: PLL hasn't had any unlock condition since the last register read access. Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. TRG-IN Status: Read current logical level on TRG-IN input. [31:17] Reserved.	[7]	PLL Unlock Detect: PLL unlock flag.
Note: In normal functioning it must be always read 1. [8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. 7RG-IN Status: Read current logical level on TRG-IN input. 8Reserved. 1: Reserved.	0x00000080	0: PLL has had an unlock condition since the last register read access.
[8] Board Ready: Board readiness for acquisition. 0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. 7 TRG-IN Status: Read current logical level on TRG-IN input. 8 Reserved. 1 TRG-IN Status: Read current logical level on TRG-IN input.		1: PLL hasn't had any unlock condition since the last register read access.
0: Board is not ready to start acquisition. 1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. TRG-IN Status: Read current logical level on TRG-IN input. Reserved. [31:17] Reserved.		Note: In normal functioning it must be always read 1.
1: Board is ready to start acquisition. [9] Time Bomb Status: Time bomb expiration status. 0: Channel firmware is licensed. Time bomb is not active. Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. [16] TRG-IN Status: Read current logical level on TRG-IN input. [31:17] Reserved.	[8]	Board Ready: Board readiness for acquisition.
[9] Time Bomb Status: Time bomb expiration status. 0x00000200 Default: 0 1: Channel firmware is licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. 0x00008000 [16] TRG-IN Status: Read current logical level on TRG-IN input. 7 Reserved. Reserved. Reserved.	0x00000100	0: Board is not ready to start acquisition.
0: Channel firmware is licensed. Time bomb is not active. 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. [16] TRG-IN Status: Read current logical level on TRG-IN input. [31:17] Reserved.		1: Board is ready to start acquisition.
Default: 0 1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes. [14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. [16] TRG-IN Status: Read current logical level on TRG-IN input. [31:17] Reserved.	[9]	Time Bomb Status: Time bomb expiration status.
[14:10] Reserved. [15] S-IN Status: Read current logical level on S-IN input. 0x00008000 [16] 0x00010000 TRG-IN Status: Read current logical level on TRG-IN input. [31:17] Reserved.	0x00000200	0: Channel firmware is licensed. Time bomb is not active.
[15] S-IN Status: Read current logical level on S-IN input. 0x00008000 TRG-IN Status: Read current logical level on TRG-IN input. 0x00010000 Reserved.	Default: 0	1: Channel firmware is not licensed. Time bomb will expire within a maximum time of 30 minutes.
0x00008000 TRG-IN Status: Read current logical level on TRG-IN input. 0x00010000 Reserved.	[14:10]	Reserved.
[16] TRG-IN Status: Read current logical level on TRG-IN input. 0x00010000 [31:17] Reserved.	[15]	S-IN Status: Read current logical level on S-IN input.
0x00010000 [31:17] Reserved.	0x00008000	
[31:17] Reserved.	[16]	TRG-IN Status: Read current logical level on TRG-IN input.
(*)	0x00010000	
0xFFFE0000	[31:17]	Reserved.
	0xFFFE0000	

Tab. 1.27: ACQUISITION_STATUS

SOFTWARE_TRIGGER

Address: 0x8108
Bits: [31:0]
Access Mode: Write Only

An access to this register, with any value, generates a software trigger. If this trigger source is enabled and acquisition is running a new global trigger will be generated towards all board channels at the same time.

GLOBAL_TRIGGER_MASK

Address: 0x810C Bits: [31:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description	
[0]	Channel O Trigger Enable.	
0x00000001	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[1]	Channel 1 Trigger Enable.	
0x00000002	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[2]	Channel 2 Trigger Enable.:	
0x00000004	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[3]	Channel 3 Trigger Enable.	
0x00000008	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[4]	Channel 4 Trigger Enable.	
0x00000010	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[5]	Channel 5 Trigger Enable.	
0x00000020	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[6]	Channel 6 Trigger Enable.	
0x00000040	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[7]	Channel 7 Trigger Enable.	
0x00000080	0: Channel trigger out is not sensed for global trigger generation.	
Default: 0	1: Channel trigger out generates a global trigger.	
[29:8]	Reserved.	
[30]	External Trigger Enable.	
0x40000000	0: External triggers are disabled.	
Default: 1	1: External trigger generates a board global trigger.	
[31]	Software Trigger Enable.	
0x80000000	0: Software triggers are disabled.	
Default: 1	1: Software trigger generates a board global trigger.	

Tab. 1.28: GLOBAL_TRIGGER_MASK

TRIGGER_OUT_MASK

Address: 0x8110 Bits: [31:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[0]	Channel 0 Trigger Enable.
0x00000001	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[1]	Channel 1 Trigger Enable.
0x00000002	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[2]	Channel 2 Trigger Enable.
0x00000004	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[3]	Channel 3 Trigger Enable.
0x00000008	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[4]	Channel 4 Trigger Enable.
0x00000010	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[5]	Channel 5 Trigger Enable.
0x00000020	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[6]	Channel 6 Trigger Enable.
0x00000040	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[7]	Channel 7 Trigger Enable.
0x00000080	0: Channel trigger out is not propagated to TRG-OUT signal (front panel).
Default: 0	1: Channel trigger out is propagated to TRG-OUT signal (front panel) through a logical OR with other enabled
	trigger sources.
[29:8]	Reserved.
[30]	External Trigger Enable.
0x40000000	0: External trigger (TRG-IN front panel signal) is not propagated to TRG-OUT.
Default: 1	1: External trigger (TRG-IN front panel signal) is propagated to TRG-OUT.
[31]	Software Trigger Enable.
0x80000000	0: Software trigger is not propagated to TRG-OUT.
Default: 1	1: Software trigger is propagated to TRG-OUT.

Tab. 1.29: TRIGGER_OUT_MASK

LVDS_DATA

Address: 0x8118 Bits: [31:0]

Access Mode: Read and Write

Read/Write front panel LVDS I/O logical state if the pin is configured as general purpose input/output (see pag. 23). A write operation sets the corresponding pin logical states if configured as output. A read operation returns the state of the corresponding pins.

Bit(s) Info	Bit(s) Description
[0]	LVDS I/O [0].
[1]	LVDS I/O [1].
[2]	LVDS I/O [2].
[3]	LVDS I/O [3].
[4]	LVDS I/O [4].
[5]	LVDS I/O [5].
[6]	LVDS I/O [6].
[7]	LVDS I/O [7].
[8]	LVDS I/O [8].
[9]	LVDS I/O [9].
[10]	LVDS I/O [10].
[11]	LVDS I/O [11].
[12]	LVDS I/O [12].
[13]	LVDS I/O [13].
[14]	LVDS I/O [14].
[15]	LVDS I/O [15].
[31:16]	Reserved.

Tab. 1.30: LVDS_DATA

FRONT_PANEL_CONTROL

Address: 0x811C Bits: [31:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[0]	LEMO I/Os (TRG-IN, TRG-OUT/GPO, S-IN/GPI) Electrical Levels.
0x00000001	0: NIM.
Default: 0	1: TTL.
[1]	LVDS GPIO Output Enable.
0x00000002	0: Enabled.
Default: 0	1: High impedance.
Delauit. 0	Note: the output enable is meaningful only for the GPIOs that are used as outputs according to bits [5:2].
[2]	LVDS GPIO[3:0] direction.
0x00000004	0: Input.
Default: 0	1: Output.
[3]	LVDS GPIO[7:4] direction.
0x00000008	0: Input.
Default: 0	1: Output.
[4]	LVDS GPIO[11:8] direction.
0x00000010	0: Input.
Default: 0	1: Output.
	LVDS GPIO[15:12] direction.
[5] 0x00000020	
Default: 0	0: Input. 1: Output.
[8:6]	1: Output. LVDS GPIO mode.
0x000001C0	
	(14)
Default: 0	Front Panel IO Data at address 0x8118.
	001: Predefined IO settings (see the table below).
	010: Trigger pattern: all GPIOs are used as input and their value is latched at the arrival of the trigger and
	saved in the event header in place of the trigger time tag.
	011: Individual trigger In-Out: GPIO[7:0] = TrgOut from channels; GPIO[15:8] = TrgIn to channels. NOTE: bit 2
	of the Channel Config Register (at address 0x8000) must be enabled.
	100: Reserved.
	101: Reserved.
	110: Reserved.
[0]	111: Reserved.
[9]	Trigger Pattern Mode: Selects when pattern is latched.
0x00000200	0: Pattern is latched when the (internal) global trigger is sent to channels, as a consequence of an external
Default: 0	trigger. It accounts for post trigger settings and input latching delays.
[40,40]	1: Pattern is latched when the external trigger arrives.
[13:10]	Reserved.
[14]	Force TRG-OUT (VME) / GPO (Desktop-NIM): Sets TRG-OUT logical level, if TRG-OUT test mode (see bit[15]) is
0x00004000	enabled.
Default: 0	0: Force TRG-OUT to 0.
F 3	1: Force TRG-OUT to 1.
[15]	TRG-OUT (VME) / GPO (Desktop-NIM) Test Mode.
0x00008000	0: TRG-OUT test mode disabled.
Default: 0	1: TRG-OUT test mode enabled.
[17:16]	TRG-OUT (VME) / GPO (Desktop-NIM) Mode.
0x00030000	00: TRG-OUT/GPO propagates the internal trigger sources according to the Trigger_Out_Mask Register
Default: 0	(0x8110).
	01: TRG-OUT/GPO is used to propagate signals of the Mother Board, according to the bits [19:18] of this
	register (Common Signals Virtual Probe).
	10: TRG-OUT/GPO is used to propagate signals of the Daughter boards (Channel Signals Virtual Probe).
[40,40]	11: Reserved.
[19:18]	Common Signal Virtual Probe (propagated onto TRG-OUT (VME) / GPO (Desktop-NIM)): this bit are meaningful
0x000C0000	only when bits[17:16] = 01.
Default: 0	00: RUN: the signal is active when the acquisition is running. This option can be used to synchronize the
	start/stop of the acquisition through the TRGOUT/GPO -> TRGIN or TRGOUT/GPO -> SIN/GPI daisy chain.
	01: Trigger Sampling CLK (125 MHz). This clock is synchronous with the sampling clock of the ADC and this
	option can be used to align the phase of the clocks in different boards.
	10: Trigger Reference CLK (62.5 MHz)). This clock is synchronous with the sampling clock of the ADC and this
	option can be used to align the phase of the clocks in different boards.
re :	11: Reserved.
[31:20]	Reserved.
	PANEL CONTROL

Tab. 1.31: FRONT_PANEL_CONTROL

Predefined GPIO setting (GPIO Mode = 001):

GPIO	Direction	Function		
[7:0]	out	Individual Trigger Outputs from channels		
[8]	[8] out Memory Full			
[9]	out Event Data Ready			
[10]	out	Global trigger		
[11]	[11] out Acquisition Run Status [12] in Time Tag Reset			
[12]				
[13]	in Memory clear			
[14] in Reserved [15] in Reserved		Reserved		
		Reserved		

Tab. 1.32: Predefined GPIO setting (GPIO Mode = 001)

Individual TrgIn/TrgOut mode (GPIO Mode = 011):

	GPIO	Direction	Function
	[7:0]	out	Individual Trigger Outputs from channels
Ì	[15:8]	in	Individual Trigger Inputs to channels

Tab. 1.33: Individual TrgIn/TrgOut mode (GPIO Mode = 011)

CHANNEL_ENABLE_MASK

Address: 0x8120 Bits: [31:0]

Access Mode: Read and Write

Sets a channel enable mask to enable selected channel to participate to events readout.

This register MUST not be changed while the acquisition is started.

Bit(s) Info	Bit(s) Description	
[0]	Channel 0 Enable.	
0x00000001	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[1]	Channel 1 Enable.	
0x00000002	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[2]	Channel 2 Enable.	
0x00000004	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[3]	Channel 3 Enable.	
0x00000008	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[4]	Channel 4 Enable.	
0x00000010	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[5]	Channel 5 Enable.	
0x00000020	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[6]	Channel 6 Enable.	
0x00000040	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[7]	Channel 7 Enable.	
0x00000080	0: This channel doesn't contribute to events.	
Default: 1	1: This channel contribute to events.	
[31:8]	Reserved.	
0xFFFFFF00		
Default: 0		

Tab. 1.34: CHANNEL_ENABLE_MASK

ROC_FIRMWARE_REVISION

Address: 0x8124
Bits: [31:0]
Access Mode: Read Only

Firmware revision and build date of the ROC FPGA (i.e. the interface FPGA).

Bit(s) Info	Bit(s) Description
[7:0]	Firmware minor revision: This field is the firmware minor revision number.
0x000000FF	
[15:0]	Firmware major revision: This field is the firmware major revision number.
0x0000FF00	
[19:16]	Build Day (lower digit).
[23:20]	Build Day (upper digit).
[27:24]	Build Month. Es.: 1: January; 12: December.
[31:28]	Build Year. Es.: 0: 2000; 15: 2015.
0xFFFF0000	

Tab. 1.35: FIRMWARE_REVISION

Example:

0xB5120302 firmware revision must be interpreted as follows:

- Firmware revision is 3.2
- Build Year is 2011
- Build Month is May
- Build Day is 12

MONITOR DAC CONTROL

Address: 0x8138 Bits: [31:0]

Access Mode: Read and Write

Sets Monitor DAC value when it is configured to generate a programmable voltage level.

This register is only significant for V1720. Desktop/NIM devices doesn't mount the programmable DAC.

Bit(s) Info	Bit(s) Description
[11:0]	DAC Voltage Setting = N.
0x00000FFF	DAC Output voltage = N * 0.244 Volt.
Default: 0	
[31:12]	Reserved.
0xFFFFFC00	

Tab. 1.36: MONITOR_DAC_CONTROL

SW_CLOCK_SYNC

Address: 0x813c
Bits: [31:0]
Access Mode: Write Only

A write access to this register, with any data, forces the PLL to re-align all the clock outputs with the reference clock. In case of daisy chain clock distribution between boards, during the initialization and configuration, the reference clocks along the daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLKIN and the internal clocks. **NOTE:** the command must be issued starting from the first to the last board in the clock chain.

BOARD_INFO

Address: 0x8140
Bits: [31:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Digitizers Family Code: It must be 0x03 for 720 digitizer series and 0x05 for 751 digitizer series.
0x00000FF	
Default: 0	
[15:8]	Channel Memory Size Code.
0x0000FF00	2: Each channel is equipped with 1.25 MS/ch acquisition memory (in case of 720 series) or 1.8/3.6 MS/ch (in case of 751 series)
	16 (0x10): Each channel is equipped with 10 MS/ch acquisition memory (in case of 720 series) or 14.4/28.8 MS/ch (in case of 751).
[23:16]	Equipped Channels Number: It gives the number of channels equipped on the board. If this number is lower than
0x00FF0000	physical channels, there could be a communication problem with some of the channel mezzanines.
[31:24]	Reserved.
0xFF000000	

Tab. 1.37: BOARD_INFO

MONITOR_DAC_MODE

Address: 0x8144 Bits: [31:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description	
[2:0]	Analog Monitor Output Mode.	
0x0000007	001: Test Mode. A full-scale (1Vpp) saw- tooth is generated by the internal DAC.	
Default: 0	100: Voltage Level Mode.	
	Others: Reserved.	
[31:3]	Reserved.	
0xFFFFFF8		

Tab. 1.38: MONITOR_DAC_MODE

EVENT_SIZE

Address: 0x814C Bits: [31:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[31:0]	Event Size (in 32-bit words): It represents the current available event size in 32-bit words.
0xFFFFFFF	The value is updated after complete readout of each event.
Default: 0	

Tab. 1.39: EVENT_SIZE

TIME_BOMB_DOWNCOUNTER

Address: 0x8158
Bits: [31:0]
Access Mode: Read Only

This is a down counter value. If the value is constant, the firmware time bomb license is not enabled: the current module firmware is enabled without any time limitation. If the value is decreasing, the firmware will stop working (no possibility to enter RUN mode) after 30 minutes after module power-on.

If the value is 0, the time bomb has expired, and module is not allowed to enter RUN mode without module power cycle.

RUN_START_STOP_DELAY

Address: 0x8170 Bits: [31:0]

Access Mode: Read and Write

When the start of run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the start (or stop) signal through the chain. This register sets the delay (expressed in trigger clock cycles) between the arrival of the start signal at the input of the board (either SIN or TRGIN) and the actual start of run. The delay is usually zero for the last board in the chain and rises going backward along the chain.

VETO

Address: 0x817C Bits: [31:0]

Access Mode: Read and Write

Bit(s) Info		Bit(s) Description
[0]	External trigger veto:	
Default: 0	0:	External trigger enabled.
	1:	External trigger disabled (veto).
[31:1]	Reserved.	

Tab. 1.40: VETO

READOUT_CONTROL

Address: 0xEF00 Bits: [15:0]

Access Mode: Read and Write

This register is mainly significant for VME modules. Some bit is anyway applicable even to non-VME modules.

Bit(s) Info	Bit(s) Description		
[2:0]	VME Interrupt Level (applicable to VME modules only): Sets VME interrupt Level (1-7). If set to 0, VME interrup		
0x0007	are disabled.		
Default: 0			
[3]	Optical Link Interrupt Enable: Enable interrupt generation over CONET2 optical link.		
0x0008	0: Interrupts disabled.		
Default: 0	1: Interrupts enabled.		
[4]	VME Bus Error / Event Aligned Readout Enable.		
0x0010	0: VME Bus Error/ Event Aligned Readout disabled.		
Default: 0	1: VME Bus Error/ Event Aligned Readout enabled.		
[5]	VME Align64 Mode (applicable to VME modules only).		
0x0020	0: 64 bit aligned readout disabled.		
Default: 0	1: 64 bit aligned readout enabled.		
[6]	VME Base Address Relocation (applicable to VME modules only).		
0x00000040	0: Address relocation disabled: VME Base Address is set by the on-board rotary switches.		
Default: 0	1: Address relocation enabled: VME Base Address is set by the VME_BASE_ADDRESS register.		
[7]	Interrupt Release Mode.		
0x0080	0: Release On Register Access (RORA). Interrupts are removed by disabling them either by setting VME		
Default: 0	Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable bit to 0.		
	1: Release On AcKnowledge (ROAK). Interrupts are automatically disabled at the end of an VME interrupts		
	acknowledge cycle (INTACK cycle).		
	Note: ROAK mode supported ONLY for VME Interrupts. ROAK mode is not supported on interrupts generated over		
	Optical Link.		
[8]	Extended Block Transfer Space Enable: Selects Memory Interval allocated for Block Transfers. If disabled, block		
0x0100	transfer region is a 4 KB in the 0x0000-0x0FFC interval. If disabled, block transfer region is a 16 MB in the		
Default: 0	0x00000000-0x0FFFFFFC interval. In Extended mode, the board VME Base Address is only set via on board [31:28]		
	rotary switches or bit[31:28] of the VME_RELOCATION register.		
	0: Extended Block Transfer Space Disabled.		
	1: Extended Block Transfer Space Enabled.		
[15:9]	Reserved.		
Default: 0			
[31 10]	Reserved.		

Tab. 1.41: READOUT_CONTROL_REGISTER

READOUT_STATUS

Address: 0xEF04 Bits: [15:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[0]	Event Ready.
0x0001	
Default: 0	
[1]	Reserved.
0x0002	
Default: 0	
[3]	VME Bus Error / Event Aligned Readout Status.
0x0004	
Default: 0	
[31:4]	Reserved.
Default: 0	

Tab. 1.42: READOUT_STATUS_REGISTER

VME_GEO_ADDRESS

Address: 0xEF08 Bits: [4:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[4:0]	GEO Address.
0x1F	
Default: 0	
[31 5]	Reserved.

Tab. 1.43: VME_GEO_ADDRESS

The meaning and usage of this register depends on which VME crate the board is inserted in: VME64X crate: this register can be accessed in read mode only and contains the GEO address of the module read from backplane connectors; when a CBLT cycle is performed, the GEO address is inserted in event headers. Other crates: this register can be accessed both in read and write mode; it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address is inserted in event headers.

VME_MULTICAST_CONTROL

Address: 0xEF0C Bits: [9:0]

Access Mode: Read and Write

Set board configuration for VME Multicast Cycles.

Bit(s) Info	Bit(s) Description
[7:0]	MCST/CBLT address.
0x0FF	
Default: 0	
[9:8]	Board Position in Daisy Chain.
0x300	00: Board disabled.
Default: 0	01: Last board.
	10: First board.
	11: Intermediate board.
[31 10]	Reserved.

Tab. 1.44: VME_MULTICAST_CONTROL

VME_ADDRESS_RELOCATION

Address: 0xEF10 Bits: [15:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[15:0]	Relocation address: These bits contains the A31A16 bits of the address of the module. If address relocation is
0xFFFF	enabled (see READOUT_CONTROL_REGISTER), this register sets the VME base address of the module.
Default: 0	
[31 16]	Reserved.

Tab. 1.45: VME_ADDRESS_RELOCATION

VME_INTERRUPT_ID

Address: 0xEF14 Bits: [31:0]

Access Mode: Read and Write

Bit(s) Info	Bit(s) Description
[31:0]	Interrupt Status ID: This register contains the STATUS/ID that the module places on the VME data bus during the
0xFFFFFFF	Interrupt Acknowledge cycle.
Default: 0	

Tab. 1.46: VME_INTERRUPT_ID

READOUT_INTERRUPT_CONDITION (EVENT NUMBER)

Address: 0xEF18 Bits: [9:0]

Access Mode: Read and Write

Sets the number of events that cause an interrupt request. If interrupts are enabled, the module generates a request whenever the number of stored events > Interrupt Event Number.

Bit(s) Info	Bit(s) Description
[9:0]	Interrupt Event Number.
Default: 0	
[31 10]	Reserved.

Tab. 1.47: READOUT_INTERRUPT_CONDITION

READOUT_BLT_AGGREGATE_NUMBER

Address: 0xEF1C Bits: [15:0]

Access Mode: Read and Write

Sets the maximum number of complete aggregates to be transferred for each block transfer (VME BLT/MBLT cycles or block readout through Optical Link).

Bit(s) Info	Bit(s) Description
[15:0]	Maximum Aggregate Number for Block Transfer.
Default: 0	
[31 16]	Reserved.

Tab. 1.48: READOUT_BLT_EVENT_NUNBER

DUMMY

Address: 0xEF20 Bits: [31:0]

Access Mode: Read and Write

Scratch register (to be used for register access test purposes).

Bit(s) Info	Bit(s) Description
[31:0]	Scratch.
Default:	
0xAAAAAAAA	

Tab. 1.49: DUMMY

SOFTWARE_RESET

Address: 0xEF24 Access Mode: Write Only

A write access to this location of any value allows to perform a software module reset.

SOFTWARE_CLEAR

Address: 0xEF28
Bits: [31:0]
Access Mode: Write Only

A write access to this location of any value clears all internal memories.

BOARD_CONFIGURATION_RELOAD

Address: 0xEF34 Bits: [31:0]

Access Mode: Read and Write

A write access to this register of any value causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration. This means that when the command is issued, all the parameters that are stored in flash are reloaded into FPGA internal memory: not only PLL values are read back, but also Configuration ROM content (which is anyway invariable).

CONFIGURATION_ROM_CHECKSUM

Address: 0xF000
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM Checksum.
[31:8]	Reserved.

Tab. 1.50: CONFIGURATION_ROM_CHECKSUM

CONFIGURATION_ROM_CHECKSUM_LENGTH2

Address: 0xF004
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM Checksum Length [23:16].
[31:8]	Reserved.

Tab. 1.51: CONFIGURATION_ROM_CHECKSUM_LENGTH2

CONFIGURATION_ROM_CHECKSUM_LENGTH1

Address: 0xF008
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM Checksum Length [15:8].
[31:8]	Reserved.

Tab. 1.52: CONFIGURATION_ROM_CHECKSUM_LENGTH1

CONFIGURATION_ROM_CHECKSUM_LENGTHO

Address: 0xF00C Bits: [7:0] Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM Checksum Length [7:0].
[31:8]	Reserved.

Tab. 1.53: CONFIGURATION_ROM_CHECKSUM_LENGTH0

CONFIGURATION_ROM_CONSTANT2

Address: 0xF010
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM Constant2 fixed value.
Default: 0x83	
[31:8]	Reserved.

Tab. 1.54: CONFIGURATION_ROM_CONSTANT2

CONFIGURATION_ROM_CONSTANT1

Address: 0xF014
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM Constant1 fixed value.
Default: 0x84	
[31:8]	Reserved.

Tab. 1.55: CONFIGURATION_ROM_CONSTANT1

CONFIGURATION_ROM_CONSTANTO

Address: 0xF018
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM Constant0 fixed value.
Default: 0x01	
[31:8]	Reserved.

Tab. 1.56: CONFIGURATION_ROM_CONSTANTO

CONFIGURATION_ROM_C_CODE

Address: 0xF01C Bits: [7:0] Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	ASCII 'c' character code.
Default: 0x43	
[31:8]	Reserved.

Tab. 1.57: CONFIGURATION_ROM_C_CODE

CONFIGURATION_ROM_R_CODE

Address: 0xF020
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	ASCII 'r' character code.
Default: 0x52	
[31:8]	Reserved.

Tab. 1.58: CONFIGURATION_ROM_R_CODE

CONFIGURATION_ROM_OUI2

Address: 0xF024
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM OUI2 value.
Default: 0x00	
[31:8]	Reserved.

Tab. 1.59: CONFIGURATION_ROM_OUI2

CONFIGURATION_ROM_OUI1

Address: 0xF028
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM OUI1 value.
Default: 0x40	
[31:8]	Reserved.

Tab. 1.60: CONFIGURATION_ROM_OUI1

CONFIGURATION_ROM_OUIO

Address: 0xF02C Bits: [7:0] Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Configuration ROM OUI0 value.
Default: 0xE6	
[31:8]	Reserved.

Tab. 1.61: CONFIGURATION_ROM_OUIO

CONFIGURATION_ROM_VERSION

Address: 0xF030
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Board Version Code: Every Digitizer has its own version code.
[31:8]	Reserved.

Tab. 1.62: CONFIGURATION_ROM_VERSION

CONFIGURATION_ROM_FORM_FACTOR

Address: 0xF034
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Board Form Factor CAEN Code.
	0: VME64.
	1: VME64X.
	2: Desktop.
	3: NIM.
[31:8]	Reserved.

Tab. 1.63: CONFIGURATION_ROM_FORM_FACTOR

CONFIGURATION_ROM_BOARD_ID1

Address: 0xF038
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description	
[7:0]	Board Number ID 1 (bit[15:8]).	
[31:8]	Reserved.	

Tab. 1.64: CONFIGURATION_ROM_BOARD_ID1

CONFIGURATION_ROM_BOARD_ID0

Address: 0xF03C Bits: [7:0] Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Board Number ID (bit[7:0]).
[31:8]	Reserved.

Tab. 1.65: CONFIGURATION_ROM_BOARD_IDO

CONFIGURATION_ROM_REVIS3

Address: 0xF040
Bits: [31:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Reserved.
[31:8]	Reserved.

Tab. 1.66: CONFIGURATION_ROM_REVIS3

CONFIGURATION_ROM_REVIS2

Address: 0xF044
Bits: [31:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Reserved.
[31:8]	Reserved.

Tab. 1.67: CONFIGURATION_ROM_REVIS2

CONFIGURATION_ROM_REVIS1

Address: 0xF048
Bits: [31:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description
[7:0]	Reserved.
[31:8]	Reserved.

Tab. 1.68: CONFIGURATION_ROM_REVIS1

CONFIGURATION_ROM_PCB_REVISION

Address: 0xF04C Bits: [7:0] Access Mode: Read Only

Bit(s) Info	Bit(s) Description	
[7:0]	PCB Revision.	
[31:8]	Reserved.	

Tab. 1.69: CONFIGURATION_ROM_PCB_REVISION

CONFIGURATION_ROM_SERNUM1

Address: 0xF080
Bits: [7:0]
Access Mode: Read Only

	Bit(s) Info	t(s) Info Bit(s) Description	
	[7:0]	Board Serial Number (bit[15:8]).	
[31:8] Reserved.		Reserved.	

Tab. 1.70: CONFIGURATION_ROM_SERNUM1

CONFIGURATION_ROM_SERNUMO

Address: 0xF084
Bits: [7:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Description	
[7:0]	Board Serial Number (bit[7:0]).	
[31:8]	Reserved.	

Tab. 1.71: CONFIGURATION_ROM_SERNUMO

CONFIGURATION_ROM_VCXO_TYPE

Address: 0xF088
Bits: [31:0]
Access Mode: Read Only

Bit(s) Info	Bit(s) Desc	ription
[31:0]	VCXO Type Code.	
	VME Digitizer	
	0: AD9510 with 1 GHz.	
	1: AD9510 with 500 MHz (not programmable).	
	2: AD9510 with 500 MHz (programmable).	
	Desktop/NIM Digitizer	
	0 : AD9520-3.	

Tab. 1.72: CONFIGURATION_ROM_VCXO_TYPE



Electronic Instrumentation



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