RISC-V Processor Design 🚀

Building Tiny Vedas

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Lecture 5

Agenda

- Top-level design
- Top-level testbench
- Instruction Memory (ICCM)
- Instruction Decode - Stage 0
- Instruction Decode - Stage 1

Top-level design

- Instantiates the following units:
  - ICCM
  - IFU
  - IDU0
  - IDU1

Top-level testbench

- Instantiates the core and the ICCM
- Generates the clock and reset signal
- Applies the reset
- Runs the simulation for a certain number of cycles
- Verilator will run the simulation and check the output

Instruction Memory (ICCM)

- Byte-addressable, word-aligned
- 1024 words (4096 bytes)
- 1CC instruction latency

Instruction Decode - Stage 0

- Gets the instruction from the IFU Stage
- Decodes the instruction by going through the decode tables
- Generates the control signals for the IDU1 and EXU units
- Generates the register file read addresses

Decode Tables

- Custom format to define the instructions and the control signals
- Converted into Espresso Logic Synthesis format
- Run through the Logic Synthesis tool to get the minimized logic and converted to SystemVerilog files

Instruction Decode - Stage 1

- Gets the instruction from the IDU0 Stage
- Gets the data from the register file
- Generates the control signals for the EXU unit