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A Comparative Study of Advanced MOSFET Concepts

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Abstract—**Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has been the major device for integrated circuits over the past two decades. With technology advancement, there have been numerous MOSFET structures for channel length of 0.1 μm and below reported in industrial research. A side-by-side comparison of these advanced device structures can provide useful understanding in device physics and the design trade-offs among MOSFET's parameters. In this work we employ experimental data, device simulation, and analytical modeling for device comparison. The devices were developed at several different research laboratories. Guided by experimental data and simulations, analytical models for topics such as threshold voltage, short-channel effect, and saturation current for these different MOSFET structures are developed. These analytical models are then used for optimizing each device structures and comparing the devices under the same set of constraints for a fair comparison. The key design parameters are highlighted and the strength and weakness of each device structure in various performance categories are discussed.**

I. Introduction

METAL-OXIDE-SEMICONDUCTOR Field Effect Transistor (MOSFET) has been the major device for integrated circuits over the past two decades. With technology advancement and the high scalability of the device structure, silicon MOSFET based VLSI circuits have continually delivered performance gain and/or cost reduction to semiconductor chips for data processing and memory functions. Industrial research has already set sight on MOSFET's of channel length 0.1 μm and below; the motivations for continued scaling include not only better speed and density but also less power consumption for integrating a complete system on a chip [1]. There have been numerous device structures of 0.1 μm MOSFET reported in the literature. Each device structure has its merits and demerits; hence it is desirable to compare the major proposed device structures side-by-side in the same set of constraints. However a comprehensive device comparison is not easy since there are many trade-offs among MOSFET's parameters. For example, comparison on ring oscillator speed data can be quite meaningless even for MOSFET's of similar channel lengths but of different threshold voltages or varying degrees of short-channel effect. Device simulation is a good tool for device comparison [2], provided the simulator is calibrated to real devices otherwise the results are in doubt. Analytical models provide good physical insight. In this work we employ experimental data, device simulation, and analytical modeling for device comparison. The devices were developed at several different research laboratories. The development of analytical models is closely guided by simulation and experimental data. Device simulators are used to extrapolate data available. The analytical models are then used for optimizing each device structures and for comparing different device structures under the same set of constraints for a fair comparison. MOSFET devices included in this study are:

- MOSFET with uniformly doped substrate (UD);
- Delta-doped MOSFET (DD) [3]–[6] (Fig. 1);
- Pocket-implanted MOSFET (PI) [7];
- Partially-depleted SOI MOSFET (PDSOI);
- Fully-depleted SOI MOSFET (FDSOI);
- Dynamic-threshold MOSFET (DT) [8]; and
- Double-gate MOSFET (DG) [9]–[11] (Fig. 1).

DD MOSFET's used in this study are fabricated as in [3]. The body contact scheme of DT MOSFET is the same as in [8]. DG MOSFET are fabricated as in [9]. The generic extensions of above devices cover a wider range of MOSFET structures. For example, DD MOSFET can also represent the atomic-layer doping MOSFET [4] and MOSFET with retrograded doping channel doping using ion implantation [5] and [6]. PI MOSFET also represents halo-doping [12]. DG MOSFET also represents the surrounding-gate MOSFET [10] and the DELTA MOSFET [11]. It should be mentioned that we use the uniformly-doped channel MOSFET to represent a more conventional design than delta-doping and to simplify analysis, even though MOSFET made with the conventional approach using ion-implantation does not have uniform channel doping profile.

The following topics are discussed in device comparison:

- Threshold Voltage Control and Subthreshold Swing;
- Short-Channel Effect;
- Mobility and Saturation Current; and
- Capacitance and Relative Gate Delay.

These topics by no means cover the interests of every device engineer and circuits designer. We have limited ourselves to the structural differences between devices, therefore issues

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related to manufacturing cost are not addressed. Some device structures considered in this work might not be manufacturable at this time. However, they serve to illustrate the possibilities that a breakthrough in manufacturing technology could unleash.

II. Threshold Voltage and Subthreshold Swing

A. V_t and S by Back Gate x_{bg}

The role of threshold voltage V_t subthreshold swing S has become increasing important with VLSI applications emphasizing low-voltage, low-power, and high speed design [14], [15]. In this section, we summarize some basic equations for V_t and S highlighting the role of the back-gate thickness x_{bg} for later use (Fig. 1). We also clarify a quantity δ, the difference between threshold voltages defined in two different methods, namely the extrapolation method and the constant current method. Let $\Delta = V_{fb} + 2\phi_b$, a parameter which depends on the gate work function. For n^+-polysilicon-gate NMOSFET and p^+-polysilicon-gate PMOSFET (dual-gate CMOS), Δ is close to 0. V_t and S for the UD MOSFET are

$$V_t = \Delta + \frac{\sqrt{2\epsilon_s q N_{sub}(2\phi_b + V_{sb})}}{C_{ox}} = \Delta + 6(2\phi_b + V_{sb})\frac{t_{ox}}{x_{bg}}, \tag{1a}$$

$$S = \left(\frac{kT}{q}\ln 10\right)\left(1 + \frac{\epsilon_s t_{ox}}{\epsilon_{ox} x_{bg}}\right) = 60\,\text{mV}\left[1 + \frac{V_t - \Delta}{2(2\phi_b + V_{sb})}\right]. \tag{1b}$$

x_{bg} in (1) is the depletion layer width. For a truly DD MOSFET with ideal step-doping profile

$$V_t = \Delta + \frac{\epsilon_s}{\epsilon_{ox}}\frac{t_{ox}}{x_{bg}}(2\phi_b + V_{sb}) = \Delta + 3(2\phi_b + V_{sb})\frac{t_{ox}}{x_{bg}}, \tag{2a}$$

$$S = 60\left(1 + \frac{\epsilon_s t_{ox}}{\epsilon_{ox} x_{bg}}\right) = 60\left(1 + \frac{V_t - \Delta}{2\phi_b + V_{sb}}\right). \tag{2b}$$

x_{bg} in (2) is the lightly-doped layer width. Note that the ideal delta or step doping profile is difficult to obtain, thus in practice V_t and S will be in between (1) and (2) for any MOSFET technology that has retrograded channel doping profile.

Depending on the body doping profile, V_t of the DT MOSFET is similar to (1a) or (2a) except for substituting V_{sb} with V_g. DT MOSFET has ideal S (Fig. 2) because in general S is determined by capacitance coupling, V_c/V_g

$$V_c = V_g\frac{C_{ox}}{C_{ox} + C_{bg}} + V_{bg}\frac{C_{bg}}{C_{ox} + C_{bg}} \tag{3}$$

where V_c is the channel voltage. In DT MOSFET $V_{bg} = V_g$, hence $S \approx 60$. For DG MOSFET $x_{bg} = t_{\text{Si}}/2$ and $V_{bg} = V_g$,

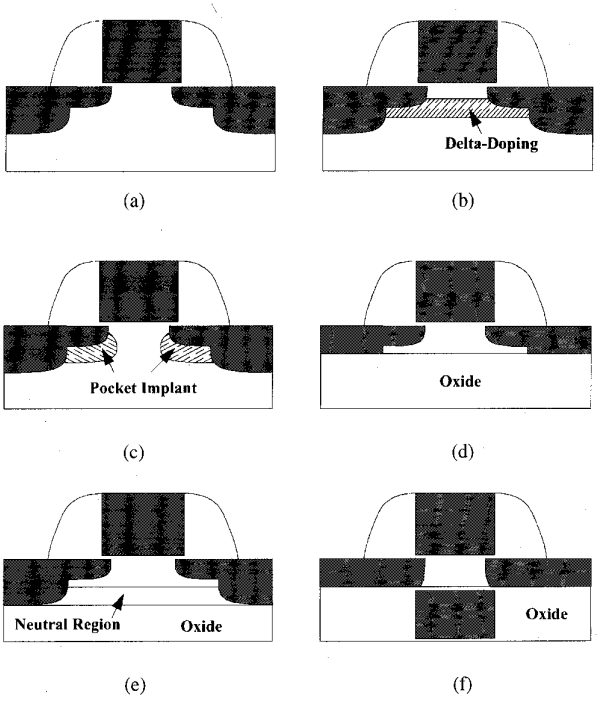

Fig. 1. Schematic device cross sections of MOSFET devices and the definitions of their back gate thicknesses x_{bg}. (a) Uniformly-doped (UD) MOSFET is used to approximate conventional MOSFET. x_{bg} is depletion width. (b) Delta-doped (DD) MOSFET [3], x_{bg} is lightly-doped layer width (x_{ld}). Other examples: ALD [4], retrograded channel doping [5] and [6]. (c) Pocket-Implanted (PI) MOSFET, x_{bg} is depletion width. Other example: TIPS [7], Halo-doping [12]. (d) Fully-depleted SOI (FDSOI) MOSFET's which has large x_{bg}. (e) Partially-depleted SOI (PDSOI) MOSFET. (f) Double-gated (DG) MOSFET [9]. x_{bg} is $t_{\text{Si}}/2$. Other examples: SGT [10], DELTA [11].

and

$$V_t = \Delta + \frac{qN_b t_{\text{Si}}}{2\epsilon_{ox}}t_{ox}, \quad \frac{qN_b t_{\text{Si}}^2}{8\epsilon_s} \le 2\phi_b \tag{4a}$$

$$S = 60. \tag{4b}$$

The second equation in (4a) is to ensure that the silicon film is fully-depleted thus nearly ideal S results. Note that x_{bg} in (4) is in the numerator instead of being in the denominator as in (1) and (2); the impact on device scaling will be discussed in Section III.

V_t and S of PDSOI SOI MOSFET is similar to (1) or (2), depending on the body doping profiles, if the body is grounded. The complication caused by the floating body effect will be addressed in Section II-C. V_t and S of FDSOI MOSFET are given as

$$V_t \approx \Delta + \frac{qN_b t_{\text{Si}}}{\epsilon_{ox}}t_{ox}, \quad \frac{qN_b t_{\text{Si}}^2}{2\epsilon_s} \le 2\phi_b \tag{5a}$$

$$S = 60, \tag{5b}$$

$S \approx 60$ is because in (3) $C_{bg} \ll C_{ox}$. Note that the back-gate thickness of FDSOI MOSFET is very large. One may estimate x_{bg} from the measured subthreshold swing

$$x_{bg} \approx \frac{\epsilon_s t_{ox}}{\epsilon_{ox}\left(\frac{S}{60} - 1\right)}. \tag{5c}$$

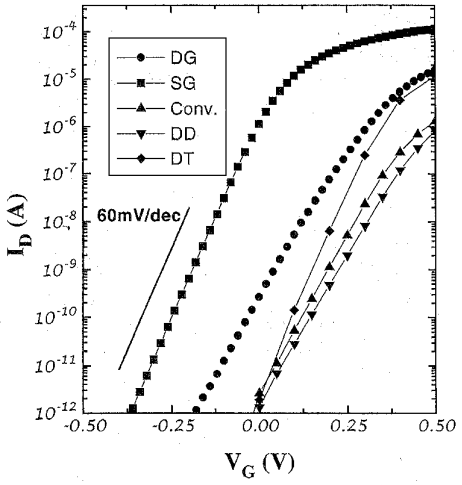

Fig. 2. Comparison of the subthreshold swings of various device structures (not of the same device size) in this study. The double-gate MOSFET and the dynamic-threshold MOSFET have ideal subthreshold swings (~60 mV/dec).

B. V_t Defined by Extrapolation and by Constant Current

The information that V_t provides are: A) the voltage when on-current is negligible and B) some information about the off-state leakage current. For on-current modeling, the threshold voltage is usually measured by extrapolating the gate voltage to zero drain current in a linear scale. Another popular definition of the threshold voltage, more appropriate for B) is the gate voltage at which the drain current equals to a preset value I_{th}. Choices of I_{th} can be 0.1 μA per W/L [9], 0.1 μA per μm of W [3], or 2 nA per μm of W [15]. I_{th} is usually chosen at the weak inversion [16] region where the subthreshold slope is well defined thereby the off-state leakage can be inferred from V_t and S. The difference δ between the two threshold voltages, which is usually small but can have a significant role, can be estimated by a channel charge function similar to [17]

$$Q_{ch} = \eta \upsilon_{th} C_{ox} \ln\left[1 + \frac{C_x}{\eta C_{ox}} \exp\left(\frac{V_g - V_x}{\eta \upsilon_{th}}\right)\right] \quad (6)$$

where C_x, V_x are to be determined below. Equation (6) becomes $C_{ox}(V_g - V_{t-ex})$ asymptotically if the extrapolation V_{t-ex} is equal to

$$V_{t-ex} = V_{ref} - \eta \upsilon_{th} C_{ox} \ln\left(\frac{C_{ref}}{\eta C_{ox}}\right). \quad (7)$$

Equation (6) also agrees asymptotically with the exponential subthreshold conduction. By comparing (6) with the MOSFET subthreshold current [18], we find $V_x = V_g(\phi_s = 2\phi_b)$, $C_x = C_d$. The constant current threshold voltage can be derived by equating the subthreshold current to I^*_{th} ($I^*_{th} = I_{th} \times W/L$ or $I^*_{th} = I_{th} \times W$)

$$I_{ds} = \mu \eta \upsilon_{th}^2 \frac{W}{L} C_{ox} \ln\left[1 + \frac{C_d}{\eta C_{ox}} \exp\left(\frac{V_g - V_{ref}}{\eta \upsilon_{th}}\right)\right] = I^*_{th}. \quad (8)$$

Thus the difference between the two threshold voltages is

$$\delta = V_{t-ex} - V_{t-cc} = -\eta \upsilon_{th} \ln\left[\exp\left(\frac{I^*_{th} L}{\mu \eta \upsilon_{th}^2 W C_{ox}}\right) - 1\right]. \quad (9)$$

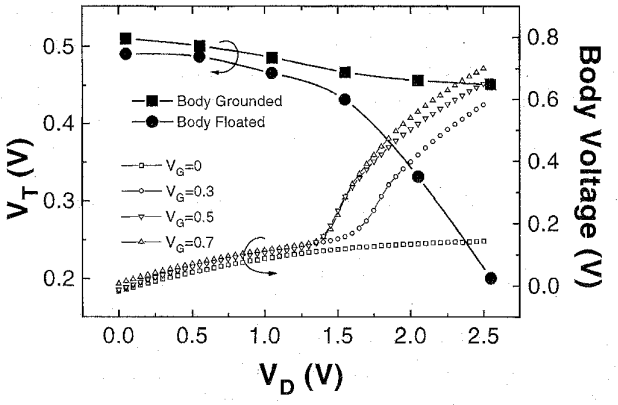

Fig. 3. (Static) V_t and V_b of an SOI NMOSFET depend strongly on V_d. V_b of SOI MOSFET is measured by a body contact.

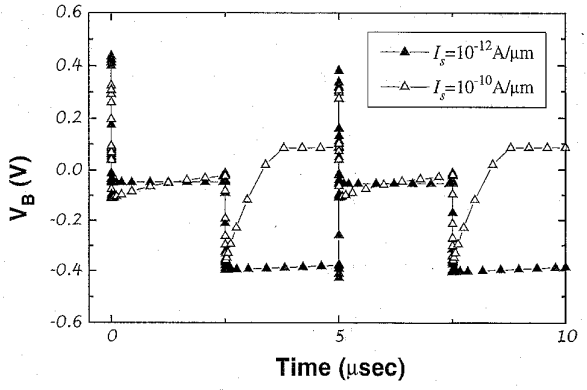

Fig. 4. V_b of a PDSOI NMOSFET in an inverter chain depends on the coupling to V_g and V_d, and the amount of body charge. The larger the junction leakage current Is, the faster V_b is restored to its equilibrium value, and the smaller V_b is resulted during V_g turning-on.

The value of δ is close to 0 when I_{th} is chosen as 0.1 μA per W/L and is about 0.15 V when I_{th} is chosen as 2 nA/μm per W/L. However, a smaller value of I_{th} better ensures that the resulting constant current V_t has a well-defined S.

C. Dynamic Floating-Body Effect in SOI MOSFET

Both V_t and S of PDSOI MOSFET depend on the history of operation as well as how fast the device is operated [19]. For example, V_t measured in the static case depends on the amount of the charge stored in the body as in Fig. 3. In this particular case the coupling from the body voltage V_b to ΔV_t is about 0.5. The exact coupling ratio depends on the vertical body doping profile [20]. In the dynamic situation, how V_t and V_b change with time is even more complicated due to both the amount of the body charge and the capacitance coupling. When V_b change is taken into consideration in calculating S using (3), it can be shown that $S \rightarrow 60$ if the junction leakage and V_b coupling to V_d are small. V_b at standby restores to its equilibrium value by the junction leakage and impact ionization currents. The V_b change with time can be visualized in simulation in Fig. 4 [21], which shows that the larger the replenishing junction current, the faster the device is restored to the equilibrium state. Also the larger the body-to-source

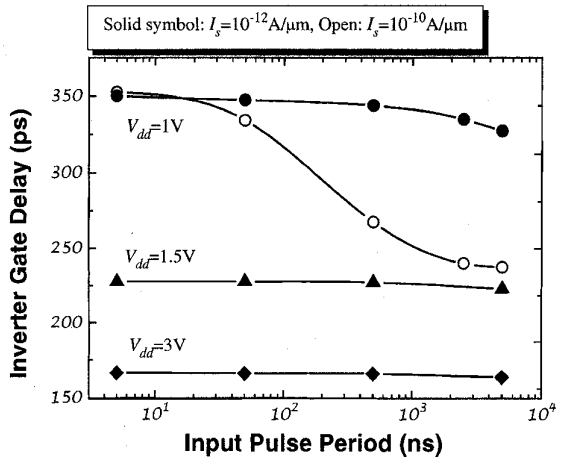

Fig. 5. The inverter gate delay of PDSOI MOSFET depends on the input pulse period and the junction leakage. The more body charge is replenished, the better improvement in speed.

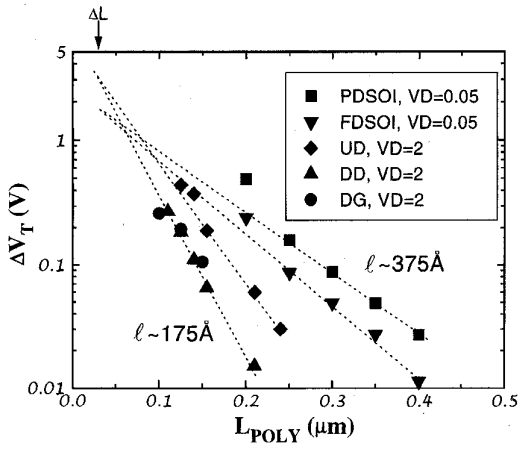

Fig. 6. The short-channel characteristic length l can be determined by extracting the slope of ΔV_t (log scale) versus L plot for different device structures.

junction current, the smaller the peak V_b value. Fig. 5 shows that the inverter delay can be improved if more body charge is replenished. The exact amount of improvement depends on the amount of body charge, the duty cycle (active time versus standby time), the output loading, the channel doping profile, and the junction leakage characteristics. The impact of the floating body effect on circuit speed can be significant hence is included for estimating the circuit speed in Section V.

III. Short-Channel Effect

A. Short-Channel Effect Model

MOSFET short-channel effect is a major challenge for scaling the gate length down and below 0.1 μm. The dependence of V_t on channel length is stronger as compared to other factors that also cause V_t fluctuation at small device dimension such as random dopant distribution [22]–[24]. The short-channel effect, which includes the threshold voltage roll-off and the drain-induced barrier lowering, can be modeled as [26]

$$V_t = V_{to} - 1.8\sqrt{V_{ds}+0.8}e^{-L_{eff}/2l},$$
$$l \approx x_{ox}^{1/3}x_{bg}^{1/3}x_j^{1/3}. \tag{10}$$

In (10) V_{to} is the long-channel threshold voltage, V_{ds} is the drain voltage, l is the characteristic length of the threshold voltage roll-off, and is an important device design parameter. We have updated the empirical expression of l with x_{bg} defined in Section II-A, except for DG MOSFET of which $l \approx \sqrt{(3/2)t_{ox}t_{Si}[1+(t_{Si}/12t_{ox})]}$ [9]. L_{eff} in (10) might be slightly different from the metallurgical junction due to depletion of the source/drain extension. The difference is usually a small quantity (within ± 0.02 μm) by device design since drain depletion should be minimized otherwise the current driving capability will suffer [27] thereby offsetting the advantage obtained by scaling polysilicon gate length. It should be noted that (10) is valid only when ΔV_t is not too large, which is also the case of practical interest. Fig. 6 provides a way to extract l experimentally.

A parameter $L_{\min}$ may be defined as the minimum channel length that meets some specified short-channel-effect criterion [26], [28]. From (10) $L_{\min}$ can be expressed in terms of l once a criterion of the threshold voltage roll-off is selected. For example, one can define $L_{\min}$ by an acceptable V_t roll-off such as $\Delta V_t = 0.1$ V when $V_{ds} = 2$ V, therefore $L_{\min}$ is give as

$$L_{\min} = 2l \cdot \ln\left(\frac{1.8\sqrt{V_{ds}+0.8}}{\Delta V_t}\right)$$
$$\approx 7l. \tag{11}$$

Often it is not the absolute threshold voltage roll-off ΔV_t that is of concern, it is dV_t/dL that is important. From (10) we have $dV_t/dL = \Delta V_t/2l$, thereby $L'_{\min}$ is given as

$$L'_{\min} = 2l \cdot \ln\left(\frac{1.8\sqrt{V_{ds}+0.8}}{\frac{dV_t}{dL}\cdot 2l}\right)$$
$$\approx 2l \cdot \ln\left(\frac{1.8\sqrt{V_{ds}+0.8}}{\frac{L_{\min}}{3.5}\frac{dV_t}{dL}}\right), \tag{12}$$

where dV_t/dL may be chosen to be $3.5\Delta V_t/L_{\min}$ so that $L'_{\min} = L_{\min}$. Conversely, at $L_{\min}$, $dV_t/dL = 3.5\Delta V_t/L_{\min}$. In this paper, $L_{\min}$ is mostly defined by constant ΔV_t roll-off as in (11). With (11) and (12) it is easy to convert between the two criteria.

B. MOSFET Substrate Engineering Using Delta-Doping

One major motivation of substrate engineering, which can be applied to bulk, PDSOI and DT MOSFET's, is to achieve good short-channel effect without having high V_t. MOSFET V_t depends on the back gate thickness x_{bg} as in (1)–(5). Unlike t_{ox} or x_j, x_{bg} cannot be measured directly. However we can substitute x_{bg} with V_t by using (10), (11), and obtain the

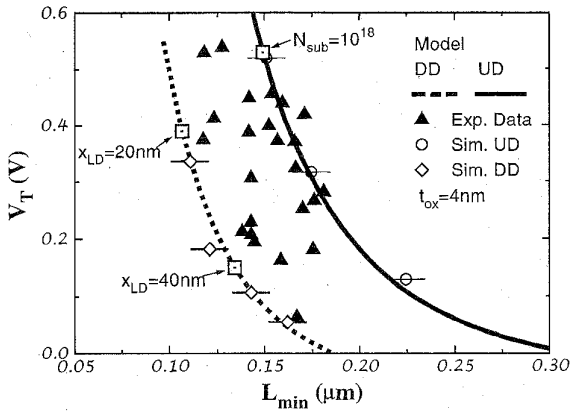

Fig. 7. By varying x_{bg}, the relation between the long-channel V_t and $L_{\min}$ is shown for UD and DD MOSFET. t_{ox} is 40 Å. x_j is 400 Å for DD MOSFET and varies from 400 Å to 700 Å for UD MOSFET (due to the difference in N_{sub}). Experimental data scatter between the UD and DD model curves due to different degrees of retrograded doping.

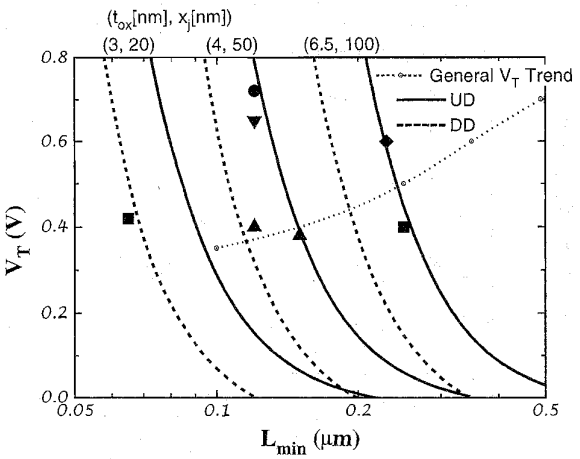

Fig. 8. A similar plot to Fig. 7 but with various t_{ox} and x_j combinations [3] [29]–[31] to study the role of substrate engineering in device scaling.

relation between V_t and $L_{\min}$

$$L_{\min} \approx 7[3n(2\phi_b + V_{sb})]^{1/3} t_{ox}^{2/3} x_j^{1/3} (V_t - \Delta)^{-1/3}. \quad (13)$$

In (13) $n = 2$ for UD devices and $n = 1$ for DD devices. Fig. 7 compares the model (13) with experimental data and device simulations of conventional MOSFET using ion-implanted channel and DD MOSFET using selective epitaxial channel with $t_{ox} = 40$ Å and $x_j \approx 400$–700 Å (depending on substrate doping profiles). As expected, the experimental data points with varying degree of substrate engineering fall between the DD and UD model curves. Optimized selective epitaxy process can be close to ideal DD model curve and achieve around 300 Å x_{bg} using 400 Å epitaxial layer thickness after dopant out-diffusion. The improvement by ideal DD substrate engineering is about one generation of $L_{\min}$ scaling or approximately one half of V_t at the same $L_{\min}$. Fig. 8 examines the same relationship as in Fig. 7 but with several different t_{ox} and x_j for three generations of technologies. For $t_{ox} \approx 65$ Å and $x_j \approx 1000$ Å as in technologies of $L_{\min} \approx 0.25\,\mu$m [29], [30], substrate engineering is not important, but $L_{\min}$ below 0.2 μm can be achieved using substrate engineering. Since V_t can be reduced rather easily by using thinner t_{ox}, substrate engineering is not always needed if V_t adjustment is the only consideration. For example, when $t_{ox} = 40$ Å and $x_j = 400$ Å UD MOSFET can achieve 0.15 μm $L_{\min}$ at acceptable low V_t, while substrate engineering can further improve $L_{\min}$ to 0.1 μm. With aggressive scaling on t_{ox} and x_j, UD MOSFET can achieve $L_{\min} \sim 0.07\,\mu$m ($t_{ox} = 30$ Å, $x_j \approx 100$ Å) [31]. However, in some applications when t_{ox} is limited by other considerations such as reliability or direct tunneling leakage, or when x_j is limited by high source/drain series resistance, substrate engineering provides an alternative scaling approach. There are performance penalties of substrate engineering which will be discussed in Section IV. It should also be noted that, similar to UD MOSFET, delta-doping is also limited by the upper limit of N_{sub} for junction leakage consideration, but not so much for the junction capacitance consideration if the delta-doping is place only underneath the channel (Fig. 1). When the delta-doped layer is depleted, the effectiveness of substrate engineering is reduced. This might be the case of some of the experimental data points in between the UD and DD curves in Fig. 7. Finally, the anomalous short-channel behavior of SOI MOSFET [32] between PD to FD can also be explained by the x_{bg} change from the depletion width in PD to very large in FD as predicted by (5c).

C. Source and Drain Engineering Using Pocket Implant

Pocket implant is a popular technique for improving short-channel effect. Compared with substrate engineering, pocket implant can place the implanted ions near the location where it is needed the most around the drain (and the source). Compared with epitaxial channel, pocket implant using ion implantation is rather low cost. The exact doping profile can be quite intractable analytically. Our approach starts with simplified step pocket profiles. It can be shown that with the ideal step pocket profiles, the short-channel effect model as in (10) for PI MOSFET is

$$\Delta V_t \approx -(V_{ds} + 2)e^{-L_{eff}/l} + 1.8(\kappa - 1)\sqrt{V_{ds} + 0.8}\, e^{-L_{eff}/2l} \quad (14a)$$

$$\kappa \approx \sqrt{\frac{V_{th} \ln \dfrac{N_p}{N_{sub}}}{V_{ds}}} \frac{L_p}{l}. \quad (14b)$$

In (14b) N_p is the pocket implant concentration and L_p is the pocket implant length measured from the source/drain extension to the background channel doping (Fig. 1). $\kappa = 0$ if $L_p = 0$ or $N_p = N_{sub}$. Note that the parameter κ in (14b) is in general a representation of a combination of N_p and L_p, therefore we will extend κ as a parameter representing general pocket implant profiles. This generalization is valid as seen in Fig. 9 in which short-channel effect of PI MOSFET with different pocket implant dose can be successfully modeled by varying one parameter κ. Therefore one can visualize what ultimately can be achieved using pocket implant to

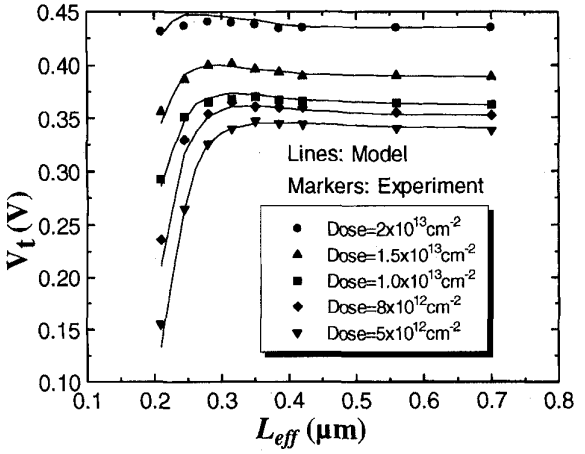

Fig. 9. One parameter κ can be used to described a combination of pocket dose, energy, and implantation angle. By varying κ one can visualize what can be achieved ultimately to improve the short-channel effect using pocket implant. In this figure the implant dose is varied.

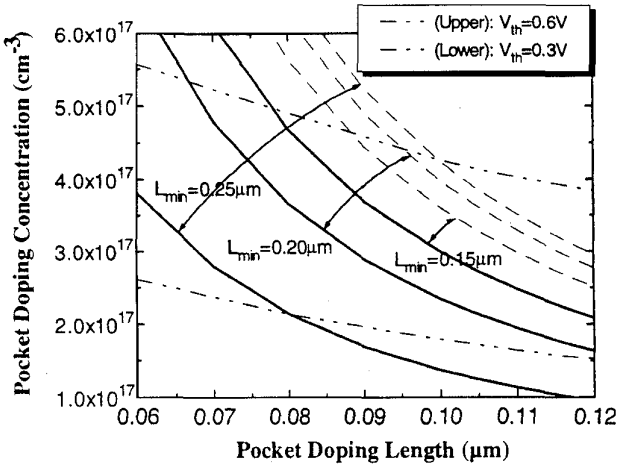

Fig. 10. Each κ value in (9) represents combinations of N_p and L_p. The feasibility of a particular κ can be examined by the N_p–L_p design space. Pocket implant can improve short-channel effect by two generations of $L_{\min}$.

improve short-channel effect by varying κ. Since each κ value represents many possible combination of N_p and L_p, the feasibility of a particular κ value can then be examined using Fig. 10, the N_p–L_p design space, by taking process control into consideration. By optimizing the pocket process, it is possible to improve $L_{\min}$ from 0.25 to 0.2 μm or even 0.15 μm as seen in Figs. 9 and 10. The improvement in pocket implant lies in the pocket profile control. More than one generation of $L_{\min}$ improvement might be obtained by pocket implant.

D. Double-Gate MOSFET

Similar to (13), the relationship between V_t and $L_{\min}$ of DG MOSFET can be derived

$$L_{\min} \approx 7 \sqrt{\frac{3\epsilon_{ox}(V_t - \Delta)}{qN_b}\left(1 + \frac{t_{\rm Si}}{12t_{ox}}\right)}. \qquad (15)$$

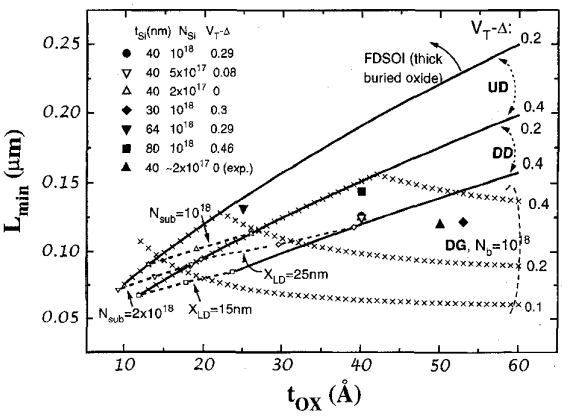

Fig. 11. Analysis of the impact of t_{ox} scaling on $L_{\min}$ for UD, DD, FDSOI, and DG MOSFET. The possible boundaries by N_{sub} and x_{ld} are also shown. PDSOI and DT MOSFET's have the same limitations and capabilities as UD/DD MOSFET depending on the channel doping profiles. Note that the trend of $L_{\min}$ versus t_{ox} of the DG MOSFET is to the opposite of the other devices.

Equation (13) indicates that bulk MOSFET with higher V_t in general has smaller $L_{\min}$. However from (15), for DG MOSFET the opposite case is true: devices of smaller V_t has smaller $L_{\min}$. This is because in DG MOSFET of higher $V_t - \Delta$ requires thicker silicon film therefore degrades short-channel effect. The relation between $L_{\min}$ and t_{ox} for DG MOSFET and other MOSFET's is shown in Fig. 11. It is very difficult to obtain DG MOSFET of $V_t - \Delta \sim 0.4$ V with good short-channel effect. Adjusting V_t via gate workfunction might be a better alternative (e.g., tungsten, TiN, and polycrystalline Si–Ge [33]). On the otherhand, DG MOSFET is the only device which can achieve very small $L_{\min}$ with low V_t and thick t_{ox} (>40 Å). For multiple-V_t technology, DG MOSFET automatically gives high V_t devices by operating in the single-gate mode. Note that DG MOSFET operated in the single-gate mode is effectively a DD MOSFET with delta-doping concentration as high as 10^{20} cm^{-3} and the lightly-doped layer controlled by the silicon film thickness $t_{\rm Si}$ and t_{ox}. It is also noted from Fig. 11 that for a given junction depth, conventional scaling scenario by reducing t_{ox} and increasing N_{sub} can not be continued if N_{sub} hit the its upper limit, e.g., 10^{18} cm^{-3} as seen in Fig. 11 when t_{ox} is about 25 Å (x_j = 400 Å). After that, the dependence of $L_{\min}$ on t_{ox} is weakened (from power of 2/3 to 1/3) and workfunction engineering might be required for V_t adjustment.

There also exist trade-offs between V_{dd} and t_{ox} using (10) and (11) as seen in Fig. 12. Thinner t_{ox} alleviates the short-channel effect constraint and allows larger V_{dd}, however the reliability constraints and the gate leakage current will limit the magnitude of V_{dd} [34]. DD MOSFET provides more design latitude in this case. In general, bulk and DT MOSFET's have similar short-channel effect capability that depend on the doping profiles. PDSOI and DG MOSFET can have worse short-channel effect when the drain junction has large leakage current in the static case. Delta-doping and pocket doping can be applied to bulk, DT, and PDSOI MOSFET's. FDSOI MOSFET has poor short-channel effect due to large x_{bg}. To control the short-channel effect, parameters V_t, Δ, V_{dd}, x_{bg},

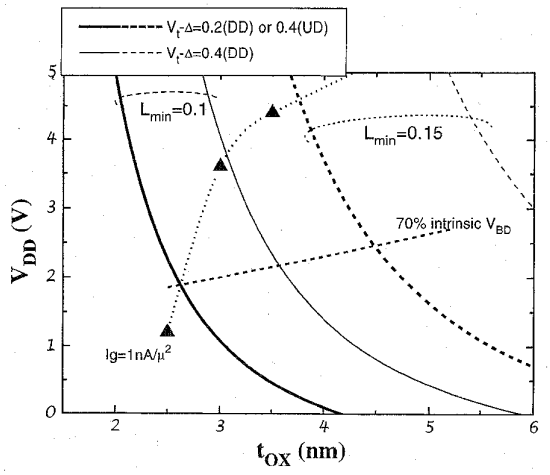

Fig. 12. The constraints between V_{dd} and t_{ox} using (10) and (11). The constraints imposed by 70% of intrinsic oxide breakdown and the gate leakage currents are also shown.

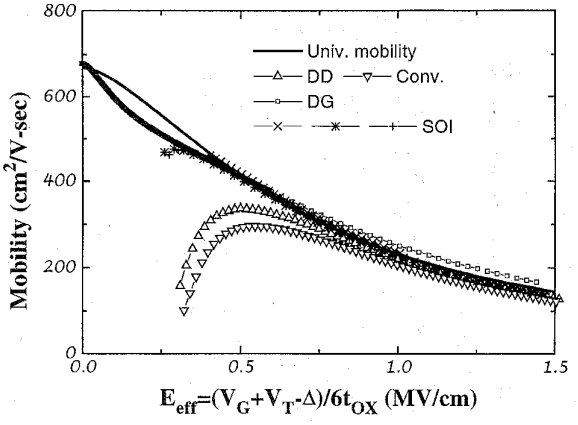

Fig. 13. The effective mobilities of various devices in this study. They exhibit universal dependence at large E_{eff} which is computed as $(V_g + V_t + D)/6t_{ox}$. Very high mobility of DG MOSFET in the small E_{eff} regime can be used for device applications because the small V_t of DG MOSFET does not degrade short-channel effect.

x_j, and t_{ox} are all closely interrelated and should be considered as an integrated issue in device, circuit, process, and reliability design for sub-0.1 μm MOSFET technologies.

IV. Mobility and Saturation Current

A. Effective Inversion Layer Carrier Mobility

The effective inversion layer carrier mobility affects strongly the MOSFET current as well as the onset of velocity overshoot for short-channel MOSFET [35], [36]. For conventional MOSFET, the mobility can be universally expressed in terms of the effective vertical electric field E_{eff} [37]

$$\mu_{eff} = \frac{670}{1 + \left(\frac{E_{eff}}{0.67}\right)^{1.67}},$$
$$E_{eff} = \frac{\frac{Q_n}{2} + Q_b}{\epsilon_s}. \tag{16}$$

Q_n can be easily approximated by $C_{ox}(V_g - V_t)$, but Q_b is difficult to estimate, especially for novel device structures. However, according to (1)–(5), the total depletion charge is approximately given as [38]

$$Q_b = C_{ox}(V_t - \Delta), \tag{17}$$

thus E_{eff} becomes

$$E_{eff} = \frac{V_g + V_t - 2\Delta}{6t_{ox}}. \tag{18}$$

Using (18) for E_{eff}, with $\Delta \sim 0$ for n^+ polysilicon gate, the effective mobility is plotted Fig. 13. The double-gate MOSFET, due to its smallness of threshold voltage (i.e., low doping concentration), has very high mobility at low vertical field. Note that the empirical effective mobility model was not developed for the low field regime in Fig. 13. It is possible to employ such high mobility for device operation with V_t adjusted by gate workfunction and maintains good short-channel effect control for DG MOSFET.

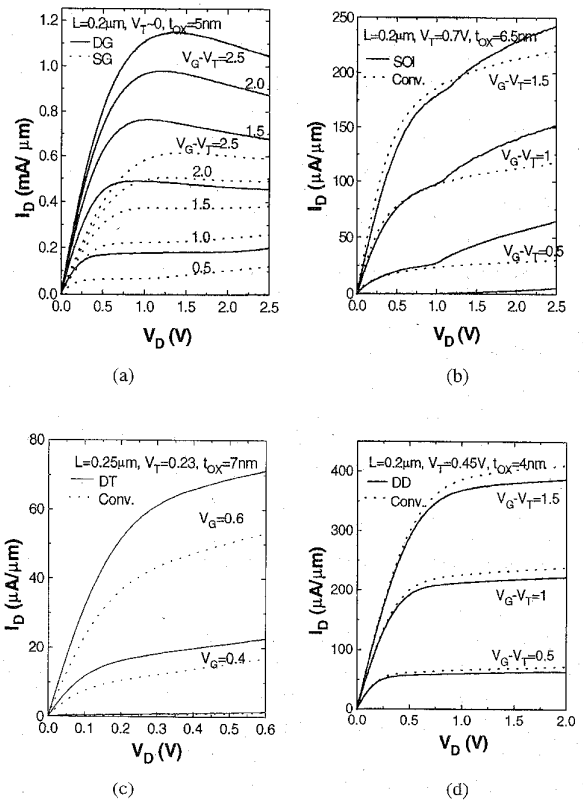

Fig. 14. MOSFET I_d–V_d characteristics of some devices in this study: (a) DG MOSFET, (b) PDSOI MOSFET, (c) DT MOSFET, and (d) DD MOSFET.

B. Drain Saturation Current

MOSFET I_d–V_d characteristics of the devices in this study are shown in Fig. 14(a)–(d). In general observations, DG MOSFET delivers twice the current with the same footprint. SOI-based MOSFET has to take into account the floating-

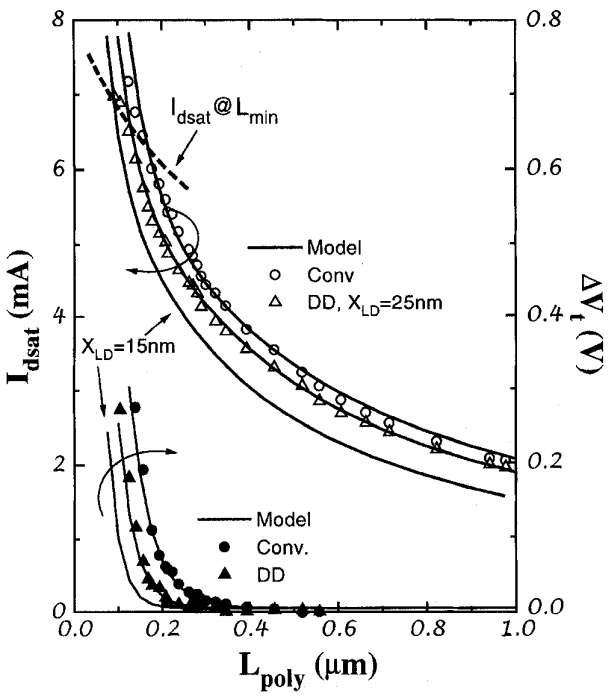

Fig. 15. Experimental data of I_{dsat} and ΔV_t of the DD MOSFET and the conventional MOSFET are compared. Also shown are the models using (10) and (22). Though DD MOSFET has smaller I_{dsat} at the same channel length as compared with the conventional MOSFET, it has larger I_{dsat} than that of the conventional MOSFET when both devices are compared at $L_{\min}$.

body effect and the self-heating effect. DT MOSFET can only operated at below 0.6 V but can improve approximately 25% of I_{dsat}, depending on V_t. DD MOSFET has smaller I_{dsat} than the conventional MOSFET at the same channel length due to the effect of back-gate coupling, i.e., the bulk-charge effect. In this section, we present a unified analytical I_{dsat} model for comparing and highlighting the I_{dsat} difference resulting from x_{bg} dependence. In addition to comparing the saturation current at the same gate length, using the short channel effect model we are able to compare the saturation current at $L_{\min}$ for different device structures. The basic saturation current model for conventional MOSFET gives [37]

$$I_{dsat} = W v_{sat} C_{ox}(V_g - V_t - V_{dsat})$$
$$V_{dsat} = \frac{(V_g - V_t)E_{sat}L}{V_g - V_t + E_{sat}L}. \tag{19}$$

A simple interpretation of (19) is that at the onset of velocity saturation near the drain-end, by definition, the drain voltage is V_{dsat}, the charge density near the drain end is $C_{ox}(V_g - V_t - V_{dsat})$ and travels at saturation velocity v_{sat}. When V_d exceeds V_{dsat}, the saturation current increases slightly due to finite output resistance [39] which will not be considered. To incorporate the back-gate effect into (19), we note that V_t in (19) should be the threshold voltage near the drain end (bulk-charge effect), not the usual threshold voltage defined at the source end. It can be shown that when the threshold voltage near the drain end is taken into account, the saturation current becomes [40]

$$I_{dsat} = W v_{sat} C_{ox} \frac{(V_g' - V_t)^2}{V_g' - V_t + \alpha E_{sat} L},$$
$$V_g' = V_{gs} - I_{dsat} R_s, \tag{20}$$
$$\alpha \approx 1 + \frac{\gamma}{2\sqrt{2\phi_b}}$$
$$\approx 1 + \frac{C_d}{2C_{ox}}$$
$$\approx 1 + \frac{3t_{ox}}{2x_{bg}}. \tag{21}$$

from (20) I_{dsat} can be solved in (22), shown at the bottom of the page. Fig. 15 shows good agreement between the experimental data of conventional MOSFET and DD MOSFET using (22) and (10). Since α is always larger than one, MOSFET with smaller x_{bg} results in smaller I_{dsat}. Though DD MOSFET usually has higher effective mobility due to less channel doping concentration as seen in Fig. 13 thereby improving I_{dsat}, α is usually a stronger factor because from (20) it can be shown that the combined effect of the bulk charge and the mobility are determined by the ratio of α/μ_{eff} and the variation of α is usually larger to control the short-channel effect. It can be argued that the I_{dsat} comparison should be made at $L_{\min}$, not at a fixed L. Since smaller x_{bg} improves $L_{\min}$, I_{dsat} at $L_{\min}$ is usually larger for device with smaller x_{bg} because the dependence of I_{dsat} on L is stronger than a in (20). Combined with improved gate capacitance, the improvement in speed by delta-doping can be significant.

Comparing I_{dsat} at $L_{\min}$ hence the same degree of V_t roll-off only addresses part of the issue for device and circuit design. In many application such as memory and low-power circuits where the off-state leakage I_{off}, in addition controlling V_t roll-off, is important. The impact of small x_{bg} on I_{dsat} is relatively minor as compared with the its impact on I_{dsat}/I_{off} due to increase in S. For a maximum tolerable I_{off}, the required V_t is

$$V_t = \frac{S}{60} \ln\left(\frac{I_{th}}{I_{off}}\right) + \delta. \tag{23}$$

$$I_{dsat} = \frac{1}{2(R_s + W v_{sat} C_{ox} R_s^2)} \Big[V_g - V_t + 2W v_{sat} C_{ox}(V_g - V_t)R_s$$
$$- \sqrt{(V_g - V_t)^2 + 2(V_g - V_t)\alpha E_{sat} L + 4\alpha E_{sat} L W v_{sat} C_{ox}(V_g - V_t)R_s}\Big]. \tag{22}$$

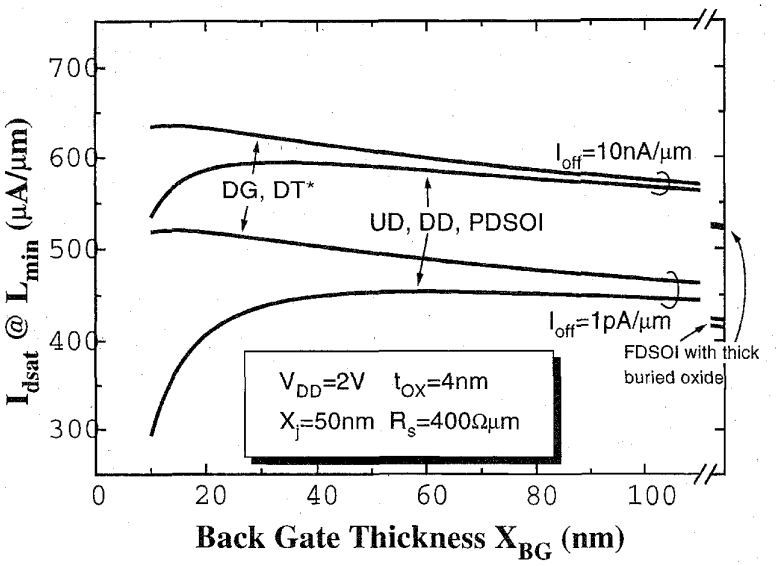

Fig. 16. For the same I_{off}, I_{dsat} can be calculated using (11), (22), and (23). Though smaller $L_{\min}$ can be obtained by having smaller x_{bg}, the increase in subthreshold swing has significant impact on I_{dsat}. Having subthreshold swing independent of x_{bg} scaling, DG and DT MOSFET's are immune to S degradation. *Scale does not apply to DT MOSFET due to limitation in V_{dd}.

Substitute (23) into (22) and using S in (1) and (2), δ in (9), and $L_{\min}$ in (11), we obtain I_{dsat} shown in Fig. 16, in which we have assumed the gate workfunction is adjusted to give the desired V_t. The smaller the I_{off} requirement, the worse the I_{dsat} degradation by scaling x_{bg}; for larger I_{off}, the impact of x_{bg} scaling on I_{dsat} is less severe. In some cases I_{off} can place a more stringent constraint than V_t roll-off in device design. Fig. 17 gives one such example: Devices A and B have the same $L_{\min}$ and $V_t - \Delta$. Though they should have similar degree of V_t roll-off, they have orders of magnitude difference in I_{dsat}/I_{off}. Suppose Δ can be adjusted using workfunction engineering to give desirable V_t values, at the same I_{dsat} device A has more than two orders of magnitude less I_{off} than device B. For applications whose I_{off} is not a major concern but V_t roll-off control is vital, DD MOSFET is a good candidate. DD MOSFET is also the choice when one wants to reduce oxide stress and oxide leakage. DG MOSFET excels in I_{dsat}/I_{off} due to its nearly ideal S regardless of x_{bg}. DT MOSFET is even superior to DG MOSFET when V_{dd} less than 0.6 V because V_t can be varied. PDSOI MOSFET is also competitive in I_{dsat}/I_{off} when the dynamic floating-body effect is considered because in fast V_g ramp S is close to its ideal value of 60. FDSOI MOSFET, due to its difficulty in $L_{\min}$ scaling, has poor I_{dsat} at a given I_{off} regardless of the nearly ideal S.

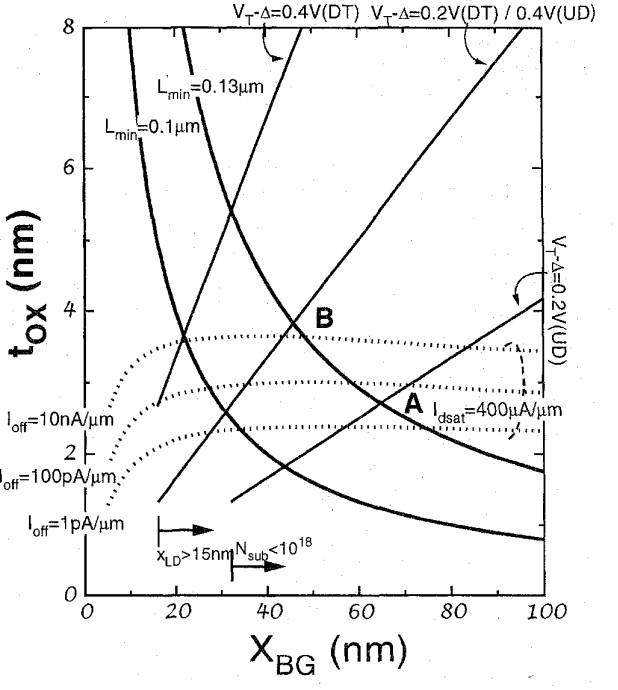

Fig. 17. The design space of t_{ox} and x_{bg} as constrained by V_t roll-off, and by I_{dsat}/I_{off} ratio. Device A and B have the same $L_{\min}$ in terms of V_t roll-off. If A is a UD MOSFET and B is a DD MOSFET, they also have the same $V_t - \Delta$. However device A can achieve larger I_{dsat}/I_{off} ratio than device B. Therefore in some cases the constraint imposed by I_{off} requirement might be more stringent than by V_t roll-off. Scaling t_{ox} always gives advantage for both but increases I_g.

V. Capacitances and Relative Gate Delay

A comparison of the relative gate delay is shown in Table I. The devices are compared using the following set of parameter sets are: $V_{dd} = 1.5$ V, $t_{ox} = 30$ Å, $x_j = 400$ Å (DG MOSFET $t_{\rm Si} = 500$ Å), $R_s = 500\,\Omega\,\mu$m, dual-polysilicon gate MOSFET $\Delta = V_{fb} + 2\phi_b \approx 0$ (except for DG MOSFET). The device parameters The devices I_{dsat} and relative gate delay τ are compared at a fixed $L = 0.125$ μm and at $L_{\min}$. The capacitance components in the unloaded case are estimated as in [41]: 67% from gate capacitance,

TABLE I
RELATIVE GATE DELAY ANALYSIS

MOSFET	$L_{\min}$	I_{dsat}		$C(C_g \propto L_{\min}^{-1})$		$\tau = \sigma C/I_{dsat}$			
	$V_t - \Delta = 0.4$	$L_{\min}$	$0.125\,\mu$	C_g	C_j	@$L_{\min}$		@$0.125\,\mu$m	
						$C_{int} = 0.2$	$C_{int} = 2^*$	$C_{int} = 0.2$	$C_{int} = 2$
UD	0.125	1		1	0.3	1	1	1	1
DD	0.1	1.07	0.92	0.8	0.1#	0.69	0.82	0.94	1.02
UD SOI	0.125	1.11†		1	0.05	0.75	0.83	0.75	0.83
DD SOI	0.1	1.25†	1.09†	0.8	0.05	0.56	0.69	0.76	0.85
FD SOI	~0.18	0.98	—	1.4	0.05	1.12	1.07	—	—
DG	0.125*	2		2	0.05	0.75	0.68	0.75	0.68

‡V_{dd} = 1.5 V, t_{ox} = 30 Å, x_j = 400 Å, $R_s = 500\,\Omega\,\mu$m, dual-polysilicon gate MOSFET ($\Delta = V_{fb} + 2\phi_b \approx 0$). DT MOSFET is not included in this table because of the chosen V_{dd} is not applicable.

†Estimated by average V_b = 0.2 V. ΔV_t is calculated as in [20].

*t_{Si} = 500 Å, $V_t - \Delta$ = 0.2. Assume gate workfunction is adjusted for 0.4 V V_t.

#Smaller C_j due to reduced overlap between delta-doped layer and source/drain (Fig. 1).

20% junction capacitance, and 13% interconnect capacitance. τ under larger load capacitance is also compared. PDSOI MOSFET are further divided into UD PDSOI and DD PDSOI to highlight the impact of channel doping engineering and the dynamic floating-body effect. For simplicity, an average V_b change of 0.2 V when the transistor is switching is used for modeling the dynamic floating-body effect. The coupling ratio from V_b to V_t is 0.5 for UD and 0.75 for DD [20]. I_{dsat} of every device is normalized to that of the UD MOSFET of $L = 0.125$ μm. All the capacitances are normalized to the gate capacitance of UD MOSFET of $L = 0.125$ μm. The junction capacitance of DD MOSFET is smaller than that of the UD MOSFET by assuming the delta-doping is only under the channel (Fig. 1). The relative gate delay τ is calculated based on these assumptions. By comparing UD and DD MOSFET, one might note that the bulk charge effect and the mobility effect gives a total of 8% reduction of I_{dsat} for DD MOSFET. But approximately 15% of I_{dsat} is gained by smaller $L_{\min}$, therefore 5–10% net improvement in I_{dsat} can be obtained. Combined with smaller C_{ox} and C_j, DD MOSFET can be significantly faster than UD MOSFET. However, when compared at the same L, DD MOSFET might be even slower. A 10% improvement in I_{dsat} can be obtained by the dynamic floating-body effect for UD PDSOI, and 15% for DD PDSOI, based on the above model. This make DD PDSOI the fastest device in some categories, and the improvement in speed ranges from 15–40%, depending on how the comparison is made. It should also be mentioned that the improvement in τ by the dynamic floatingbody effect also depends on the duty cycle and the output load, both of which are not considered in the table for simplicity. FDSOI suffers from its scalability in speed performance. DG MOSFET, with its $2 \times I_{dsat}$ (and $2 \times C_g$), has decent performance in every category and excels when driving large output load.

VI. CONCLUSION

All major advanced MOSFET device structures are studied and compared. We use a framework of analytical models, calibrated by experimental data and device simulation, to analyze these device structures. Based on these models, the interdependence of the device parameters, such as t_{ox}, V_t, S, I_{dsat}, I_{off}, etc., can be quantified and the design space can be explored. The usefulness of the models are demonstrated in studying the threshold voltage, the subthreshold swing, the short channel effect, the effective mobility, the drain saturation current, and the relative gate delay. The major conclusions are summarized below:

- MOSFET with uniform channel doping has lower I_{off} than delta-doped MOSFET—an important trait for some applications. UD MOSFET of 0.09 μm $L_{\min}$ can be achieved with $t_{ox} = 30$ Å, $N_{sub} = 10^{18}$ cm^{-3}, $x_j \approx 200$ Å, and $V_t \approx 0.35$ V.
- Ideal retrograded (delta) doping profile can improve $L_{\min}$ by 20%. For $t_{ox} = 30$ Å, $x_j \approx 200$ Å, $L_{\min} = 0.07$ μm can be achieved.
- Fully-depleted SOI MOSFET is difficult to be scaled down below 0.15 μm with satisfactory short-channel effect.
- Partially-depleted SOI MOSFET has the same potential for scaling as bulk MOSFET, but can improve speed by 15–40%, depending on load capacitance, channel doping profile, etc. Dynamic-threshold MOSFET provides the largest I_{dsat}/I_{off} at low V_{dd} operation.
- Double-gate MOSFET provides the largest I_{dsat} per unit channel width among all devices in this study. It can achieve small $L_{\min}$ with relatively thick t_{ox} (~50 Å). It also features high carrier mobility for small $L_{\min}$ devices. x_{bg} effect will affect I_{dsat} but not S.
- DD MOSFET is suitable for applications where larger current drive (small $L_{\min}$), good digital design noise margin (V_t roll-off control) are needed but the stand-by power consumption can be relaxed, such as in high-end microprocessors.
- For applications where I_{off} is important such as devices in memory array, UD MOSFET is better than DD MOSFET in terms of I_{dsat}/I_{off}. Though difficult to fabricate in random logic, DG MOSFET, with ideal S, might first appear as devices in periodic memory array.
- The speed advantage of PDSOI MOSFET can be further enhanced by capitalizing on its lack of the body effect and the presence of the dynamic-floating body effect. DT MOSFET can be a good candidate for ultra-low-voltage

applications where even multiple V_t technology is not adequate.

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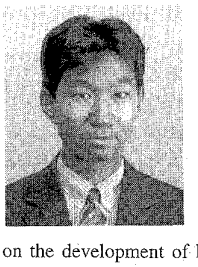

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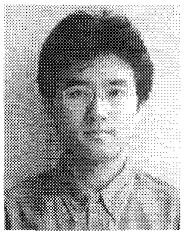

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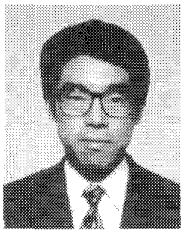
He joined Fujitsu Laboratories Ltd. in 1990, where he has been engaged in the research on the highly-scaled MOS devices including SOI devices. From 1994 to 1995, he was a visiting industrial fellow in the University of California at Berkeley, where he studied the device physics of MOSFET's. He is currently working on the physics and technology of 0.1 μm CMOS devices.



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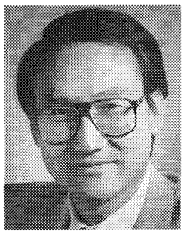
Mr. Yoshida is a member of the IEEE Electron Devices Socieety.



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