True Figure of Merit (FOM) of a Power Semiconductor Switch

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True "Figure of Merit (FOM)" of a Power Semiconductor Switch

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Abstract

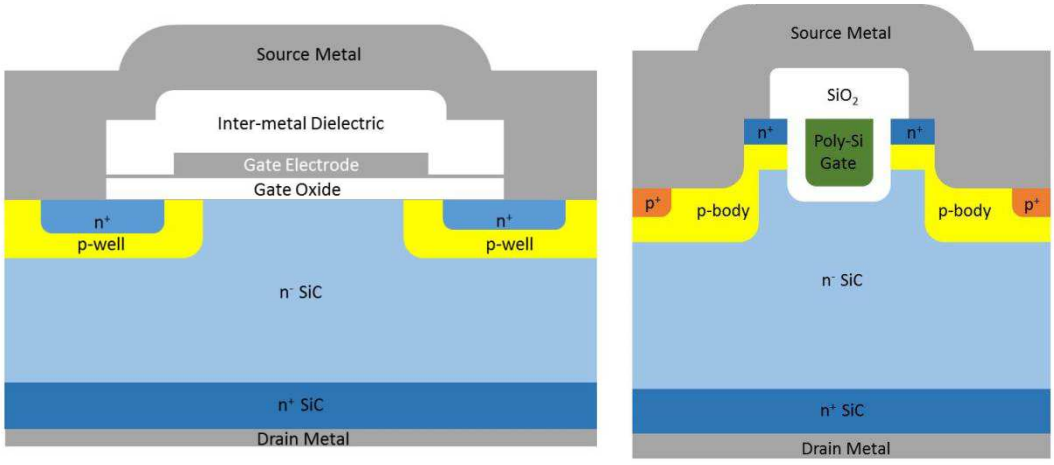
Wide Band Gap (WBG) semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are known to be superior materials for the fabrication of power electronics switching devices compared to the industry work-horse silicon. This advantage primarily stems from wider energy bandgap, higher electric field strength for avalanche breakdown, and improved thermal conductivity of SiC and GaN semiconductors compared to silicon. This paper reviews the various "Figures of Merit (FOM)" proposed in the literature for the WBG power semiconductors. Unipolar power transistors with MOS channel conduction as well as transistors that employ two-dimensional electron gas (2DEG) channels are considered. A true FOM for a power semiconductor switching device needs to take into account all electrical power losses and thermal limitations. A new Safe Operating Area (SOA) limit that relates material defect density (D_{it}) to the switching current density (J_{on}) for a specified maximum junction temperature limit (T_{jmax}) is proposed as the true FOM for a power semiconductor switching device.

I. Introduction

It has been well-known for more than two decades that power electronic switching devices made from Wide Band Gap (WBG) semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) offer much lower on-state resistance ($R_{DS(on)}$) than comparable silicon power devices because of their superior electrical and thermal conductivities, and breakdown field compared to silicon [1, 2]. Single-chip SiC JBS power diodes rated up to 1,700V/25A [3], and more recently, 1,700V vertical GaN Schottky power diodes [4] have been introduced into the commercial market in limited quantities. Although these devices are finding applications in computer/telecom power supplies, motor control, and smart grid [5-7], serious concerns pertaining to long-term reliability of these devices in compact power converters under stressful field operating conditions remain [8]. For example, majority of WBG commercial power diodes are not dv/dt- and avalanche-rated, and the data sheets rarely mention of the Safe-Operating Area (SOA), especially at elevated temperatures.

For high efficiency and high-frequency power conversion, MOS-controlled power semiconductor switches are needed [9]. Power MOSFET is the basic building block for other MOS-controlled high-power switches such as IGBT's. The "best-in-class" commercial 1,200V SiC power DMOSFET's [10] and trench-gate MOSFET's [11, 12] have a specific on-state resistance $R_{sp,on}$ of 3.7 mΩ-cm^2 and 2.6 mΩ-cm^2, respectively and a single-chip current rating of 50 amps. Figure 1 illustrates the unit cell cross-

sections of these devices; the unit cell pitch is typically in the range of 10 to 12 microns for a 1,200V rated device. In the current state-of-the-art SiC power MOSFET's, the gate dielectric suffers from reliability problems, especially at elevated temperatures above 150°C. For example, gate MOS threshold voltage has been found to be unstable with prolonged gate voltage stress [13]. Low MOS inversion channel mobility and poor gate dielectric reliability have been largely attributed to a high density of interface states, especially in the upper half of the bandgap close to the conduction band edge. Recently, AlON/SiO_2 gate dielectric films deposited by CVD technique have been shown to improve both MOSFET performance and reliability of planar as well as trench-gate



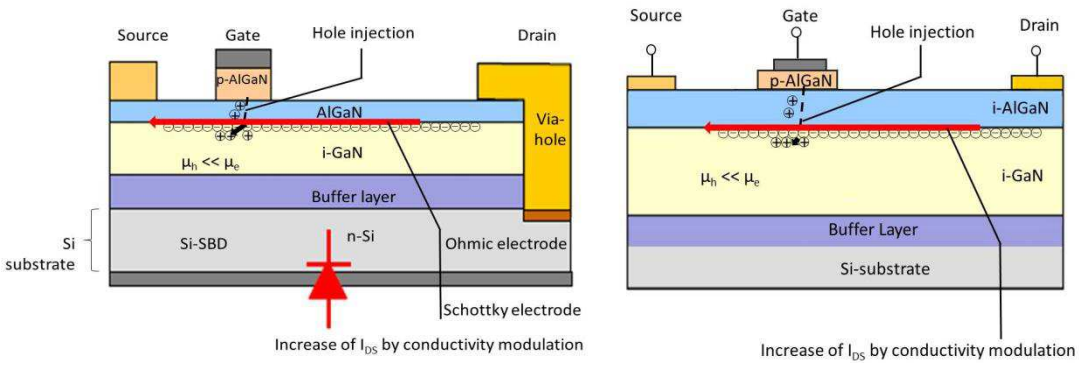
(a) (b)

Figure 1: Cross-sections of "industry-best" normally-off vertical SiC power (a) DMOSFET and (b) trench-gate MOSFET unit cells [10-12].

devices [14]. For "industry-best" 1,200V SiC power MOSFET's, measured reverse leakage currents are typically high; and, devices are not rated for dv/dt and avalanche capabilities, especially at elevated temperatures. At the time of this writing, SiC power MOSFET's have not been proven reliable in power converter applications and their application is limited to junction temperatures below 150°C [15].

The best-in-class commercial GaN power transistors are rated at 600V and have single-chip current ratings of < 20 amps [16]. These gate-controlled normally-off GaN-on-Si power switches are lateral in configuration as shown in Figure 2, have a gate threshold voltage of ~ 1.5V, and a specific on-state resistance $R_{sp,on}$ = 2.5 mΩ-cm^2. The device utilizes hole-injection at the gate electrode from the p-AlGaN to the AlGaN/GaN hetero-junction, which simultaneously increases the electron density in the channel, resulting in a dramatic increase of the drain current due to conductivity modulation. A recent advance in this transistor technology pertains to an integrated Schottky diode that provides the reverse-conducting current path during switching [17]. Using GaN lateral enhancement-mode switches, a three-phase motor drive inverter rated at 900 Watts and switching at 6 kHz was demonstrated with a switching energy efficiency of 99.3% [18].

For "industry-best" lateral GaN power transistors, the measured reverse leakage currents are high, especially at elevated temperatures; device breakdown is primarily caused by breakdown at the buffer-substrate and/or at the device surface, and hence, these devices are not optimized for power switching. Furthermore, these devices are not rated for dv/dt and avalanche capabilities; and, are 3-5X more expensive than silicon power transistors with identical current ratings.

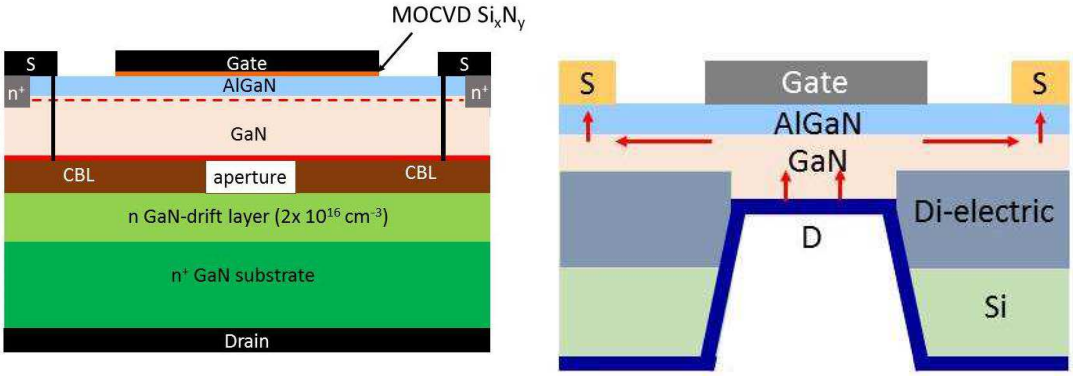


(b) (b)

Figure 2: Cross-sections of "industry-best" normally-off lateral GaN-on-Si lateral power transistor (a) with and (b) without integrated body Schottky diode [16-18]

To the best of our knowledge, there is not a single silicon discrete lateral high-power switch available in the commercial market. This lack of market pull for a lateral power switch is largely due to the fact that lateral power devices are not scalable to higher voltages and currents, and are not cost-effective and reliable in power converter circuits [9]. Hence, vertical power transistor technology on free-standing bulk n^+GaN substrates must be developed.

Previous attempts to develop vertical power transistors in GaN using current aperture [19] and backside etching [20] technologies have not resulted in cost-effective and reliable and power switching devices. The CAVET device [19] shown in Figure 3(a) employs Mg-ion-implanted current blocking layer (CBL), and is similar in its operation



(a) (b)

Figure 3: Cross-sections of state-of-the-art vertical GaN power transistor devices (a) normally-on CAVET transistor on free-standing GaN substrate and (b) normally-on GaN-on-Si power transistor fabricated using substrate etch-back technology

to the static induction transistor (SIT) in silicon [21]. Silicon SIT technology has not been commercially successful because of poor performance, reliability, and manufacturing issues. It is unlikely that GaN-based SIT-type devices can overcome the fundamental issues that have rendered silicon SIT's impractical for high-volume power electronics applications. The vertical GaN-on-Si power transistor structure shown in Figure 3(b) [20] suffers from the same issues as lateral GaN-on-Si power transistors currently deployed in the commercial market – severe manufacturing and reliability problems. The basic construction of the device structure does not allow for heat to diffuse easily from active regions of the device, and thus causes severe self-heating and leads to thermal

destruction. Hence, a commercially viable and scalable vertical power transistor technology on free-standing GaN substrates is needed to adequately address these challenges.

II. Power Semiconductor "Figure of Merit (FOM)"

Traditionally, power semiconductor devices (and power electronics circuits) have been developed with a primary focus on achieving the highest power conversion efficiency [22]. This "performance-driven" practice is about to change as the end-customers are now demanding, in addition to energy-efficiency, improved field-reliability of power converters at reduced cost [23]. A paradigm shift in power converter design is needed in order to assure its field-reliability. A systematic approach to "reliability-driven" power technology development is also likely to lead to dramatic reduction in cost and significant performance gains; however, such a methodology is yet to be realized. On the other hand, for more than three decades, microprocessor (and other signal electronics) chips have been developed to guarantee at least 100,000 hours of active field-operation in a personal computer (PC) environment [24]. It is our contention that a similar "built-in" reliability design approach is exactly what is needed to further advance semiconductor power switching in order to meet the challenges of 21st century electric transmission and distribution infrastructure [25].

A power semiconductor switch operates quite differently from an analog or a digital semiconductor switch [9]. It is expected that when the power semiconductor switch is turned on, it should present the least electrical resistance in order to minimize the ohmic power loss; in the off-state, it should conduct zero leakage current with a very high avalanche breakdown voltage. Shenai first proposed the specific on-state resistance R_{sp} [1] and input switching charge Q_g [2] as the "Figures of Merit (FOM)" in order to assess the value of a given power semiconductor technology for power converter applications; these two FOM are respectively given by:

$$R_{sp} = \frac{4V_B^2}{\varepsilon_s \mu E_c^3} \qquad (1a)$$

$$Q_g = C_{iss} V_{gs} \qquad (1b)$$

where V_B is the breakdown voltage, ε_s is the permittivity, μ is the drift-region mobility, and E_c is the critical electric field strength at avalanche breakdown of the semiconductor material; the input switching charge assumes an MOS-controlled power switch where C_{iss} is the net input capacitance at zero gate bias voltage and V_{gs} is the gate-to-source voltage needed to fully control the "on" and "off" switching transitions. For a given power converter application, both $R_{sp,on}$ and Q_g must be minimized in order to obtain the highest electrical conductivity and the lowest input power loss. These two FOM have been adapted by the silicon power semiconductor industry to successfully optimize the power switching technology; since their first introduction more than two and half decades ago, $R_{sp,on}$ and Q_g have become "industry standards." A third FOM was also proposed by Shenai [1] which takes into account electrical and thermal conductivities in addition to avalanche breakdown field, and is given by:

$$Q_{F2} = \kappa \sigma_{sp} E_c \qquad (2)$$

where κ is the thermal conductivity and $\sigma_{sp} = 1/R_{sp}$ is the specific electrical conductance. Subsequently, a number of authors [26-28] have proposed various FOM to characterize power semiconductor switching devices. The high-frequency FOM proposed by Baliga [26] minimizes the chip area by considering the input switching power in addition to conduction power loss, and hence, it is really a combination of R_{sp} and Q_g first proposed by Shenai [1]. Note that BHFFOM does not include the output switching power. Recently, it has been shown that the output switching power is a significant portion of the total power loss, especially at higher switching frequencies using power switches with smaller capacitances [29, 30]. The FOM proposed by Kim et al [27] for high-frequency power switching, NHFFOM, although considers the output capacitance of the switch in addition to the on-state conduction power loss, it does not directly relate the output switching power loss to semiconductor material parameters, and there is no mention of the input switching power loss. Furthermore, the analysis by Kim et al optimizes the power switch die area by neglecting the input power loss. Huang [28] has proposed four FOM's; the first three FOM's (HDFOM, HMFOM, and HCAFOM) essentially convolve around specific on-state resistance and gate charge, and do not account for the output switching power loss or consider thermal limitations. The last FOM proposed by Huang, i.e., HTFOM, does refer to the semiconductor thermal conductivity; however, only heating due to on-state conduction and input switching power losses at the junction die attachment are included.

Thus, it is clear that there is a need for a "true" FOM for a power semiconductor switching device that considers all of the power loss mechanisms in addition to the thermal limitations of the semiconductor material and the package. This is particularly important given that superior high-voltage high-frequency SiC and GaN power devices capable of much higher temperature operation than silicon power devices are being introduced into the commercial market. At the time of this writing, both lateral and vertical power devices are being developed in SiC and GaN materials; lateral GaN power transistors are mostly based on two-dimensional electron gas (2DEG) formed at the AlGaN/GaN hetero-structure due to the polarization charge. Figure 4 illustrates the electric field profiles in the reverse-blocking mode for typical vertical and lateral gate-

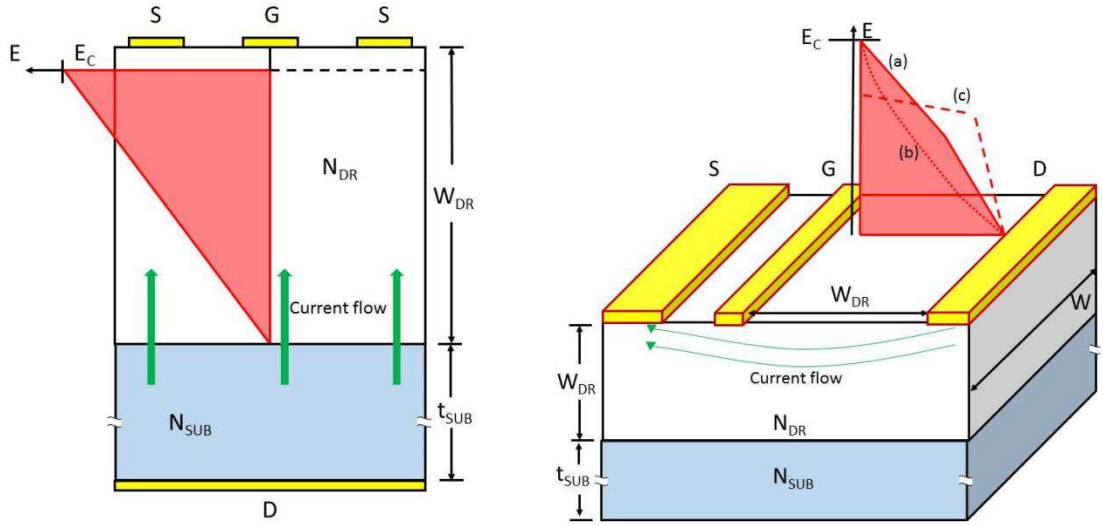


Figure 4: Schematic electric field profiles in the reverse blocking mode and current flow lines in typical (a) vertical-geometry and (b) lateral-geometry power switching devices.

controlled power switching devices; also shown are the current flow lines in the on-state. The peak electric field for a vertical power switch typically occurs near the top surface of the chip; for a lateral device, the electric field profile can be significantly adjusted using RESURF [31] and lateral charge control concepts [32]. The optimum breakdown and on-resistance performance is obtained when the drift-region parameters are adjusted such that the breakdown occurs by avalanche mechanism. The specific on-state resistance for a vertical device is given by eqn. (1a) and that of the lateral power switch with 2DEG conduction is given by:

$$R_{spl} = \frac{V_B^2}{q\mu_s n_s E_c^2} \qquad (3)$$

where μ_s and n_s are the mobility and sheet carrier density of the 2DEG, respectively in the lateral conduction channel. The results of calculations for various semiconductors are plotted in Figure 5 using the latest set of material parameters [1, 33-37]; for GaN, vertical devices that employ bulk material conduction are also evaluated. As the lateral devices

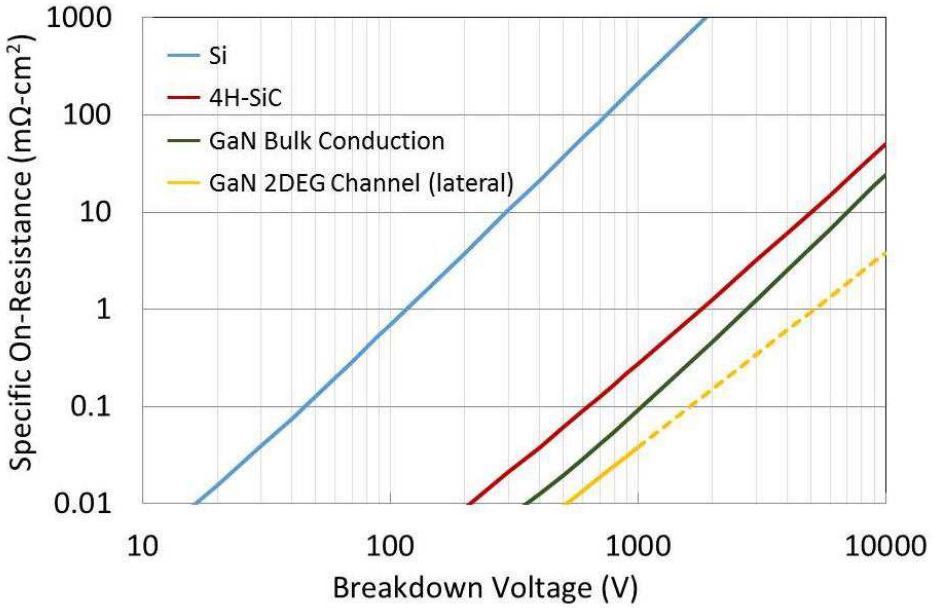


Figure 5: Calculated specific on-state resistance vs. avalanche breakdown for vertical and lateral power devices made in silicon, 4H-SiC and GaN materials.

are typically no scalable to higher voltages and higher currents, we expect GaN lateral power transistors to be limited to below 1,000 volts and 25 amps single-chip current ratings. The calculated values of various FOM are listed in Tables 1(a) – 1(c); also included are Johnson's [38] and Keye's [39] FOM although they are not relevant for power switching applications. In our calculations, accurate doping dependencies of electron mobility and critical field strength for avalanche breakdown are used.

Table 1(a) Calculated FOM's for various power semiconductor devices.

Material		Si	4H-SiC	GaN
BM ($\varepsilon_s \mu E_C^3$)		4.26E+20	1.83E+23	2.88E+23
BHM (μE_C^2)		1.22E+14	6.30E+15	9.80E+15
JM ($E_c v_{sat}/2\pi)^2$		9.09E+23	3.64E+26	6.87E+26
KM $\kappa(v_{sat}/\varepsilon_s)^{1/2}$		1.39E+03	6.46E+03	3.85E+03
Q_{F2} ($\kappa\sigma_{sp}E_C$)	V_B			
	1,000	1.76E+06	5.58E+10	4.51E+10
	10,000		2.32E+08	5.33E+08
	20,000		4.20E+07	1.34E+08
Q_{Fl} ($\kappa\sigma_{spl}E_C$)	V_B			
	1,000			1.99E+11
	10,000			1.99E+09
	20,000			4.99E+08

Table 1(b) Specifc on-state conductance of lateral GaN power transistors using eqn. (3)

V_B	σ_{spl} ($q\mu_s n_s E_c^2/V_B^2$)
1,000	26283.015
10,000	262.83015
20,000	65.7075375

Table 1(c) Normalized values of FOM's for semiconductors.

Material		Si	4H-SiC	GaN
BM ($\varepsilon_s \mu E_C^3$)		1	429.88	674.98
BHM (μE_C^2)		1	51.85	80.67
JM ($E_c v_{sat}/2\pi)^2$		1	400.00	756.25
KM $\kappa(v_{sat}/\varepsilon_s)^{1/2}$		1	4.66	2.78
Q_{F2} ($\kappa\sigma_{sp}E_C$)	V_{BD}			
	1,000	1	3.17E+04	2.56E+04
Q_{F2} ($\kappa\sigma_{sp1}E_C$)	V_{BD}			
	1,000			1.13E+05

III. Summary and Conclusions

Various "Figures of Merit" (FOM's) proposed for power switching devices are critiqued and it is shown that there is a need to develop a "true" FOM that accounts for various forms of power losses and also considers thermal limitation of the semiconducting material and that of the package. Both vertical and lateral power devices that employ bulk charge conduction as well as 2DEG channel conduction are studied. It is shown that for voltages above 600V and single-chip current ratings > 20 amps, there is significant opportunity to develop vertical GaN power devices with 2DEG channels; vertical GaN 2DEG devices are shown to have nearly an order of magnitude improved overall power switching performance than the lateral GaN 2DEG power devices.

An important measure of robustness of a power semiconductor switch in power electronics switching is the Safe Operating Area (SOA). The SOA of a power semiconductor device refers to voltage and current limits within which the device can be safely switched. The SOA deviates from rectangular shape due to thermal heating as shown in Figure 6; the loss of SOA occurs when power dissipation is at its maximum and is a function of several parameters including switching frequency, duty ratio, dv/dt and di/dt among others. Provided bond wires and die-to-package interface remain intact, and

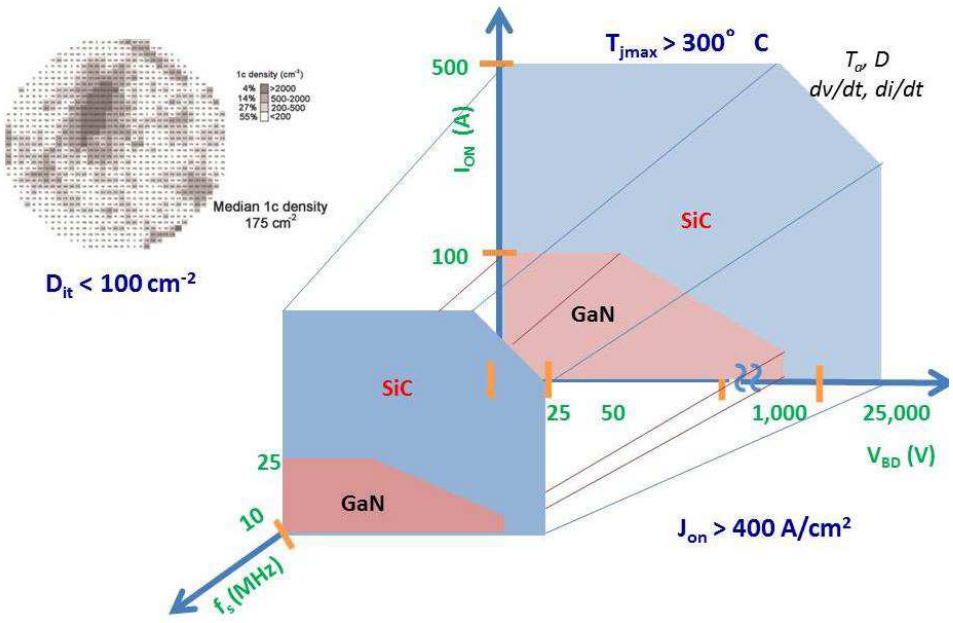


Figure 6: A proposed new "Figure of Merit (FOM)" for a power semiconductor switching device that relates the defect density, D_{it} in the drift-region of the device to the current density, J_{on} that can be reliably switched in given power converter under field-operating conditions at a specified junction temperature, T_{jmax} that the semiconductor chip can tolerate under "long-term" repetitive switching conditions

assuming isothermal die boundary conditions, it is known that "hot spots" occur locally during power switching and can lead to current filamentation and local "burn outs" primarily caused by Joule heating [40-42]. Maximum power dissipation occurs within the drift-region of the device where the electric field is high. The challenge is then to rapidly remove heat away from the local "hot spot" to avoid material burn-out; the thermal time

constant must be small (typically less than a microsecond), and hence, substrate must be thinned down so that the cooling surface is brought closer to the drift-region of the device. As shown in Figure 6, the SOA of a GaN power device is expected to be smaller than that of a SiC power device primarily due to its relatively lower thermal conductivity. Also, because of the direct energy bandgap of GaN, minority carrier lifetime is small; hence, conductivity modulation of the drift-region is difficult; and, bipolar-mode power devices are not likely in GaN. Therefore, for higher voltage (above few kilo volts) and higher current (above 100 amps), it is our contention that the vertical SiC power devices hold the greatest promise.

As shown in Figure 6, the SOA of a semiconductor power switch is reduced as the power switching frequency is increased. This is largely due to the fact that at higher switching frequencies, switching power losses in the semiconductor power device increase. As is well-known in the literature [9, 22], SOA can be defined for single pulse as well as repetitive switching conditions. As the switch failure is caused by local temperature rise, separate SOA diagrams can be generated for the same semiconductor power switch for varying switching current densities, J_{on}. Hence, T_{jmax} must be specified as a function of J_{on} at a given ambient temperature, T_a of the power converter circuit. While this approach has had reasonable success with silicon power devices where the material crystal defect density is below 1 per cm^2, the same approach may not be valid in case of SiC and GaN power devices with several orders of magnitude higher defect densities. Assuming that crystal defects are uniformly distributed in the space-charge region of the device, SOA limits may have to be evaluated as a function of the net defect density, D_{it}. A revised SOA diagram shown in Figure 6 is proposed as a new "Figure of Merit (FOM)" that represents the amount of current density that can be reliably switched under field operating conditions at a specified T_{jmax} for a semiconductor power switching device with a space-charge region containing a net crystal defect density of D_{it}. It is therefore imperative that the revised SOA must be evaluated for SiC and GaN power devices and "bench-marked" against silicon power devices with identical voltage and current ratings, and packaging configurations.

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