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A radiation hard bandgap voltage reference for the ARCADIA project

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Abstract: This work presents the design and characterization results of a radiation hard bandgap reference circuit fabricated in a 110nm CMOS technology for the Main Demonstrator chip of the ARCADIA project. The design, based on a current-mode approach in order to be able to output a smaller than 1.2V reference voltage, employs diode-connected MOSFETs instead of BJTs to enhance the radiation hardness and a second amplifier to improve the current mirror of the output branch and therefore the line regulation of the circuit. This paper describes the features of the circuit and its measured results.

Keywords: Analogue electronic circuits, Radiation-hard electronics.

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Contents

1 Introduction

A bandgap voltage reference (BGR) is a block of paramount importance in both analog and mixed-signal circuits: it is used to provide a reference voltage, constant and independent, as much as possible, of process variations, supply voltage, and temperature. It combines an element that shows characteristics Proportional To the Absolute Temperature (PTAT) with another one that features Complementary To the Absolute Temperature (CTAT) characteristics using a circuit that is insensitive to variations in the supply voltage or to process parameter fluctuations. Conventional BGR architectures, also named voltage-mode bandgap, generate an output voltage of about 1.2V [1], which is close to or even higher than the supply voltage of CMOS technologies with a minimum channel length equal to or lower than 130nm. However, several solutions employing a current-mode approach have been implemented allowing sub-1V operation [2]. This work will focus on the design of a current-mode bandgap reference that will be used in the ARCADIA (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays) project, which aims at developing a sensor with fast charge collection, a scalable readout and low-power capabilities. Toward this goal, the collaboration has worked on the first main demonstrator: a low-power, high-density (25µm pitch) pixel matrix of CMOS monolithic sensors developed for high-energy physics applications, astrophysics experiments, and medical imaging. Both applications pose some additional requirements to the design of the circuit. The high fluences expected at the future colliders advise against using bipolar transistors, due to their sensitivity to bulk damage. On the other hand, deep-submicron CMOS technologies, thanks to the reduced thickness of the gate oxide and the addition of some layout techniques, have demonstrated to be resistant to hundreds of Mrad of TID (total ionizing dose) and can be used to implement a radiation-tolerant bandgap voltage reference [3]. The circuit described in this work is based on enclosed-layout, diode-connected MOSFETs biased in weak inversion region, which, together with DTMOST devices, are devices that have been proven to be inherently radiation hard [4]. The design also includes two programmable resistors that make it possible to adjust the voltage-to-temperature slope and the absolute value of the reference voltage respectively. This work discusses the main design solutions and some relevant simulation and measurement results.

2 Circuit description and simulation results

The schematic of the bandgap is shown in Figure 1 and targets the output voltage of 600mV. As mentioned in the previous section, the scheme employs diode-connected MOSFETs M3 and M4, biased in the sub-threshold region, instead of BJTs to improve its radiation hardness [5]. These devices are biased with the same current but have a different aspect ratio, in particular, $(W/L)_{M4} = N \cdot (W/L)_{M3}$. In this design, N has been chosen equal to 8. The amplifier connected to the drains of M1 and M2 allows the drains of M3 and M4 to stay at roughly the same voltage. The current in M2 is the sum of two components, the one that flows in M4 and the one that flows in R1. The former, which is proportional to the absolute temperature (PTAT), is given by the voltage drop across resistor R0 divided by its resistance, while the second, which is complementary to the absolute temperature (CTAT), can be calculated as V_{GS3} divided by R1. By properly choosing the values of R0 and R1, the current in M2, which is mirrored in the output branch by M5, can be tuned in order to minimize its temperature dependence. Thus, the output voltage of the circuit is:

$$V_{OUT} = \left[\frac{V_{GS3}}{R_1} + \frac{V_T \cdot ln(N)}{R_0} \right] \cdot R_2. \tag{2.1}$$

The scheme also includes an additional amplifier, maintaining the same V_{DS} for M2 and M5, therefore improving the performance of the M2-M5 current mirror. The resistor R0 can control the PTAT part of the equation, providing a well-defined trimming point for user compensation of the reference voltage vs temperature slope, $\partial V_{OUT}/\partial T$. The same function is done by resistor R2, which can be used to trim the absolute value of the reference voltage. Both programmable resistors R0 and R2 have been designed as a series of binary-weighted resistors, each of which has a pass-gate in parallel to short the resistor terminals.

The bandgap reference has been simulated in a temperature range between -40°C – 70°C and the nominal output voltage at room temperature (300K) is 597.2mV. The temperature-related parameters

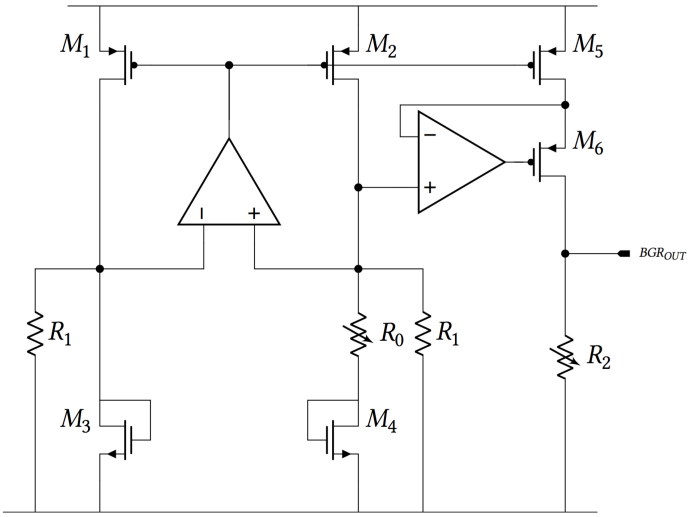

Figure 1. Schematic of the bandgap voltage reference.

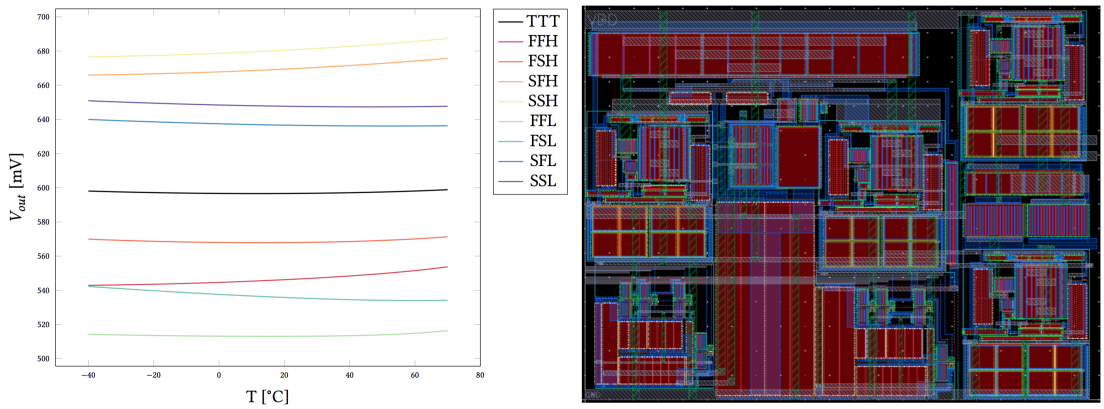

Figure 2. Simulated output voltage for all corners. The first two letters in the corner name indicate the MOSFET corner while the last one indicates the polyresistor corner (left) and layout of the bandgap voltage reference block (right). The layout has an area of 100×80m^2.

have been simulated for all MOSFETs corners plus two additional ones to account for polysilicon resistor variation, resulting in a total of 9 simulated cases, shown in Figure 2 (left). From these simulation results, together with the process and mismatch variations obtained in Monte Carlo simulations, a compensation range for resistors R0 and R2 of about ±25mV (referred to V_{OUT}) has been set. Figure 2 (right) shows the layout of the bandgap reference.

3 Measurement results

The circuit has been characterized in a climatic chamber in order to validate the expected behavior with temperature variations. Also, the effects of the voltage supply variation have been investigated at room temperature. The output voltage as a function of temperature for different values of the trimmable resistors R2 and R0 is shown in Figure 3 and Figure 4 respectively. In the temperature

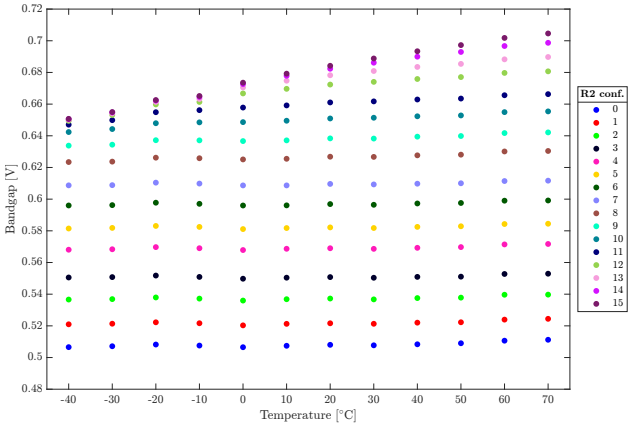

Figure 3. Measured Vout as a function of the temperature for different values of R2.

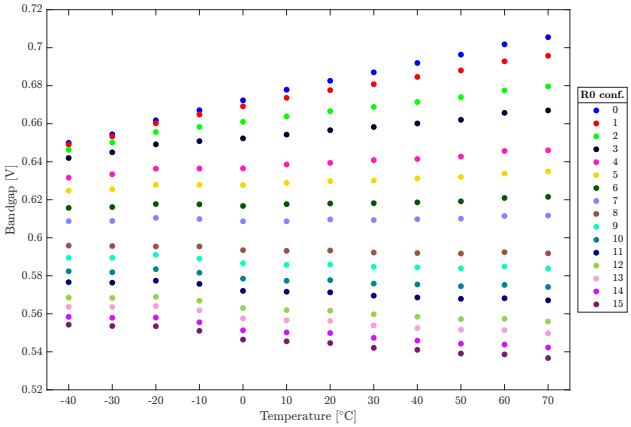

Figure 4. Measured Vout as a function of the temperature for different values of R0.

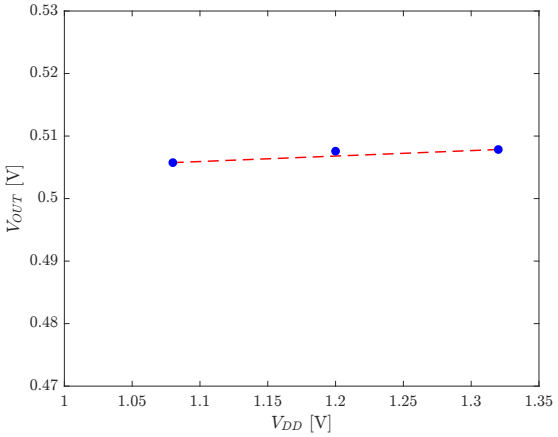

Figure 5. Measured Vout as a function of supply voltage variation in best case condition.

range considered in this characterization activity, which is -40°C – 70°C with steps of 10°C, the best configuration, shown in Figure 3, is obtained with R2 conf. = 7, which results in a variation of the output voltage as a function of the temperature of ≈1.85mV. A different sample has been tested for variation of Vdd between 1.08V and 1.32V (nominal value ±10%) leading to a maximum variation of 2.1mV, as shown in Figure 5.

4 Conclusions

A current-mode, bandgap voltage reference circuit with an output voltage of ≈600 mV and trimmable mean value has been designed in a 110 nm CMOS technology. Preliminary characterization results show a maximum variation of the output voltage as a function of the temperature of ≈1.85mV (best case) and as a function of the voltage supply of ≈2.1mV (considering a variation with respect to the nominal value of about ±10%). In this circuit, particular attention has been focused on designing the sensing elements, MOSFETs biased in weak inversion region, to minimize the effects of radiation

damage. In particular, the polysilicon gate has been extended along the channel sides mitigating the radiation induced effects of the charge build-up in the shallow trench isolations. An irradiation campaign of the bandgap circuit with X-rays up to tens of Mrad(SiO_2) is already foreseen to assess the radiation hardness of the circuit and the effectiveness of the layout technique implemented.

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