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Low-Noise Analog Channel for the Readout of the Si(Li) Detector of the GAPS Experiment

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***Abstract*—This work is focused on the design and the experimental characterization of an analog channel developed for the read out of lithium-drifted silicon detectors of the General AntiParticle Spectrometer experiment aimed at the search for dark matter. The instrument is designed for the identification of antideuteron particles from cosmic rays during an Antarctic balloon mission scheduled for late 2022. A low-noise analog front-end, featuring a dynamic signal compression to comply with the wide input range, has been designed in a commercial 180 nm CMOS technology. The channel was fabricated in 2018 and is the first building block toward the development of a multichannel readout ASIC. The paper will provide a description of the design criteria, the architecture of the channel, and a summary of the results of the experimental characterization.**

***Index Terms*—Low-noise, front-end, CMOS, dynamic signal compression.**

I. Introduction

THE identification of the nature of dark matter is one of the towering problems of early 21^{st} century physics. The GAPS (General AntiParticle Spectrometer) experiment has the objective of detecting indirect signatures of dark matter through the identification of low-energy antinuclei (<0.25 GeV/n), in particular rare antideuterons, from cosmic rays [1]. The experiment involves the use of a stratospheric balloon and consists of two types of detectors: the first is a plastic scintillator time-of-flight (ToF) system surrounding the second one, a tracker composed of 10 layers of 12×12 large-area lithium-drifted silicon, Si(Li), detectors [2]. In the GAPS particle detection scheme, first the ToF system measures energy deposition, velocity, and provides precise timing information of the incoming low-energy cosmic antinucleus. Next, the antinucleus enters the Si(Li) tracker and slows down in the tracker material, with energy depositions typically increasing as it slows, until it is captured by the target material forming an exotic atom, with the antinucleus orbiting the nucleus of the target material. This exotic atom de-excites emitting X-rays with characteristic energies that depend on the reduced mass of the nucleus-antinucleus system. Finally, the antinucleus annihilates with the target material, producing pions and protons. The lower-energy characteristic X-rays are in the 20-100 keV range, which can be detected by the Si(Li) detectors. Tracks from the charged annihilation products can be reconstructed using both the tracker and ToF, providing measurements of these products' energy depositions and velocities. Together, all these characteristics can be used to uniquely identify an antinucleus species while providing rejection power against protons and other non-antimatter cosmic-ray particles, which produce neither characteristic X-rays nor hadronic annihilation products [3].

The Si(Li) tracker, of which the detector readout channel is the focus of the R&D activity described in this work, will be realized in a modular structure. Each module comprises four Si(Li) detectors, with 8 strips per detector, and the readout electronics. For this purpose, a full custom 32-channels mixed-signal integrated circuit is being designed to interface with each of the 32 silicon strip detectors of one module and to send digital information to the data acquisition system. In the final system, 360 ASICs with a total of 11,520 channels will be used for the readout of 1440 detectors. The core of the ASIC is a low-noise analog readout channel consisting of a charge-sensitive preamplifier with dynamic signal compression, a unipolar semi-Gaussian time-invariant filter, a hit discriminator and a sample-and-hold (S&H). The analog information is digitized with an 11-bit hybrid Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). To save space, only one ADC per ASIC is foreseen and an analog 32:1 multiplexer is used to connect the output of each channel to the converter. The first step towards the realization of the final flight ASIC has been the design and the production of a first prototype of the low-noise analog readout channel fabricated in a commercial 180 nm CMOS technology

This paper, besides discussing the architecture and the main features of the analog readout channel, also presents the results coming from the experimental characterization, and is organized in three sections. In Section II, all details concerning the architecture of the analog readout channel are discussed together with the constraints and the requirements determined by the use in the GAPS instrument. In Section III, a detailed study of a single MOS device with same dimension of the input channel device is reported. In Section IV, measurement results are presented and discussed with the purpose of validating the proposed architecture for the final 32-channels flight ASIC, which will be ready for the first balloon flight scheduled for late 2022 from the McMurdo Station in Antarctica.

Manuscript received July 21, 2021.

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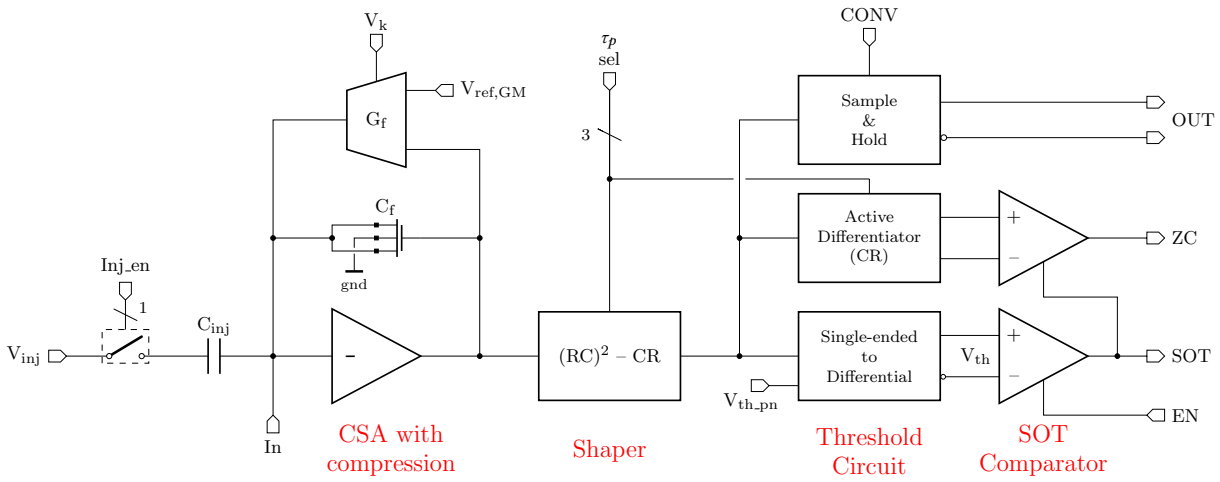

Fig. 1. Simplified schematic diagram of the analog channel for the readout of the Si(Li) detector.

II. Analog Readout Channel Design

A. General Considerations and Specifications

To comply with the GAPS experiment requirements, the analog readout channel must be capable of resolving both X-rays in the range from 20 to 100 keV and charged particles with energy depositions of up to 100 MeV. Moreover, an energy resolution below 4 keV FWHM in the 20-100 keV range is required to clearly distinguish X-rays from antiprotonic and antideuteronic exotic atoms. The readout electronics, which is expected to run at a temperature of about $-40°$C, has to comply with a detector leakage current of the order of 5 nA per-strip and with a 40 pF detector capacitance. The power dissipation is limited to less than 10 mW/channel to be compatible with the balloon nature of the experiment and the limited power that will be supplied by custom solar panels. The channel must also work with two trigger functionalities for full and sparse readout. In full readout mode, an external trigger is provided and all channels are read out. In sparse readout, however, the trigger signal is self-generated only by the channels in which an event is detected.

B. Design details

The analog readout channel has been designed in a commercial 180 nm mixed-signal CMOS process. This technology, which is considered a good compromise among several criteria such as core voltage, analog performance, digital density, availability, and cost, provides 6 metal layers, core thin-oxide and I/O thick-oxide devices with a bias voltage of 1.8 V and 3.3 V, respectively. Core devices are made available in two flavours: with nominal (NVT) and with medium (MVT) threshold voltages. The area occupancy of a single analog channel is 0.15×1.0 mm^2. The analog readout channel prototype has been integrated together with a single MOS transistor with the same polarity, geometry, and layout of the CSA input device. This MOSFET was added specifically to perform single device static, signal, and noise analysis.

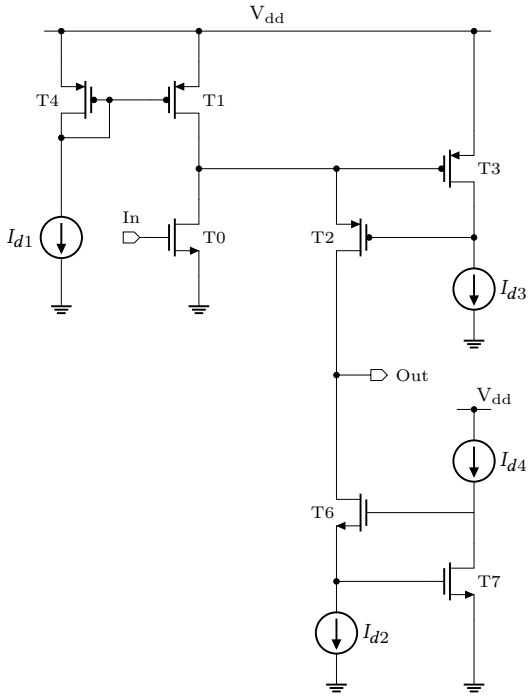

Fig. 2. Transistor-level schematic diagram of the CSA forward gain stage.

C. Readout Channel Architecture

The simplified schematic diagram of the analog readout channel is shown in Fig. 1. A low-noise charge-sensitive amplifier (CSA) integrates the current signal associated with the charge collected by a strip of the Si(Li) detector. The schematic diagram of the CSA forward gain stage is shown in Fig. 2. It is based on a complementary folded cascode architecture with a local feedback and a regulated cascode load serving the purpose of boosting the impedance seen at the amplifier output node. The preamplifier input device (T_0) is an NMOS with W/L=2400/0.5 µm/µm biased at a drain current I_D=1.62 mA. The choices of the input device and of

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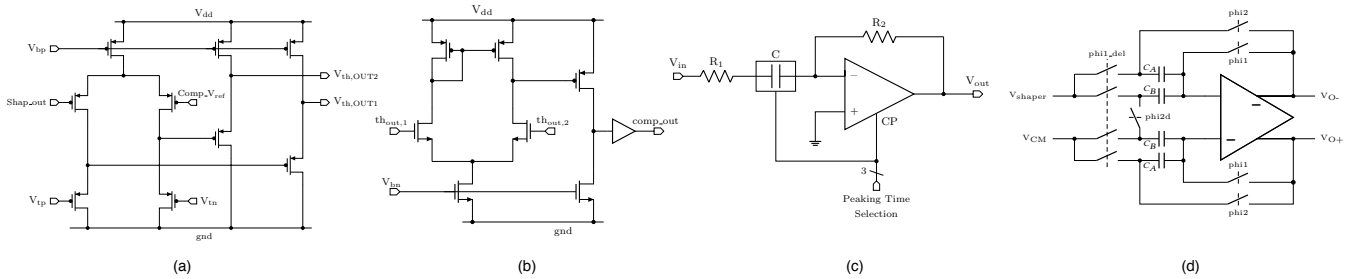

Fig. 3. Schematic diagrams of single-ended to differential threshold circuit (a), discriminator (b), active differentiator (c) and single-ended to differential S&H (d).

its bias current were made on the basis of noise optimization criteria adopted for deep submicron technologies [4], taking into account the specifications on power dissipation, which sets a constraint on the drain current. As shown in [4], noise is a relatively weak function of the input device bias if the current is set at the minimum of the noise-to-current plot. Nonetheless, in the final version of the channel, this current will be fine trimmed by means of an external current reference. To comply with the wide input dynamic range while maintaining good resolution at low energies, a non-linear MOS capacitor (C_f), yielding dynamic signal compression, is used in the amplifier feedback loop [5], [6]. A Krummenacher network, with transconductance gain G_f, is responsible for charge restoration in the feedback capacitance and for compensation of the detector leakage current [7]. This stage is also used to apply a voltage shift to the gate-to-source/drain terminals of the feedback MOS, which enables a precise variation of the voltage at which the kink in the compression occurs [5]. An injection capacitance (C_{inj}) has been integrated at the CSA input for calibration purposes. For Signal-to-Noise optimization, the amplifier is followed by a unipolar second order semi-Gaussian time invariant filter featuring eight selectable peaking times (from 0.3 to 1.8 µs). The choice of the peaking times to be implemented relies on preliminary considerations about all the noise sources in the front-end and in the detector. Other aspects commonly involved in this process, such as the event rate or the large area required by the capacitor for long shaping times, are not relevant for this specific experiment and were not involved in the choice of the peaking times. The filter is comprised of two stages: the integrator and the shaper. The peaking time of the filter is easily adjusted by changing capacitors in both stages. The signal from the strip, after amplification and filtering, undergoes three different conditioning processes. On one side, it is converted from single-ended to differential and then compared to a preset differential threshold (V_{th_pn}) of a discriminator, which generates a Signal-Over-Threshold (SOT) pulse. A single-ended to differential S&H stores the shaper output peak value and feeds the differential analog signal to the ADC for conversion. In sparse readout operation mode, the S&H sampling signal (CONV) is provided from outside with a trigger generated by the TOF system. Instead, when the channel is operated in self-trigger mode, for example during calibration with X-ray sources, the sampling signal is generated internally starting from the information provided by the zero-crossing discriminator output signal (ZC). This internal trigger, which must be synchronous with the shaper signal peak, is obtained with a further differentiation of the shaper output provided by an active first-order differentiator. The schematic diagrams of the the blocks involved in this part of the processing chain are shown in Fig. 3.

III. Single Device Test Results

A single MOS test device was included specifically for the main purpose of testing device noise performance, particularly for $1/f$-noise, which is known to be strongly dependent on the CMOS process. The resulting parameters were examined in depth in order to better understand the performance, in terms of resolution, of the entire analog chain. A study of static and signal parameters of this MOSFET has also been carried out to evaluate fundamental parameters such as channel transconductance g_m, threshold voltage V_{Th}, and transistor inversion level. All measurements were performed at ambient temperature.

A. Static and Signal measurements

Signal and static parameters have been measured with a Semiconductor Parameter Analyzer (Agilent B1500A mainframe with B1511A SMU Modules) with the main purpose of evaluating the inversion region where the device is operated since it affects the channel transconductance g_m, hence, the channel thermal noise. The actual inversion level of a MOS transistor can be extracted by the plot of the transconductance efficiency, defined as the ratio of the transconductance g_m to the drain current I_D, as a function of the normalized drain current $I_D L/W$. From this plot, it is possible to extract the characteristic normalized drain current I_Z^* as the intersection between the straight lines tangent to the transconductance efficiency in the weak inversion region and in the strong inversion region respectively, when a logarithmic scale is used. For the investigated NMOS device, with W/L=2400/0.5 µm/µm, the plot shown in Fig. 4 provides a value of $I_Z^* = 0.36$ µA. At a given current, the inversion level of the channel is expressed by the inversion coefficient, I_{C0}, which depends on I_Z^* and is defined as:

$$I_{C0} = \frac{I_D}{I_Z^*}\frac{L}{W}. \quad (1)$$

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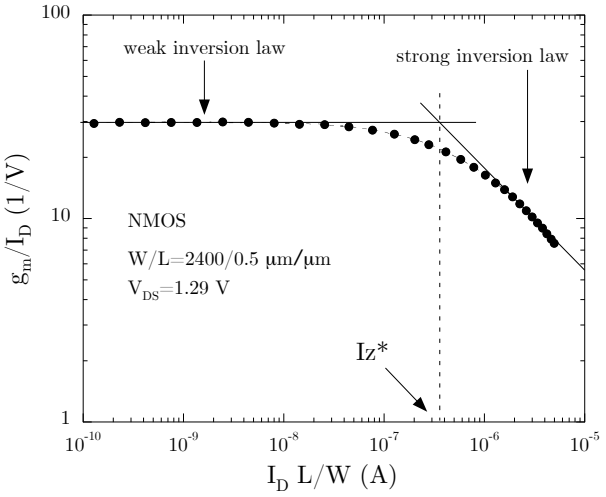

Fig. 4. Transconductance efficiency g_m/I_D as a function of the normalized drain current $I_D L/W$ for the tested NMOS device with W/L=2400/0.5 µm/µm biased at a drain-to-source voltage V_{DS}=1.29 V.

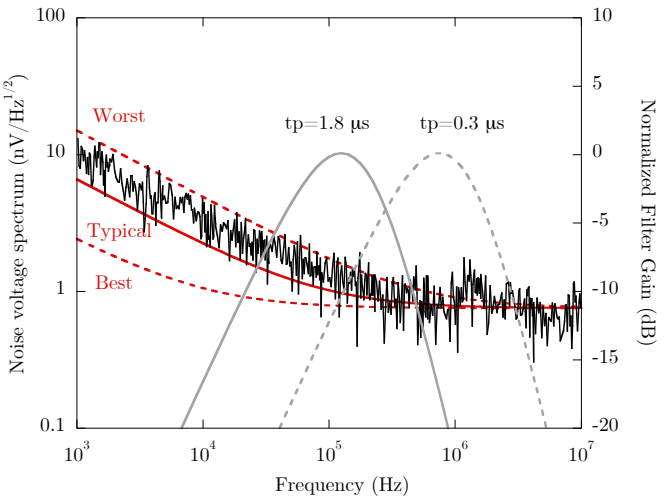

Fig. 5. Measured and simulated noise voltage spectrum of the NMOS with W/L = 2400/0.5 µm/µm biased at I_D=1.62 mA and V_{DS}=1.29 V. Simulation results are provided for 3 flicker noise models named *best*, *typical* and *worst*. The normalized transfer functions of the filter for the shortest (τ_p=0.3 µs) and longest (τ_p=1.8 µs) selectable peaking time are superimposed.

The steady current I_D=1.62 mA at which the input device of the CSA is operated results in an inversion coefficient of I_{C0}=0.94. According to this value the device is operated at the center of the moderate inversion region. The measured device transconductance $g_{m,exp}$=31.6 mS is close to the simulated value of $g_{m,sim}$=30.2 mS. For the sake of completeness, these values have also been compared with the one provided by the following equation, valid in all inversion regions [8], [9]:

$$g_{m,teo} = \frac{I_D}{n\phi_T} \frac{2}{1+\sqrt{1+4I_{C0}}} = 30.2 \text{ mS} \qquad (2)$$

where ϕ_T=k_BT/q is the thermal voltage (k_B is Boltzmann's constant, T is the absolute temperature and q is the elementary charge) and n=1.3 is a coefficient proportional to the inverse of the subthreshold slope of the I_D-V_{GS} plot.

These values have been summarized in Table I and will be the basis of the subsequent noise analysis.

B. Noise measurement results

Noise power spectral density in the channel current was analyzed by measuring the gate-referred series noise voltage spectrum. This measurement was performed using a Network/Spectrum Analyzer (Agilent 4395A) and an ad-hoc developed interface circuit, with the device biased in the same way as the charge amplifier (V_{DS}=1.29 V, I_D=1.62 mA). The measured noise voltage spectrum $S_e(f)$ is shown in Fig. 5. The results provided by post-layout simulations (PLS) are also shown on the same graph and relate to three different noise models. Moreover, the normalized transfer function of the semi-Gaussian time-invariant filter included in the readout channel is superimposed on the plot to highlight the frequency region of interest at shorter and longer peaking time settings. The spectra consist of two contributions and can be described with the following equation:

$$S_e(f) = 4k_BTR_{eq} + \frac{A_f}{f^{\alpha_f}}. \qquad (3)$$

In (3), the first term accounts for the frequency-independent noise dominating the high frequency portion of the spectrum. Since the nature of this contribution is thermal noise, it can be better expressed by an equivalent noise resistance R_{eq}. The second term, which instead dominates the spectrum at lower frequencies, describes the $1/f$-noise contribution which, in turn, depends on the α_f and A_f coefficients. α_f determines the slope of this low frequency term and A_f is inversely proportional to the device dimensions and is strongly dependent on the process. The values of these noise parameters, as extracted from measurement and simulation results, are reported in Table I.

Furthermore, it is of some interest to compare the values of R_{eq} with the one predicted by the theory. To this purpose, it should be noted that the main contribution to the white noise component of the spectrum comes from thermal noise in the channel current of the device. Other thermal noise sources can be found in the gate ($R_{GG'}$), drain ($R_{DD'}$) and source ($R_{SS'}$) series resistors. For a wide transistor, as the one considered here, source and drain resistance contributions are negligible whereas the one coming from the gate distributed resistance may become noticeable [10]. $R_{GG'}$ is the sum of the resistance of the polysilicon gate and of the gate interconnection and is

TABLE I
SIGNAL AND NOISE PARAMETERS

	Experimental	Simulated		Theoretical
g_m [mS]	31.6	30.2		30.2
R_{eq} [Ω]	35.0	34.2		37.1
α_f	0.97	0.98		-
		$4.61{\cdot}10^{-15}$	best	
A_f [V^2]	$8.7{\cdot}10^{-14}$	$3.75{\cdot}10^{-14}$	typical	-
		$1.96{\cdot}10^{-13}$	worst	

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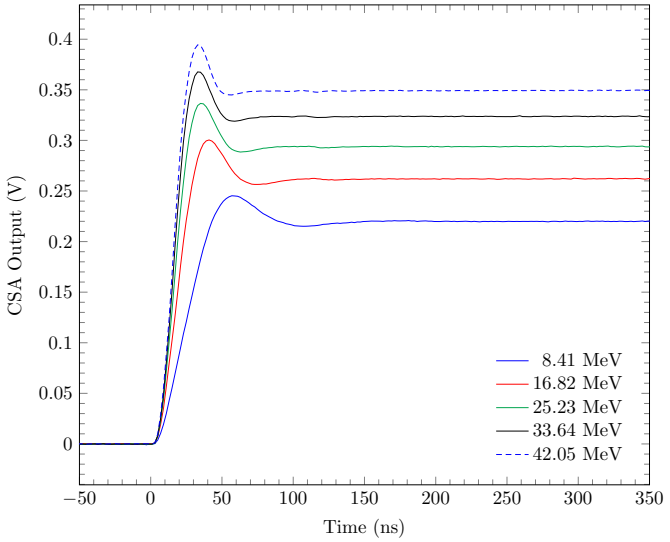

Fig. 6. Measured voltage step at the output of the charge sensitive amplifier (AC coupled) for an emulated input particle energy varying from 8.41 MeV (370.04 fC) to 42.05 MeV (1.85 pC) with 8.41 MeV (370.04 fC) step.

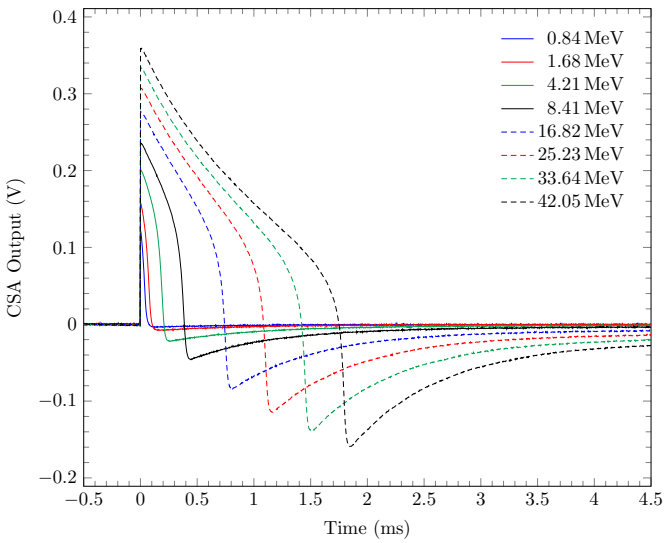

Fig. 7. Measured time response of the charge sensitive amplifier (AC coupled) for an emulated input particle energy varying from 0.84 MeV (37 fC) to 42.05 MeV (1.85 pC).

strongly dependent on the actual gate structure. The device examined here is of the interdigitated multifinger type with each gate finger contacted at both sides. Therefore, $R_{GG'}$ is calculated according to the following relationship [11]:

$$R_{GG'} = \frac{1}{n}\frac{R_i}{12} + \frac{(m+1)(2m+1)}{12m}R_{int} \tag{4}$$

where R_i=341 Ω is the resistance of one gate finger, m=120 is number of fingers and R_{int}=0.35 Ω is the resistance of the connections between gate fingers. These numbers, that were derived from layout inspection and process parameters, provide a value of $R_{GG'}$=12.1 Ω.

By considering both noise sources, the complete expression of R_{eq} can be written as follows [12]:

$$R_{eq} = \alpha_w \frac{n\gamma}{g_m} + R_{GG'}. \tag{5}$$

The first term in eq. (5) is due to the channel thermal noise. Since the gate length of the device is far from the minimum allowed by the technology, a short channel effects coefficient α_w=1 has been used. Moreover, a coefficient γ=0.58 has been evaluated by considering the actual inversion level of the transistor, as derived from the following equation [13]:

$$\gamma(I_{C0}) = \frac{1}{1+I_{C0}}\left[\frac{1}{2} + \frac{2}{3}I_{C0}\right]. \tag{6}$$

Based on eq. (4) and (5) a value of R_{eq}=37.1 Ω has been obtained, in good agreement with both experimental and simulation results.

As far as $1/f$ noise is concerned, the results reported in Table I show that the α_f coefficient is close to 1 for both measurement and simulation results. The A_f coefficient, on the other hand, requires a more in-depth discussion. In Fig. 5 the simulated noise voltage spectrum is provided for three different flicker noise models named *best*, *typical* and *worst*, as provided by the foundry. The measured $1/f$ noise is well within the range between *best* and *worst* case models. Nonetheless, it should be noted that the *typical* model, that is commonly adopted in the design phase, underestimates the $1/f$ noise contribution. This can have a non negligible impact in particular for the filter setting that provides peaking times of the order of 2 µs, as can be seen from the modulus of the frequency response of the time-invariant filter reported in Fig. 5 and corresponding to the minimum and the maximum selectable peaking times, τ_p=0.3 µs and τ_p=1.8 µs, respectively.

IV. Front-end Performance

The complete analog readout channel has been successfully tested. All the main blocks can be accessed through additional analog outputs for an extensive characterization of the front-end. The experimental results reported in the following are relevant to measurements performed at room temperature.

A. Power Consumption

With a bias of V_{DD}=1.8 V, the channel dissipates a power of 7.2 mW, which is lower than the limit of 10 mW imposed by the requirements of the application. Most of the power (60%) is drawn by the amplifier to achieve low noise performance.

B. Time Response

The waveform at the output of the main blocks of the implemented analog readout channel has been measured with a LeCroy WavePro 735Zi Digital Signal Oscilloscope. The input signal is generated by exploiting the dedicated injection circuit shown in Fig. 1 and by varying the emulated input particle energy with an external 16-bit commercial DAC that sets the amplitude of the V_{inj} voltage.

Fig. 6 shows the waveforms measured at the output of the CSA for an emulated incoming energy varying from

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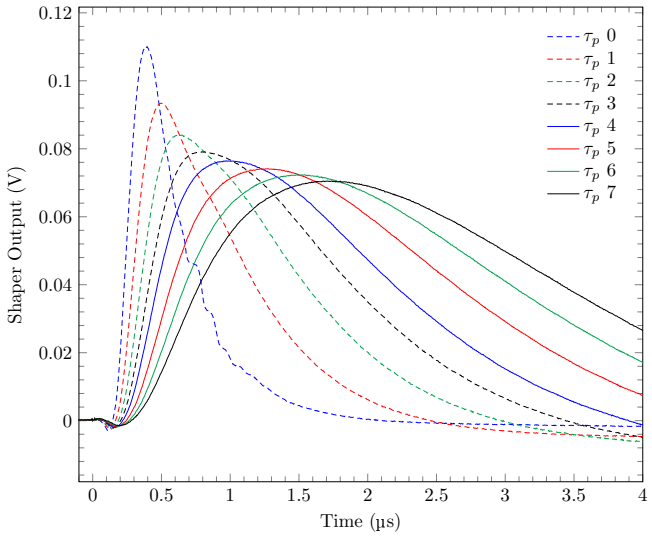

Fig. 8. Measured time response of the time-invariant filter (AC coupled) for an emulated input particle energy of 841 keV (37 fC) and for the 8 selectable peaking times.

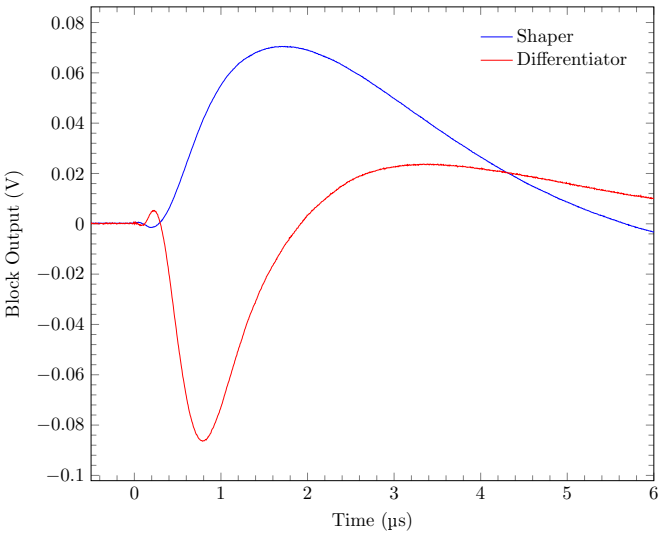

Fig. 9. Measured time response of the time-invariant filter and the active differentiator (AC coupled) for an emulated input particle energy of 841 keV (37 fC) and for the peaking time τ_p=1.82 µs.

8.41 MeV (370.04 fC) to 42.05 MeV (1.85 pC). It can be seen that the rise time, intended here as the time taken by the signal amplitude to change from 10% to 90%, decreases with increasing input charge. The effect is expected and attributed to the non-linear nature of the CSA feedback capacitance, which increases with the voltage step amplitude, thus pushing the dominant pole of the transfer function to higher frequencies.

The charge restoration phase of the CSA feedback capacitance, that starts after signal injection, is shown in Fig. 7 for different values of the collected energy up to 42.05 MeV (1.85 pC). The Krummenacher feedback network, when unbalanced, is expected to provide a linear discharge of the feedback capacitance. The non-linear nature of the integrating MOS capacitance makes the discharge a non-linear process. The slow discharge region corresponds to large output levels, when the feedback capacitance is large, while the fast discharge region corresponds to small output levels, when the feedback capacitance is small. It can be observed that, for large values of the collected charge, an undershoot appears at the end of the restoration phase. This effect is related to the complete unbalance of the Krummenacher stage that occurs for large voltage steps at the CSA output. Nonetheless, a complete recovery of the stage is reached in less than 10 ms, which is fully compatible with the low event rate per strip, ess than 1 counts per second including background, expected for the experiment.

TABLE II
CHANNEL MAIN PERFORMANCE.

Setting #	τ_p [µs]	Gain (X-ray detection) [mV/keV]	Energy resolution [keV FWHM]	
			C_D=0	C_D=40 pF
0	0.30	1.85	3.38	6.81
1	0.47	1.69	3.16	5.44
2	0.65	1.61	3.09	5.46
3	0.83	1.57	3.12	5.10
4	1.00	1.53	3.16	5.16
5	1.27	1.48	3.23	5.12
6	1.54	1.45	3.33	5.22
7	1.82	1.41	3.43	5.24

The time response of the time-invariant filter is shown in Fig. 8 for an emulated input particle energy of 841 keV (37 fC) and for the 8 selectable peaking times. The channel provides a good unipolar semi-Gaussian (CR-RC^2) shape, with a decrease of the peak amplitude with the increase of the peaking time that can be attributed to the zero in the CSA transfer function introduced by the charge restoration stage. The measured peaking times, shown in Table II, are consistent with the values expected from simulation.

A waveform measured at the output of the active differentiator is shown (in red) in Fig. 9 for an emulated input particle energy of 841 keV (37 fC) and for a peaking time τ_p=1.82 µs. As stated in Section II-C, this block, together with the zero-crossing comparator, is responsible for shaper peak detection when the channel is operated in self-trigger mode. For an optimal operation of the conditioning scheme, two main properties are essential for this part of the processing chain: a minimum delay between the shaper peak and the firing of the zero-crossing comparator, and a gain of the differentiator greater than one and independent of the shaper peaking time. To comply with these requirements, the derivative of the shaper signal is implemented with an active differentiator, whose pole location is changed in agreement with the selected peaking time. By comparing the waveforms of the shaper (in blue) and of the active differentiator (in red) shown in Fig. 9 it can be seen that the aforementioned requirements are well met: the gain of the stage is greater than one and the zero crossing of the signal is delayed with respect to the shaper

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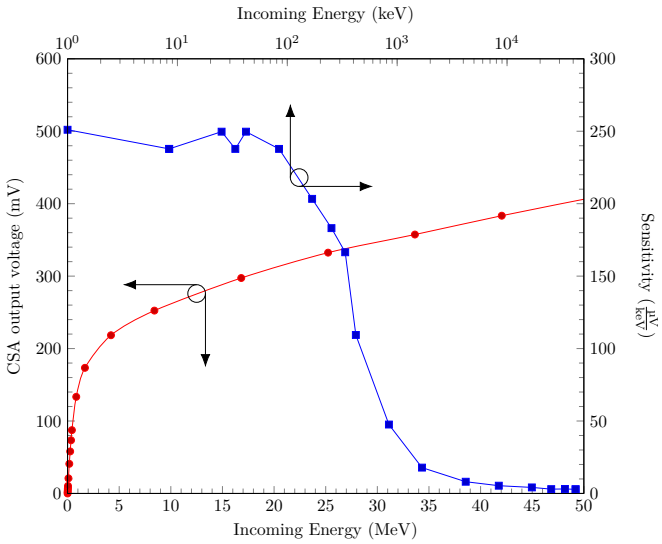

Fig. 10. Input-output trans-characteristic (red curve) and sensitivity (blue curve) of the CSA with dynamic compression.

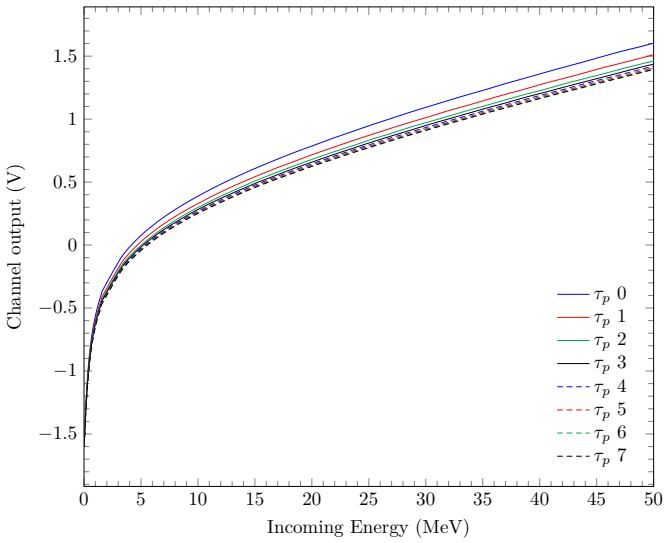

Fig. 11. Input-output trans-characteristics of the channel at all the selectable peaking times.

peak by less than 100 ns.

C. Energy Sensitivity and Dynamic Range

The input-output trans-characteristic of the charge sensitive amplifier and the relevant sensitivity are shown in Fig. 10. Thanks to the non-linear MOS capacitor in the feedback network, the trans-characteristic exhibits an almost bilinear shape with a transition of the sensitivity occurring at an output voltage of about 200 mV, corresponding to an input particle energy of about 1 MeV (44 fC). The sensitivity for the initial high gain region is about 250 μV/keV (5.7 mV/fC), corresponding to an equivalent feedback capacitance of 175 fF, and decreases to 3.0 μV/keV (68 μV/fC), corresponding to a feedback capacitance of 14.7 pF in the low gain region with a compression factor of about 80. The signal at the output of the CSA is further amplified by the time-invariant filter and by the Sample & Hold. Both stages exhibit a linear trans-characteristic that provides an additional gain of 1.5 V/V and 5.14 V/V respectively. The Sample & Hold, that has been implemented according to the architecture shown in Fig. 3[14], provides a differential output signal suitable for the subsequent ADC block. The output signal ranges from -1.8 V to +1.8 V with an almost rail-to-rail output dynamic range. Fig. 11 shows the input-output trans-characteristic of the full analog channel, as acquired at the output of the Sample & Hold stage for the 8 peaking times. By design, the channel can handle a wide input dynamic range that extends up to 100 MeV but, due to a limitation in the calibration circuit, the test has been limited to 50 MeV. The calibration strategy of the multichannel system will be based on an external 16-bit commercial DAC that will be used to measure the input-output characteristic of each channel. Moreover, an X-ray source will be applied to properly anchor each channel characteristic to the energy scale.

Data obtained from values of the collected energy in the X-ray detection range (lower than 100 keV) have been fitted using the linear regression in order to obtain the low energy gain for the eight selectable peaking times reported in Table II.

D. Energy Resolution

The FWHM energy resolution of the channel has been obtained from the equivalent noise charge (ENC) according to the following equation:

$$FWHM = 2.35 \cdot \varepsilon \cdot \frac{ENC}{q} \tag{7}$$

where ε is the ionization energy of silicon (3.6 eV per electron-hole pair).

The measurement of the critical parameters of the channel, such as resolution and threshold, was performed by detecting the firing efficiency of the SOT discriminator with the threshold scan technique [15]. The threshold voltage is applied with an external 16-bit commercial DAC. Measurements have been performed with and without an external input capacitance of 40 pF, emulating the one of the detector. Fig. 12 shows the experimental results obtained for the 8 selectable peaking times. The channel resolution and the threshold of the channel were extracted by fitting the measured Hit/NoHit discriminator threshold scan data to a complementary error function.

Channel resolution, in terms of energy, has been obtained by applying eq. (7) and results are reported in Table II. Also, Fig. 13 shows the energy resolution FWHM, and the relevant ENC values measured at the 8 peaking time settings superimposed with values expected from different types of simulation. We measure an energy resolution as low as 5.1 keV for peaking times in the range of 0.83 μs to 1.27 μs. This value is higher than the 4 keV (480 e^- rms) that is the target of the envisioned application. Comparing the measured and schematic (SCH) simulation set of data, it can be noticed that measured values are higher than simulated ones for all the selectable peaking times. After a thorough analysis of the design, it was found that the excess noise can be explained by two

This article has been accepted for publication in IEEE Transactions on Nuclear Science. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TNS.2021.3118980

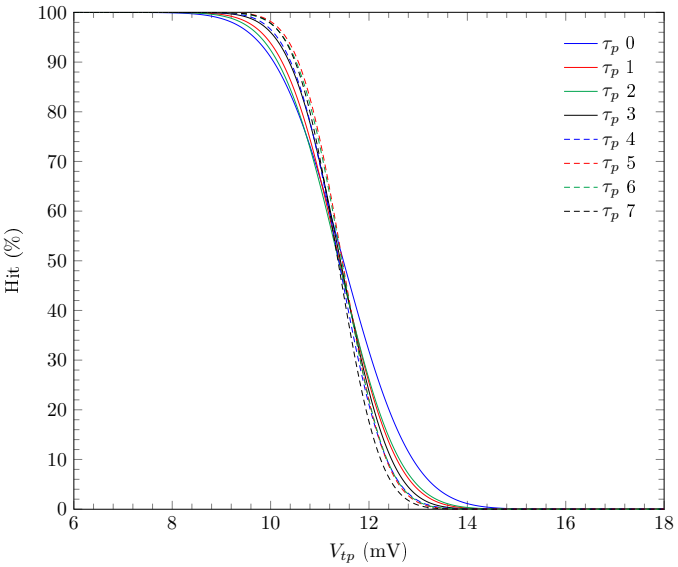

Fig. 12. Threshold scan of the channel as obtained by varying the peaking time. An external capacitance of 40 pF is applied at the channel input.

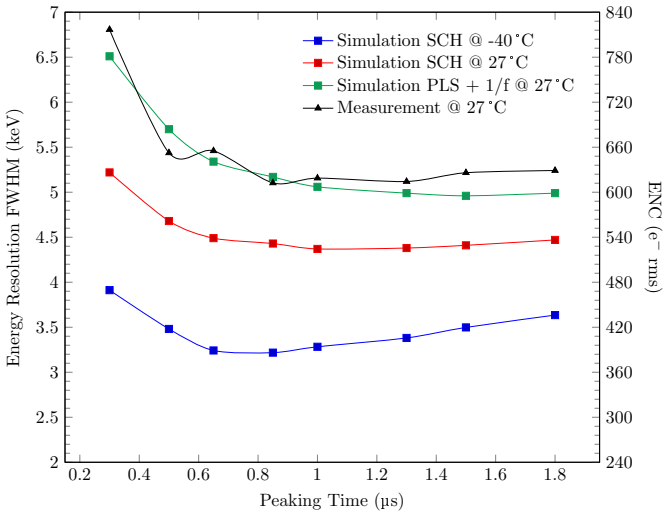

Fig. 13. Measured and simulated FWHM energy resolution (and equivalent noise charge) as a function of the peaking time for a detector capacitance C_D=40 pF.

different reasons. First, a critical investigation of layout design has shown that a non-negligible parasitic resistance R_p exists between the gate of the CSA input device and the detector wire bonding pad. This resistance, which is of about 20 Ω, is mainly responsible for the increase in noise observed at the shorter peaking times. Moreover, the noise characterization of the single test device discussed in Section III yielded a flicker noise coefficient A_f that is almost twice the one provided by technology models in the *typical* case. By performing post layout simulation and including this excess $1/f$ noise factor into the model, it is possible to obtain the green curve in Fig. 13 that is consistent with measured data at ambient temperature. From this simulation results, the contribution of noise sources to the total integrated output noise has been extrapolated. In particular, the following contributors have been evaluated: the CSA input device (T_0) and the complete amplifier, the parasitic resistance (R_P), the Krummenacher restoration network (G_f), and the integrated bias network. Results are reported in Table III. It can be observed that, in the CSA, the noise is mainly due to the input transistor as expected. Nonetheless, other devices have a non negligible impact on the noise. In particular, by referring to the schematic diagram in Fig. 2, a critical element is represented by the current source T_1, whose bias current is nearly equal to the one of the input device T_0 and its reference T_4 [17]. Also, transistor T_2 in the folded branch may affect the $1/f$-noise, as discussed in [18], thus spoiling the resolution for all the peaking times. Although the channel input stage, comprised of the CSA, the parasitic resistance R_P, and the Krummenacher restoration network G_f, contributes most of the integrated output noise, this is not the dominant part and some excess noise from other components is evident. In particular, a non-negligible contribution, around 20%, comes from a non-optimum design of the transistors bias network and an additional 20% comes from the conditioning blocks that follow the CSA. Based on these results and considerations, a thorough analysis will be conducted to reduce the effect of the excess noise sources and improve the resolution in the next version of the channel. As a last remark, it can be noticed that at the experiment operating temperature of -40°C, the noise performance is expected to improve thanks to the reduction of the channel thermal noise contributions, as shown in Fig. 13.

To provide more insights on the results of the channel resolution, a theoretical analysis has been carried out starting from results reported in Section III and taking into account noise contributions coming from the CSA input device and restoration network. The ENC was derived by considering the following equation:

$$ENC^2 = (C_D^*)^2 \left(\frac{4k_B T R_{eq}^*}{\tau_p} A_1 + A_2 2\pi A_f \right) + 2qI_k \tau_p A_3 \tag{8}$$

where C_D^* is the total capacitance shunting the input node of the charge amplifier and is mainly given by the sum of the detector capacitance C_D=40 pF and the amplifier input device gate capacitance which is a function of the gate dimensions

TABLE III
CONTRIBUTION, IN %, OF CHANNEL NOISE SOURCES TO THE TOTAL INTEGRATED OUTPUT NOISE.

τ_p [µs]	T_0	CSA (total)	R_p	G_f	Bias network	Other blocks
0.30	35	45	13	3	16	23
0.47	34	43	11	6	15	25
0.65	32	41	10	10	17	22
0.83	30	39	8	13	18	22
1.00	29	37	7	16	17	23
1.27	27	35	6	21	19	19
1.54	25	33	5	25	20	17
1.82	24	31	4	28	20	17

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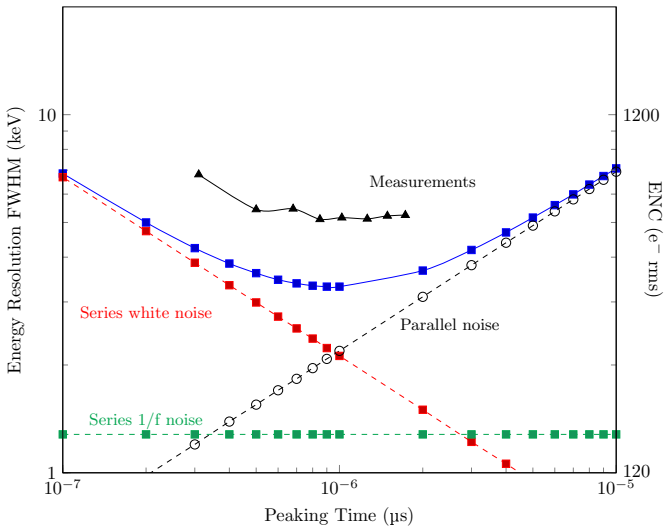

Fig. 14. Measured (black triangles) and computed (blue squares) energy resolution FWHM as a function of the peaking time for a detector capacitance C_D=40 pF. The contributions from individual noise sources (input device thermal and $1/f$-noise, parallel shot noise) are shown in the plot.

W, L and the bias current I_D. A value of C_{in}=5 pF has been extracted from SPICE simulations. R^*_{eq} is the equivalent input noise resistance that is responsible for the white noise contribution. R^*_{eq} is given by the sum of the R_{eq} extracted in Section III, and the aforementioned stray resistance R_p. A_f is the measured flicker noise coefficient. Beside the series noise source, the ENC is also affected by a parallel noise contribution coming from the charge restoration network. The nature of this source is mainly thermal noise in the channel current of the Krummenacher stage transistors. Nonetheless, since these devices are biased in weak inversion region, the power spectral density can be described with the shot noise model adopted in eq. (8) where I_k=10 nA is an equivalent current accounting for all the noise contributions in the restoration network, τ_p is the peaking time and A_1=0.85, A_2=0.54 and A_3=0.64 are three coefficients accounting for the semi-Gaussian second order shape of the filter [16].

In Fig. 14, the measured energy resolution is compared with the contribution expected from the CSA input device and the restoration network as predicted using eq. (8). It can be observed that these two sources contribute to the total measured noise for around 40-50 % in the range of the selectable peaking times. These results are in good agreement with the ones obtained from simulation and with data reported in Table III.

V. Conclusions

This work discusses the design and the experimental results of a low-noise analog channel for the read-out of the lithium-drifted silicon, Si(Li), detectors of the GAPS experiment. The channel, implemented in a commercial 180 nm CMOS technology, has been successfully tested. Experimental results have proven the correct operation of all the integrated blocks and of the whole processing chain. The architecture meets all of the experiment specifications but energy resolution at ambient temperature. According to simulation results, better performance are expected at the -40°C operating temperature. Moreover, noise measurements performed on the analog read-out channel and on a single test device have provided useful hints that will be considered as the base for an improved version of the design optimizing the channel resolution. As a next step, the architecture will be integrated in a multichannel circuit that will be the first prototype of the flight ASIC.

Acknowledgment

The authors wish to acknowledge the constant support provided by M. Boezio and G. Zampa throughout this research, and they wish to thank the colleagues in the GAPS collaboration, whose helpful and stimulating discussions contributed to improving the work.

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