# Optimum Design of DACs for Threshold Correction in Multichannel Processors for Radiation Detectors

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***Abstract*—This work is intended to provide a set of guidelines for the design of digital-to-analog converters enabling the reduction of threshold dispersion in multichannel readout circuits for radiation detectors. The design criteria are first established through a theoretical approach and then confirmed by means of a simulation tool based on Monte Carlo methods. This latter tool provides a fast and flexible way to predict the performance of a DAC for threshold correction, also accounting for possible non-idealities, such as differential and integral non linearities and gain and offset errors. The proposed guidelines have been validated through simulations on front-end circuits for a real application, the silicon vertex tracker for the SuperB Factory, and through comparison with data available in the literature.**

***Index Terms*—Analog integrated circuits, CMOS, radiation detectors, threshold correction.**

## I. Introduction

In present and even more in future high energy physics (HEP) experiments, silicon vertex detectors are and will be required to provide a very precise measurement of the position and momentum of charged particles. In order to enable an accurate separation of the collision vertices, detectors have to be placed very close to the beam interaction point and feature a very high degree of segmentation. Design of multichannel processing electronics for such high granularity detectors (pixels or strips with a pitch that may be well below 100 $\mu$m) can take advantage of the continuous minimum feature size scaling of CMOS technologies [1] and of the availability of vertical integration processes [2], [3]. Very high functional density is achieved in the front-end part of the readout circuits, generally featuring both an analog and a digital section. The analog channel, including, in its most common version, a charge preamplifier and a shaping filter and followed by a discriminator, is often used to provide simply hit/no hit (binary) information by comparing the signal with a voltage threshold, chosen in such a way to maximize the rate of detected true events without having the system flooded with false, noise-induced hits. Needless to say, noise performance of the analog front-end processor is of paramount importance in establishing the system properties in terms of detection efficiency which, on the other hand, is also affected by possible channel-to-channel threshold non-uniformities (or dispersion). Therefore, a careful design is required to minimize both noise and threshold dispersion, while coping with power dissipation and area constraints. Minimum noise in the design of charge preamplifiers is achieved through well established capacitive matching criteria [4], [5], with a lower limit set by the input device noise characteristics. As far as threshold dispersion is concerned, the main source is represented by transistor mismatch, particularly in the discriminator and in the shaping stage, caused by both random fluctuations and deterministic variations in process parameters. Dispersion may be increased by other systematic effects, like voltage drop along power and ground lines. When threshold dispersion requirements cannot be guaranteed by design, circuits for fine threshold tuning are included in each channel. A couple of different strategies have been proposed and are used in the design of threshold correction blocks. The first one consists in dynamically storing an analog voltage on a capacitor [6]. While offering a wide tuning range and virtually unlimited resolution (charge quantization representing the only theoretical limitation), this technique requires that the voltage value be periodically refreshed to compensate for charge leakage effects. Therefore, it is more suitable for applications where the circuit is operated for short time intervals (with respect to the refresh period) or synchronously with a periodic event. Whenever continuous operation is envisioned (therefore in most of the applications to HEP experiments), a solution based upon a pixel level, trimming digital-to-analog converter is adopted. This paper aims at providing a set of criteria enabling the design of DACs for threshold correction in multichannel chips for capacitive detectors. The main part of the work includes the theoretical treatment of the problem and the resulting design guidelines. Also, a Monte Carlo simulation tool will be presented, developed in the LabVIEW® environment and capable of accounting for the effects of DAC non-idealities in threshold correction. The proposed criteria have been validated through results from circuit simulations on a pixel front-end circuit for applications to the SuperB silicon vertex tracker and by comparison with results available in the literature.

## II. Threshold Dispersion and Detection Efficiency

Fig. 1 shows the block diagram of a charge measuring system, including a delta pulse current source, modeling the capacitive detector, a charge preamplifier with feedback capacitor $C_F$ and a filtering stage with transfer function $T(st_p)$, $t_p$ being a characteristic time of the filter (typically the peaking time of the delta response of the system), and DC output voltage $V_{bl}$. In the preamplifier, the feedback restoring network has been neglected for the sake of simplicity. A number of different solutions for feedback capacitor discharge have been proposed and are available in the literature [7]. At the end of the chain, a discriminator

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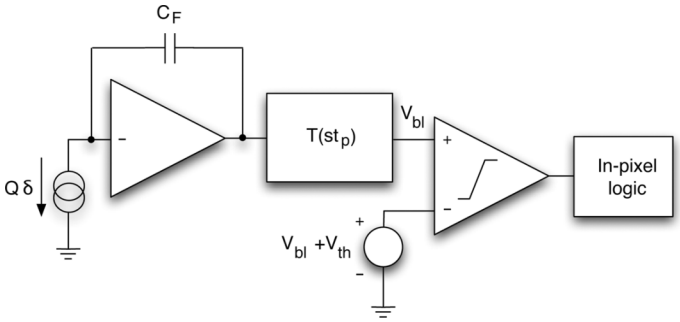


Fig. 1. Block diagram of a typical front-end analog processor for capacitive detectors.

compares the signal at the shaper output with a preset threshold $V_{\rm th}$. The in-pixel logic may include blocks for hit storage and pixel-to-periphery communication enabling data driven or triggered readout and time stamping. As already mentioned, in a binary channel, the discriminator threshold $V_{\rm th}$ is chosen with the aim of optimizing the detection efficiency of the system (the ratio between the true hits detected and sent off chip and the true hits). Efficiency optimization is generally constrained by the chip readout architecture, i.e., by the speed of the readout electronics in collecting data from the detector matrix and sending them off chip in the case of data-push systems, or by the pipeline depth in data-pull (triggered) architectures. Actually, channels with a low threshold are susceptible to noise hits, while channels with a high threshold may miss some true hit. Typically, in a multichannel binary readout system, a maximum noise hit rate $f_{n,\max}$, i.e., a maximum rate of noise-induced transitions at the discriminator output, exists beyond which the system is not capable to guarantee a given, target readout efficiency (defined as the ratio between the number of hits actually sent off chip and the number of detected, real or noise-induced, hits). Under some very general assumptions, in a binary channel the noise hit rate $f_n$, whose analysis represents a specific aspect of the more general level crossing problem, can be written as [8]

$$f_n = f_{n0} \cdot e^{-\frac{V_{\rm th}^2}{2\sigma_n^2}}, \tag{1}$$

where $V_{\rm th}$ is the discriminator threshold, $f_{n0}$ is the noise hit rate at zero threshold (i.e., when the threshold voltage equals the mean value of the voltage at the other discriminator input, corresponding to the output of the analog processor) and $\sigma_n$ is the root mean square value of the noise at the analog processor output. In a multichannel binary readout circuit, random and systematic variations of process (doping) and geometrical (device dimensions, thickness of the various involved layers) parameters may be responsible for introducing non uniformities in the parallel path followed by the signals. As a result, two channels like that in Fig. 1, nominally identical to each other and featuring a common threshold at the inverting input of the discriminator, may provide different responses to the same charge pulse at the preamplifier input. Typically, the main contributions to such non uniformities come from the shaper (generally AC coupled to the preamplifier) and from the discriminator. The overall effect is usually simply referred to as threshold dispersion, as it can be

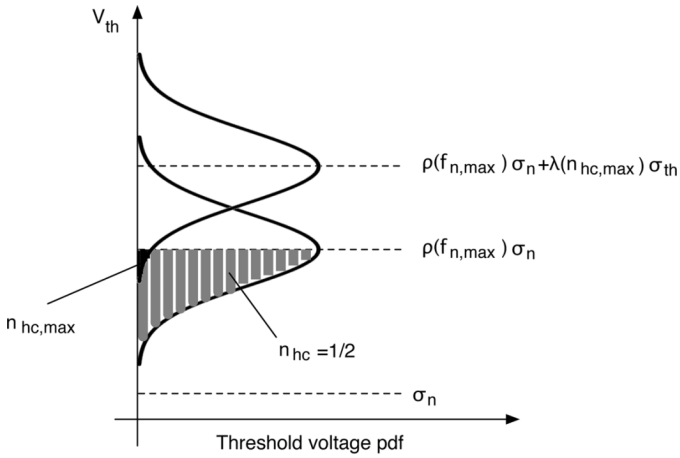


Fig. 2. Threshold setting in a multichannel chip. The fraction of hot channels is represented by the gray plus black shaded areas if the threshold is set without accounting for threshold dispersion effects, by the black shaded area alone when such effects are taken into consideration.

equivalently represented in terms of a statistical distribution of the discriminator threshold voltage [9], [10]. The choice of the threshold voltage value in a multichannel system can be discussed with reference to Fig. 2. If the effect of threshold dispersion is neglected, a minimum threshold value $V_{\rm th,min}$ can be found for all the channels to satisfy the requirements on the maximum noise hit rate,

$$V_{\rm th,min} = \sigma_n \cdot \sqrt{2 \cdot \ln\left(\frac{f_{n0}}{f_{n,\max}}\right)} = \rho(f_{n,\max}) \cdot \sigma_n, \tag{2}$$

where $\rho(f_{n,\max}) = \sqrt{2 \cdot \ln((f_{n0})/(f_{n,\max}))}$ is a slowly decreasing function of $f_{n,\max}$. Actually, if the threshold is set according to (2), due to threshold dispersion, the noise hit rate could exceed $f_{n,\max}$ in a significant fraction of the channels (also called hot channels, gray plus black area in Fig. 2). In order to limit the fraction of hot channels, threshold dispersion has to be taken into account and $V_{\rm th,min}$ has to be moved towards higher values according to the following equation,

$$V_{\rm th,min} = \rho(f_{n,\max}) \cdot \sigma_n + \lambda(n_{\rm hc,max}) \cdot \sigma_{\rm th}, \tag{3}$$

where the threshold dispersion is represented by means of the standard deviation $\sigma_{\rm th}$ of the threshold distribution in the multichannel chip. In (3), $\lambda$ is a decreasing function of $n_{\rm hc,max}$, the maximum acceptable fraction of hot channels. If $V_{\rm th}$ is normally distributed, for the fraction of hot channels not to be larger than $n_{\rm hc,max}$, $\lambda$ should be chosen such that

$$\lambda(n_{\rm hc,max}) = \sqrt{2} \cdot {\rm Erfc}^{-1}(2n_{\rm hc,max}), \tag{4}$$

where ${\rm Erfc}(x)$ is the complementary error function. While, on the one hand, shifting the threshold voltage allows the system to comply with the noise hit rate constraints, on the other hand it reduces the detection efficiency, in particular for those channels which are located towards the higher end tail of the distribution. Therefore, in order to make the detection efficiency as

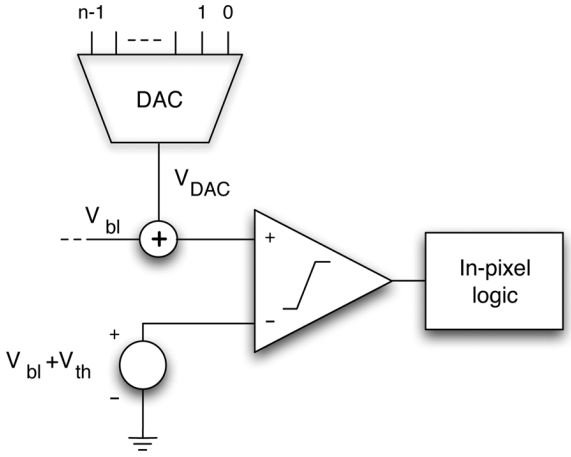


Fig. 3. Block diagram of the discriminator with the DAC for threshold correction.

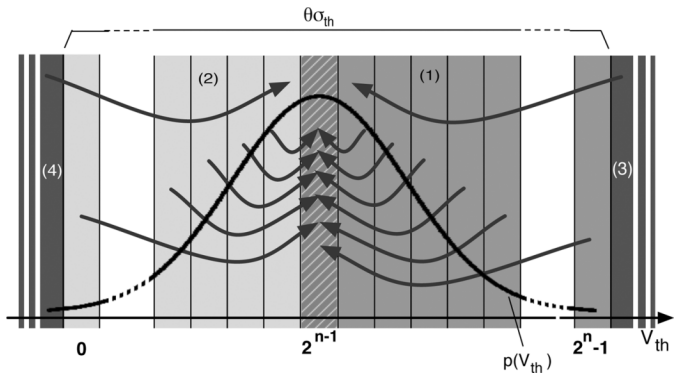


Fig. 4. Graphical representation of the threshold correction as the folding of the threshold probability density function onto the average value. In the figure, reference is made to the terms of (6).

high and uniform as possible, measures have to be taken to minimize threshold dispersion.

## III. Optimum DAC Design for Threshold Correction

As already mentioned, excessive threshold dispersion in a multichannel chip for capacitive detectors is generally managed by means of a D/A converter adjusting the threshold in each individual channel. Fig. 3 shows the final part of a typical readout channel, with a block diagram of the discriminator and a DAC for threshold correction acting on the non inverting input of the discriminator. The correction could be equivalently applied to the other input. It is quite reasonable to expect that the larger the resolution (number of bits) of the DAC, the finer the threshold adjustment and, eventually, the narrower the dispersion among the channels. On the other hand, a wide output range might be necessary to cope with channels featuring a largely offset threshold, resulting in a degradation of the DAC trimming performance. In this section, a theoretical discussion of the problem will be presented, aiming at determining the best compromise between the above two requirements and the best achievable threshold correction performance as a function of the resolution. The theoretical treatment is followed by the description of a Monte Carlo analysis tool, which was developed for fast simulation, at a behavioral level, of D/A converters for threshold correction. The tool has also been used to validate the results obtained from the theoretical model.

### A. Analytical Model

In order to represent threshold dispersion in a multichannel chip, the threshold voltage $V_{\rm th}$ is generally treated as a random variable with Gaussian distribution,

$$p(V_{\rm th}) = \frac{1}{\sigma_{\rm th}\sqrt{2\pi}} \cdot e^{-\frac{(V_{\rm th}-\langle V_{\rm th}\rangle)^2}{2\sigma_{\rm th}^2}} \tag{5}$$

where $\langle V_{\rm th}\rangle$ is the average value of the threshold calculated over the set of channels. For the sake of simplifying the calculations, in the following, $\langle V_{\rm th}\rangle = 0$ will be assumed with no effect on the validity and generality of the results. In order to correct the threshold in each individual pixel, a digital to analog converter can be included in the elementary cell in such a way that the voltage generated at the DAC output $V_{\rm DAC}$ is added to the baseline voltage $V_{bl}$ at the analog channel output, as shown in Fig. 3. Threshold correction is studied under the following hypothesis:

- the output range of the $n$ bit DAC is a (not necessarily integer) multiple of the threshold dispersion $\sigma_{\rm th}$ by a factor $\theta$; the output range is therefore subdivided in $2^n$ equal intervals, numbered from 0 to $2^n - 1$;
- in each cell, the threshold correction is obtained by programming the DAC so as to shift the actual threshold $V_{\rm th}$ as close as possible to $\langle V_{\rm th}\rangle$, under the constraint that, due to the very nature of the correction technique, involving a D/A converter, the shift can be applied only in discrete steps, depending on the DAC resolution.

Application of the above procedure is graphically represented in Fig. 4. Correction of the threshold through a D/A converter has the same effect as folding the probability density function (PDF) $p(V_{\rm th})$ onto the average value of the distribution. The threshold PDF is subdivided into $2^n + 2$ intervals; of them, $2^n$ are $(\theta\sigma_{\rm th})/(2^n)$ long, while the remaining two, going to $+\infty$ and to $-\infty$ respectively, include the PDF portions not covered by the DAC range. When correcting $V_{\rm th}$, the same shift is applied to all the channels with a threshold voltage lying in a given interval. In the figure, the black strips at the left and right ends of the graph lay outside the DAC output range $\theta\sigma_{\rm th}$ (which is centered on the distribution average value). As a consequence, the corresponding portion of the PDF cannot be turned right onto the central, obliquely striped area but just pushed as close as possible to it. The best that can be done in this case is apply the maximum voltage shift made available by the DAC. All the other portions of the PDF, laying against the dark and light gray strips and included in the DAC output range, can be folded directly onto the central one. This operation results in a new PDF for the corrected threshold, $p_{n,\theta}(V_{\rm th})$, depending on the parameter $n$ (the DAC resolution) and $\theta$ (the ratio between the DAC

output range and the threshold dispersion before correction). The analytical expression of the PDF is provided by (6),

$$p_{n,\theta,}(V_{\rm th}) = \frac{1}{\sigma_{\rm th}\sqrt{2\pi}} \cdot \left\{ H\left(\frac{\theta\sigma_{\rm th}}{2^{n+1}} - |V_{\rm th}|\right) \cdot \left[ \underbrace{\sum_{i=0}^{2^{n-1}} \exp\left[-\frac{\left(V_{\rm th} + i\frac{\theta\sigma_{\rm th}}{2^n}\right)^2}{2\sigma_{\rm th}^2}\right]}_{(1)} + \underbrace{\sum_{i=1}^{2^{n-1}-1} \exp\left[-\frac{\left(V_{\rm th} - i\frac{\theta\sigma_{\rm th}}{2^n}\right)^2}{2\sigma_{\rm th}^2}\right]}_{(2)} \right] \right\} + \frac{1}{\sigma_{\rm th}\sqrt{2\pi}} \cdot \left\{ \underbrace{H\left(V_{\rm th} - \frac{\theta\sigma_{\rm th}}{2^{n+1}}\right) \cdot \exp\left[-\frac{\left(V_{\rm th} + \frac{\theta\sigma_{\rm th}}{2}\right)^2}{2\sigma_{\rm th}^2}\right]}_{(3)} + \underbrace{H\left(\frac{\theta\sigma_{\rm th}}{2^{n+1}} + V_{\rm th}\right) \cdot \exp\left[-\frac{\left(V_{\rm th} - \frac{2^{n-1}-1}{2^n}\theta\sigma_{\rm th}\right)^2}{2\sigma_{\rm th}^2}\right]}_{(4)} \right\} \tag{6}$$

where the equation terms are linked to the various sections of Fig. 4, marked with shades of gray and numbered from 1 to 4 (numbers 3 and 4 referring to the PDF portions laying outside the DAC output range). In (6), $H(x)$ is the Heaviside function. The standard deviation $\sigma_{\rm th,c}$ of the threshold distribution after correction can be calculated as

$$\begin{aligned}\sigma_{\rm th,c} &= \sqrt{\int_{-\infty}^{+\infty} p_{n,\theta}(V_{\rm th}) V_{\rm th}^2 dV_{\rm th}} \\ &= \sigma_{\rm th}\sqrt{\int_{-\infty}^{+\infty} \sigma_{\rm th} \cdot p_{n,\theta}(\sigma_{\rm th}u) u^2 du}. \end{aligned} \tag{7}$$

Therefore,

$$\frac{\sigma_{\rm th,c}}{\sigma_{\rm th}} = \sqrt{\int_{-\infty}^{+\infty} \sigma_{\rm th} \cdot p_{n,\theta}(\sigma_{\rm th}u) u^2 du}, \tag{8}$$

where, taking into account that (for $a \neq 0$) $H(ax) = H(x)$, it can be demonstrated that $\sigma_{\rm th} \cdot p_{n,\theta}(\sigma_{\rm th}u)$ (and, as a consequence, $(\sigma_{\rm th,c})/(\sigma_{\rm th})$) is independent of $\sigma_{\rm th}$ and is a function of $n$ and $\theta$ only. For the sake of accuracy, it has to be pointed out that the above equality ($H(ax) = H(x)$) should actually be regarded as a weak one [11]. This is apparent if one calculates the following integral

$$\begin{aligned} I &= \int_{-\infty}^{+\infty} [H(ax) - H(x)]\delta(x)dx \\ &= \left[\frac{1}{2a} \cdot H^2(ax) - \frac{1}{2} \cdot H^2(x)\right]_{-\infty}^{+\infty} = \frac{1-a}{2a}, \end{aligned} \tag{9}$$

where $\delta(x)$ is the Dirac delta function. Since, for $a \neq 1$, $I \neq 0$, (9) points out that $H(ax) \simeq H(x)$, in the sense that they are not identical, but rather, they differ in some way at $x = 0$. On the other hand, if $\phi(x)$ is a well-behaved function, then $\int_{-\infty}^{+\infty}[H(ax) - H(x)]\phi(x)dx$ is infinitesimal.

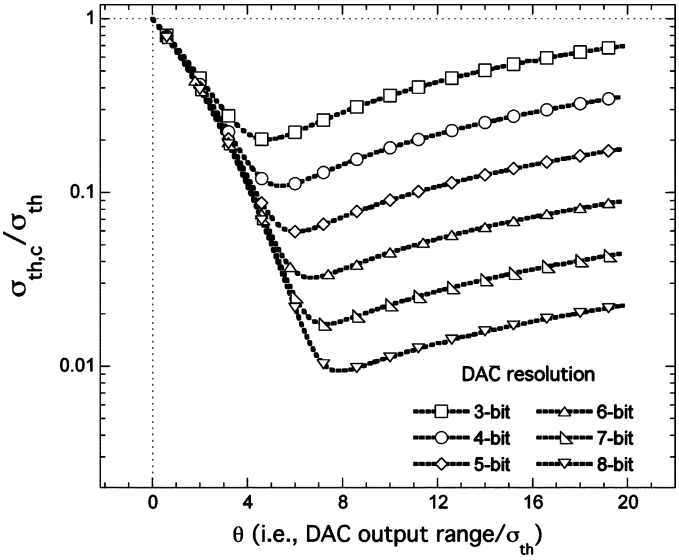


Fig. 5. $(\sigma_{\rm th,c})/(\sigma_{\rm th})$ ratio as a function of the parameter $\theta$ for different values of the DAC resolution.

Fig. 5 shows the $(\sigma_{\rm th,c})/(\sigma_{\rm th})$ ratio (in the following also referred to as correction factor) as a function of the parameter $\theta$ for different values of the DAC resolution (i.e., number of bits). As already suggested, for a given resolution $n$, small values of the DAC range leave a significant fraction of the thresholds out of the correction span, therefore limiting the effectiveness of the process. Suboptimal results are obtained also when too large a range is set, as the consequently large width of the correction step is unsuitable for fine threshold adjustment. Actually, an optimum value of the DAC output range can be found, depending on the resolution. Fig. 6 shows $\theta_{\rm opt}$, i.e., the optimum DAC range divided by the threshold dispersion $\sigma_{\rm th}$, as a function of the number of bits of the DAC. The points can be interpolated by the following linear equation,

$$\theta_{\rm opt}(n) = a + b \cdot n, \tag{10}$$

with $a \simeq 2.96$ and $b \simeq 0.63$. Fig. 7 shows the minimum $\sigma_{\rm th,c}/\sigma_{\rm th}$ ratio as a function of the correction DAC resolution.

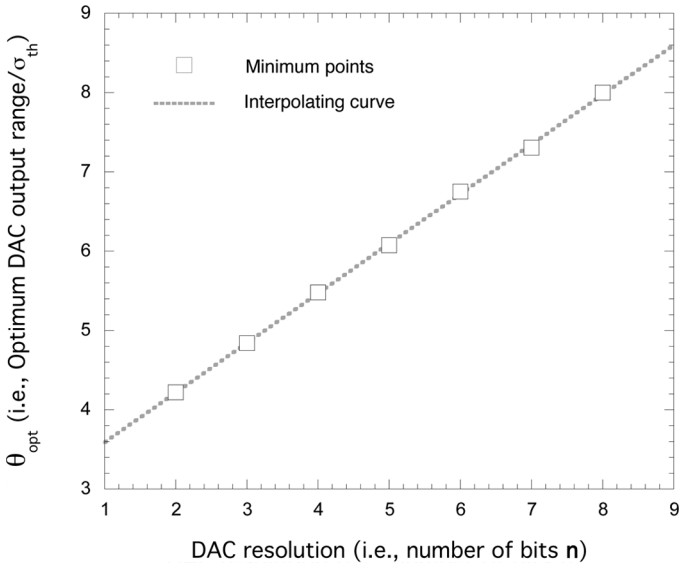


Fig. 6. Optimum DAC range divided by the threshold dispersion $\sigma_{\rm th}$, as a function of the number of bits of the DAC. The interpolating function (10) is shown together with the minimum points (open squares) obtained from Fig. 5.

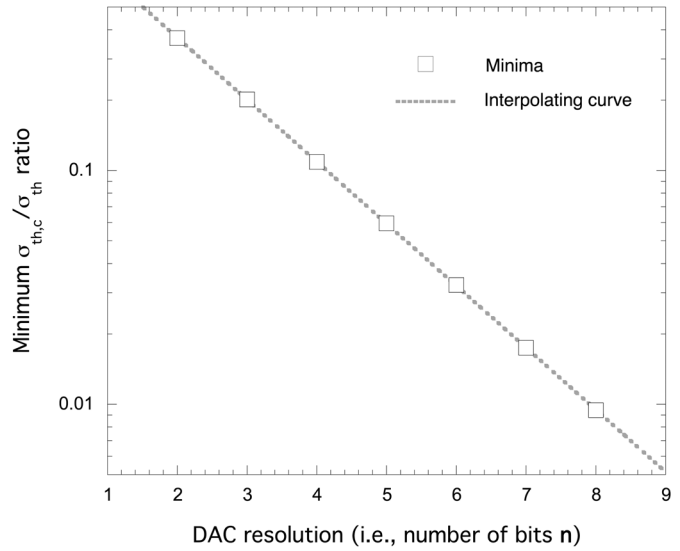


Fig. 7. Minimum $\sigma_{\rm th,c}/\sigma_{\rm th}$ ratio as a function of the correction DAC resolution. The interpolating function (11) is shown together with the minima (open squares) obtained from Fig. 5.

The minimum correction factor was found to follow an exponential law, given by the following interpolating function,

$$\min_{\theta}\left\{\frac{\sigma_{\rm th,c}}{\sigma_{\rm th}}\right\}(n) = c\cdot e^{-d\cdot n}, \tag{11}$$

with $c \simeq 1.26$ and $d \simeq 0.61$. Note from Fig. 7 that a 4 bit correction DAC can theoretically reduce the system threshold dispersion by a factor of 10. From (11), once the required correction factor $cf$ has been specified, the minimum theoretical resolution $n_{\rm min}$ of the correction DAC can be derived as

$$n_{\rm min} = \left\lceil d\cdot \ln\left(\frac{c}{cf}\right)\right\rceil, \tag{12}$$

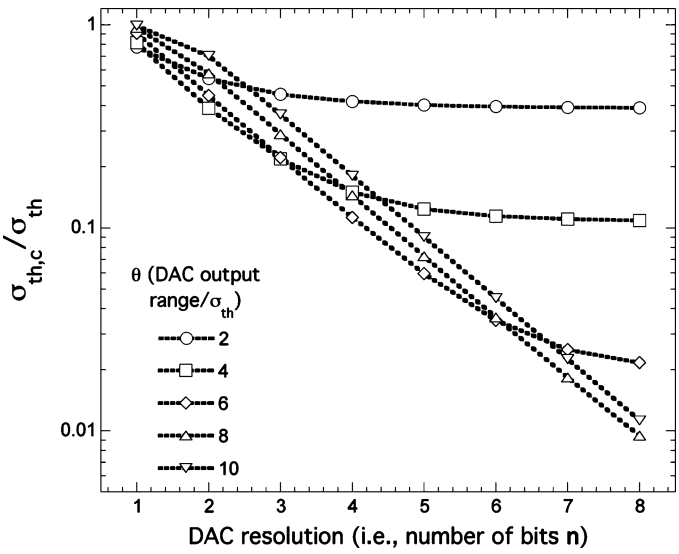


Fig. 8. Threshold correction factor as a function of the DAC resolution for different values of the DAC output range/$\sigma_{\rm th}$ ratio.

where $\lceil x\rceil$ is the minimum integer larger than x. Fig. 8 shows the threshold correction factor as a function of the DAC resolution for different values of the DAC output range. For a given value of the DAC range, the correction factor as a function of the DAC resolution is found to reach an asymptotic value, which can be shown to be given by

$$\begin{aligned}\lim_{n\to+\infty}\frac{\sigma_{\rm th,c}}{\sigma_{\rm th}} &= \left\{\sqrt{\frac{2}{\pi}}\int_0^{\infty} e^{-\frac{(u+\frac{\theta}{2})^2}{2}}u^2du\right\}^{\frac{1}{2}}\\ &= \frac{1}{2}\left(\frac{-4e^{-\frac{\theta^2}{8}}+\sqrt{2\pi}(4+\theta^2)\mathrm{Erfc}\left(\frac{\theta}{2\sqrt{2}}\right)}{\sqrt{2\pi}}\right)^{\frac{1}{2}}.\end{aligned} \tag{13}$$

The locus of the asymptotic values of the correction factor, which is a function of $\theta$, is shown in Fig. 9. For DAC output ranges exceeding about $6\sigma_{\rm th}$, the distribution tails outside the DAC range can be neglected in the calculation of the post-correction threshold voltage distribution. In this case, $p_{n,\theta}(V_{\rm th})$ can be approximately expressed as

$$p_{n,\theta}(V_{\rm th}) \simeq \frac{2^n}{\theta\sigma_{\rm th}}\int_{-\infty}^{\infty} p(V_{\rm th})dV_{\rm th} = \frac{2^n}{\theta\sigma_{\rm th}}, \tag{14}$$

which leads to the following expression for the threshold correction factor

$$\frac{\sigma_{\rm th,c}}{\sigma_{\rm th}} = \frac{1}{\sigma_{\rm th}}\left(\int_{-\frac{\theta\sigma_{\rm th}}{2^{n+1}}}^{\frac{\theta\sigma_{\rm th}}{2^{n+1}}}\frac{2^n}{\theta\sigma_{\rm th}}V_{\rm th}^2dV_{\rm th}\right)^{\frac{1}{2}} = \frac{\theta}{2^n\sqrt{12}}. \tag{15}$$

The approximated expression shown in (14) for the post-correction distribution is obtained by moving all the thresholds of the original distribution in a bin $(\theta\sigma_{\rm th})/(2^n)$ wide. Note that, from the previous equation

$$\sigma_{\rm th,c}(\theta) = \frac{\theta\sigma_{\rm th}}{2^n\sqrt{12}} = \frac{\mathrm{DAC\,range}}{2^n\sqrt{12}} = \frac{\mathrm{LSB}(\theta)}{\sqrt{12}}, \tag{16}$$

where $\mathrm{LSB}(\theta)$ is the DAC least significant bit. Equation (16) indicates that, for large enough values of $\theta$, the corrected threshold dispersion equals the quantization error of the system. The behavior of the correction factor as obtained from (15) for large $\theta$ values is compared in Fig. 9 with the curves of Fig. 5. As expected, at large values of the $\theta$ coefficient, the approximated curves are virtually indistinguishable from those obtained from the complete expression of $p_{n,\theta}(V_{\mathrm{th}})$ given by (6).

### B. Monte Carlo Model

The results presented in the previous section, in particular the correction factor curves, were obtained by means of the Mathematica® software by Wolfram Research. Calculation of the correction factor involves computing $(\sigma_{\mathrm{th},c})/(\sigma_{\mathrm{th}})$ as represented in (8), which includes the distribution of the corrected threshold voltage $p_{n,\theta}(V_{\mathrm{th}})$. The number of terms appearing in $p_{n,\theta}(V_{\mathrm{th}})$ increases exponentially with the DAC resolution $n$, obviously impacting on the computing time. In order both to validate the results obtained in the previous section and to implement a faster and more versatile tool for DAC design, a model of the system, based on a Monte Carlo (MC) algorithm, has been developed in the LabVIEW® environment. The block diagram of Fig. 10 describes the operation and features of the program. The first block generates a random m-element vector (with $m$ the number of channels of the system) of threshold voltages. The vector elements are distributed with a Gaussian probability density function with standard deviation $\sigma_{\mathrm{th}}$ provided by the program user. The threshold correction is obtained by subtracting from each threshold voltage element of the random vector the value of the same element after quantization with a suitable stair-step function. The amount of correction that can be made to the threshold is limited by the DAC output range. This is accounted for by the limiter block following the quantizer, featuring a negative saturation level, $-(2^n-1)/(2)\cdot q$, and a positive one, $(2^n+1)/(2)\cdot q$. The developed Monte Carlo model also offers the possibility to include DAC non-idealities in the analysis, in particular, as shown in Fig. 10, offset and gain errors, differential non linearity (DNL) and integral non linearity (INL). Fig. 11 shows the correction factor as a function of the correction DAC output range for different values of the DAC resolution $n$ obtained from the described Monte Carlo model. The results are perfectly consistent with the values obtained through computation with the analytical model discussed in the previous section, also displayed in the figure. As an example of the Monte Carlo tool capabilities, Fig. 12 shows the correction factor as a function of the DAC output range as obtained from MC simulations in the case of a 6-bit converter. The ideal curve is compared with four other plots accounting for the effects of differential non-linearity on the DAC correction capabilities. DNL is forced into the DAC response by generating a set of $2^n$ uniformly distributed, pseudorandom numbers in the range $[-(\mathrm{DNL_{MAX}}\cdot\mathrm{LSB})/(2),(\mathrm{DNL_{MAX}}\cdot\mathrm{LSB})/(2)]$ to be added to the $2^n$ levels of the converter input-output characteristic. As a result, $|\mathrm{DNL}|\leq\mathrm{DNL_{MAX}}$. While the correction factor is barely affected by DNL at small $\theta$ values, around the minimum and for larger values of the DAC output range, the effect becomes significant. This result can be explained by assuming that, in the case of a DAC affected by a differential

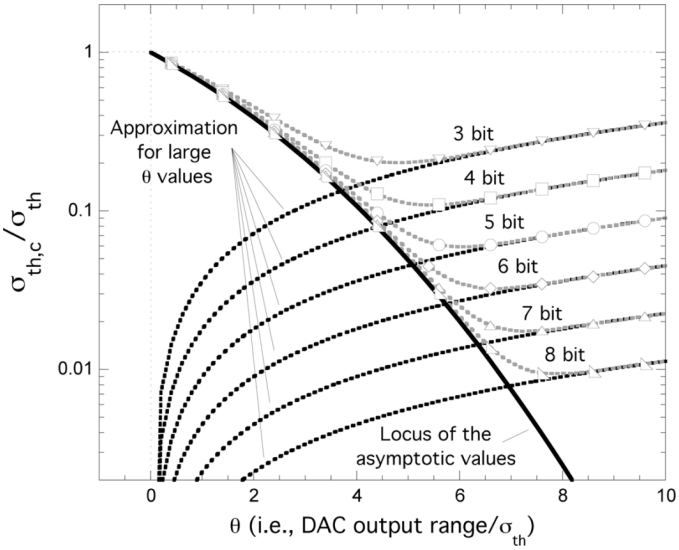


Fig. 9. Approximated correction factor curves as obtained for large $\theta$ values together with the curves obtained from the complete expression of $p_{n,\theta}(V_{\mathrm{th}})$ given by (6) (same curves as in Fig. 5). The locus of the asymptotic values of the correction factor for large DAC resolution is also shown.

non-linearity, the corrected threshold dispersion $\sigma_{\mathrm{th},c,\mathrm{DNL}}$ accounting for the DNL can be obtained as the quadratic sum of the ideal corrected threshold dispersion $\sigma_{\mathrm{th},c}$ and the standard deviation of the DNL-induced error in the DAC output level (which can be calculated to be $(\mathrm{DNL_{MAX}}\cdot\mathrm{LSB})/(\sqrt{12})$),

$$\sigma_{\mathrm{th},c,\mathrm{DNL}}=\sqrt{\sigma_{\mathrm{th},c}^2+\frac{\mathrm{DNL_{MAX}^2}\cdot\mathrm{LSB}^2}{12}}=\sqrt{\sigma_{\mathrm{th},c}^2+\frac{\mathrm{DNL_{MAX}^2}\cdot\theta^2\cdot\sigma_{\mathrm{th}}^2}{12\cdot 2^{2n}}}. \tag{17}$$

From the previous equation, the expression of the correction factor accounting for a DNL error in the DAC can be obtained,

$$\frac{\sigma_{\mathrm{th},c,\mathrm{DNL}}}{\sigma_{\mathrm{th}}}=\sqrt{\frac{\sigma_{\mathrm{th},c}^2}{\sigma_{\mathrm{th}}^2}+\frac{\mathrm{DNL_{MAX}^2}\cdot\theta^2}{12\cdot 2^{2n}}}. \tag{18}$$

In Fig. 12, as an example, (18) has been computed in the case $\mathrm{DNL_{MAX}}=0.75$. The resulting curve is in good agreement with the outcomes of the Monte Carlo simulations.

## IV. Validation of the Design Criteria

The results presented in the previous sections have been validated both through circuit simulation and by comparison with experimental data available in the literature. The case of a 4-bit correction DAC part of a binary readout channel for pixel detectors is discussed in the following subsection.

### A. Circuit Simulations

Fig. 13 shows a circuit schematic describing the operation of a correction DAC, which, incidentally, has been implemented in the analog readout channels for hybrid and monolithic pixel detectors for the SuperB silicon vertex tracker [12]. The circuit is being designed in a vertically integrated CMOS technology with minimum feature size of 130 nm [13]. The PMOS $M_P$,

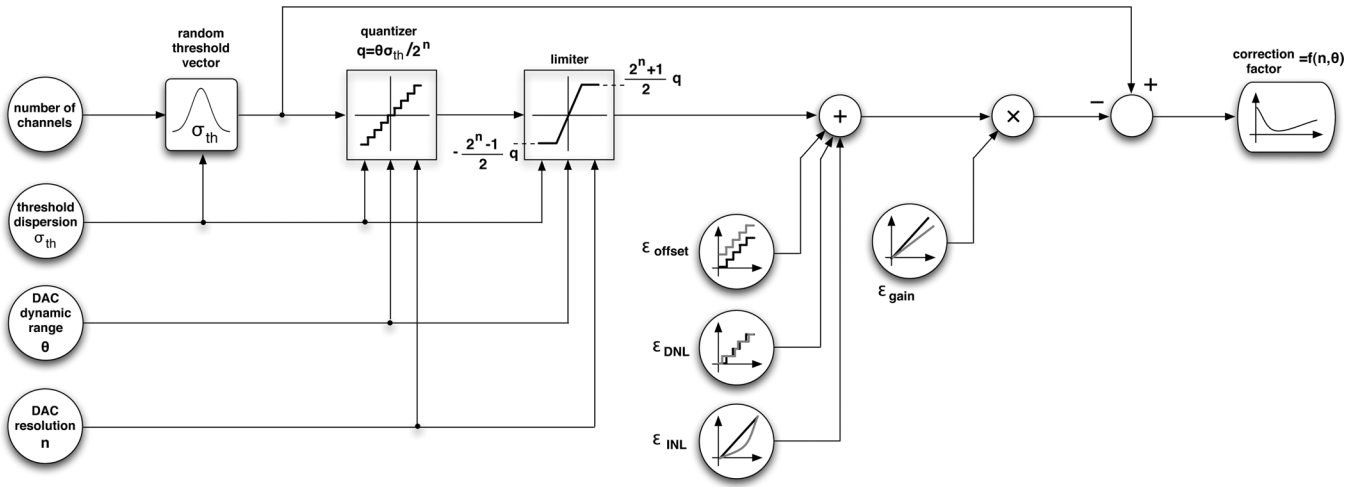


Fig. 10. Block diagram of the Monte Carlo tool for threshold correction modeling and simulation.

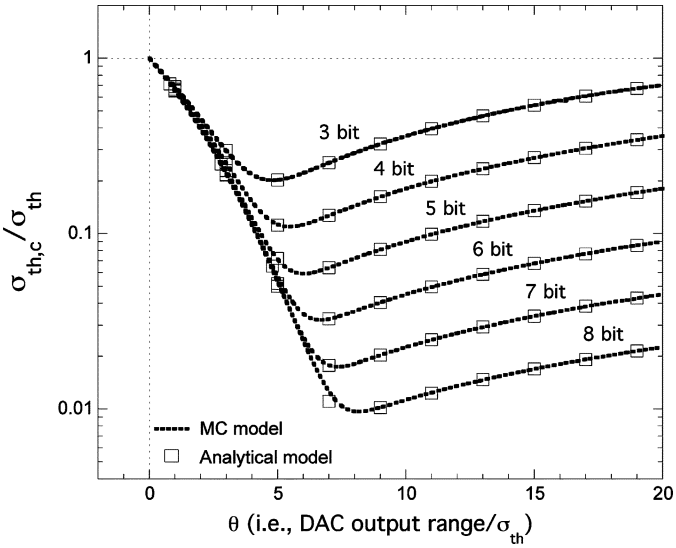


Fig. 11. Correction factor as a function of the correction DAC output range for different values of the DAC resolution $n$ obtained from the Monte Carlo (MC) model. The curves are compared with the values obtained with the analytical model discussed in Section III.A.

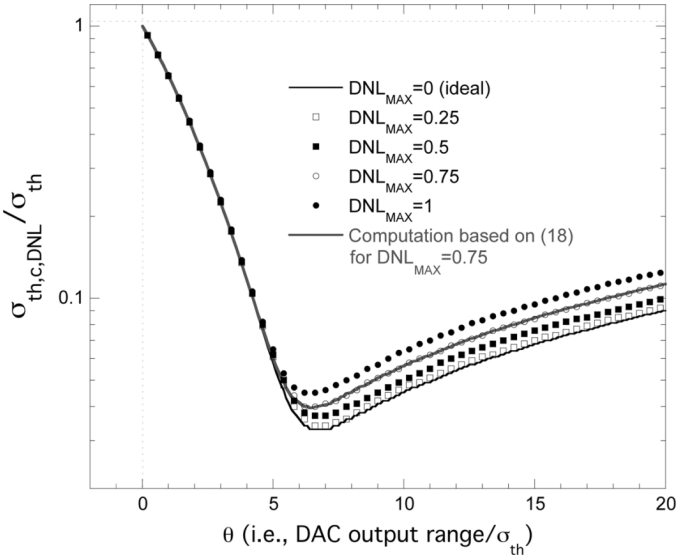


Fig. 12. Effect of differential non-linearity on the correction factor in the case of a 6-bit DAC.

biased through the current source $I_b$, acts as a level shifter between the shaper output and the discriminator input. The voltage shift $V_{\rm DAC}$ can be changed by changing the current in the $I_{\rm DAC}$ current source. In particular

$$V_{\rm disc} - V_{\rm sh} = V_{\rm DAC} = V_{\rm DAC0} + v_{\rm DAC}, \qquad (19)$$

where $V_{\rm sh}$ is the voltage at the shaper output, $V_{\rm disc}$ is the voltage at the discriminator input and $V_{\rm DAC0}$ is the value of $V_{\rm DAC}$ for $I_{\rm DAC} = 0$, while $v_{\rm DAC}$ depends on $I_{\rm DAC}$. Fig. 14 shows the threshold distribution in the case of a set of 9000 channels before and after correction with the 4 bit DAC. The starting threshold distribution has been obtained through a circuit Monte Carlo simulation, accounting for random parameter variations in the microelectronic process and for the subsequent channel-to-channel mismatch in the DC operating point at the discriminator input. In the case considered in Fig. 14, $M_P$ was operated at $I_b = 350$ nA, while an elementary step of 10 nA was used in the correction DAC, resulting in a correction factor of 0.192. Fig. 15 shows the correction factor as a function of the parameter $\theta$ as obtained through circuit simulations (open square markers). The simulation data are compared to the ideal threshold correction curve resulting from (8) for $n = 4$. They can be observed to be in fair agreement, especially around the minimum values of the plot. At larger output ranges of the DAC, a slight discrepancy (about 10% in the worst case) can be detected between circuit simulations and theoretical curve. In order to understand the results of Fig. 15, the operation of the correction circuit of Fig. 13 is worth a more detailed treatment. In the specific case discussed here, $I_{\rm DAC}$ is generated by means of a current steering DAC architecture based on the thermometric selection of unity current cells [14]. However, the following considerations are independent of the particular solution adopted for the converter design. Even in

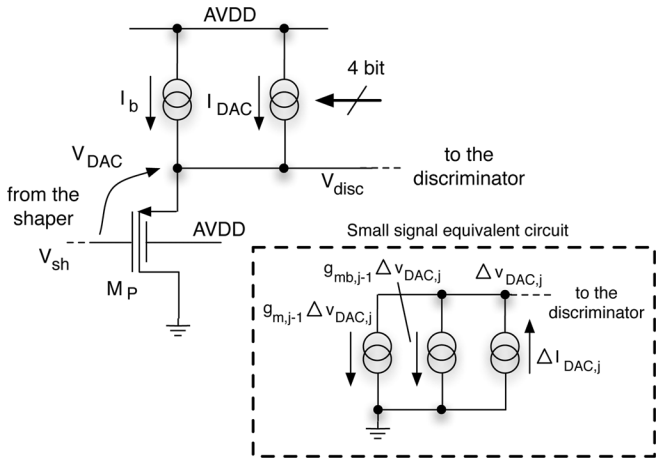


Fig. 13. Circuit schematic describing the operation of the correction DAC. Also, the small signal equivalent model of the circuit is shown.

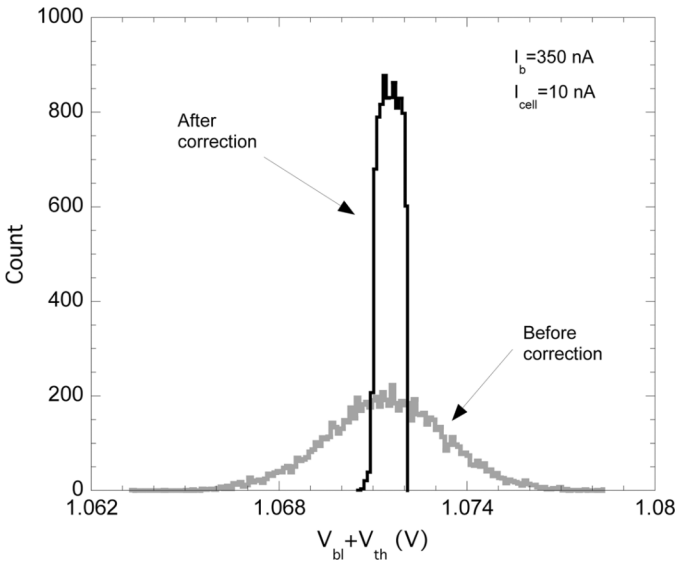


Fig. 14. Simulated effect of a 4-bit threshold correction on a set of 9000 channel.

the ideal case where the DAC controlling the $I_{\rm DAC}$ current is not affected by any non-linearity, the change in $V_{\rm DAC}$, i.e., $v_{\rm DAC}$, corresponding to a change in $I_{\rm DAC}$, is intrinsically non linear with the programming code of the converter due to the non linear $I_D$-$V_{\rm SG}$ characteristic of the MOSFET $M_P$. In the simulations shown in Fig. 15, $M_p$, which features $W/L = 10$ $\mu$m/4 $\mu$m, is made to work at currents ranging from 150 nA to 3 $\mu$A, corresponding to a normalized drain current $I_{D,\rm norm} = I_D \cdot (L)/(W)$ ranging from 60 nA to 1.2 $\mu$A. If compared to the characteristic normalized drain current $I_z^*$, which is by definition located at the center of the moderate region of operation, separating the weak from the strong inversion region, the considered interval of $I_b$ values forces the device to operate in moderate inversion [15]. Actually, although experimental data are not available for the 130 nm CMOS technology considered here, an $I_z^*$ of a few hundreds of nA can be extracted from simulations. This is also in fair agreement with the value of $I_z^*$ obtained from experimental characterization of PMOS devices belonging to a different 130 nm process [16]. In

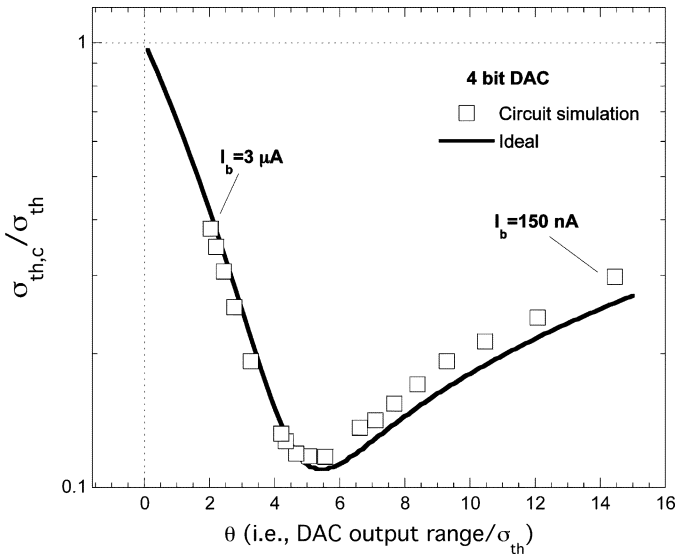


Fig. 15. Simulated threshold correction factor compared with the performance of an ideal DAC and of a current steering DAC like the one of Fig. 13 with its intrinsic non-linearity.

the moderate region of operation, no simple representation of the $I_D - V_{\rm SG}$ relationship can be used, as it would be the case instead in the weak or in the strong inversion approximations. Still, some general considerations can be made by referring to the schematic in the inset of Fig. 13, representing the small signal behavior of the threshold correction circuit at each incremental step of the $I_{\rm DAC}$ current. The circuit also accounts for the body effect in $M_p$ through the bulk transconductance $g_{mb,j-1}$. In the following, the DAC will be assumed to be ideal. Therefore, if $I_{{\rm DAC},j} = j \cdot I_{\rm cell}$, where $I_{\rm cell}$ is the current of the unity cell of the DAC, $j = 0, \ldots, 2^n - 1$ and $n$ is the DAC resolution, then $\Delta I_{{\rm DAC},j} = I_{{\rm DAC},j} - I_{{\rm DAC},j-1} = I_{\rm cell}$, is independent of $j$. From the small signal model of Fig. 13,

$$\Delta v_{{\rm DAC},j} = \frac{I_{\rm cell}}{g_{m,j-1} + g_{mb,j-1}}, \tag{20}$$

where $\Delta v_{{\rm DAC},j}$ is the change in $v_{\rm DAC}$ due to $j$-th step in the DAC current and $g_{m,j-1}$ and $g_{mb,j-1}$ are the channel and the bulk transconductance respectively as they result from the $j-1$-th increment in $I_{\rm DAC}$. If $v_{\rm DAC}(j)$ is the voltage change at the output of the correction circuit after the $j$-th step of the DAC current, then

$$\begin{aligned} v_{\rm DAC}(j) &= \sum_{i=1}^{j} \Delta v_{{\rm DAC},i} \\ &= I_{\rm cell} \cdot \sum_{i=1}^{j} (g_{m,i-1} + g_{mb,i-1})^{-1}. \end{aligned} \tag{21}$$

Note that, since both the channel and the bulk transconductances increase with the drain current, then $\Delta v_{{\rm DAC},j} < \Delta v_{{\rm DAC},j+1}$, from which it can be concluded that $v_{\rm DAC}$ is not linear with $I_{\rm DAC}$. A non linearity error $\epsilon$(j) can be defined as

$$\epsilon(j) = \frac{v_{\rm DAC}(j) - v_{{\rm DAC},id}(j)}{{\rm LSB}_{id}}, \tag{22}$$

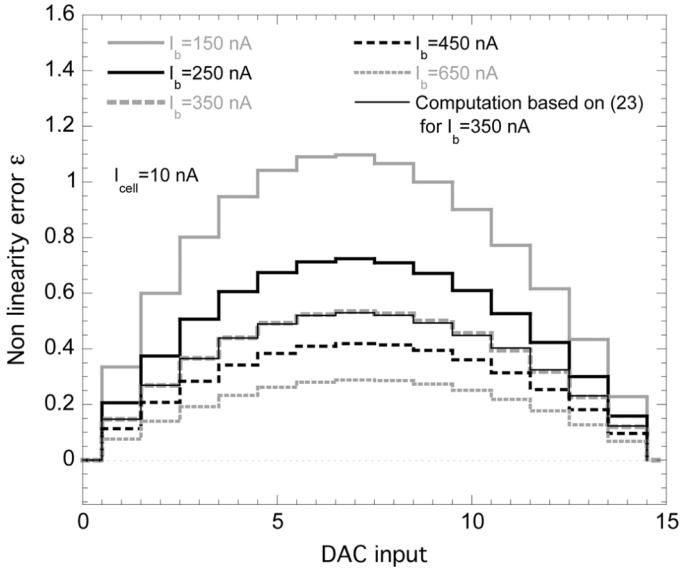


Fig. 16. Non linearity error as resulting from circuit simulations.

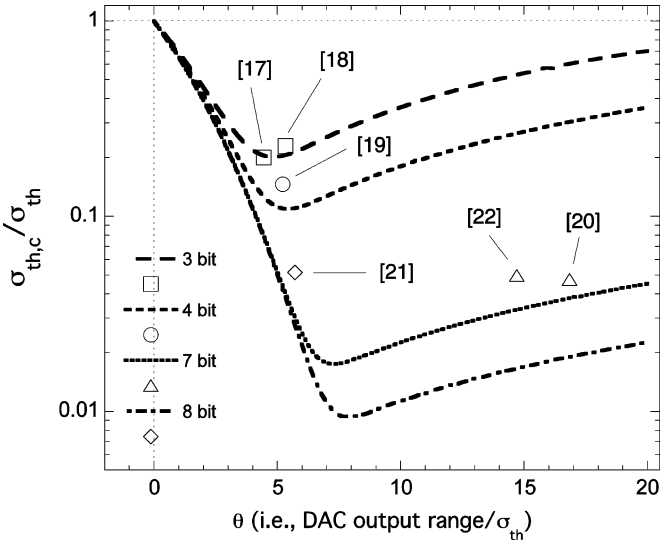


Fig. 17. Comparison between ideal threshold correction curves and published experimental data.

where

$$\mathrm{LSB}_{id} = \frac{\sum_{i=1}^{2^n-1} \Delta v_{\mathrm{DAC},i}}{2^n - 1}, \quad v_{\mathrm{DAC},id}(j) = j \cdot \mathrm{LSB}_{id}.$$

Obviously, $\epsilon(j) = 0$ would indicate that the correction circuit is linear with $I_{\mathrm{DAC}}$. Fig. 16 shows the non linearity error as obtained from circuit simulations of the 4-bit DAC at different values of the bias current $I_b$. The non-linearity, which can be seen to increase with decreasing $I_b$, can actually provide an explanation for the slight discrepancy observed in Fig. 15 between the simulation points and the ideal curve. If (21) is used in the definition of $\epsilon(\mathrm{j})$, then

$$\epsilon(j) = (2^n - 1) \cdot \frac{\sum_{i=1}^{j} (g_{m,i-1} + g_{mb,i-1})^{-1}}{\sum_{i=1}^{2^n-1} (g_{m,i-1} + g_{mb,i-1})^{-1}} - j. \quad (23)$$

Again in Fig. 16, the non-linearity error as obtained from simulations by straightforward application of (22) is compared with the error computed by means of (23) with $g_{m,i-1}$ and $g_{mb,i-1}$ provided by circuit simulations. The two staircase curves are in very good agreement, demonstrating that the small signal model of Fig. 13 is able to predict the nonlinear behavior of the correction circuit.

### B. Comparison With Published Experimental Data

As already mentioned in the introduction to this work, the use of a digital-to-analog converter for fine tuning of the threshold in a binary multichannel readout circuit is common practice when continuous, non synchronous operation is involved. Several examples of implemented correction DACs are available in the literature [17]–[22]. Fig. 17 shows the threshold correction factor as a function of the DAC output range/$\sigma_{\mathrm{th}}$ ratio for four different values of the DAC resolution. Ideal curves (dashed and dash-dotted lines) are compared with data points extracted from the literature (open markers). In the figure, reference is made to the papers listed in the bibliography. As it can be observed, the experimental data are fully compatible with the theoretical behavior predicted by (8). Difference between the experimental data and the ideal curves can likely be ascribed to non linearity errors in the DAC operation.

## V. Correction Capabilities, Area and Power Dissipation Trade-Off

The discussion in this paper has been mainly focused on the theoretical aspects of the threshold correction problem and on its optimum solution, completely disregarding the impact it may have on the converter design and performance. It may be considered quite intuitive that, as the number of bit increases, the correction power of a DAC is also increased. The improvement has actually been quantified in Section III.A by means of (11), showing that the minimum $(\sigma_{\mathrm{th},c})/(\sigma_{\mathrm{th}})$ ratio decreases by a factor $\exp(-d) \simeq 0.54$ for every additional bit of resolution. However, a price has to be paid for the correction performance improvement in terms of area occupancy and static power dissipation (dynamic power consumption is not considered here, as, in the application of interest, the DAC configuration is set once for all before front-end operation is started, or may be changed just occasionally during operation). The price obviously depends on the adopted architecture. However, for the purpose of providing the reader with some practical example, reference can be made to the current steering DAC discussed in detail in Section IV.A. In that case, increasing the resolution by one bit entails doubling the number of unity current cells and more than doubling the area of the logic circuitry for binary-to-thermometric encoding [14]. Power dissipation $P(n)$ as a function of the DAC resolution can be expressed as

$$P(n) \simeq V_{\mathrm{DD}} \cdot [I_b + (2^n - 1) \cdot I_{\mathrm{cell}}], \quad (24)$$

where the contribution from bias networks has been neglected. The power dissipation may actually be dominated by the contribution from $I_b$ at small resolutions ($n \leq 5$), as it happens in the case of the correction DAC discussed in the previous section.

The area occupancy $A(n)$ as a function of the DAC bit number can instead be calculated as

$$A(n) \simeq A_u \cdot (2^n - 1) + A_d \cdot n \cdot 2^n \tag{25}$$

where $A_u$ is the area of the unity current source and $A_d$ is the area of a single logic gate. The area covered by the bias networks, the level shifter ($M_p$ in Fig. 13) and the interconnects has not been included. As it is apparent from (25), the steep increase in $A(n)$ with the resolution can make the design of a DAC unpractical for $n > 8$, all the more so in high granularity systems for particle detectors. However, techniques for the generation of the thermometric code are available that help reduce the impact of the encoder on the overall DAC area. For very large resolutions, segmented DACs, resulting from the combination of the unary (thermometer-coded) and binary weighted approaches, may guarantee a better trade-off between performance and area [23].

## VI. Conclusion

In this paper, to the best of the authors' knowledge for the first time, a detailed theoretical treatment of the threshold correction problem in multichannel, binary readout systems for radiation detectors has been presented. The proposed model provides the designer with guidelines on how to choose, based on the application requirements, the minimum number of bits and the output range of the DAC for threshold correction, once a target value for the threshold dispersion at the input of the voltage discriminator is given. The design of the latter stage in the considered applications is generally constrained by area and speed specifications, which prevents the designer from satisfying the minimum threshold dispersion requirements without additional blocks. In general, the correction DAC can be designed in such a way that the output range and, as a consequence, the threshold change for trim step, is adjustable, thereby allowing the chip user to optimize DAC operation. On the other hand, the DAC resolution has to be set during the design phase, based on the desired correction factor. A Monte Carlo model, also accounting for DAC non idealities, has been developed both to corroborate the theoretical results and to provide a faster and more flexible design tool. The models have been validated both through circuit simulations, concerning a 4 bit correction DAC for pixel readout chips, and by comparison with data available in the literature. The results presented in this paper have been exploited in the design of the front-end circuits for hybrid and monolithic pixel detectors of the SuperB silicon vertex tracker. Chip characterization will be used to provide further experimental validation of the proposed model.

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