



UNIVERSITY OF BERGAMO

School of Engineering

Master Degree in Computer Engineering

Class N. LM-32 - Ingegneria Informatica

Characterisation of the readout electronics of the Si(Li) tracker for the first flight of the GAPS experiment

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Master Thesis

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ACADEMIC YEAR 2021 / 2022

Acknowledgment

I am overwhelmed in all humbleness and gratefulness to acknowledge my depth to my advisor Prof. Massimo Manghisoni for the continuous support of my thesis work, for his patience, motivation, enthusiasm and immense knowledge. His guidance helped me in all the time of research and writing of this thesis. I could not have imagined having a better advisor and mentor for master thesis work.

I would also like to thank Elisa and Paolo for their encouragement, insightful comments and support during my entire stay in the electronics laboratory.

Finally, I wish to thank my parents Luisa and Bortolo for their unconditional trust, timely encouragement, and endless patience.

If offered a seat on a rocket ship, don't ask what seat.
Just get on.

Christa McAuliffe, Challenger Astronaut

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Introduction

According to what is supported by some astrophysics theories, about 90% of the mass of the universe is made by a hypothetical form of matter named Dark Matter and its discovery is one of the main scientific objectives of the 21st century in the field of physics research. Dark Matter is not directly observable, since, unlike normal matter, it does not emit electromagnetic radiation and only manifests itself through gravitational effects.

In this context, the General AntiParticle Spectrometer (GAPS) project stands as a modern approach to the indirect search of Dark Matter through the detection of cosmic antideuterium. The experiment is developed by an international collaboration that includes Japanese, US and Italian institutes, and it is funded by NASA, INFN, ASI, JAXA and other research and academic institutions. The instrument relies on two detectors: a time-of-flight system, which tags candidate events for the detector to save and makes a precise velocity measurement, and a tracker system based on lithium-drifted silicon, Si(Li), detectors, which serves as the target and tracker for the initial cosmic-ray particle and its annihilation products. An Application Specific Integrated Circuit (ASIC) called *SLIDER32* designed in a commercial 180 nm CMOS technology is currently employed for the readout of the lithium-drifted silicon detectors and will be used for the first flight of the experiment scheduled for late 2023 from the the McMurdo station in Antarctica. The experimental characterisation of the ASIC is the focus of the thesis work discussed in the following pages.

The manuscript is organised as follows. Chapter 1 describes the characterisation work that has been performed on the ASIC using a purposely built test board in order to carry out an analysis of the performance of the integrated circuit under varying temperature conditions. The measurements were performed to highlight the variations to which the transfer function, current reference, global threshold voltage and electronic noise are subjected.

Introduction

Chapter 2 analyses the test and validation work that has been carried out on the flight components of the lithium-drifted silicon tracker of the GAPS experiment. The test procedures for each of the items and the results obtained are reported, detailing for each component the expected performance compared to that obtained during the test procedure.

Lastly, Chapter 3 reports the results obtained during the experimental demonstration of cosmic muon detection using a fully assembled Si(Li) tracker module, using the ArduSiPM cosmic ray and nuclear radiation detector as a trigger for the readout electronics. In addition, this Chapter discusses the characterisation of the fully assembled Si(Li) tracker module, which was also carried out using an Americium 241 source. A full description of the setup used during the experiment and the results obtained are given in this Chapter.

A detailed description of the GAPS experiment, its scientific aims in the context of physics research and the instrument on which it is based are provided in Appendix A, with Section A.1 providing a brief introduction to Dark Matter.

Chapter 1

Evaluation of temperature effects on ASIC performance

This Chapter describes the characterisation activity that has been carried out on the SLIDER32 ASIC, described in Appendix A.2. Specifically, the measurements were taken with a purposely developed test board described in Section 1.1 and were aimed at the evaluation of thermal effects on:

1. Bandgap reference current.
2. Channel input-output characteristic.
3. Digital-to-Analog Converter (DAC) used to set the global threshold voltage.

The characterisation activity has also been focused on the evaluation of electronic noise performance of the readout channel in the form of Equivalent Noise Charge (ENC), measured at a temperature of -40°C , that is, the temperature at which the readout electronics will work during the experiment [1], therefore a precise evaluation of the noise contribution at this temperature is of fundamental importance.

1.1 Test setup description and characterisation process

The setup used for the temperature characterisation of the SLIDER32 ASIC has been designed in two variants, which only differ on one component, namely an Agilent 34461A digital multimeter in version 1, shown in Figure 1.1, in place of a Keysight E3631A DC power supply in version 2, shown in Figure 1.2.

Evaluation of temperature effects on ASIC performance

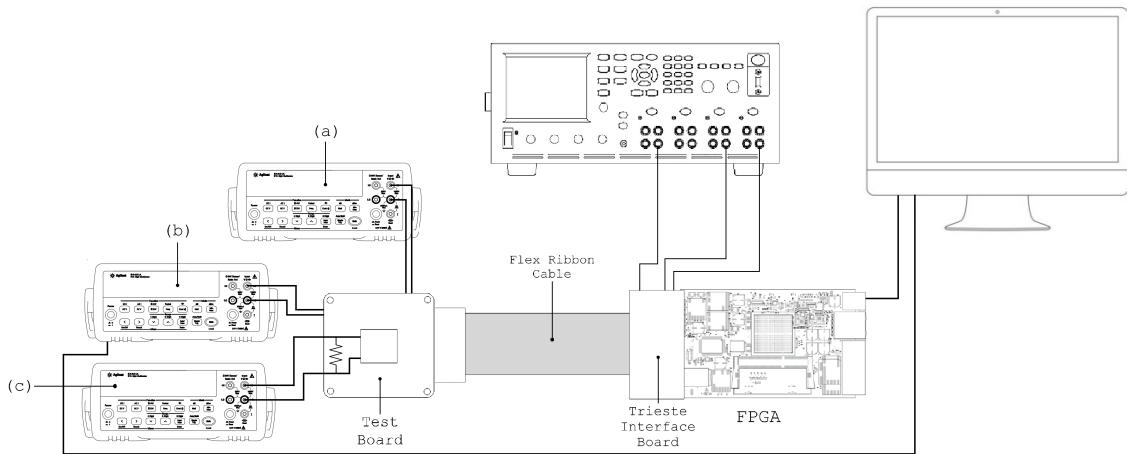


Figure 1.1: SLIDER32 ASIC test board setup 1.

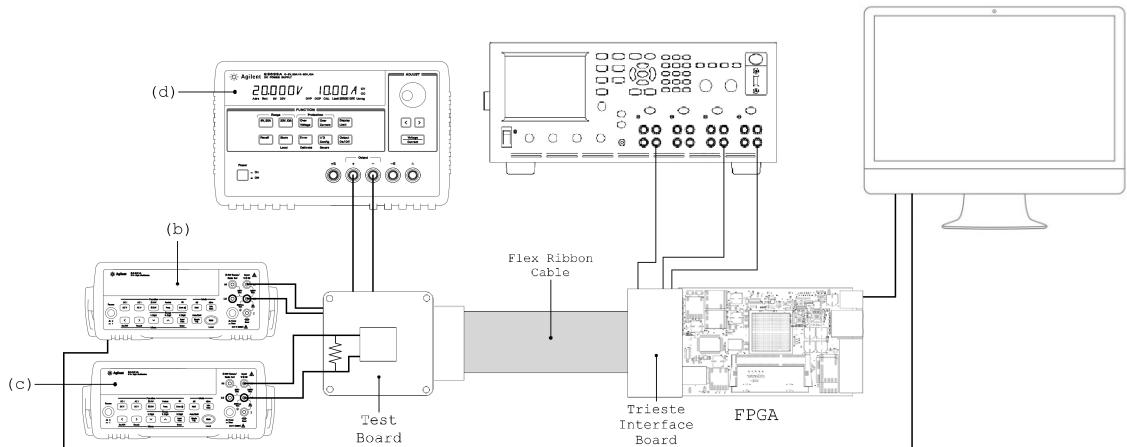


Figure 1.2: SLIDER32 ASIC test board setup 2.

Both variants comprise the components discussed in the following.

- A custom designed test board that allows tests to be performed on the ASIC without having to solder it to the board and then desolder it. This is made possible by a specific test socket that allows the ASIC to be mounted and removed without having to solder it to the test board. This solution also allows several ASICs to be tested using a single board, although being not being the case of the proposed measurements, that involved only ASIC No. 536.

Test setup description and characterisation process

- A Keysight N6705C DC Power analyser providing both analog and digital voltages to the test board. Figure 1.3 shows a screen capture of the power supply. Specifically, channel 1 provides the analog supply voltage (2.4 V), channel 3 provides the digital supply voltage (2.4 V) and channel 4 the 16-bit calibration DAC supply voltage (3.6 V).



Figure 1.3: Keysight N6705C DC power analyser displayed voltages and currents on channels 1, 3 and 4.

- An interface board specifically designed to route the power supplies and the signals through the flex ribbon cable to the test board.
- A flex ribbon cable connecting the interface board to the main test board.
- An ALTERA Cyclone V Field Programmable Gate Array (FPGA).
- A PC running a Python-based testing program called `GAPS_ModuleTester`, currently in its 4th version, connected to the FPGA via two Universal Serial Bus (USB) cables. This software has been specifically developed to perform a series of tests on the SLIDER32 ASIC and it is later described in Section 2.1.
- An Agilent 34401A digital multimeter (b) used to measure the global threshold voltage generated by an 8-bit DAC described in Section 1.4.
- An Agilent 34401A digital multimeter (c) used to measure the reference current as a voltage drop across a $18\text{ k}\Omega$ resistor mounted on the test board.

Specific to version 1 of the test setup is the Agilent 34461A digital multimeter (a) that has been used to measure the `CSAVrefGM` voltage, automatically regulated by a bandgap with respect to the temperature at which the system operates in order to guarantee the correct gain of the readout channel.

Version 2 of the test setup employs a Keysight E3631A DC power supply (d) in order to force the `CSAVrefGM` voltage to a fixed 530 mV value. This voltage corresponds to the one provided by the bandgap at a temperature of -40°C .

The test board has been placed in a climate chamber (model ACS DY110) at temperatures spanning from -40°C to 30°C with 10°C increments. The -40°C to -30°C region has been spanned with 2°C increments. In each test, before performing a test session, the climate chamber has been maintained at the desired temperature for 15 minutes in order to ensure that the electronics reached the correct temperature.

1.2 Current reference

The analog front-end channel designed for the readout of the Si(Li) detectors of the GAPS experiment is comprised of several blocks, as discussed in detail in Appendix A.3. Each element of the channel requires one or more current references to be properly biased. These references should remain constant regardless of external conditions like temperature, variations in the ASIC supply voltage and process parameter mismatch during fabrication. To comply with this requirement, a solution where the reference currents are generated starting from a precise Process, Voltage and Temperature (PVT) voltage reference has been adopted. Starting from this voltage, a 3-bit adjustable current can be obtained. This reference value has been chosen to be $5\,\mu\text{A}$.

A complete set of measurements of the reference current is shown in Figure 1.4. It has been taken by varying both the temperature from -40°C to 30°C and the bias setting on all the 8 possible values. It can be seen that, for a given bias setting expressed as a combination of 3 bits (BBB), the reference current remains almost constant with the temperature and experiences a variation that is presented in Table 1.1. The plot also shows the trend of the reference current as predicted by simulations in 3 different CMOS process corners, namely *Typical-Typical* (TT), *Fast-Fast* (FF) and *Slow-Slow* (SS).

The reference current has been evaluated by measuring the voltage drop across the resistor R_3 on the test board, a 0603 SMD resistor with 0.1% tolerance and 10 ppm/ $^{\circ}\text{C}$ temperature coefficient. The current value has been calculated as

$$I_{ref} = \frac{V_{ref}}{R_3} \tag{1.1}$$

Current reference

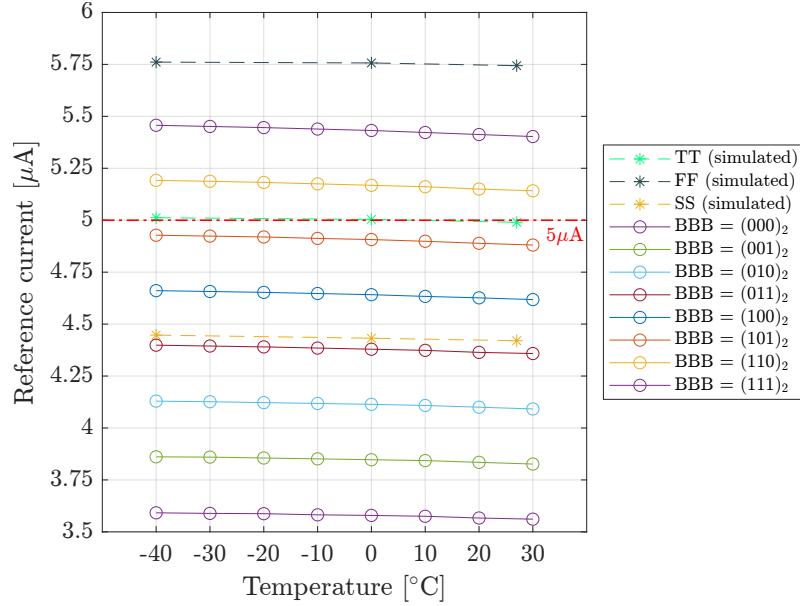


Figure 1.4: Reference current values for a given bias setting with respect to temperature varying from -40°C to 30°C with 10°C increments.

It is possible to see that, among all bias settings (BBB), the one being the closest to the $5\mu\text{A}$ reference value is 101 at almost every temperature considered, thus validating the choice of using this bias setting as the default one in all the other tests performed.

Bias setting [BBB]	Reference current at -40°C [mA]	Reference current at 30°C [mA]	Variation [%]
000	3.59	3.56	0.85
001	3.86	3.83	0.90
010	4.13	4.09	0.91
011	4.40	4.36	0.92
100	4.66	4.62	0.92
101	4.93	4.88	0.96
110	5.19	5.14	0.96
111	5.46	5.40	0.99

Table 1.1: Reference current values and variations with respect to temperature from -40°C to 30°C for each bias settings.

Figure 1.5 proposes on the left the plot of the reference current at temperatures

Evaluation of temperature effects on ASIC performance

varying from -40°C to 30°C with respect to the bias setting. On the right, the measurement at 30°C is compared with simulations and a previously taken measurement at a temperature of 27°C .

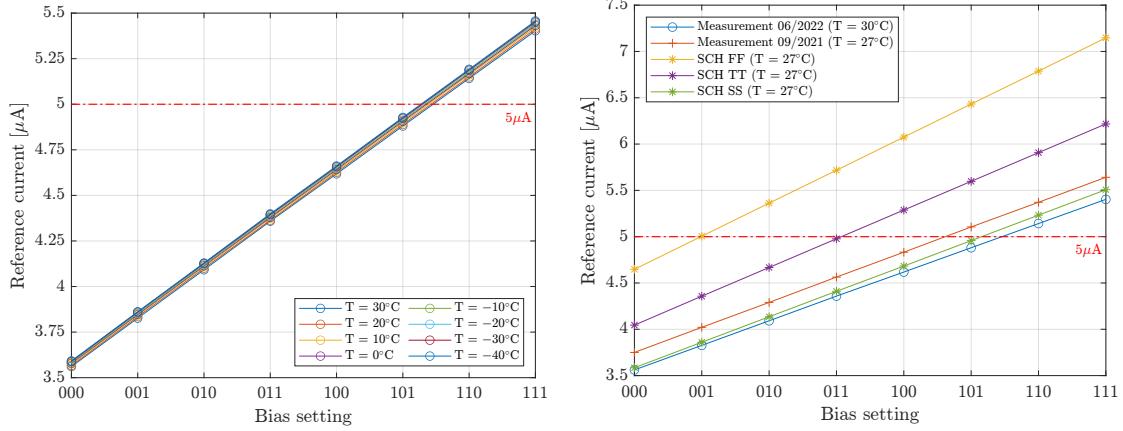


Figure 1.5: Current reference values given temperature with respect to bias setting (on the left) and with respect to simulations at 27°C (on the right).

Figure 1.6 reports the normalised reference current measured at temperatures varying from -40°C to 30°C and compared to the values coming from simulations in the same temperature range.

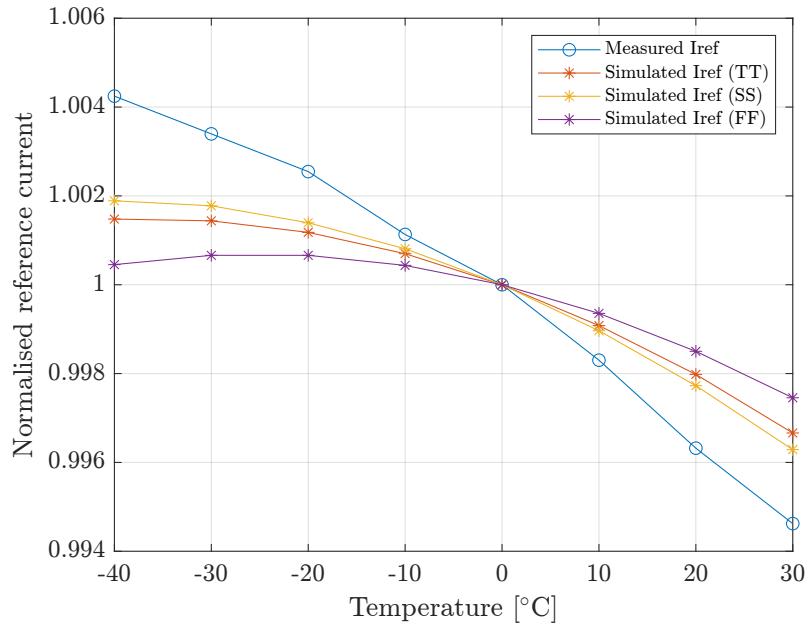


Figure 1.6: Normalised current reference values compared to TT, FF and SS simulations with respect to temperature from -40°C to 30°C .

Current reference

The reference current measurements have also been evaluated by extracting the temperature coefficient, α . The temperature coefficient can be defined as the ratio of change in resistance with respect to a variation of one degree in temperature and can be expressed as

$$\alpha = \frac{1}{I_{T_0}} \cdot \frac{\Delta I}{\Delta T} \quad (1.2)$$

where I_{T_0} represents the current value measured at a reference temperature of 0 °C and ΔT is defined as the difference between the maximum and the minimum temperatures at which the measurements have been performed and it can be expressed as

$$\Delta T = |T_{max} - T_{min}| \quad (1.3)$$

In the same way, ΔI represents the difference between the current measured at the minimum temperature, T_{min} , and that measured at the maximum temperature, T_{max} , and is defined as

$$\Delta I = I_{T_{min}} - I_{T_{max}} \quad (1.4)$$

In the specific case of the presented measurements and simulations, the temperature delta is equal to $\Delta T = 70$ °C. The estimated temperature coefficients, expressed as ppm/°C, are reported in Table 1.2. It is clear to see that the temperature coefficient of the measured reference current is above every one of the temperature coefficients evaluated over the readings coming from simulations in all of the 3 process corners. Nevertheless, the performances are adequate to what is required by the experiment.

α [ppm/°C]	
Measured	137.42
TT model	68.57
SS model	80.00
FF model	42.86

Table 1.2: Estimated temperature coefficients.

1.3 Input-output channel trans-characteristic

In this Section an analysis of the temperature effects on the Si(Li) detector analog readout channel input-output characteristic is given. The curve trend is mainly due to the Charge Sensitive Amplifier (CSA) circuit block, which is responsible for converting the incident charge on the Si(Li) detector into a voltage step signal that is subsequently supplied to the shaper, described in Section A.3.3.

The CSA, whose schematic is shown in Figure 1.7, is based on an inverting gain stage and a feedback capacitor where charge restoration is achieved by a continuous-time Krummenacher network [2].

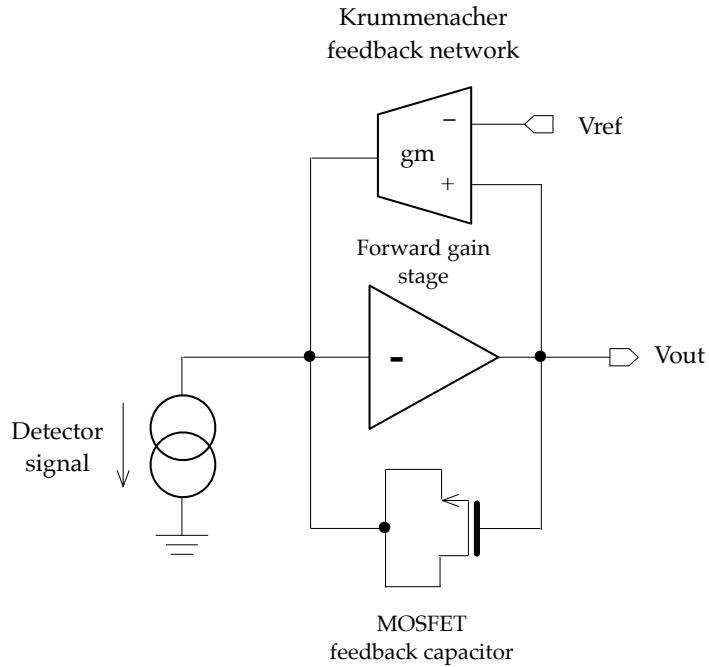


Figure 1.7: Schematic of the charge-sensitive preamplifier, with the forward gain stage, the nonlinear MOSFET capacitor and the Krummenacher feedback network.

The main feature of the CSA is the dynamic signal compression that is achieved by implementing the feedback capacitor with an NMOSFET operating in the inversion mode [3]. In this transistor, source and drain are shorted to form the capacitor terminal connected to the amplifier input, while the gate terminal is connected to the output. At small signal amplitudes, the gate-to-channel voltage is smaller than the transistor threshold voltage and the capacitance is equal to the sum of gate-source and gate-drain overlap capacitances. At larger signal amplitudes, the gate-to-channel voltage becomes larger than the the transistor threshold and the

Input-output channel trans-characteristic

capacitance increases including also the gate-to-channel capacitance. According to this mechanism, the feedback capacitance increases from 175 fF at small input signal amplitudes to 14.7 pF at large signal amplitudes. Since the gain of the CSA is proportional to the inverse of the capacitance this effect results in a gain that decreases with increase in the charge released in the detector.

A reference voltage in the Krummenacher feedback network, denoted as V_{ref} in Figure 1.7 and referred to as **CSAVrefGM** in the following, makes it possible to adjust the amplifier output voltage, so that the signal amplitude at which the CSA switches from high to low gain can be finely tuned, compensating for process and temperature variations. In the nominal setting, the kink in the input-output characteristic occurs at an energy deposited in the detector of about 1 MeV.

In order to obtain the input-output characteristic of the CSA, the channel output must be sampled precisely at the peaking time, set by bit configuration TTT, that for the presented measurements has been chosen to be $\tau_p = 0.98 \mu\text{s}$ (peaking time 4, meaning TTT equal to 100). The value of the injected charge is set by means of an external 16-bit DAC, therefore it ranges from 0 to 65 535 DACu (DAC unit). The code is converted in the equivalent energy value using the conversion factor of 1 DACu = 0.841 keV, whose value is later derived in Equation (1.14), therefore the range can be equivalently expressed as spanning from 0 to 55.11 MeV.

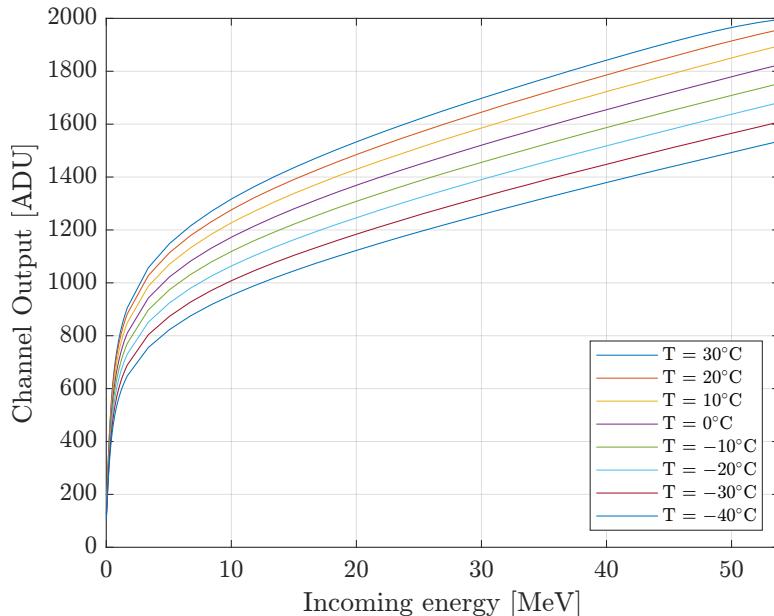


Figure 1.8: Mean input-output channel trans-characteristics with respect to temperature varying from -40°C to 30°C and automatically regulated **CSAVrefGM** voltage.

Evaluation of temperature effects on ASIC performance

Figure 1.8 shows the input-output trans-characteristic obtained as the mean of the 32 channels of the ASIC with respect to temperature ranging from -40°C to 30°C . In this case, the `CSAVrefGM` voltage has been left free to automatically adapt to the given temperature and has been measured using the test setup 1 described in Figure 1.1. The CSA REFERENCE REGULATION setting (`HRRR` bits) has been set to 0011. The first bit, `H`, is set to 0 when the ASIC is operated at -40°C and to 1 when operated at room temperature. The last three bits, `RRR`, allow to set the charge sensitive amplifier reference.

The `CSAVrefGM` values measured at each temperature are presented in Table 1.3. It comprises measurements taken with `HRRR` respectively set to 0011 and 0111 and the relative percentage variation between the two. It is of immediate comprehension that neither configuration is capable of reaching the desired 530 mV at -40°C . It is in fact necessary to set `RRR` to 111 in order to get the closest possible to the reference value.

Temperature [°C]	CSAVrefGM [mV]		Variation [%]
	<code>HRRR = 0011</code>	<code>HRRR = 0111</code>	
30	360.5	370.9	2.80
20	383.1	392.0	2.27
10	405.3	413.8	2.05
0	432.1	436.3	6.73
-10	450.5	458.4	1.72
-20	473.2	480.6	1.54
-30	495.1	504.3	1.82
-40	517.5	525.8	1.58

Table 1.3: `CSAVrefGM` voltage measured at temperatures varying from -40°C to 30°C with CSA REFERENCE REGULATION bits set to 0011 and 0111 respectively.

Figure 1.9 shows the mean input-output channel trans-characteristics calculated over the 32 channels of the ASIC given temperatures ranging from -40°C to 30°C . In this case, the `CSAVrefGM` has been set to a fixed value of 530 mV using the test setup 2 described in Figure 1.2. It is possible to notice that by fixing the voltage to the automatically regulated value at -40°C regardless of the temperature, the channel transfer function assumes an unwanted trend.

Input-output channel trans-characteristic

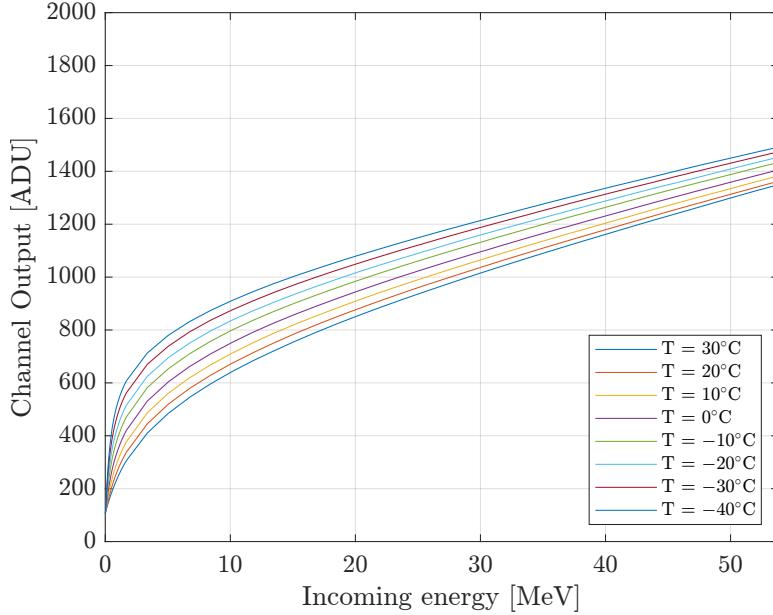


Figure 1.9: Mean input-output channel trans-characteristics given temperatures varying from -40°C to 30°C and `CSAVrefGM` voltage fixed to 530 mV.

As it can be seen from the charts, the channel input-output trans-characteristic is a non-linear function that can be described as an almost piecewise linear function whose sensitivity is determined by the dynamic compression feature of the CSA. Through this non-linearity the resolution of the signals changes as a function of the charge generated by the energy release of the incident particle in the detector: in a low energy range, the resolution of the signal must be high and, consequently, the charge signal must be amplified adequately and vice versa in the high energy range. This implies that in the first segment the transfer function has a high slope. In the high energy range, however, the required resolution is not so stringent, consequently the gain of the transfer function is less than that in the first section. The channel transfer function can therefore be divided into two regions, based on the incoming energy:

- *Low energy region*: Also known as X-ray detection region, it ranges from approximately 10 to 100 keV.
- *High energy region*: Also described as muon detection region, it spans an energy range comprised between 40 and 55 MeV.

In both X-ray and muon detection regions, the characteristic exhibits a linear behaviour and can be expressed as

$$y = p + g \cdot x \quad (1.5)$$

where

- **y** [ADU] (Analog Digital Unit) is the channel output.
- **p** [ADU] is the pedestal, which consists of a repeated sampling of the channel output without charge injected.
- **g** [ADU/keV] is the channel gain.
- **x** [keV] is the input energy.

The effect of temperature variation on the channel transfer function has been studied by evaluating gain and pedestal in both X-ray and muon detection regions. For each of the two parameters, a linear regression model has been defined in order to study the trend on both gain and pedestal with respect to temperature ranging from -40°C to 30°C , which has been demonstrated to have an almost perfect linear trend. For the gain analysis, the following linear regression model has been defined.

$$g = g_0 + g_1 \cdot (T - T_0) \quad (1.6)$$

The intercept g_0 is measured in ADU/keV, the slope g_1 in $\text{ADU keV}^{-1} ^{\circ}\text{C}^{-1}$ and the reference temperature has been set to $T_0 = 0^{\circ}\text{C}$. For the study of the gain in the high-energy region, g_0 is reported in ADU/MeV, while g_1 is expressed in $\text{ADU MeV}^{-1} ^{\circ}\text{C}^{-1}$. Similarly, the following linear regression model has been defined for pedestal analysis.

$$p = p_0 + p_1 \cdot (T - T_0) \quad (1.7)$$

The intercept p_0 is measured in ADU, the slope p_1 in $\text{ADU} / ^{\circ}\text{C}$ and the reference temperature has been set to $T_0 = 0^{\circ}\text{C}$.

Table 1.4 provides the linear regression model coefficients for both gain and pedestal obtained upon the mean channel input-output characteristics measured at temperatures ranging between -40°C and 30°C .

The channel peaking time has been set to $\tau_p = 0.98\text{ }\mu\text{s}$ (peaking time 4, TTT set to 100), with **CSAVrefGM** voltage automatically generated and **HRRR** set to 0011.

Table 1.5 presents the same linear regression models coefficients but in the case of fixed **CSAVrefGM** voltage, that has been set to 530 mV.

Input-output channel trans-characteristic

	Gain			Pedestal		
	g_0 [$\frac{\text{ADU}}{\text{keV}}$]	g_1 [$\frac{\text{ADU}}{\text{keV}^\circ\text{C}}$]	R^2	p_0 [ADU]	p_1 [$\frac{\text{ADU}}{\text{^\circ C}}$]	R^2
X-ray detection region (10÷100 keV)	1.25	0.006	0.997	182.32	0.651	0.985
Muon detection region (40÷55 MeV)	12.27	0.024	0.989	1738	6.778	0.999

Table 1.4: Gain and pedestal linear regression models coefficients obtained from measurements with automatically generated `CSAVrefGM` voltage and `HRRR` set to 0011.

	Gain			Pedestal		
	g_0 [$\frac{\text{ADU}}{\text{keV}}$]	g_1 [$\frac{\text{ADU}}{\text{keV}^\circ\text{C}}$]	R^2	p_0 [ADU]	p_1 [$\frac{\text{ADU}}{\text{^\circ C}}$]	R^2
X-ray detection region (10÷100 keV)	0.46	-0.012	0.992	128.66	-0.530	0.974
Muon detection region (40÷55 MeV)	12.61	0.033	0.997	1325.4	-2.406	0.988

Table 1.5: Gain and pedestal linear regression models coefficients obtained from measurements with `CSAVrefGM` voltage set at a fixed value of 530 mV.

Graphs presented below show the trend of gain and pedestal with respect to temperature in the low and high energy regions for the configurations where `CSAVrefGM` is automatically adjusted (with `HRRR` set to 0011) and set to 530 mV respectively. The measurements were carried out by varying the temperature from -40°C to 30°C in steps of 10°C , while the region between -40°C and -30°C was studied with steps of 2°C .

The effect of keeping the CSA regulation voltage fixed can be seen in Figure 1.10, which manifests itself in a decreasing gain trend at low energies. This can be explained by the fact that, when the `CSAVrefGM` voltage is fixed at 530 mV, it deviates considerably from the automatically adjusted nominal value at temperatures above -40°C , shown in Table 1.3, until it reaches a difference of approximately 170 mV at 30°C , the result of which is evident from the trend of the transfer function in Figure 1.9.

Figure 1.11 shows the gain trend in the high energy region under the same

Evaluation of temperature effects on ASIC performance

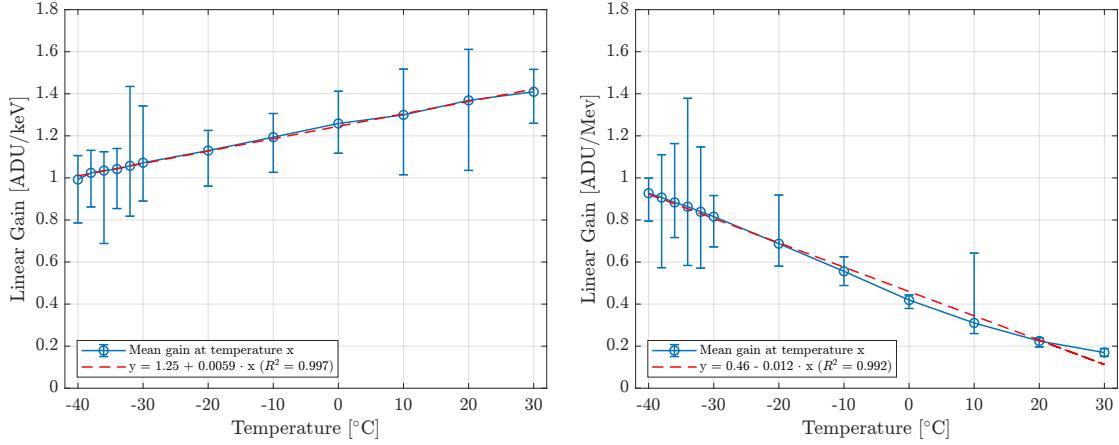


Figure 1.10: Low energy gain trend with respect to temperature from -40°C to 30°C for automatically regulated CSAVrefGM voltage (on the left) and fixed to 530 mV (on the right).

conditions, presenting the configuration with automatically regulated CSAVrefGM voltage on the left and fixed to 530 mV on the right.

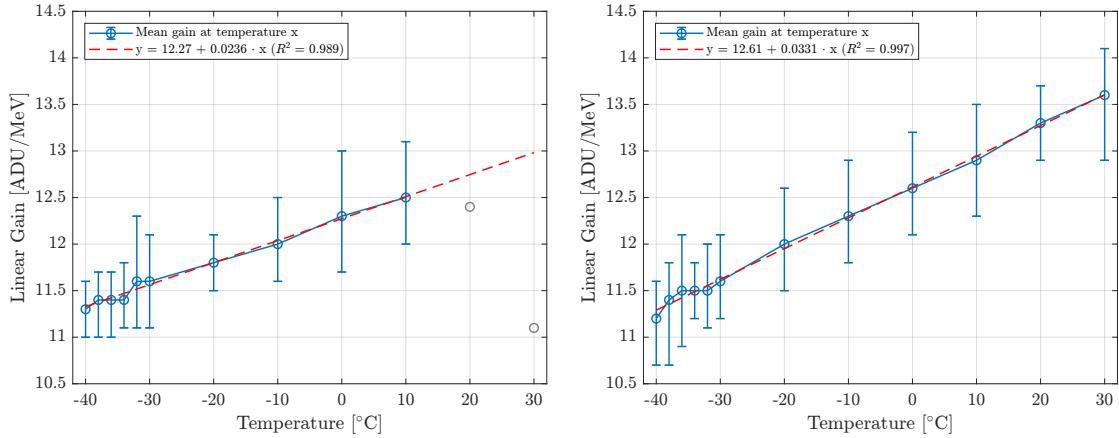


Figure 1.11: High energy gain trend with respect to temperature from -40°C to 30°C for automatically regulated CSAVrefGM voltage (on the left) and fixed to 530 mV (on the right). The linear gain is expressed in ADU/MeV.

It can be seen that, although g_0 assumes a value that is almost comparable between the two configurations, g_1 presents an increment of $\approx 28.7\%$ when CSAVrefGM is set to 530 mV, thus resulting in a higher increase in gain with respect to temperature. Figure 1.12 and Figure 1.13 present the trend of the pedestal as a function of temperature under the same conditions illustrated above.

Pedestal and gain measurements were used to study the variation in the position

Input-output channel trans-characteristic

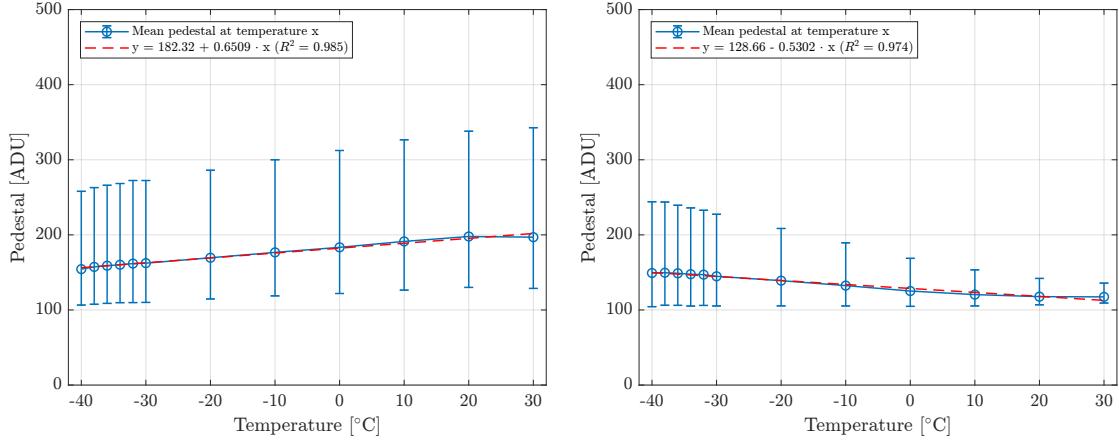


Figure 1.12: Low energy pedestal trend with respect to temperature from -40°C to 30°C for automatically regulated CSAVrefGM voltage (on the left) and fixed to 330 mV (on the right).

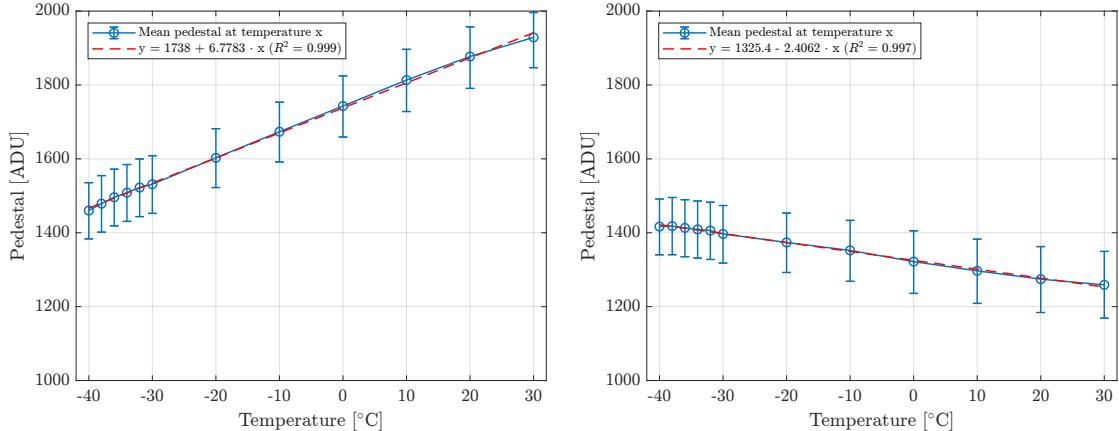


Figure 1.13: High energy pedestal trend with respect to temperature from -40°C to 30°C for automatically regulated CSAVrefGM voltage (on the left) and fixed to 330 mV (on the right).

of the transfer function kink as temperature changes. In particular, Figure 1.14 shows the interpolation curves of the transfer function in the low and high energy regions, previously referred to as *X-ray* and *muon* detection regions respectively. In particular, their intersection determines the point, expressed in MeV, at which the change of slope occurs in the channel's input-output characteristic, which, in the particular example case, refers to the measurement obtained at a temperature of -40°C . The two curves refer to the model shown in Equation (1.5) and the resolution of the system shown in Equation (1.8) allows the value of the kink at each temperature step to be determined as the intersection of the two straight lines

Evaluation of temperature effects on ASIC performance

that linearly approximate the transfer function in the high and the low energy region.

$$\begin{cases} y = p_{LE} + g_{LE} \cdot x \\ y = p_{HE} + g_{HE} \cdot x \end{cases} \quad (1.8)$$

In particular, the subscript *LE* refers to the model that describes the trend of the transfer function in the *Low Energy* region, while the subscript *HE* describes its trend in the *High Energy* region.

Solving the system reported in Equation (1.8) allows the kink value expressed in MeV to be obtained:

$$x = \frac{p_{LE} - p_{HE}}{g_{HE} - g_{LE}} \quad (1.9)$$

From the graph shown in Figure 1.15 it is possible to appreciate the kink trend of the channel transfer function as the temperature varies, for temperature values between -40°C and 30°C . In particular, the kink trend is shown in red when the `CSAVrefGM` voltage is fixed at 530 mV, while it is shown in blue when this voltage is automatically varied on the basis of temperature.

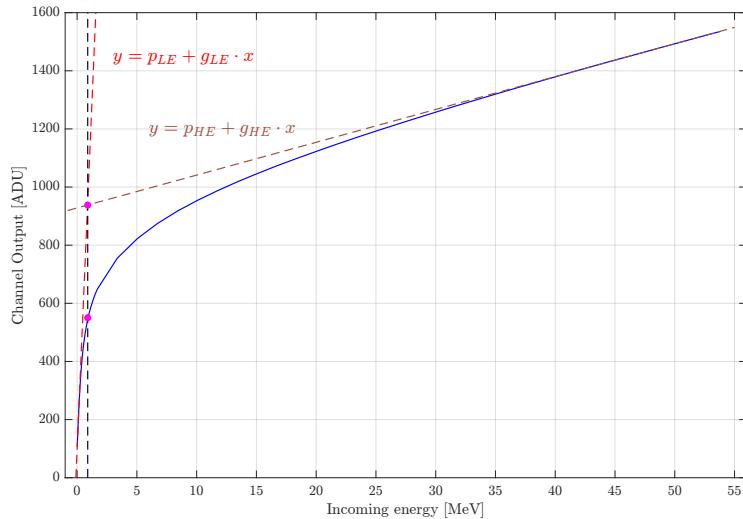


Figure 1.14: Method for determining the kink position: the linear models used to interpolate the transfer function in the low and high energy region are also reported.

It is easy to see that in the case where `CSAVrefGM` varies dynamically on the basis of temperature, the kink remains at an almost constant value, varying only 6.95 % between -40°C and 30°C . Conversely, in the case where this voltage is set at 530 mV regardless of temperature, the kink undergoes a 429 % variation between the two temperature extremes.

Global threshold voltage

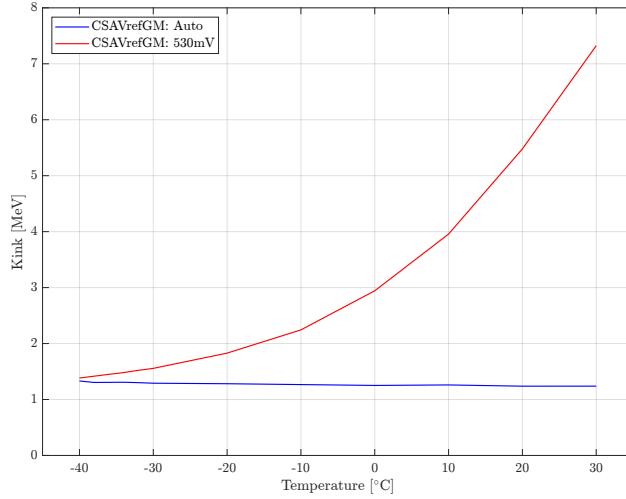


Figure 1.15: Kink behaviour as a function of temperature when `CSAVrefGM` is either fixed at 530 mV (in red) or automatically varied as a function of temperature (in blue).

1.4 Global threshold voltage

This Section illustrates the measurements performed on the 8-bit DAC that provides two voltages V_{tp} and V_{tn} used by the threshold generator (described in Appendix A.3) to generate the Signal-Over-Threshold (SOT) comparator voltage. In particular, the difference between the two voltages $\Delta V_t = V_{tp} - V_{tn}$ is the meaningful quantity and will be referred to as *global threshold voltage*: the higher ΔV_t , the higher the threshold of the SOT comparator. It has to be noted that the voltage V_{tp} remains constant by varying the DAC codes, whereas the voltage V_{tn} can vary from 0 V to $(V_{tp} + V_s)$, where V_s is a voltage margin which permits to obtain negative ΔV_t .

During design of this circuit, the DAC voltage Least Significant Bit (LSB) has been chosen to be [4]

$$V_{tn, \text{ LSB}} = 1.2 \text{ mV} \quad (1.10)$$

Since the DAC bits are 8, the maximum value of the DAC codes is $2^8 - 1$. This forces the maximum value of V_{tn} to be

$$V_{tn, \text{ max}} = V_{tn, \text{ lsb}} \cdot 255 = 306 \text{ mV} \quad (1.11)$$

Figure 1.16 shows the ΔV_t voltage with respect to DAC codes varying from 0 to 255 measured at temperatures comprised between -40°C and 30°C on channel 31.

Evaluation of temperature effects on ASIC performance

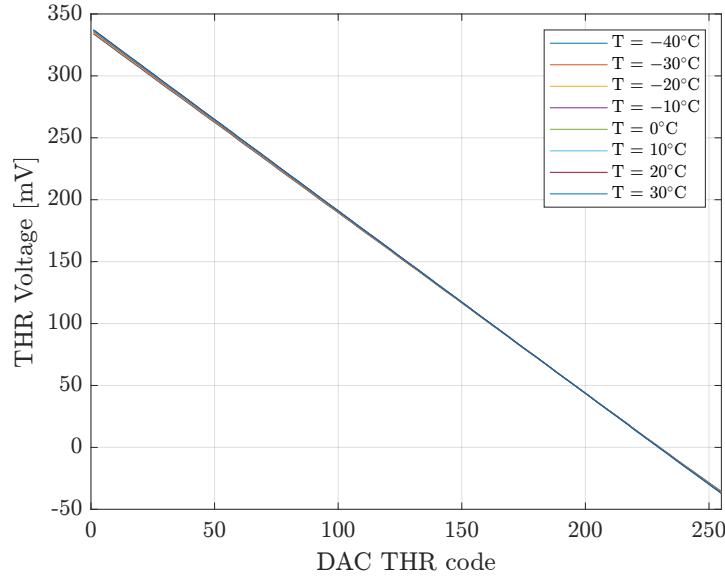


Figure 1.16: ΔV_t voltage with respect to DAC code varying temperature between -40°C and 30°C .

Table 1.6 shows the maximum value assumed by V_{tn} and the corresponding DAC voltage LSB measured at each temperature.

Temperature [$^{\circ}\text{C}$]	$V_{tn, \text{max}}$ [mV]	$V_{tn, \text{lsb}}$ [mV]
-40	333.87	1.45
-30	334.32	1.45
-20	335.35	1.46
-10	335.91	1.46
0	336.46	1.46
10	336.78	1.46
20	337.15	1.47
30	337.26	1.47

Table 1.6: $V_{tn, \text{max}}$ and $V_{tn, \text{lsb}}$ measured at temperatures ranging from -40°C to 30°C .

Threshold voltage measurements have been evaluated by interpolating experimental results with the linear regression model shown in Equation (1.12). Coefficient a is expressed in mV and coefficient b in mV/ $^{\circ}\text{C}$. The Root Mean Square Error (RMSE) is reported for each temperature.

$$y = a + b \cdot x \quad (1.12)$$

Global threshold voltage

Table 1.7 offers a list of the model coefficients calculated over the threshold voltage measurements taken at temperatures spanning from -40°C to 30°C along with the model RMSE.

Temperature [°C]	a [mV]	b [mV/°C]	RMSE
-40	335.12	-1.46	0.15
-30	335.67	-1.46	0.14
-20	336.58	-1.46	0.13
-10	337.15	-1.47	0.13
0	337.79	-1.47	0.11
10	338.17	-1.47	0.10
20	338.51	-1.47	0.10
30	338.64	-1.48	0.09

Table 1.7: Linear regression model coefficients evaluated over global threshold measurements taken at temperatures varying from -40°C to 30°C .

Figure 1.17 shows the global threshold voltage trend with respect to the DAC code for temperatures ranging from -40°C to -30°C and 2°C increments. As done previously, the global threshold voltage measurements have been evaluated by interpolating the same linear regression model described in Equation (1.12). The model coefficients are proposed in Table 1.8. It is immediate to see that in the -40°C to -30°C temperature range, the slope, b , of the DAC trans-characteristic remains constant with respect to temperature, while the intercept, a , slightly increases with an increase of temperature.

Temperature [°C]	a [mV]	b [mV/°C]	RMSE
-40	335.12	-1.46	0.15
-38	335.27	-1.46	0.14
-36	335.50	-1.46	0.14
-34	335.62	-1.46	0.14
-32	335.74	-1.46	0.13
-30	335.67	-1.46	0.13

Table 1.8: Linear regression model coefficients evaluated over global threshold measurements taken at temperatures varying from -40°C to -30°C .

Evaluation of temperature effects on ASIC performance

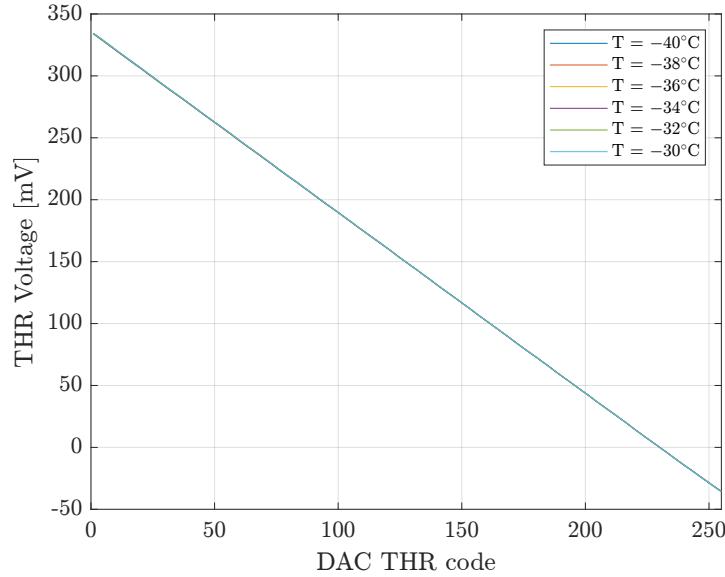


Figure 1.17: ΔV_t voltage with respect to DAC code varying temperature between -40°C and -30°C .

Figure 1.18 presents the trend of the global threshold voltage with respect to the DAC code by varying the 3 bits fine threshold code on channel 31 at a constant temperature of -40°C . As it can be appreciated in Table 1.9, the change in fine threshold code keeps the gradient unaltered while operating a shift in the DAC transfer function.

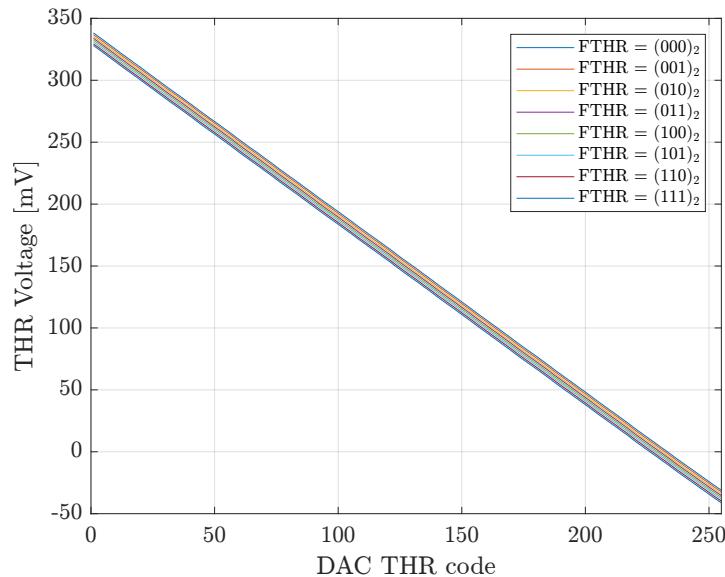


Figure 1.18: ΔV_t voltage with respect to DAC code and varying fine threshold (FTHR) code at -40°C .

Equivalent Noise Charge (ENC) at -40°C

FTHR	a [mV]	b [mV/bit]	RMSE
0 (000) ₂	339.49	-1.46	0.155
1 (001) ₂	338.10	-1.46	0.152
2 (010) ₂	336.52	-1.46	0.155
3 (011) ₂	335.12	-1.46	0.154
4 (100) ₂	333.71	-1.46	0.160
5 (101) ₂	332.22	-1.46	0.156
6 (110) ₂	330.64	-1.46	0.152
7 (111) ₂	329.29	-1.46	0.154

Table 1.9: Linear regression model coefficients evaluated over global threshold measurements taken by spanning the 8-bit DAC code and by varying the fine threshold (FTHR) code.

1.5 Equivalent Noise Charge (ENC) at -40°C

The measurement of the Equivalent Noise Charge (ENC) is of fundamental importance to evaluate the performance of the channel in terms of resolution and, therefore, of minimum detectable energy. The ENC represents the electronic noise generated by the front-end channel reported in the form of equivalent noise charge at the channel input. In the case of GAPS, the main requirement for the channel comes from the resolution, that must be less than 4 keV: this is equivalent to saying that the ENC (FWHM) for each channel must be less than 4 keV in order to consider the channel suitable for the experiment.

ENC is calculated by dividing the standard deviation of the noise, obtained from the pedestal measurement in ADU, by the low energy gain of the channel transfer function, extracted from the input-output characteristic measurements and expressed in (ADU)/(DAC injection units):

$$ENC = \frac{\sigma_{ped} \cdot 2.35}{\mu_{ch}} \cdot 0.841 \frac{\text{keV}}{\text{DAC_inju}} \quad (1.13)$$

where σ_{ped} is the channel noise standard deviation and μ_{ch} is the channel low energy gain. The $0.841 \frac{\text{keV}}{\text{DAC_inju}}$ value represents a conversion factor for obtaining the keV measurements and it is calculated as follows:

$$C_{inj} \cdot \frac{V_{LSB, CAL}}{0.044 \frac{\text{fC}}{\text{keV}}} = 1.184 \text{ pF} \cdot \frac{31.25 \frac{\mu\text{V}}{\text{DAC_inju}}}{0.044 \frac{\text{fC}}{\text{keV}}} = 0.841 \frac{\text{keV}}{\text{DAC_inju}} \quad (1.14)$$

where C_{inj} is the injection capacitance, $V_{LSB, CAL}$ is the LSB value of the 16-bit calibration DAC and $0.044 \frac{\text{fC}}{\text{keV}}$ is the conversion factor between fC and keV.

Lastly, 2.35 is the *Fano factor*. This factor is taken into account since the ENC measurement must be expressed at Full Width at Half Maximum (FWHM). One does not simply want to consider the standard deviation of the pedestal, but the width of its Gaussian distribution at half of its maximum height. To obtain this measurement, the standard deviation of the pedestal must be multiplied by the Fano factor.

Figure 1.19 represents the ENC FWHM with and without 40 pF detector capacitors, that have been soldered on the test board and connected to the first 8 (0 to 7) channels of the ASIC in order to emulate the Si(Li) detectors capacitance. It is clear to see from the graph on the right that channels with the capacitors installed experience an increase in ENC, as it should be expected [5].

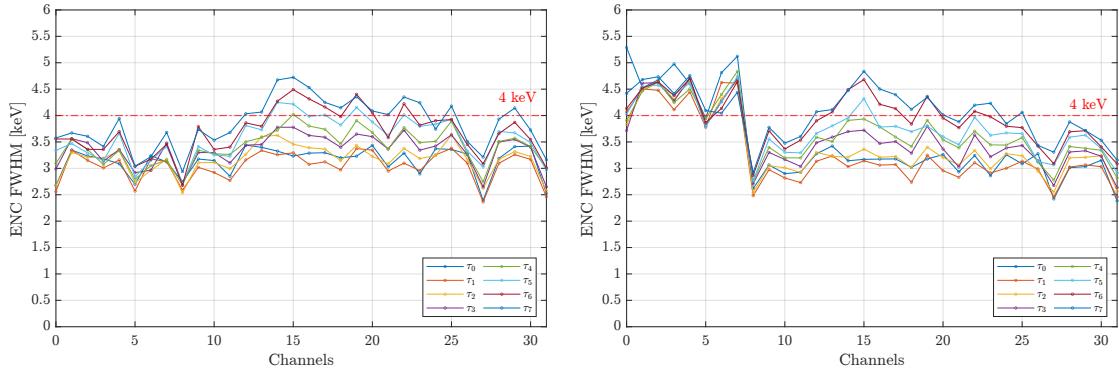


Figure 1.19: Graphs showing ENC FWHM without detector capacitors (on the left) and with detector capacitors (on the right) at -40°C without removal of external interference.

Since the ENC is a measurement derived from the pedestal, it is also subject to interference phenomena arising from electromagnetic noise present in the environment where the tests are performed. In this regard, a method was devised to remove interference contributions not directly attributable to pure electronic noise and the results of the analysis are presented in the following Sections.

1.5.1 Sampled pedestal processing

The pedestal is simultaneously dependent on both the channel on which the measurement is made, y , and the specific sample taken from the measurement, x , as the sum of 3 components. The first component, $p_0[y]$, represents the ideal pedestal

Equivalent Noise Charge (ENC) at -40°C

free of external noise and interference, which therefore only depends on the specific channel on which the measurement is made. The second component, $n[x, y]$, represents the stochastic noise and the third one represents the deterministic interference component, $d[x]$. In this first analysis, the deterministic component, $d[x]$, is assumed to be common to all channels and therefore it only depends on the specific sample. For this reason, the pedestal can be written as

$$p[x, y] = p_0[y] + n[x, y] + d[x] \quad (1.15)$$

where

- $x = 1, 2, \dots, 1000$ represents the sample number.
- $y = 0, 1, \dots, 31$ represents the channel number.
- p_0 is the ideal pedestal without noise and external interference and depends on y only.
- n is the stochastic noise component of the pedestal.
- d is the deterministic external interference, at first we assume that it is common to all channels and it depends on x only.

1.5.2 Evaluation of deterministic interference

For every sample x we evaluate the mean value p_m of the 32 channels sampled pedestal

$$\begin{aligned} p_m[x] &= \frac{1}{32} \sum_{y=0}^{31} p[x, y] \\ &= \frac{1}{32} \sum_{y=0}^{31} (p_0[y] + n[x, y] + d[x]) \\ &= p_{m,0} + d[x] \end{aligned} \quad (1.16)$$

where

$$\frac{1}{32} \sum_{y=0}^{31} p_0[y] = p_{m,0} \quad (1.17)$$

it is due to the fact that the ideal pedestal depends entirely on the specific channel on which it is measured, so averaging the ideal pedestal over all 32 channels provides

a channel-independent global average, representing the common contribution of all channels. On the other hand, it is possible to say that

$$\frac{1}{32} \sum_{y=0}^{31} n[x, y] \simeq 0 \quad (1.18)$$

and it comes from the stochastic nature of the noise, which has a constant power spectral density with respect to frequencies. This means that each frequency has the same contribution to the overall noise, thus resulting in an approximately zero average.

Assuming in this first discussion that the interference contribution is common to all channels, it is easy to state that averaging the external interference $d[x]$ over the 32 channels returns the interference itself, the latter acting with the same proportion on all channels.

$$\frac{1}{32} \sum_{y=0}^{31} d[x] = d[x] \quad (1.19)$$

1.5.3 Pedestal without external interference

For every x the evaluated interference is subtracted from the samples pedestal:

$$\begin{aligned} p'[x, y] &= p[x, y] - p_m[x] \\ &= p_0[y] + n[x, y] + \cancel{d[x]} - p_{m_0} - \cancel{d[x]} \\ &= p_0[y] - p_{m_0} + n[x, y] \end{aligned} \quad (1.20)$$

The standard deviation with respect to x of this new pedestal depends on the stochastic noise n only.

With this first method, it is therefore possible to remove the constant deterministic interference contribution, assuming to a first approximation that the disturbance acts uniformly on all 32 channels. Figure 1.20 shows the result of the application of this first algorithm on the data shown in figure Figure 1.19. It is possible to appreciate the reduction of ENC, which is free of the deterministic interference component.

1.5.4 Weighted external interference

The method illustrated in this Section interprets the contribution of external deterministic interference as channel-specific, making the disturbance channel-dependent

Equivalent Noise Charge (ENC) at -40°C

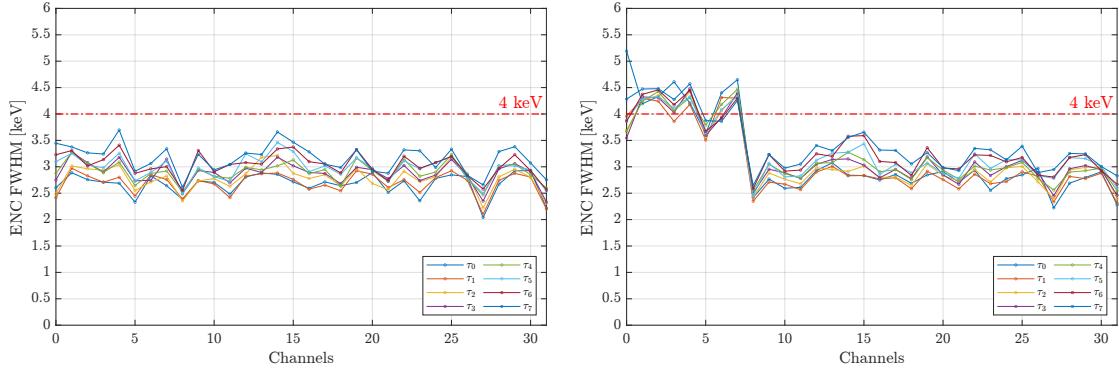


Figure 1.20: Graphs showing ENC FWHM without detector capacitors (on the left) and with detector capacitors (on the right) at -40°C without external interference.

by means of a weighting factor that determines its impact, more or less marked, on the specific channel. If we assume that the same external interference $d[x]$ affects each channel with a different weight, Equation (1.15) changes as follows

$$p[x, y] = p_0[y] + n[x, y] + k[y] \cdot d[x] \quad (1.21)$$

It can be seen that the pedestal is still represented as a sum of 3 contributions, but in this case the deterministic component is weighted by means of a weight factor that determines how much the deterministic disturbance impacts on the specific channel. It goes without saying that for this method to be effective, the sample size must be sufficiently high in order to guarantee sufficiently comprehensive statistics for each individual channel. Equation (1.16) becomes

$$p_m[x] = p_{m_0} + k_m \cdot d[x] \quad (1.22)$$

where k_m is the average over the 32 channels of the weight factor and can be represented as a constant factor common to all channels.

$$\frac{1}{32} \sum_{y=0}^{31} k[y] \cdot d[x] = k_m \cdot d[x] \quad (1.23)$$

From Equation (1.21) we derive that

$$d[x] = \frac{1}{k[y]} (p[x, y] - p_0[y] - n[x, y]) \quad (1.24)$$

and therefore by replacing $d[x]$ in Equation (1.22) we obtain

$$\begin{aligned}
 p_m[x] &= p_{m_0} + \frac{k_m}{k[y]}(p[x, y] - p_0[y] - n[x, y]) \\
 &= p_{m_0} - \frac{k_m}{k[y]}p_0[y] + \frac{k_m}{k[y]}(p[x, y] - n[x, y])
 \end{aligned} \tag{1.25}$$

By plotting $p_m[x]$ as a function of $p[x, y]$ for a given channel and by interpolating it via a linear function, the slope m of the interpolating function provides the ratio between the mean channel weight k_m and the weight $k[y]$ of channel y

$$m = \frac{k_m}{k[y]} \tag{1.26}$$

1.5.5 Pedestal without weighed external interference

As done previously, it is now necessary to remove the contribution of external deterministic interference. For this reason, for a given channel y and for every sample x we evaluate

$$\begin{aligned}
 p'[x, y] &= p[x, y] - \frac{1}{m}p_m[x] \\
 &= p_0[y] + n[x, y] + k[y] \cdot d[x] - \frac{k[y]}{k_m}(p_{m_0} + k_m \cdot d[x]) \\
 &= p_0[y] + n[x, y] - \frac{k[y]}{k_m}p_{m_0} + k[y] \cdot d[x] - \frac{k[y]}{k_m} \cdot k[m] \cdot d[x] \\
 &= p_0[y] + n[x, y] - \frac{k[y]}{k_m}p_{m_0} + \cancel{k[y] \cdot d[x]} - \cancel{k[y] \cdot d[x]} \\
 &= p_0[y] - \frac{k[y]}{k_m} \cdot p_{m_0} + n[x, y]
 \end{aligned} \tag{1.27}$$

This results in the removal of the deterministic interference component from the Equation of the pedestal of each channel, reducing it entirely to the ideal contribution to which the purely stochastic component is added. Therefore, the distribution of $p'[x, y]$ depends only on the stochastic noise $n[x, y]$ for a given channel y .

The result of the application of the latter method can be seen in Figure 1.21. It should be noted that, due to the limited sample size that characterises the dataset acquired during the measurements, this method is unable to provide an effective removal of the disturbance component, even resulting in a higher ENC contribution with respect to the initial one.

Equivalent Noise Charge (ENC) at -40°C

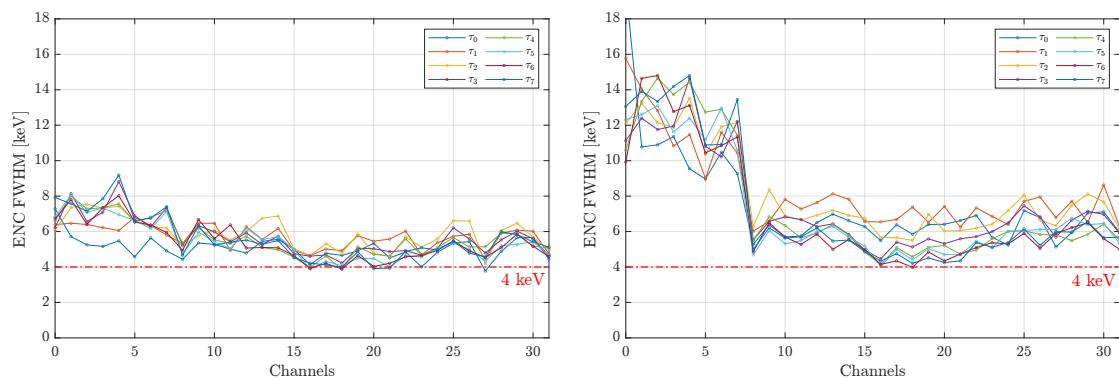


Figure 1.21: Graphs showing ENC FWHM without detector capacitors (on the left) and with detector capacitors (on the right) at -40°C without weighed external interference.

Chapter 2

Si(Li) tracker flight components validation

This Chapter provides a detailed description of the test setup and the test procedures followed to validate the flight items that will be used for the final assembly of the Si(Li) tracker of the GAPS detector. For each of the flight items, a report has been produced in order to detail all the most important parameters with their measured values. Every component has also been uniquely numbered following a specific alphanumeric pattern that can briefly sum up its most relevant characteristics, allowing it to be immediately recognised during the assembly process. This Chapter also provides a deep explanation of the results obtained during the testing activity on all the flight components.

Tests were conducted in order to verify the integrity and proper functioning of the following items:

1. Front-End Board (FEB).
2. Dummy-1 front-end board.
3. Flex-rigid board.
4. Connector for termination.
5. Front-end board shield.

The following Sections are structured as follows: First, the test setup used to verify the correct functioning of the component will be described and a description of the tests performed will be provided, then the results of the tests performed will be reported.

Si(Li) tracker flight components validation

Figure 2.1 shows the flowchart associated with the testing and validation process of all flight items.

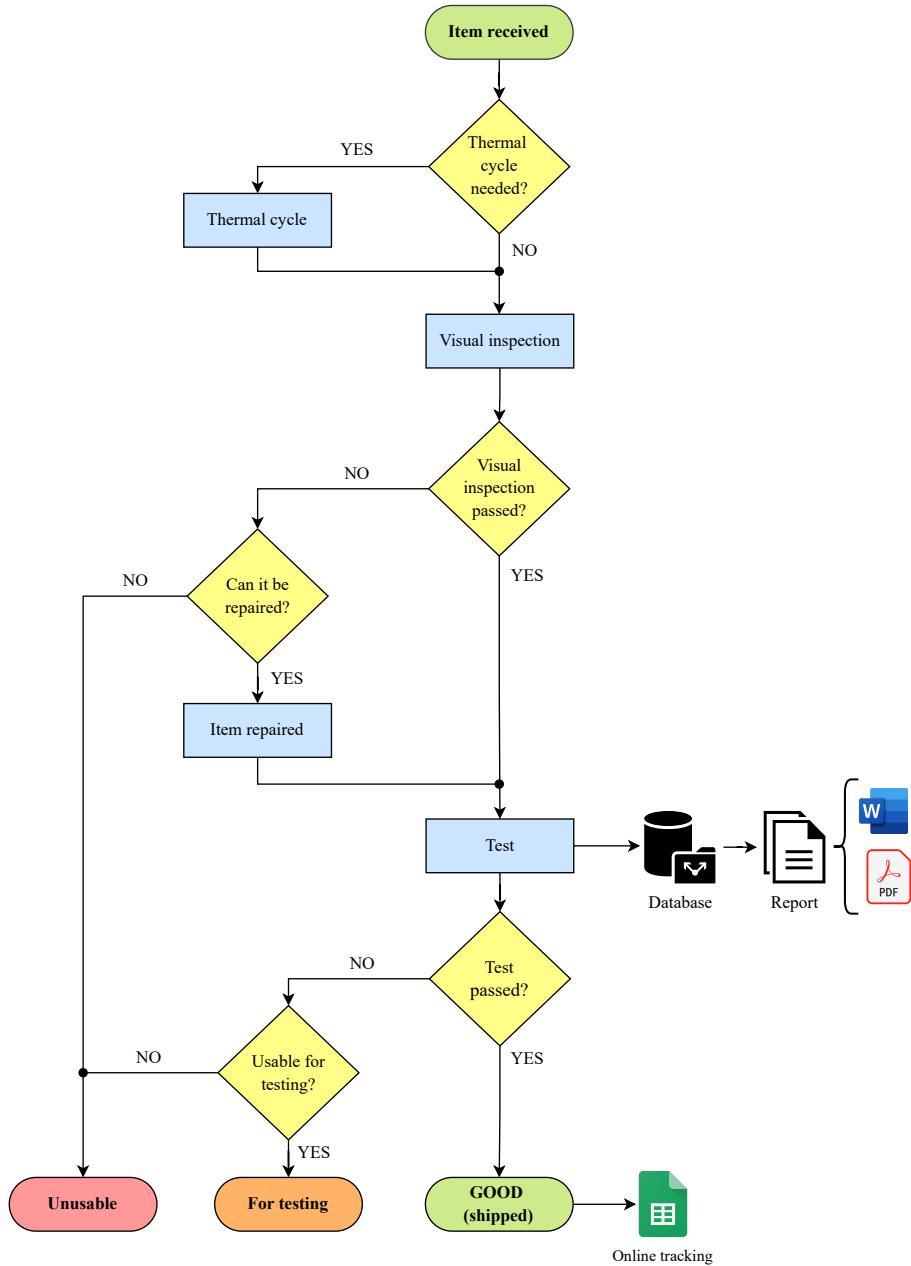


Figure 2.1: Flight item validation procedure flowchart.

At the end of the test procedure, test results are saved in a database and an item report is generated. Depending on the outcome of the tests performed, the item is classified as:

- **GOOD**, meaning it passed all tests and can be used for tracker assembly.

Front-End Board (FEB)

- **USABLE** for testing activity only, if the component had a defect that was repaired.
- **UNUSABLE**, in case the component had a defect that could not be repaired.

The items classified as **GOOD** have been shipped to *Columbia University* to be integrated into the experiment assembly process.

2.1 Front-End Board (FEB)

The Front-End Board (FEB) that houses the SLIDER32 ASIC is shown in Figure 2.2. The board was designed in a cross-like shape to make room for the four Si(Li) detectors which will be wire-bonded to the ASIC through the smooth vertical tracks running in the central section of the FEB.

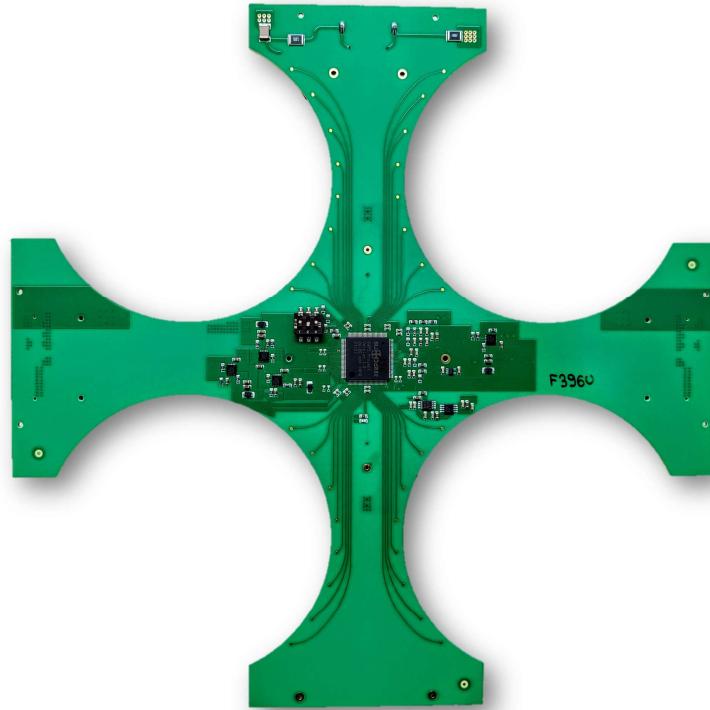


Figure 2.2: SLIDER32 front-end board No. F396U (US production).

Each FEB houses the components necessary for the operation of the ASIC and Si(Li) sensors, including the power supplies, divided into High Voltage Power Supply (HVPS) required for the four detectors, and Low Voltage Power Supply (LVPS)

necessary for the polarisation of the ASIC and its internal components. Each FEB is also equipped with a current reference for the Charge Sensitive Amplifier (CSA) input transistor, pull-up and pull-down resistors used in the transmission of the control signals, a 3-bit switch to set the address of the FEB, a 16-bit DAC for calibration and a temperature sensor. Within the tracker of the GAPS experiment, the FEBs will be connected to each other via an ERNI connector and a flex-rigid board, later described in Section 2.3. Each FEB is equipped with a male (model 254877) and female (model 354178) ERNI high-speed micro connectors, one used to connect the front-end board to the previous one and the other used to connect it to the following FEB.

The test of the front-end boards has been performed at ambient temperature and was aimed at verifying the proper functioning of the board and at looking for damages to the board or improperly soldered components, including the aforementioned ERNI connectors. The test has been performed in a twofold way:

- By measuring the DC operating point of the ASIC with a Fluke 79 III digital multimeter and a Keysight N6705C DC Power analyser (with N6762A and N6733B modules installed);
- By running a purposely developed automated validation test controlled by a terasIC OpenVino Toolkit based on an ALTERA Cyclone V Field Programmable Gate Array (FPGA) board. This procedure performs several types of tests, which are summarised in the following list:
 1. Noise (ENC).
 2. Pedestal.
 3. Self trigger.
 4. Threshold scan.
 5. Channel input-output characteristic.
 6. Waveform scan.

A detailed representation of the setup used for the tests is reported in Figure 2.3 and in Figure 2.4. At first, the setup depicted in Figure 2.3 has been used. After having realised that with this configuration the proper soldering of the ERNI output connector could not be verified, the setup has been improved by including a second front-end board connected in series with the first one via a flex-rigid board as shown in Figure 2.4. This allowed to implement a communication test between the

Front-End Board (FEB)

FEB under test and the FEB in series, thus verifying the correct functioning of the ERNI connector lodging the flex-rigid board connecting one FEB and the following. Specifically, the second version of the setup used is comprised of the following items:

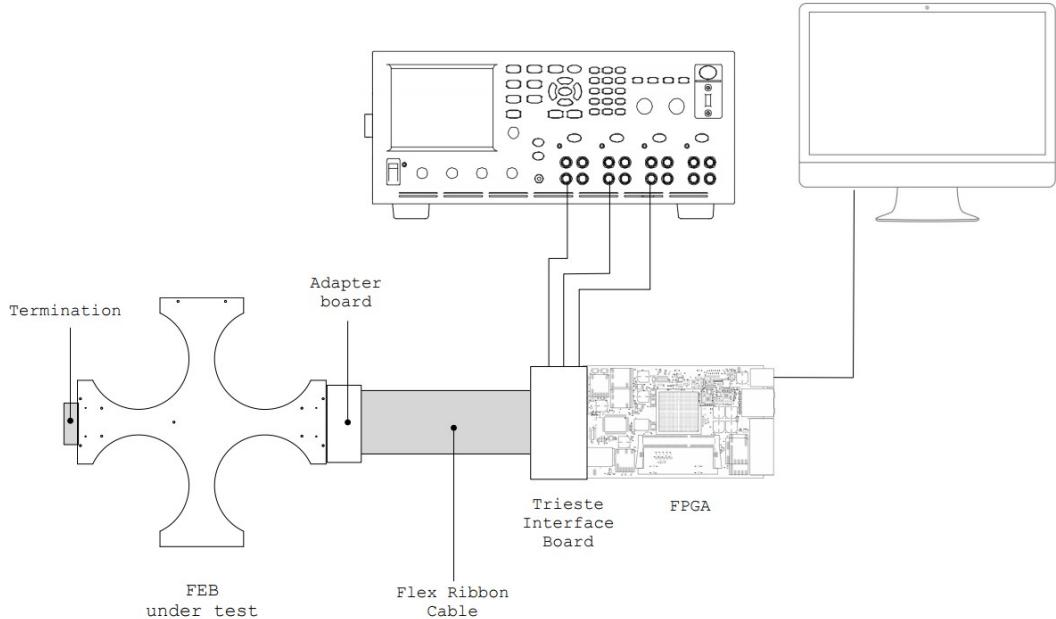


Figure 2.3: Depiction of the setup adopted for the tests on the first set of FEBs.

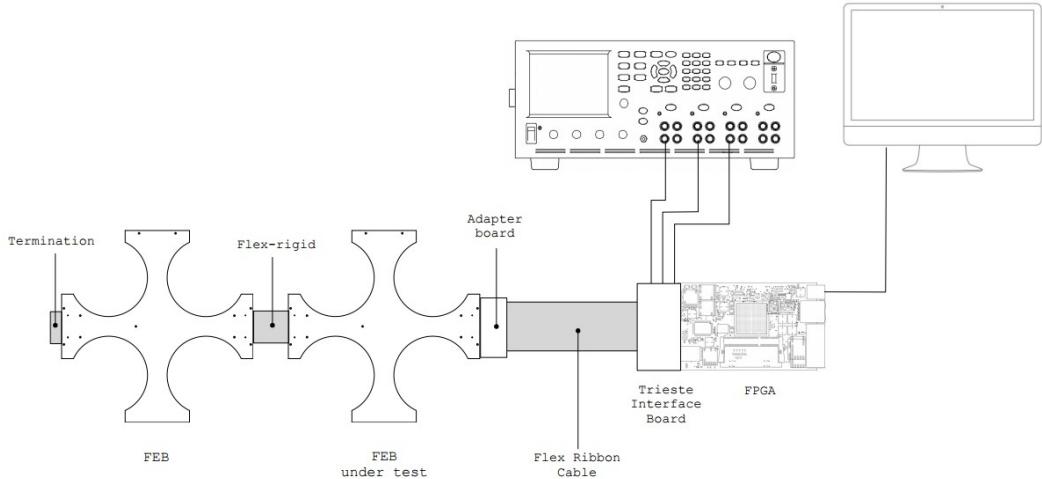


Figure 2.4: Depiction of the improved setup adopted for the tests of the FEBs.

- Two front-end boards, each of which has a SLIDER32 ASIC onboard, as described in Appendix A.3.

Si(Li) tracker flight components validation

- A flex-rigid board, later described in Section 2.3, connecting the two FEBs.
- A Keysight N6705C DC Power analyser providing both analog and digital supply voltages to the FEB, with the same configuration as the one already discussed in Section 1.1.
- A flex ribbon cable connecting the interface board to the main test board.
- An adapter board connecting the FEB through its female ERNI connector (model 354178) to the flex ribbon cable.
- An ALTERA Cyclone V Field Programmable Gate Array (FPGA) programmed using Verilog, an Hardware Description Language (HDL) that allows to describe digital electronic systems. The FPGA sends Serial Peripheral Interface (SPI) commands to the FEB according to those expected by the ASIC digital back-end, listed in Table 2.1, that are propagated through all the connected FEBs by means of the flex-rigid boards.
- An interface board specifically designed to route the power supplies and the signals through the flex ribbon cable to the front-end board under test.
- A PC running a Python-based testing program called **GAPS_ModuleTester**, currently in its 4th version, connected to the FPGA via two Universal Serial Bus (USB) cables. This software has been specifically developed to perform a series of tests on the SLIDER32 ASIC and it is later described in Section 2.1.

In order for the FPGA to be programmed, the software Intel Quartus Prime is used to upload the firmware onto the FPGA. After that, the **GAPS_ModuleTester** Python program is run so as to perform a full automated test of the FEB in all its functionalities. This software allows to set global variables related to the SPI and the ADC clock frequencies, expressed in MHz, the time limit for the self-trigger mode and the events delay generated by the FPGA, expressed in FPGA clock. The program offers three main interfaces, shown in Figure 2.5.

The first interface, called *ASIC configuration*, is dedicated to the configuration of the ASIC, namely its address, registers and configuration bits, specifically:

1. OPERATING MODE (**I**SA bit);
2. GLOBAL BIAS REGULATION (**T**BBB bits);
3. CSA REFERENCE REGULATION (**H**RRR bits, where bit H is set to 1 at ambient temperature and 0 at -40°C);

Front-End Board (FEB)

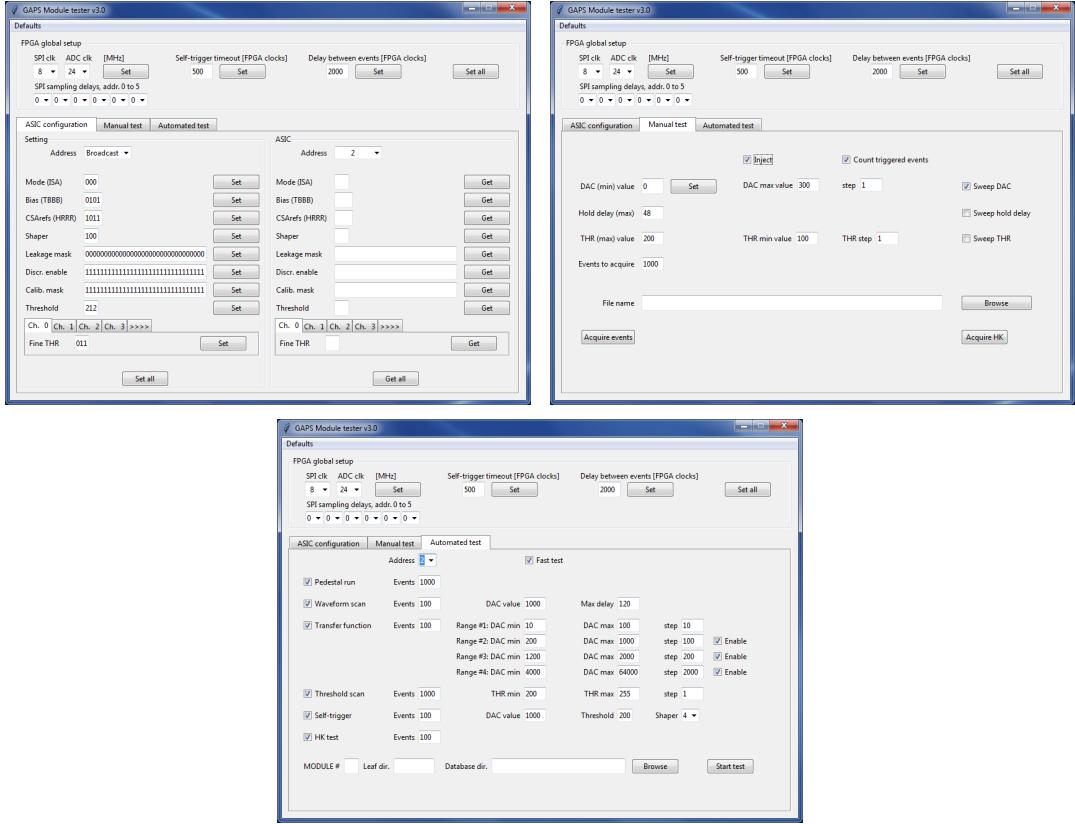


Figure 2.5: GAPS_ModuleTester main interfaces (clockwise from top-left): ASIC configuration, Manual Test, Automated Test.

4. SHAPER TIME CONSTANT (TTT bit);
5. DISCRIMINATOR ENABLE MASK (32 bit mask for channel activation);
6. LEAKAGE CURRENT MASK (for leakage current measurements);
7. CALIBRATION MASK (for calibration purposes).

Through this interface it is also possible to set the global threshold (DISCRIMINATOR THRESHOLD, 8 bit) and the fine threshold for each channel (FINE THRESHOLD, 3 bit). A detailed description of the aforementioned configuration bits can be found in Table 2.1 that presents the SPI commands accepted by the digital section of the ASIC.

The *Manual test* interface allows to configure all parameters in order to perform a manual test, like the 16-bit DAC values range for injection (expressed in DAC units), the time interval between injections (expressed in FPGA clocks, where one FPGA clock is equivalent to ≈ 20.83 ns, since the FPGA operates at a frequency of

Si(Li) tracker flight components validation

48 MHz) and the number of events to acquire. It is also necessary to set the output folder path which will contain the configuration parameters and the data generated by the test itself.

Command name	Command code	Input data	Output data
READ EVENT DATA	00000xxx	-	Event data packet
READ SEU FLAGS/TEMPERATURE SENSOR	00001xxx	-	SEU & Temperature word
READ OPERATING MODE	00010xxx	-	00000ISA
READ SHAPER TIME CONSTANT	00011xxx	-	00000TTT
READ CSA REFERENCE REGULATION	00100xxx	-	0000HRRR
READ GLOBAL BIAS REGULATION	00101xxx	-	0000TBAA
READ LEAKAGE CURRENT MASK	00111xxx	-	32 bit word
READ DISCRIMINATOR ENABLE MASK	01000xxx	-	32 bit word
READ CALIBRATION MASK	01001xxx	-	32 bit word
READ DISCRIMINATOR THRESHOLD	01010xxx	-	DDDDDDDD
READ FINE THRESHOLD ADJ. CH. NNNNN	011NNNNN	-	00000FFF
WRITE OPERATING MODE	10010ISA	-	-
WRITE SHAPER TIME CONSTANT	10011TTT	-	-
WRITE CSA REFERENCE REGULATION	v10100xxx	0000HRRR	-
WRITE GLOBAL BIAS REGULATION	10101xxx	0000TBAA	-
SET CALIBRATION DAC VOLTAGE	10110xxx	16 bit word	-
WRITE LEAKAGE CURRENT MASK	10111xxx	32 bit word	-
WRITE DISCRIMINATOR ENABLE MASK	v11000xxx	32 bit word	-
WRITE CALIBRATION MASK	11001xxx	32 bit word	-
WRITE DISCRIMINATOR THRESHOLD	11010xxx	DDDDDDDD	-
WRITE FINE THRESHOLD ADJ. CH. NNNNN	111NNNNN	00000FFF	-

Table 2.1: SPI commands and configuration bits.

The last section concerns the *Automated test* that has been used in order to perform the validation of the front-end boards. The automated test carried out on each FEB generates a folder containing the raw data acquired from the board, in the form of .dat files, and it has the following structure.

```

MODULE_000_fast/
  1/
  data/
    ConfigurationTest.dat
    HK_Leakage_chX.dat
    Pedestal_tauY.dat
    SelfTrigger_chX.dat
    ThresholdScan_fthrZ_tauY.dat
    TransferFunction_fast_tauY.dat
    WaveformScan_fast_tauY.dat

```

Front-End Board (FEB)

where X represents the channel identifier number that spans from 0 to 31, while Y represents the peaking time, that goes from 0 to 7. Specifically, the content of each of the files is defined as follows.

1. `ConfigurationTest.dat`: Basic communication and configuration tests.
2. `HK_Leakage_chX.dat`: Leakage current measurement (to be done with detectors).
3. `Pedestal_tauY.dat`: Pedestal test, in which the baseline variations due to electronic noise are measured. This test evaluates the electronic noise within the channel, measuring its output without injecting any charge. The output signal is therefore purely attributable to noise.
4. `SelfTrigger_chX.dat`: Self-trigger measurement, which reports the output of the ASIC channel (in ADU) obtained with a fixed DAC injection code and using the automatic peak detection feature of the Zero Crossing circuit, described in Appendix A.3.5.
5. `ThresholdScan_fthrZ_tauY.dat`: Threshold measurement, which reports the number of comparator hits, obtained by varying the global threshold word over its range and injecting 1000 times with a fixed DAC code at each step.
6. `TransferFunction_fast_tauY.dat`: Transfer function measurement, which lists the channel output ADC code obtained by sweeping the calibration DAC code over its range.
7. `WaveformScan_fast_tauY.dat`: Waveform scan, which reports the output ADC code sampled at delayed times making possible to reconstruct the shaper transient response.

After the data acquisition process, a MATLAB script is run in order to analyse and plot all the tests results, and the output folder has the following structure.

```
MODULE_000/
└── 1/
    └── analysis_matlab/
        ├── ENC/
        ├── Pedestal/
        ├── SelfTrigger/
        ├── ThresholdScan/
        ├── TransferFunction/
        └── WaveformScan/
```

Each sub-directory contains the following:

1. **ENC**: Equivalent Noise Charge (ENC) elaborated data and plots obtained from pedestal and transfer function (high gain) processing.
2. **Pedestal**: Pedestal elaborated data and plots representing the dispersion of the baseline due to electronic noise.
3. **SelfTrigger**: Self trigger plots (histograms) representing dispersion of the value read at the output of the ADC triggered by the Zero Crossing circuit.
4. **ThresholdScan**: Threshold scan elaborated data and plots reporting the statistics on the threshold obtained through fitting the data with an error function and a threshold dispersion minimisation analysis.
5. **TransferFunction**: Transfer function elaborated data and plots, representing channel input/output characteristic.
6. **WaveformScan**: Waveform scan elaborated data and plots representing the shaper transient response.

2.1.1 Visual inspection

A manual visual inspection has been performed on each FEB by looking over the board either with the naked eye or through magnification. The board has been compared to the design documents to ensure that all specifications were met. The purpose of this activity was to look for common defaults (missing or bad-soldered components) and defects (pits, dents, scratches, pinholes and other defects on printing traces and pads). If no or negligible defects were found, [YES] has been reported in the *Visual inspection* field of the test report module, similar to the one shown in Figure B.1. If a missing or bad-soldered component was found, the board was reworked and the operation has been reported in the *Notes* section of the report. A brief description of the most common visual defects that have been categorised is available in Figure 2.6.

It is important to emphasise the fact that the visual analysis to search for defects on the board or the components installed on it was of paramount importance in identifying problems that could have altered the proper functioning of the FEB. For example, if there was exposed copper in contact with other metals on the board, short circuits could possibly occur. Furthermore, in the event that a defect in one of the metal layers of the board was very large, this could result in a change in

Front-End Board (FEB)

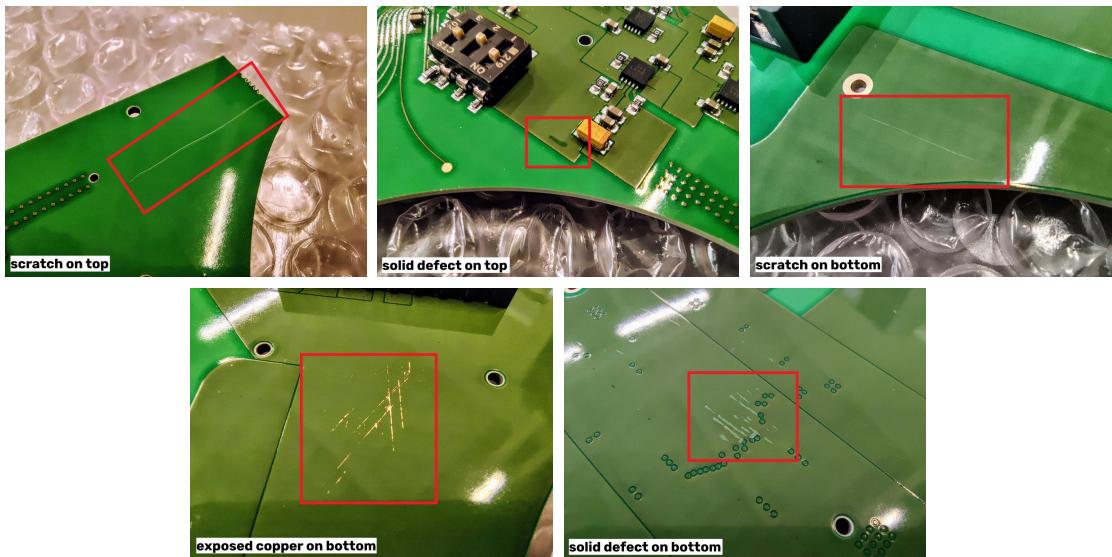


Figure 2.6: Examples of defects found during visual inspection of the FEBs (clockwise from top-left): scratch on top, solid defect on top, scratch on bottom, exposed copper on bottom, solid defect on bottom.

the resistance value of the entire metal layer (e.g. a power supply or a ground), thereby affecting the power consumption and thus altering the nominal operation of the board. In the event that one of the aforementioned defects led to the partial or total non-functioning of the board, the latter was categorised as "reworked" and separated from the others.

2.1.2 Bias

In this test, the DC voltages are measured with a Fluke 79 III digital multimeter and the DC currents are monitored with the built-in amperometer of the Keysight N6705C DC Power analyser used as power supply. The only exception is for the Ibias current that is derived from the voltage drop on a 100Ω Surface Mounted Device (SMD) test resistor (0.1 % precision) on the FEB. During the test the ASIC is biased with the following configuration: TBBB=0101 and HRRR=1011. The DC voltage and DC current measurements are reported respectively in Table 2.2 and Table 2.3.

For these measurements, the pass/fail criterion is not obvious, so the typical measurement value has been determined iteratively by analysing the results of the measurements carried out on a larger number of boards, whose test results can be found in Section 2.1.6. If a value in the range of $\pm 10\%$ with respect to the mean

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was obtained, [YES] has been reported in the corresponding section of the report.

Voltage	Nominal	Description
AVDD	1.80 V	Voltage at the output of the LDO that regulates the (ASIC) analog power supply
DVDD	1.80 V	Voltage at the output of the LDO that regulates the (ASIC) digital power supply
3V3	3.00 V	Voltage at the output of the LDO that regulates the (ASIC) calibration power supply
VCMSH	1.20 V	Reference voltage for the S&H
VCM	0.88 V	Reference voltage for the shaper
RVCM	0.90 V	Reference voltage for the ADC

Table 2.2: List of voltages measured during the bias test of the FEB.

Current	Nominal	Description
IAVDD	136 mA	Current absorbed by the LDO that regulates the (ASIC) analog power supply
IDVDD	4 mA	Current absorbed by the LDO that regulates the (ASIC) digital power supply
I3V3	3 mA	Current absorbed by the LDO that regulates the (ASIC) calibration power supply
Ibias	5 mA	Bias current for the CSA

Table 2.3: List of currents measured during the bias test of the FEB.

2.1.3 Digital

In this Section of the test report document, results coming from the *Automated test* of the **GAPS_ModuleTester** software are reported considering the following aspects:

- **Configuration test:** It checks the capability to write and read registers of the digital back-end section of the ASIC of the board under tests. For the FEBs where the improved setup shown in Figure 2.4 has been used, this test also accounts for the capability to communicate with the second FEB in the chain.

Front-End Board (FEB)

- **Wrong address test:** It checks the capability of the ASIC to ignore commands when an address, different to the one hardware coded on the board, is selected.
- **Temperature sensor:** It verifies the response of the ADC when the sensor temperature of the FEB is readout.

2.1.4 Analog

The results reported in this Section of the test report document are relevant to the performance of the analog readout channels of the ASIC. Data is obtained from the *Automated test* of the **GAPS_ModuleTester** software. The four main reference tests chosen to be included in the report are listed below.

Channel Input-output characteristic The purpose of this test is to verify that all the channels respond to the input injected signal and provide the expected input-output characteristic with dynamic signal compression. If zero non-responding channels were found, [YES] has been reported in the *Input-output characteristic* field of the test report document.

Noise The noise performance of 6 channels (No. 0, 7, 15, 16, 23 and 31) is expressed in terms of ENC FWHM in keV and results obtained for peaking time #6 are reported in this Section. Since the measurement conditions of the FEB are not optimised from a noise point of view, it is not expected that the channels provide the minimum ENC. Therefore, a value lower than 200 keV is considered good enough to have a [YES] assigned. In the case of 135 US-made FEBs, the ENC measurement was carried out by placing the board inside a metal box in order to shield it from any electromagnetic interference present in the measurement environment. In this way, it was possible to measure ENC values that could provide a more faithful representation of the board actual noise performance. The ENC measurements for 6 of the 32 channels of the ASIC are shown in Figure 2.18.

Threshold dispersion The threshold dispersion of the 32 channels of the ASIC is reported here, before and after the fine trimming procedure that is adopted to minimise the dispersion of the threshold distribution. This test is conducted in order to determine the width (i.e. the standard deviation) of the distribution of threshold values associated with the 32 channels of the readout electronics. In fact, each

channel has a threshold value associated with the minimum energy level at which the comparator is triggered: due to variations in the manufacturing process of the transistors constituting the circuit blocks of the channel (a phenomenon known as *transistor mismatch*), these may in fact have associated threshold values lower or higher than the one specified. The purpose of this test is therefore to check how far the threshold value disperses around the set value. The purpose of this test is also to verify the effectiveness of the 3-bit ADC in each channel used to fine-tune the threshold and thus reduce its dispersion.

Pedestal dispersion The distribution of the pedestal of the 32 readout channels is reported in this Section.

Each FEB has been numbered using an alphanumerical identifier, allowing the board to be uniquely recognised during the assembly of the tracker. The identifier number is composed of three parts, as shown below.

$\overbrace{\text{F} \text{ 065} \text{ I}}^{\text{1 2 3}}$

Specifically, each part of the alphanumerical sequence serves the purpose of:

1. **F**: It classifies the component ("F" as for "Flight", meaning the FEB has installed a SLIDER32 ASIC in the version intended for use in the in-flight experiment).
2. **065**: It uniquely represents the specific board via an increasing numerical value, which matches the numerical identifier of the SLIDER32 ASIC installed on the front-end board.
3. **I**: It identifies the country of the manufacturer of the board ("I" for the Italian-made FEBs and "U" for the US-made ones).

For each FEB tested, a test report has been generated in order to sum up all the information regarding the whole testing activity carried out on the front-end board. An example of the aforementioned test report is shown in Figure B.1.

2.1.5 GAPS-FEB-Report-Generator

This Section provides a brief description of the Python software that has been developed in order to automatically generate the test reports for the FEBs, as the one

Front-End Board (FEB)

shown in Figure B.1. The code can be found on GitHub at the following [link](#).

Software functionalities

The software works by taking as input two Comma Separated Values (CSV) files reporting the voltage and current measurements taken on the FEBs and the corresponding defects that have been found during the visual inspection, including optional notes, and producing a report summarising all the data both as a Microsoft Word document and a Portable Document Format (PDF) file, the contents of which are shown in Figure B.1.

The Python code is basically organised in two parts:

1. `FEB_report_fun.py`: It contains all the functions that are used in order to fill in the Word document and to export the corresponding PDF file. This file also contains the functions used to export log files and CSV tables containing a summary of the values obtained during the testing of each individual FEB.
2. `FEB_report_out.py`: It contains the function calls to the function blocks defined in the previous file and uses them to build the output document.

Software structure

The software is organised into different sub-folders, each one containing specific input or output files, as described in the following directory tree:

```
GAPS-FEB-report-generator/
  configuration/
    config.conf
  CSV_tables/
    FEB_testing - Defects.csv
    FEB_testing - Multimeter.csv
  modules/
    MODULE_000/
    ...
  output/
    FEB_report_log.pdf
    FEB_report_log.txt
    script_values.csv
    temperature_ADC.csv
    temperature_C.csv
```

```
└── report_PDF/
    └── F000I.pdf
        ...
    └── ...
    └── report_template/
        └── test_report_FEB.docx
    └── report_word/
        └── F000I.docx
        ...
    └── ...
    └── script_files/
        └── FEB_report_fun.py
        └── FEB_report_out.py
```

Moreover, each individual item serves the following function.

1. **config.conf**: Configuration file where the user can specify the nation identifier letter (`nation_letter` field) of the producer of the board (I for Italy and U for US production), the document version (`doc_version` field), the date, the author name and surname and the nationality of the manufacturer (**Italian** or **US**).
2. **FEB_testing - Defects.csv**: CSV file containing a list of the defects found during the visual inspection of the FEBs, as discussed in Section 2.1.1.
3. **FEB_testing - Multimeter.csv**: CSV file containing the voltage and current measurements taken on the FEBs, as described in Section 2.1.2.
4. **modules** folder: Containing the folders generated by the purposely developed MATLAB script, described in Section 2.1.
5. **FEB_report_log.pdf** and **FEB_report_log.txt**: Log file containing a summary of all the reports fields presented in a single, multi-page document format.
6. **script_values.csv**: CSV file containing a summary of the values obtained during the evaluation of the performance of the analog readout channels of the ASIC generated by the **GAPS_ModuleTester** testing software, as mentioned in Section 2.1.4.
7. **temperature_ADC.csv** and **temperature_C.csv**: CSV files containing the readings of the temperatures in ADU and °C respectively.
8. **report_PDF/** folder: Folder containing the PDF version of the reports generated by the software.

Front-End Board (FEB)

9. `test_report_FEB.docx`: Word template used to produce the final test reports in Word and PDF format.
10. `report_word/` folder: Folder containing the Word version of the reports generated by the software.
11. `script_files` folder: Folder containing the two main Python files used to implement the program, as described in section 2.1.5.

Software usage

The program can be launched with Python 3 installed on the PC by double-clicking on the `FEB_report_out.py` Python file and by interacting with the command-line interface shown in Figure 2.7.

```
C:\WINDOWS\py.exe
Range START: 1
Range STOP: 500
MODULE F002I
100%|██████████| 1/1 [00:02<00:00,  2.66s/it]
MODULE F003I
100%|██████████| 1/1 [00:02<00:00,  2.09s/it]
MODULE F004I
100%|██████████| 1/1 [00:02<00:00,  2.04s/it]
MODULE F005I
100%|██████████| 1/1 [00:02<00:00,  2.15s/it]
MODULE F006I
100%|██████████| 1/1 [00:00<00:00,  1.11it/s]
```

Figure 2.7: Command line interface of the GAPS-FEB-report-generator software.

At first, the software asks to input the minimum and maximum values of the FEB identifier numbers for which the user wants to generate a report. It has to be noted that for the program to be correctly executed, `FEB_testing - Defects.csv` and `FEB_testing - Multimeter.csv` have to be present in their corresponding folders. The report generation can be tracked through the loading bars showing the total time taken to compile each report. Once the generation of the reports is complete, the files can be found in `report_word/` and `report_PDF/` folders respectively.

2.1.6 Analysis of test results

This Section describes the results of the measurements carried out during the validation phase of the front-end boards. Each graph shows the data distribution for

the Italian-made front-end boards (in blue) and US-made ones (in red) separately for comparison purposes.

AVDD and IAVDD The graphs in Figure 2.8 show the distributions of the analog supply voltage, AVDD, and the corresponding current IAVDD. The nominal value of AVDD, shown in Table 2.2, is 1.80 V, while that of IAVDD, shown in Table 2.3, corresponds to 136 mA. It can be seen that both productions present an average voltage value comparable to the nominal one and have the same standard deviation. On the other hand, the average current value is below the nominal one for both productions, with the American one being on average 1.49 % lower than expected and the Italian one reaching almost exactly the desired current value (135.93 mA compared to the 136.00 mA nominal value).

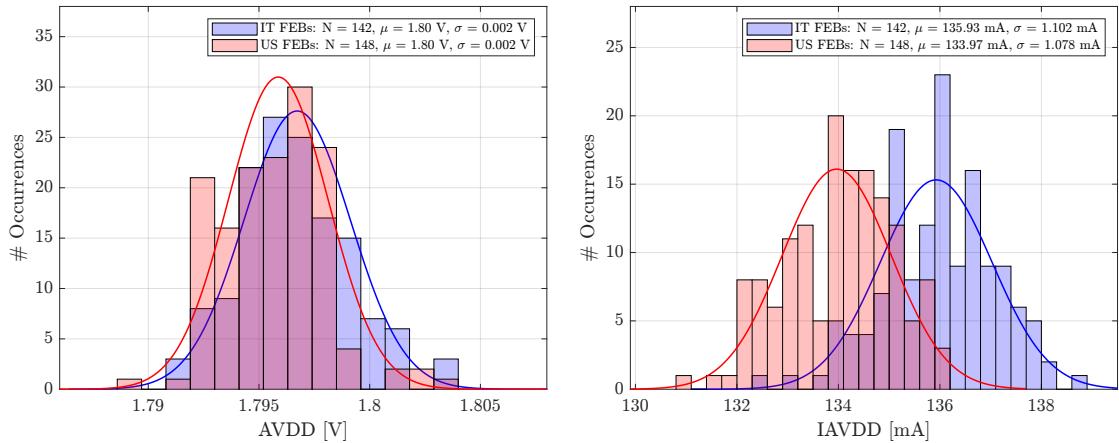


Figure 2.8: AVDD values distribution, on the left, and IAVDD values distribution, on the right. Each histogram reports the mean value and standard deviation for both Italian and US productions.

Ibias Figure 2.9 shows the distribution of the biasing current, Ibias, whose nominal value is 5 mA. For both productions, the average value of this parameter is almost comparable with the expected value, with a similar standard deviation between the two.

DVDD and IDVDD In the case of the digital supply voltage DVDD and the respective current IDVDD, the distributions of the measured values are shown in Figure 2.10. As in the case of the analogue supply voltage, the average values of both outputs are comparable with the nominal value of 1.80 V. As far as the current

Front-End Board (FEB)

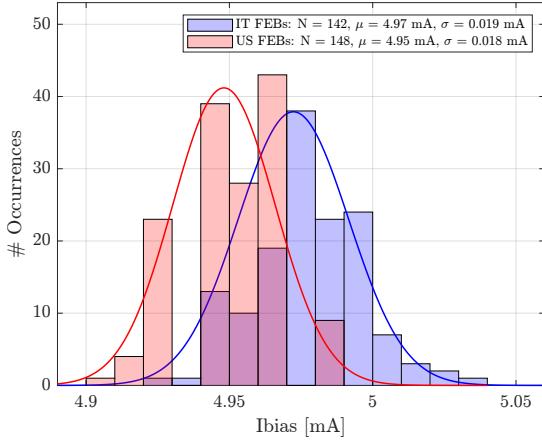


Figure 2.9: Ibias values distribution. The histogram reports the mean value and standard deviation for both Italian and US productions.

is concerned, in the case of the American production, a value of exactly 5.00 mA was found on all FEBs tested, resulting in a zero standard deviation.

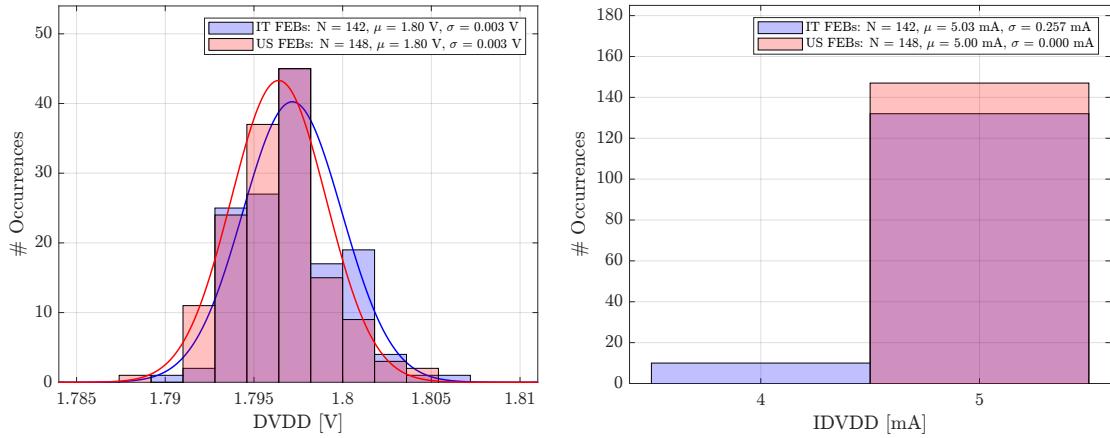


Figure 2.10: DVDD values distribution, on the left, and IDVDD values distribution, on the right. Each histogram reports the mean value and standard deviation for both Italian and US productions.

3V3 and I3V3 The distribution of the voltage used as a power supply for calibration, 3V3, and the associated current, I3V3, are shown in Figure 2.11. It can be seen that the voltage distribution in the case of American production has almost twice the dispersion of Italian production. This phenomenon is attributed to the fact that for 6 FEBs, values greatly different from the expected one are obtained, up to 2.33 % less. On the other hand, for the Italian production, all measured values are consistent with the mean, with a standard deviation of 5.00 mV.

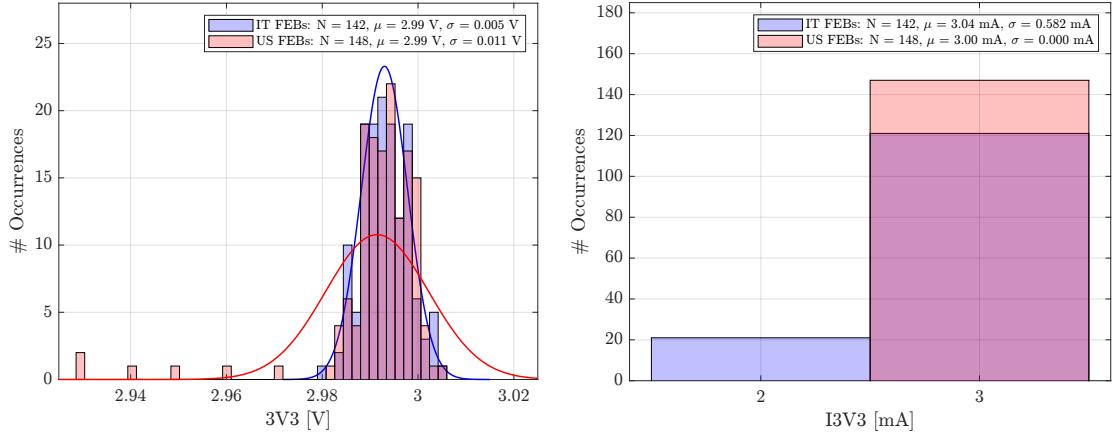


Figure 2.11: 3V3 values distribution on the left and I3V3 values distribution on the right. Each histogram reports the mean value and standard deviation for both Italian and US productions.

VCMSH, VCM and RVC Figure 2.12 shows the distributions of voltages used as references for the S&H, shaper and ADC respectively. In the case of VCMSH and RVC, the average values for both distributions are comparable with the reference value of 1.20 V and 0.90 V respectively. In the specific case of the VCM voltage, the Italian and American productions present an average value that differs by approximately 10 mV from each other, while maintaining a comparable standard deviation.

Temperature The temperature measurements shown in Figure 2.13 allows to verify the correct operation of the temperature sensor installed on the front-end board. It can be seen that the average temperature measured on the American-made FEBs is higher than that measured on the Italian-made FEBs. This is purely attributable to the period of the year in which the tests were carried out, that is, summer, therefore an increase in the average measured temperature can be expected. Furthermore, the fact that the tests on the American production were completed within approximately two weeks can be seen in the lower standard deviation, which can be attributed to a smaller fluctuation in ambient temperature. In order to obtain the temperature measurement from the sensor installed on the front-end board (Texas Instruments LMT84), it is first necessary to obtain the output voltage value V_T , which considering the sensor readout network implemented on the ASIC is evaluated as:

$$V_T = 900 \text{ mV} - \frac{(ADC_{code} - 1024) \cdot 1.72 \text{ mV}}{3.87}. \quad (2.1)$$

Front-End Board (FEB)

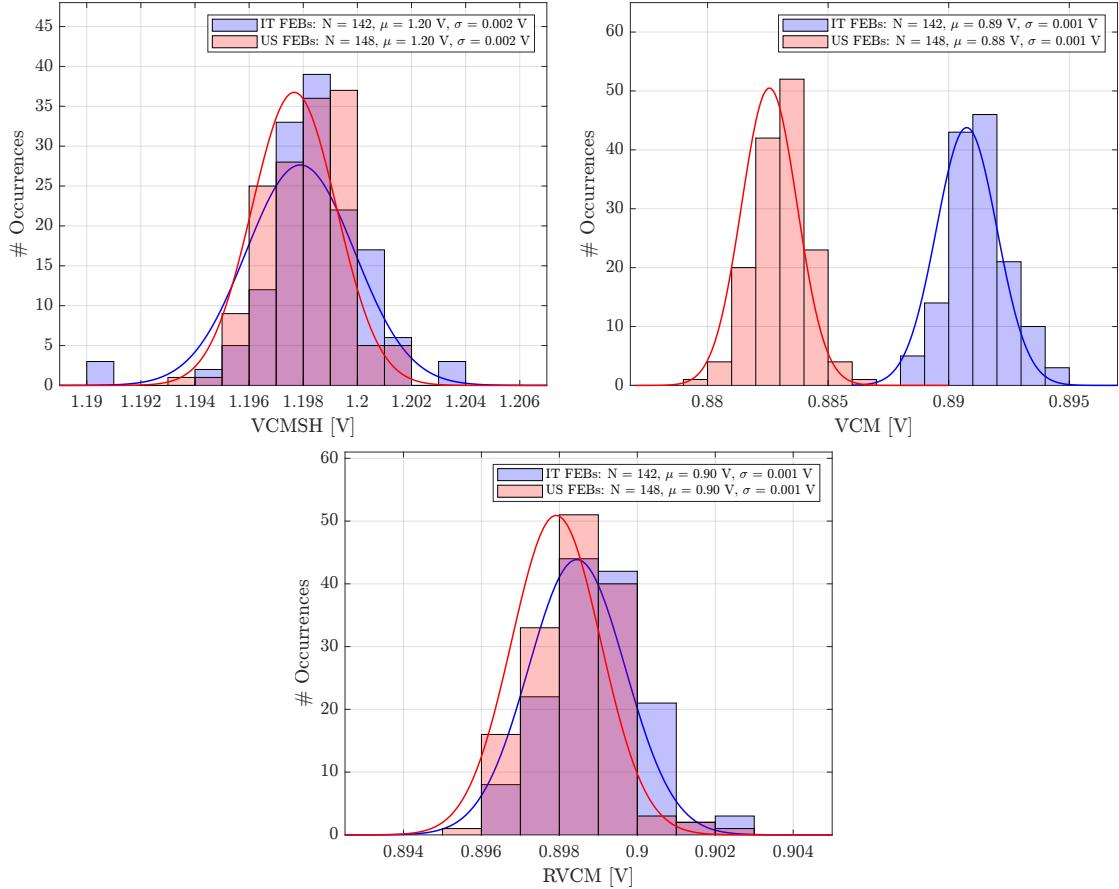


Figure 2.12: Clockwise from left to right: VCMSH, VCM and RVCM values distributions. Each histogram reports the mean value and standard deviation for both Italian and US productions.

From this Equation the temperature T can be obtained (expressed in °C):

$$T = 30^\circ\text{C} + \frac{5.506 \frac{\text{mV}}{\text{C}} - \sqrt{(-5.506 \frac{\text{mV}}{\text{C}})^2 + 4 \cdot 0.00176 \frac{\text{mV}}{\text{C}^2} \cdot (870.6 \text{ mV} - V_T)}}{2 \cdot (-0.00176 \frac{\text{mV}}{\text{C}^2})} \quad (2.2)$$

Defects detected during visual inspection Figure 2.14 shows a comparison of the categories of defects detected on Italian and American-made FEBs during visual inspection, while Figure 2.15 shows the percentage of FEBs with and without defects detected for both productions. It can be seen that although the percentage of defects detected differs significantly between the two productions, the overall percentage of defect-free front-end boards is comparable.

Si(Li) tracker flight components validation

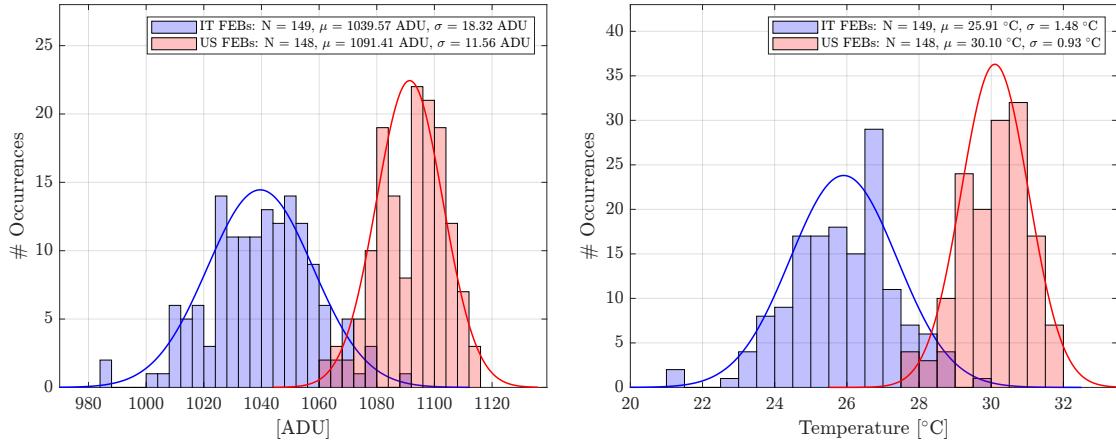


Figure 2.13: Temperature statics for Italian made FEBs: temperature expressed in Analog Digital Units (ADU) on the left and in Celsius ($^{\circ}\text{C}$) on the right. Each histogram reports the mean value and standard deviation for both Italian and US productions.

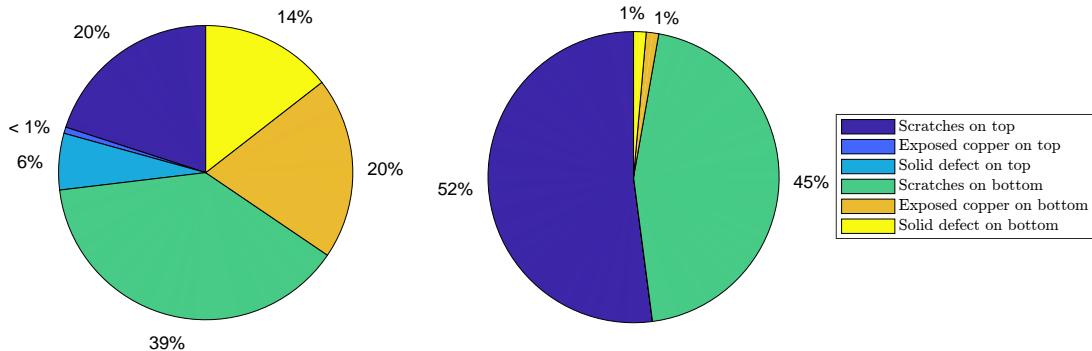


Figure 2.14: Defects found during visual inspection on Italian made FEBs (on the left) and on US-made ones (on the right).

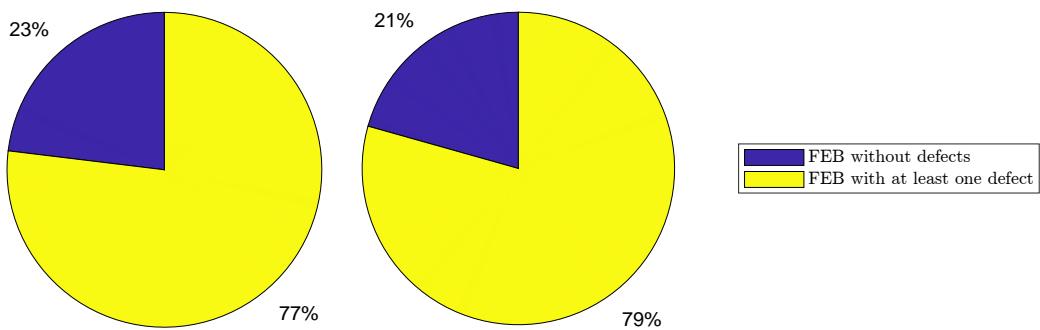


Figure 2.15: Percentage of FEB without any noticeable visual defects for the Italian production (on the left) and for the US production (on the right).

Front-End Board (FEB)

Pedestal dispersion This paragraph reports the results of the pedestal measurement used to evaluate the electronic noise of each channel in order to identify the most problematic ones, which could adversely affect the correct measurement of incident charges. The plot in Figure 2.16 represents the distribution of pedestal dispersion evaluated on the FEBs of Italian and US production. It is easy to deduce how the use of the metal box induces a reduction in pedestal dispersion, which in US-made FEBs is reduced by about 83 % in mean value and 74 % in terms of standard deviation compared to Italian-made ones.

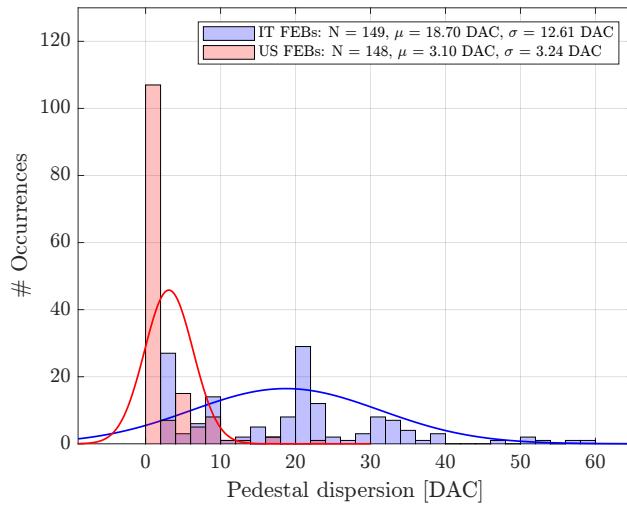


Figure 2.16: Pedestal dispersion distribution. The histogram reports the mean value and standard deviation for both Italian and US productions.

Threshold dispersion Figure 2.17 presents the distributions of threshold dispersion before fine threshold optimisation (on the left) and after (on the right). It can be seen that, after optimisation using the 3-bit DAC, both distributions from Italian and US production, have a reduced dispersion as well as a compatible mean and standard deviation since the minimisation process focuses on obtaining a threshold voltage value consistent across all the modules integrated in the tracker. Fine threshold tuning via the aforementioned 3-bit DAC in fact allows the threshold voltage to be optimised directly on the individual channel, thus making it possible to bring the threshold value of the channel closer to the global threshold value. This is made necessary by the fact that, due to variations in the manufacturing process of the transistors constituting the channel circuit blocks, each channel has a threshold value slightly different from one another and not necessarily equal to the set global

threshold value. This method therefore allows one to act at a "fine" level in order to reduce the overall threshold dispersion over all 32 channels.

The result of applying this method is immediately visible by comparing the standard deviations of the distributions shown in Figure 2.17, which highlights how the dispersion value after optimisation is on average reduced by half on both productions.

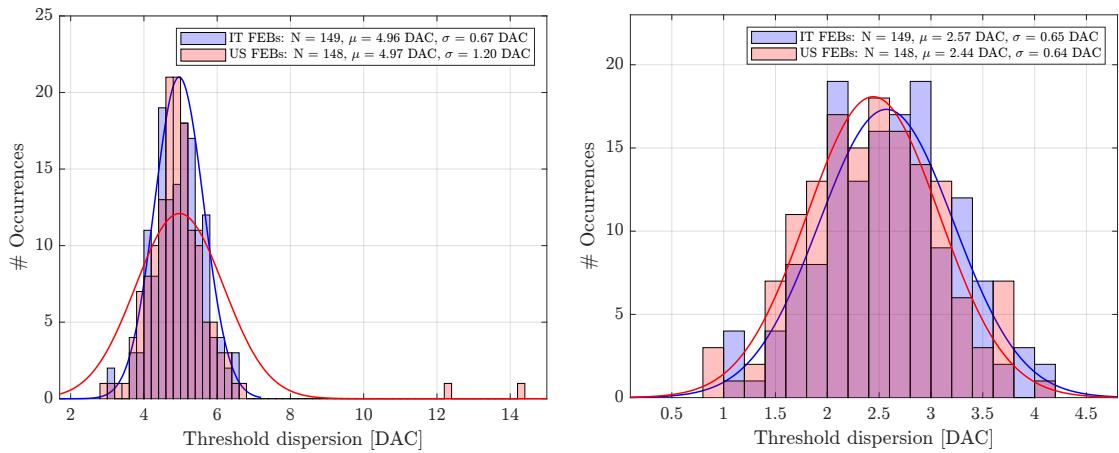


Figure 2.17: Threshold dispersion values distribution before fine threshold optimisation (on the left) and after (on the right). Each histogram reports the mean value and standard deviation for both Italian and US productions.

Noise The noise measurements carried out on 135 of the 150 American-made FEBs are shown in Figure 2.18 for channels No. 0, 7, 15, 16, 23, 31. In particular, the displayed measurements were carried out by placing the front-end board under test inside a metal box in order to shield it from the electromagnetic interferences present in the test environment. This made it possible to obtain noise measurements, in the form of ENC, that could effectively reflect the real noise performance of the boards, free of alterations due to the surrounding environment. The remaining FEBs, including those of Italian manufacture, were tested without any shielding and demonstrated ENC values even in the hundreds of keV range.

2.2 Dummy-1 front-end board

The Dummy board type 1, also known as *Dummy-1*, is a not populated board that will be used in the first launch of the experiment, scheduled for the end of 2023,

Dummy-1 front-end board

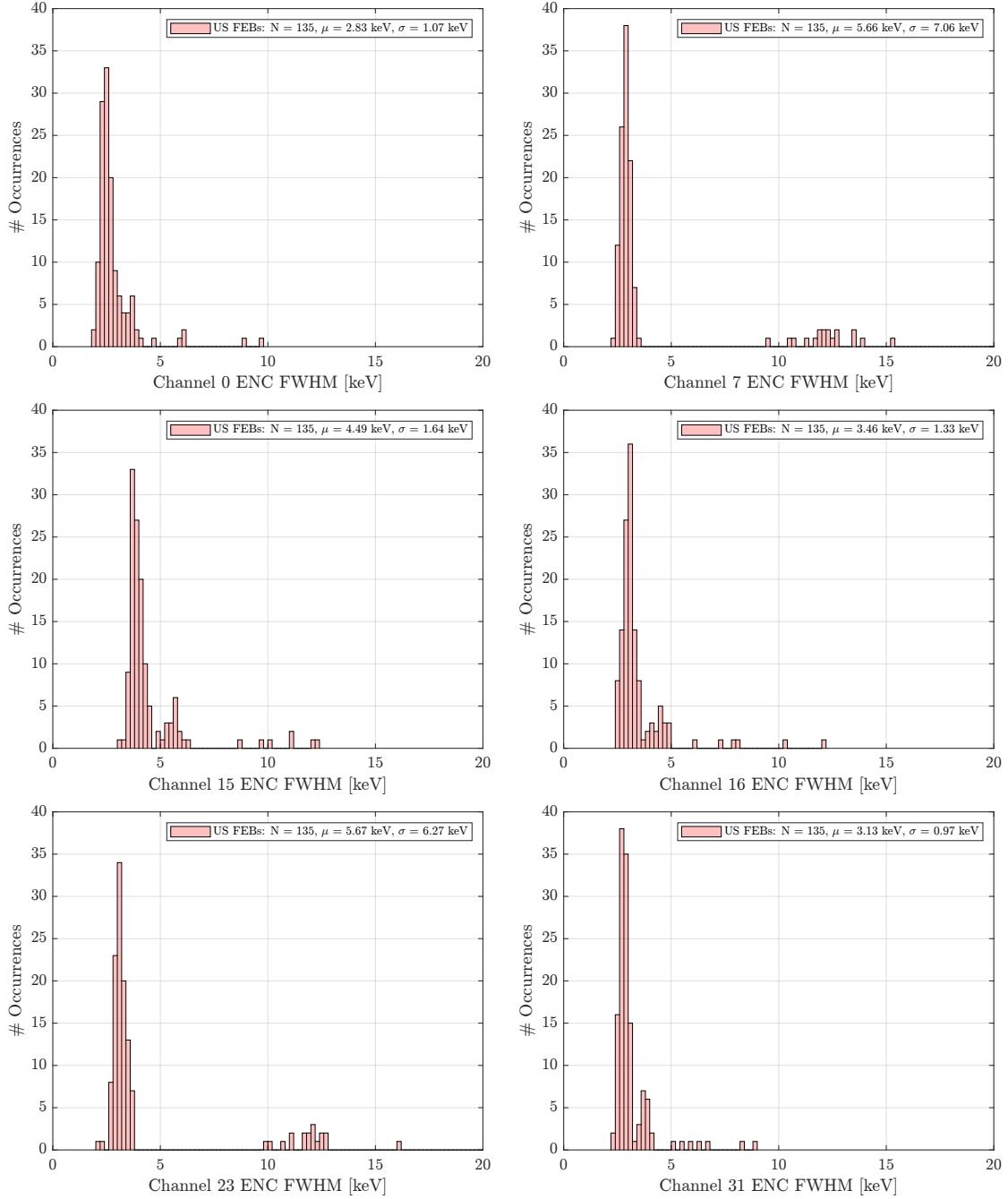


Figure 2.18: Statistical distributions of measured ENC FWHM for a limited set of boards belonging to the US production. Each histogram also reports the distribution mean value and standard deviation.

in order to replace the missing FEBs in some of the detector layers, as these are currently in a smaller number than required to fill all the tracker slots.

The validation tests of the Dummy-1 front-end boards has been performed at

ambient temperature after having soldered only a couple of resistors emulating the analog power consumption of the FEB. Specifically, two $40\ \Omega$ resistors and a $4.7\ \mu\text{F}$ capacitor 0805 SMD have been installed on the board, along with a short piece of wire ($\approx 1\ \text{cm}$ in length) in order to connect the newly installed components to the analog voltage supply line, as shown in Figure 2.19.

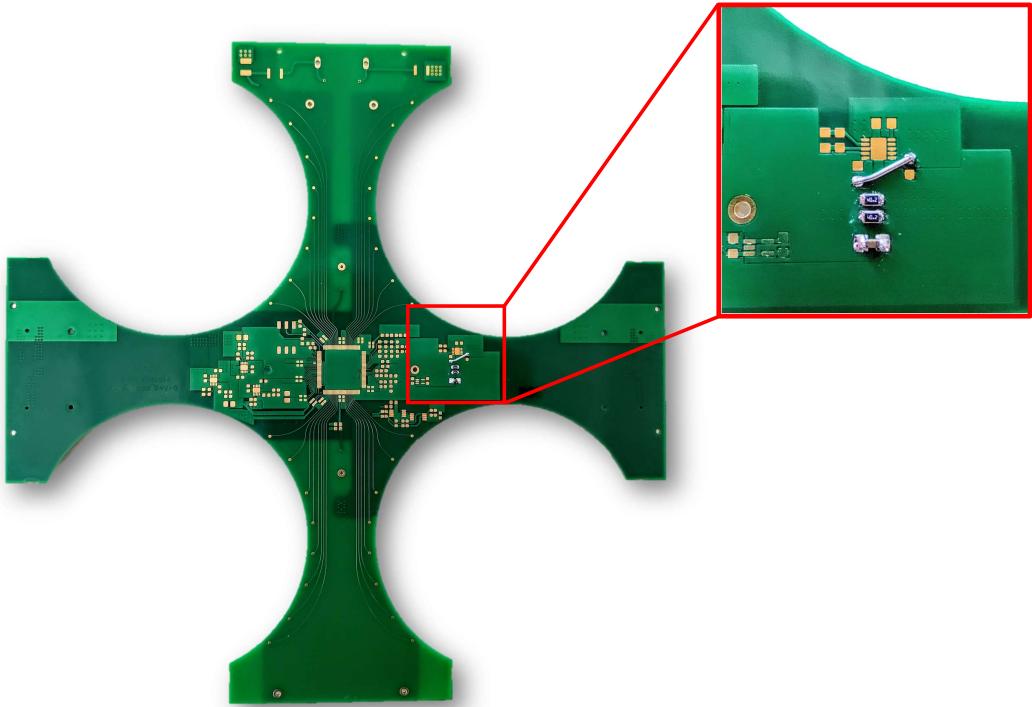


Figure 2.19: Dummy-1 front-end board with a detailed view of the soldered components.

This configuration was chosen as the one better suited to emulate the thermal behaviour of the active components installed on a fully populated FEB. Initial trials were based on a single $20\ \Omega$ 0805 SMD resistor directly connected to the AVDD supply voltage, but this configuration was soon discarded as the power dissipated by the resistor was very near to its $0.5\ \text{W}$ maximum power rating. In fact, the current flowing through the resistor is evaluated as

$$I_R = \frac{2.8\ \text{V}}{20\ \Omega} = 0.14\ \text{A} = 140\ \text{mA} \quad (2.3)$$

therefore the power dissipated by the resistor is

$$P_R = 2.8\ \text{V} \cdot 0.14\ \text{A} = 0.392\ \text{W} \quad (2.4)$$

Dummy-1 front-end board

which confirms the aforementioned. A common rule of thumb requires the power rating to be at least twice the nominal dissipated power, therefore employing two 40Ω resistors in parallel allowed the power dissipated on each resistor to be half of the total dissipated power

$$P_R = 2.8 \text{ V} \cdot \frac{0.14 \text{ A}}{2} = 0.196 \text{ W} \quad (2.5)$$

thus ensuring compliance to the aforementioned rule of thumb. Figure 2.20 shows the thermal image for the configuration with a single resistor (on the left) and with two resistors (on the right). In both cases, the analog supply voltage (AVDD) was set to 2.8 V, as a worst case scenario. It can be seen the temperature difference between the two configurations is of approximately 9.8°C for the same dissipated power.

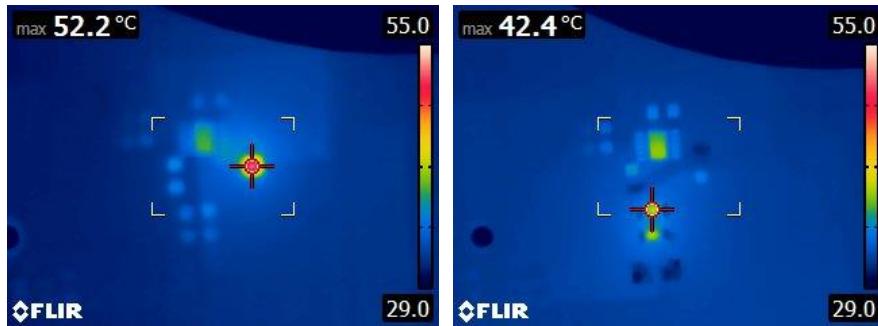


Figure 2.20: Thermal performance of Dummy-1 boards: on the left the configuration with a single 20Ω resistor, on the right the configuration with two 40Ω resistors in parallel.

Tests carried out on the Dummy-1 FEBs have the purpose of:

- Verify that the board is able to emulate the proper power dissipation.
- Verify that, once placed in series with other FEBs, it is able to properly propagate both bias voltages and digital signals to the subsequent boards.

2.2.1 Visual inspection

A manual visual inspection has been performed for each Dummy-1 sample by looking over the board either with the naked eye or through magnification. Visual inspection has been applied before and after the thermal cycle. The purpose of this activity is to look for missing or bad-soldered ERNI connectors and defects (pits, dents, scratches,

pinholes and other defects on printing traces and pads). If no or negligible defects were found, [YES] was reported in the *Visual inspection* field of the test report module. If a missing or bad-soldered component was found, the board was rejected since it is not possible to manually solder the ERNI connectors.

2.2.2 Thermal test

The boards underwent one thermal cycle in a climate chamber (model ACS DY110) in order to ensure that the board and the components installed on it are not deformed or damaged under the operating temperature conditions of the experiment, thus also verifying the correct soldering of the components on the board. The performed thermal cycle has the following characteristics:

- Minimum temperature (T_{min}): -40°C .
- Maximum temperature (T_{max}): $+60^{\circ}\text{C}$.
- Time spent at T_{min} and T_{max} : 20 minutes.
- Heating and cooling rate: Maximum $4^{\circ}\text{C}/\text{minute}$.

If, after the thermal cycle, the PCB did not show any type of defect, [YES] was reported in the *Thermal cycling* field of the test report module. A plot of the temperature in the climate chamber during thermal test can be found in Figure 2.21, where the 60°C and -40°C intervals are visible. It can be also noted that the boards underwent a further 20 minutes at controlled ambient temperature ($\approx 25^{\circ}\text{C}$) after the thermal cycle was completed in order to avoid any thermal shocks or damages coming from a sudden change in temperature.

After the thermal cycle, the boards have been left biased for at least 10 minutes. If no damage occurred to the resistors, the test is considered as passed. Moreover, a thermal picture of the resistor has been taken (with a FLIR ETS320 non-contact thermal measurement system), like the one shown in Figure 2.20.

2.2.3 Power test

In this test a nominal voltage of 2.8 V was applied to the board. The current IAVDD absorbed and the voltage APDD of the dummy resistor have been measured and reported on the test report together with the computed power consumption PAVDD. For these measurements, the pass/fail criterion is not obvious, so the typical

Dummy-1 front-end board

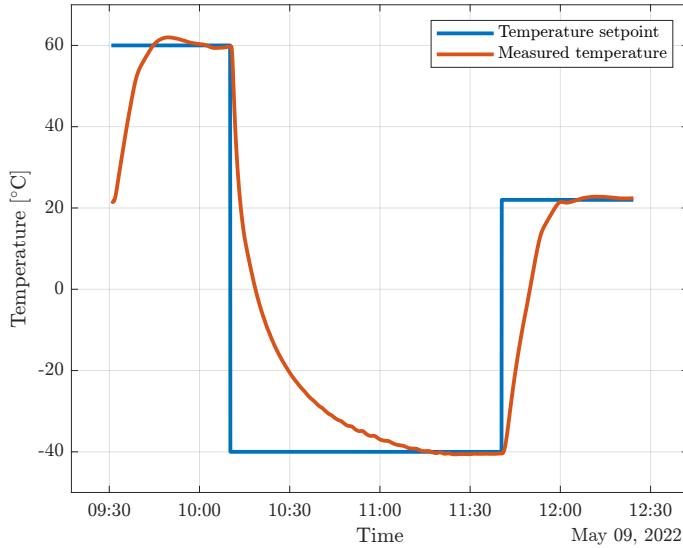


Figure 2.21: Environmental chamber temperature trend during thermal test (in orange) compared to the set-point (in blue).

measurement value has been determined iteratively by analysing the scans of a larger number of boards.

2.2.4 Bias and Digital

The purpose of this test is to validate the soldering of the input and output ERNI connectors. The board under test has been placed in series with a fully populated FEB as shown in Figure 2.4 and a configuration test was run on the FEB. If it responded correctly, it means that ERNI connectors on the Dummy-1 board are properly soldered and [YES] has been reported in the *Communication test* field of the test report.

As done for the front-end boards, a test report is generated, whose first page is shown in Figure B.2. In the case of the Dummy-1 front-end boards, a single multi-page document has been created, having the structure described in Table 2.4.

#	Board ID	Thermal cycling	Visual inspection	Communication test	IAVDD [mA]	PAVDD [mW]
1	D00	Yes/No	Yes/No	Yes/No	000.0	000.00

Table 2.4: Structure of the entry for the Dummy-1 front-end boards test report.

2.2.5 Test results

This Section reports the results of current (IAVDD) and power (PAVDD) measurements taken on all the 62 Dummy-1 front-end boards. The power value was obtained by multiplying the current value by the resistance value obtained from the parallel of the two installed resistors ($R_{tot} = 20 \Omega$). Figure 2.22 shows the distributions of current values on the left and power values on the right.

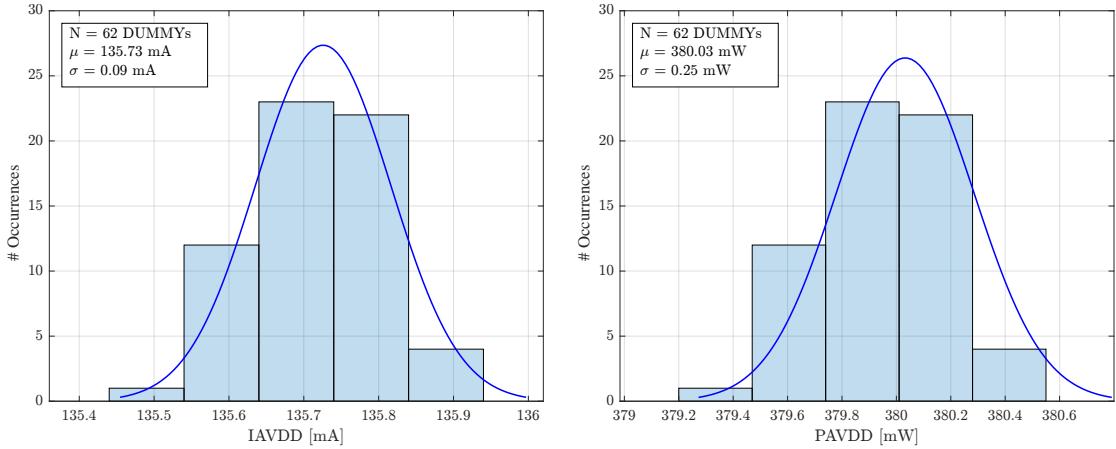


Figure 2.22: IAVDD values distribution on the left and PAVDD values distribution on the right. Both plots also provide the mean value and standard deviation of the respective distributions.

2.3 Flex-Rigid Board

Flex-rigid boards are intended to connect one front-end board with the next in the chain. They are by design flexible and allow digital signals and low power voltage supplies to be transported from one module to the next. The flexibility is given both by the material they are made of, polyamide, and by the presence of ground networks instead of rigid ground planes. The dielectric used in these boards is FR4 and they consist of 7 layers for the rigid zone, at the extremes, where the connectors are located, and 3 for the flexible interconnection zone. Figure 2.23 presents on the left a picture of a flex-rigid board next to a photograph in which the flex-rigid board is used to connect two front-end boards, where the flexibility of the flex-rigid board can be appreciated.

Flex-Rigid Board

2.3.1 Visual inspection

A manual visual inspection has been performed for each sample by looking over the board either with the naked eye or through magnification. Visual inspection is applied before and after the thermal cycle. The purpose of this activity was to look for missing or bad-soldered ERNI connectors and defects (pits, dents, scratches, pinholes and other defects on printing traces and pads). If no or negligible defects were found, [YES] has been reported in the *Visual inspection* field of the test report. If a missing or bad-soldered component was found, the board is rejected since it is not possible to manually solder the ERNI connectors.

2.3.2 Thermal cycle

The flex-rigid boards underwent one thermal cycle in a climate chamber (model ACS DY110). Thermal cycle has the same characteristics described in section 2.2.2. For flex-rigid boards that underwent thermal cycle and did not show any type of defect, [YES] has been reported in the *Thermal cycling* field of the test report.

2.3.3 Communication test

The purpose of this test is to validate the soldering of the two ERNI connectors. The board under test was placed in series with two fully populated FEBs as shown in Figure 2.4 and a configuration test was run on the second board in the chain. If it responded correctly, it means that ERNI connectors on the Flex-rigid board are properly soldered and [YES] has been reported in the *Communication test* field of the test report.



Figure 2.23: Flex-rigid board (on the left) connected to two front-end boards in series, where its flexibility can be appreciated.

As done for the front-end boards, a test report has been generated, whose first

page is shown in Figure B.3. In the case of the flex-rigid boards, a single multi-page document has been produced, having the following structure:

#	Board ID	Thermal cycling	Visual inspection	Communication test
1	FR000	Yes/No	Yes/No	Yes/No

Table 2.5: Structure of the entry for the flex-rigid boards test report.

2.4 Connector for termination

The purpose of the termination connectors is to adapt the 100Ω differential digital signal tracks through the use of 10 resistors of 100Ω each soldered onto the connector. The purpose of the tests performed on the termination connectors was to verify the correct installation of the resistors, as well as to ascertain their correct resistance value.



Figure 2.24: Connector for termination with ten 100Ω resistors installed.

2.4.1 Visual inspection

Visual inspection has been carried out to check the connector quality, then look for misaligned pins or missing termination resistor. Visual inspection is carried out before and after the thermal cycle. If no or negligible defects are found, [YES] is reported in the *Visual inspection* field of the test report.

2.4.2 Thermal cycle

The connectors underwent one thermal cycle in a climate chamber (model ACS DY110). Thermal cycle has the same characteristics described in section 2.2.2. For connectors that underwent the thermal cycle, [YES] has been reported in the *Thermal cycling* field of the test report.

2.4.3 Termination resistor soldering

The quality of the termination resistor soldering has been verified with a digital multimeter by measuring the resistance seen between two pins on the side of the connector opposite with respect to the one where components are mounted. The test has been performed after the thermal cycle for all the 10 termination resistors. If a value of $\approx 100 \pm 1\Omega$ is found for all the resistors, [YES] is reported in the *Resistor soldering* field of the test report module.

As done for the front-end boards, a test report has been generated, whose first page is shown in Figure B.4. In the case of the connectors for termination, a single multi-page document has been created:

#	Connector ID	Thermal cycling	Visual inspection	Resistor soldering
1	T00	Yes/No	Yes/No	Yes/No

Table 2.6: Structure of the entry for the termination connectors test report.

2.5 Front-end board shields

The purpose of the front-end board shields, shown in Figure 2.25, is to cover the tracks connecting the Si(Li) sensor strips with the pins of the readout integrated circuit, thereby reducing the impact of electromagnetic induced noise on each of the 32 channels of the readout ASIC. The front-end board shields installed on a front-end board are shown in Figure 2.26.

2.5.1 Visual inspection

Visual inspection has been carried out to check the surface quality, then look for the existence of pits, dents, scratches, pinholes and other defects. Visual inspection was performed before and after the thermal cycle. If no or negligible defects were found, [YES] has been reported in the *Visual inspection* field of the test report.

2.5.2 Thermal cycle

The boards underwent one thermal cycle in a climate chamber (model ACS DY110). Thermal cycle has the same characteristics described in section 2.2.2. For the front-

Si(Li) tracker flight components validation

end board shields that underwent the thermal cycle, [YES] has been reported in the *Thermal cycling* field of the test report.



Figure 2.25: Type A front-end board shield (on the left) and type B front-end board shield (on the right).

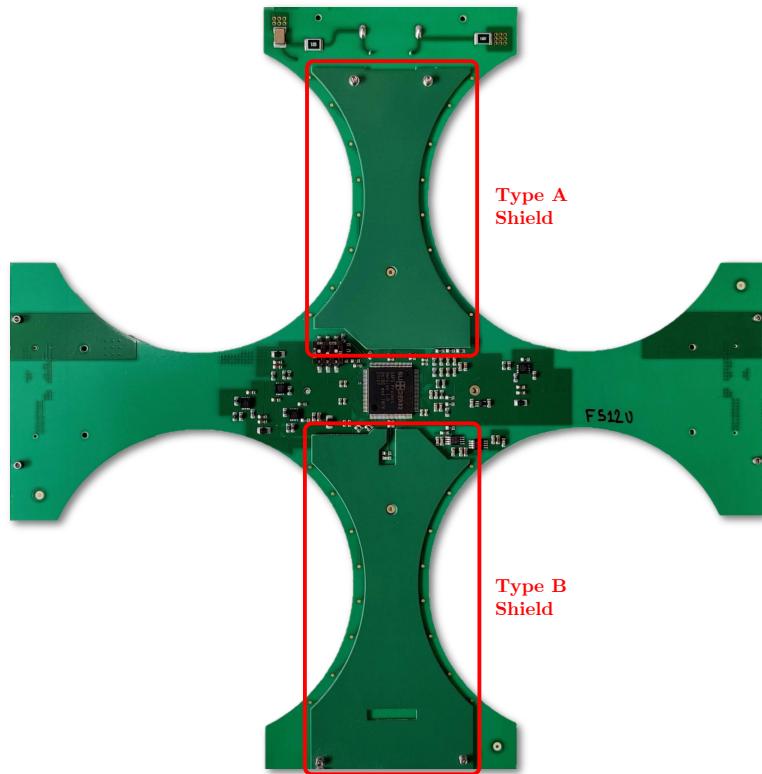


Figure 2.26: Type A and type B front-end board shields mounted on a front-end board.

Front-end board shields

As done for the front-end boards, a test report has been generated, whose first page is shown in Figure B.5. In the case of the front-end board shields, a single multi-page document has been produced, having the structure reported below.

#	Board ID	Thermal cycling	Visual inspection	Note
1	FR000	Yes/No	Yes/No	<i>Note</i>

Table 2.7: Structure of the entry for the front-end board shields test report.

Chapter 3

X-ray and particle detection with an assembled Si(Li) tracker module

This Chapter describes the test setup and the experimental results concerning the detection of X-rays from a ^{241}Am source and cosmic muons by means of an assembled Si(Li) tracker module of the GAPS experiment.

The Chapter is structured as follows. Initially, the physical background concerning cosmic muons, their nature and detection possibilities on planet Earth is given. Next, a description of the test setup adopted to carry out the measurements is provided, which is comprised of an assembled Si(Li) tracker module and an ArduSiPM ionising radiation detector, used as a trigger for the readout electronics. Finally, the experimental results obtained from the detection are reported, with an explanation of their usefulness in the context of flight item characterisation. This Section also reports the results obtained during the characterisation activity that has been performed on the fully assembled Si(Li) tracker module and the results obtained with an Americium source.

3.1 Cosmic muons

Cosmic rays are intense particles that continually rain through the Earth's atmosphere, with a portion of them penetrating the surface at relativistic speeds. Cosmic rays provide a homogeneous background ionising radiation that showers on the Earth's atmosphere at a rate of around 1000 collisions per square meter every second [6]. The sun or more exotic occurrences like supernovae and black holes can be the source of these particles. Most of the energy coming from cosmic rays reaches the

X-ray and particle detection with an assembled Si(Li) tracker module

Earth's surface in the form of muon kinetic energy.

Muons (μ^- and μ^+) are elementary particles similar to electrons, but with much greater mass. They belong to the lepton family [7] and form as a result of interactions between very energetic cosmic rays and the nuclei of atmospheric particles. They are the product of pion decay (π^- and π^+). The muons formed in the atmosphere may infiltrate the Earth's surface for hundreds of meters due to their ultra-relativistic character, which stems from the fact that these particles have a speed near to that of light. The flux of these particles may be distinguished adequately with a scintillator detection setup, as used in this experiment.

When cosmic rays collide with the atmosphere, they can cause a particle *shower*, which is a series of events that alter the character of the entering primary cosmic rays in other particles [8]. In a medium such as air, the particle shower has a hadronic core that serves as a source for electromagnetic subshowers. Figure 3.1 shows an illustration of cosmic rays interacting with the atmosphere, where the air shower effect is evident.

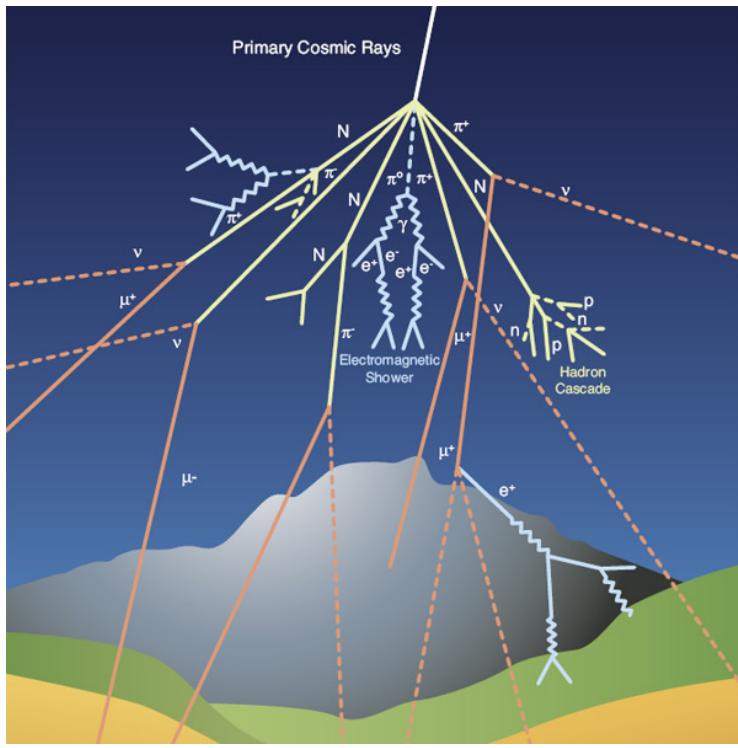


Figure 3.1: A diagram of cosmic rays interacting with the atmosphere and producing secondary particles. [9]

Cosmic muons, on the other hand, have a mean lifetime of around $2\ \mu\text{s}$ and may reach the Earth's surface at the speed of light. All of the particles in the

Experiment setup

air shower are collectively referred to as *secondary cosmic rays*. Pacini, Hess, and other physicists discovered them around the beginning of the twentieth century while studying the electric conductivity of air. They eventually realised that, in the words of Pacini, “*a sizeable cause of ionisation exists in the atmosphere, originating from penetrating radiation, independent of the direct action of radioactive substances in the crust*” [10, 11]. It was Millikan that for the first time, after these experiments, called this extraterrestrial radiation *cosmic rays*. The cosmic rays, after discovery and for a few decades before the takeover of particle accelerators, have been the main source for the early development of particle physic.

The flux of muons with a momentum greater than 1 GeV at sea level has been measured to be around $(0.94 \pm 0.12) \times 10^{-2} \text{ cm}^{-2} \text{ sr}^{-1} \text{ s}^{-1}$ [12, 13]. It can be said that 10 000 of muons per minute and per square (horizontal) meter, or alternatively $\approx 170 \text{ Hz/m}^2$, hit the ground. On average about 600 of them cross a human body every minute. Another easy to remember rule of thumb is that 1 muon per second intercepts the palm of a hand. These are indicative values, since the flux depends on many variables such as altitude, solar activity, Earth and other factors. The average energy of muons at sea level is comprised between 3 GeV and 4 GeV and the flux is maximum at the zenith (vertical direction) and it scales approximately with $\cos^2(\theta)$, θ being the angle with respect to the vertical.

3.2 Experiment setup

This Section provides a description of the setup used for the detection of cosmic muons through the joint use of the ArduSiPM ionising radiation detector and a fully assembled Si(Li) tracker module. Tests were conducted using the same setup described in Section 2.1 and shown in Figure 2.3, the only difference being that instead of testing a FEB without Si(Li) detectors, in this case a complete module with 4 Si(Li) detectors was tested. The complete experiment setup is shown in more detail in Figure 3.2.

In order to carry out the tests on the module, the latter was powered by means of two instruments:

- A Keysight N6705C DC Power Analyser providing both analog and digital supply voltages to the FEB, in the same configuration described in Section 1.1 and shown in Figure 1.3.

X-ray and particle detection with an assembled Si(Li) tracker module

- A CAEN HiVolta DT1415ET high voltage power supply used in order to bias the Si(Li) detectors with a negative DC voltage of -250 V .

Both instruments were controlled by means of a specially developed Python application in order to ensure the correct switch-on and switch-off sequence, which has to be performed by first switching on the power supply to the readout electronics via the Keysight N6705C DC Power Analyser and then the CAEN HiVolta to supply the -250 V biasing voltage to the Si(Li) detectors in a time interval of at least 1 ms and with a maximum increase of 4 V/s in order to avoid damage to the Si(Li) detectors. The switch-off sequence must be carried out in the exact reverse order with the same time constraint and voltage slope. The code can be found on GitHub at the following [link](#).

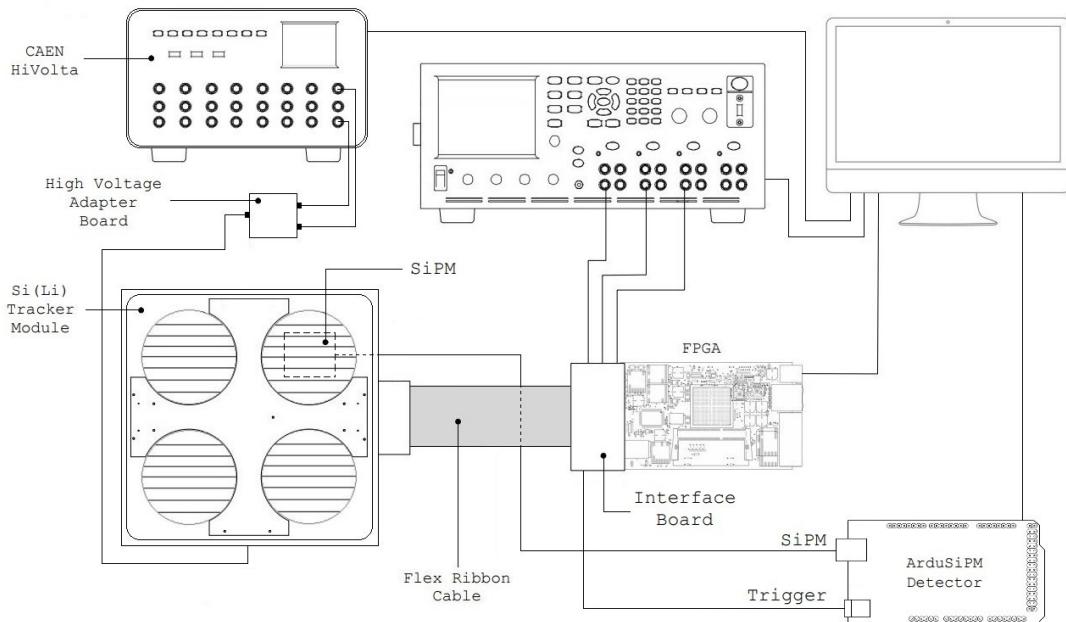


Figure 3.2: Complete cosmic muon detection experiment setup.

The tests were carried out in a climate chamber, model ACS DY110, at a constant temperature of $-40\text{ }^{\circ}\text{C}$ and 10% relative humidity. The transition from room temperature to $-40\text{ }^{\circ}\text{C}$ and vice versa was carried out with a decrease of $0.5\text{ }^{\circ}\text{C/s}$ in order to avoid sudden temperature changes and consequent damage to the Si(Li) detectors, as well as the formation of condensation.

In order to connect the high voltage lines coming from the CAEN HiVolta to the FEB, a specifically built adapter board, shown in Figure 3.3, has been developed in

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order to connect the negative and positive terminals of one channel of the CAEN HiVolta through two separate high voltage cables into a single one connected to the FEB. This adapter board presents on one end a BNC connector and on the other a HIROSE MDF51SU high voltage connector to be hooked up to the respective HIROSE MDF51SY housing on the FEB. Both connectors are shown in Figure 3.4.

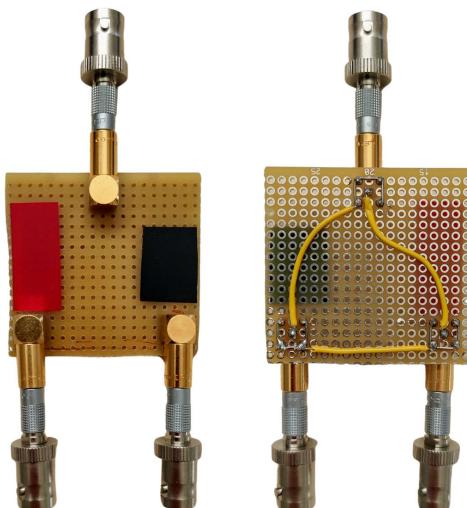


Figure 3.3: Top (on the left) and bottom (on the right) view of the purpose built high voltage adapter board designed to connect the CAEN HiVolta high voltage power supply to the Si(Li) tracker module.



Figure 3.4: HIROSE high voltage connector model MDF51SU on the left and model MDF51SY on the right.

3.2.1 ArduSiPM

ArduSiPM is a complete ionising particle detection and data acquisition system consisting of an open source Arduino Due board, a purpose-built shield connected to an Arduino 2 board called *ArduSiPM Shield* and a scintillator connected to a Silicon PhotoMultiplier (SiPM) [14].

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The scintillator was placed below one of the Si(Li) detectors, at a distance of between 4 and 5 cm. Due to the small size of the scintillator, measuring 5 cm on each side, it was not possible to cover the entire surface of the circular detector. Therefore, the scintillator was placed below the central part of channels 16, 17, 18 and 19, like shown in Figure 3.5.

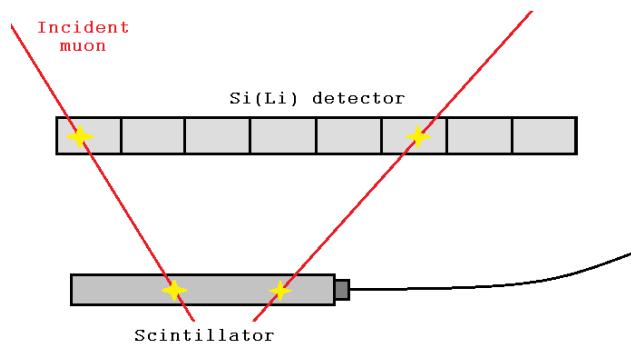


Figure 3.5: Scintillator placement with respect to the Si(Li) detector.

The transit of an ionising particle through the scintillator produces a signal in the photomultiplier that is processed by the electronics on the board. The complete device assembly is shown in Figure 3.6.

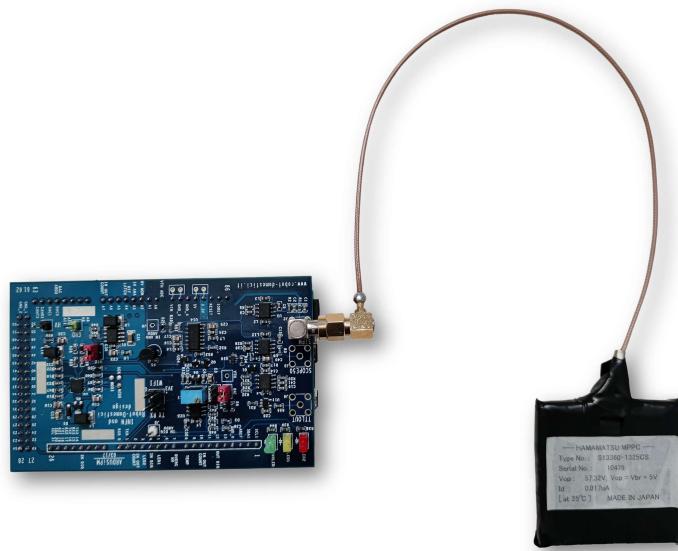


Figure 3.6: Picture of the ArduSiPM ionising particle detection and data acquisition system. It is possible to distinguish the ArduSiPM data acquisition board on the left and the detector module consisting of a scintillator and a photomultiplier on the right.

Experiment setup

The ArduSiPM shield is installed above the Arduino Due board, which takes care of acquiring data and powering it. The shield electronics, on the other hand, is responsible for powering the photomultiplier and taking readings from it. Specifically, this board consists of the following components.

- A *DC/DC converter* in the form of a boost converter capable of generating a DC output voltage between 30 and 100 V needed to power the photomultiplier. The converter takes as input a voltage of 5 V supplied directly from the Arduino Due's power supply.
- A *fast low-noise amplifier* required in order to take the signal from the photomultiplier and adapt it to the reading range of the Arduino Due's ADC, which is responsible for counting events in the form of particles entering the photomultiplier.
- A *fast discriminator* used to recognise above-threshold pulses from the photomultiplier. The output of this block is directly fed into the internal counter of the Arduino Due in order to count the photomultiplier interaction events.
- A *peak detector*, i.e. a circuit built with the purpose of maintaining the peak voltage read out by the photomultiplier. The latter switches very quickly, so this circuit block is designed to be very rapid in detecting peaks at very close time intervals.

The ArduSiPM device was used as a trigger for the readout electronics of the Si(Li) tracker module used in the experiment. For this purpose, the ArduSiPM Shield board provides a terminal on the board named TTLOUT, on which a signal of the type shown in Figure 3.7 is provided when the silicon photomultiplier registers an interaction event.

An *SMA* connector was installed on this terminal in order to connect the board to the trigger input of the interface board, visible in Figure 3.2. The connection between the photomultiplier and the board was made via a 2m-long *Lemo* coaxial cable with a delay of 10 ns. On the other hand, the connection between the board and the trigger input of the interface board was realised with a 1 m *Lemo* coaxial cable with a 5 ns delay.

The device is programmed via a specially developed firmware (version 2.1.5 is used) that allows data from the scintillator to be read via a USB connection to a PC via the serial interface of the Arduino IDE software used for programming.

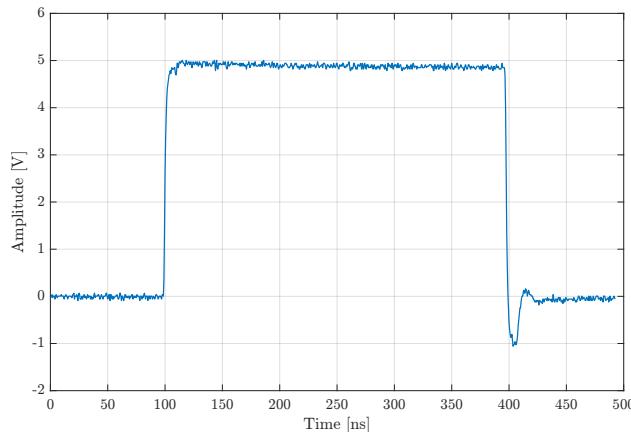


Figure 3.7: ArduSiPM trigger signal measured with a LeCroy WaveSurfer 454 oscilloscope.

Additional software is also available, called *ArduSiPM Acquisition Tool*, which allows data to be read and displayed on the screen in the form of graphs. It also allows to set some operating parameters and to monitor the serial communication. The software also makes it possible to carry out data acquisitions with tunable time duration, then exporting them in `csv` format.

An important feature of the firmware flashed on the device is the possibility of setting various detector parameters directly from the serial interface, using a predefined set of commands [15]. Those of interest for the purposes of the experiment are the detection threshold, the acquisition frequency and the output data format.

3.2.2 Si(Li) tracker module

As can be appreciated in Figure 3.8, the complete Si(Li) tracker module comprises the following components, as discussed in Chapter 2.

- A front-end board, presented in Section 2.1, which in the specific case of module No. 238, is FEB No. F202I from the Italian production.
- Two front-end board shields, described in Section 2.5, installed above the FEB by means of screws. Each module involves the use of one type A and one type B shield, that in this case are No. S019AP and No. S019BP.
- A metal scaffold placed centrally to the module above the FEB, which makes up the metal frame in which the module is housed.
- A thermal pad, not visible in the figure, placed between the FEB and the

Experiment setup

metal frame in order to act as a heatsink for the ASIC and guarantee cooling by means of a specially designed cooling system.

- Four circular Si(Li) detectors, each divided into 8 strips and connected via wire bonding to the FEB.

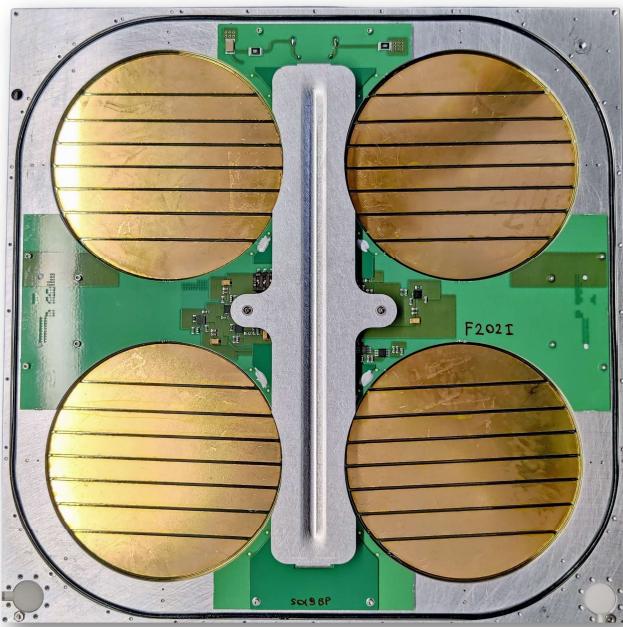


Figure 3.8: GAPS Si(Li) tracker module No. 238 mounting the FEB No. F202I from the Italian production.

The fully assembled tracker module shown in Figure 3.8, being equipped with four Si(Li) detectors, must be kept in a humidity-controlled environment, in order to avoid damage to the detectors. To do this, a portable microcontroller platform, called *Winter*, developed by the Microelectronics Laboratory of the University of Bergamo and shown in Figure 3.9, was used, as it is equipped with multiple environmental sensors, including an hygrometer, a thermometer and a barometer.

The latter was placed together with the tracker module inside an airtight case in which desiccant bags were located, thus guaranteeing a low level of humidity and preventing damage to the Si(Li) detectors. The device, equipped with a Bluetooth Low Energy (BLE) v4.1 connection, was used to transmit humidity data at regular intervals, 24 hours a day, to a Raspberry Pi on which a Python script was run in order to acquire the values and save them to a file in csv format. The code can be found on GitHub at the following [link](#).

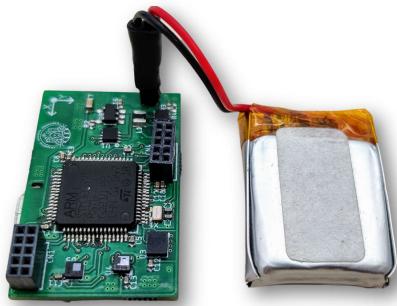


Figure 3.9: *Winter* platform connected to a 3.7 V 240 mAh lithium-ion battery.

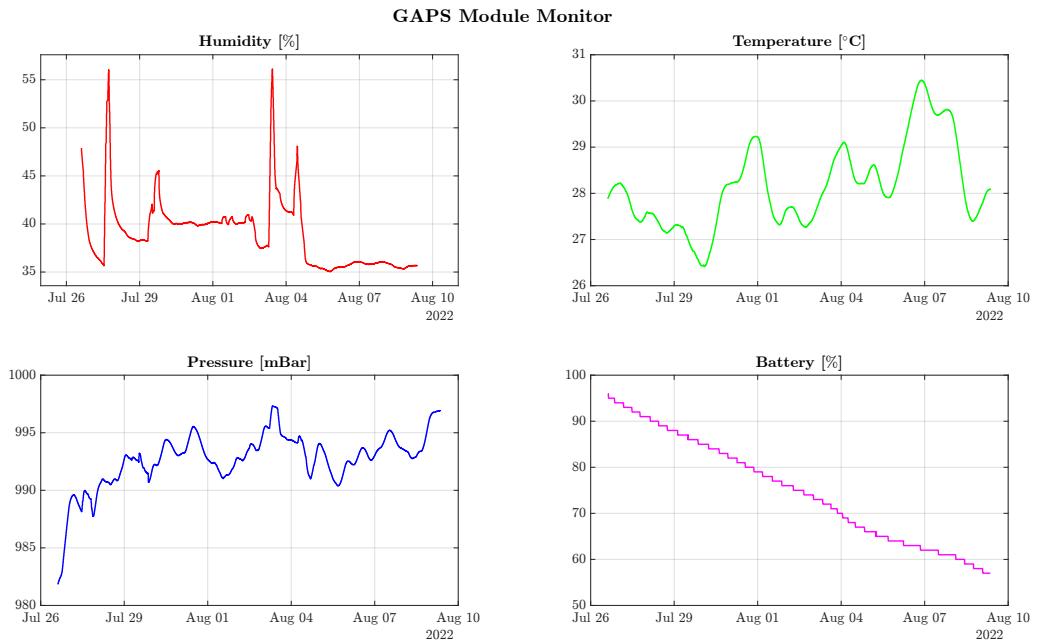


Figure 3.10: GAPS Module Monitor dashboard.

For this application, the Winter platform was programmed to transmit data every 15 minutes in a one minute-long stream in order to achieve the lowest possible energy consumption, while maintaining a sufficiently representative statistic of the internal state of the box. In fact, the device is kept in a *sleep* state for the entire time interval during the course of which no data is transmitted, and all peripherals on board the platform are kept switched off. In this state, the STM32L475R microcontroller that the device is equipped with is in a low power consumption mode called "stop mode 2" and counts the elapsed time through the Real-Time Clock (RTC) module. Once the 15-minute count is reached, the latter is used as an interrupt to bring the platform back from the sleep state to the *idle* state. In this state, the device was programmed

Experiment setup

to transmit environmental data for 1 minute, then return to the sleep state. The complete firmware code can be found on GitHub at the following [link](#).

In addition to humidity data, temperature, pressure and battery level values were also acquired. The latter parameter is of fundamental importance to check the state of the battery and determine in advance when to replace it for recharging, while the humidity data was used to check the status of the desiccant bags, thus allowing to know when to replace them in order to guarantee a constant humidity level as low as possible. The data acquired by the Winter platform via the Raspberry Pi device is finally sent to a PC, on which it is plotted, as shown in Figure 3.10.

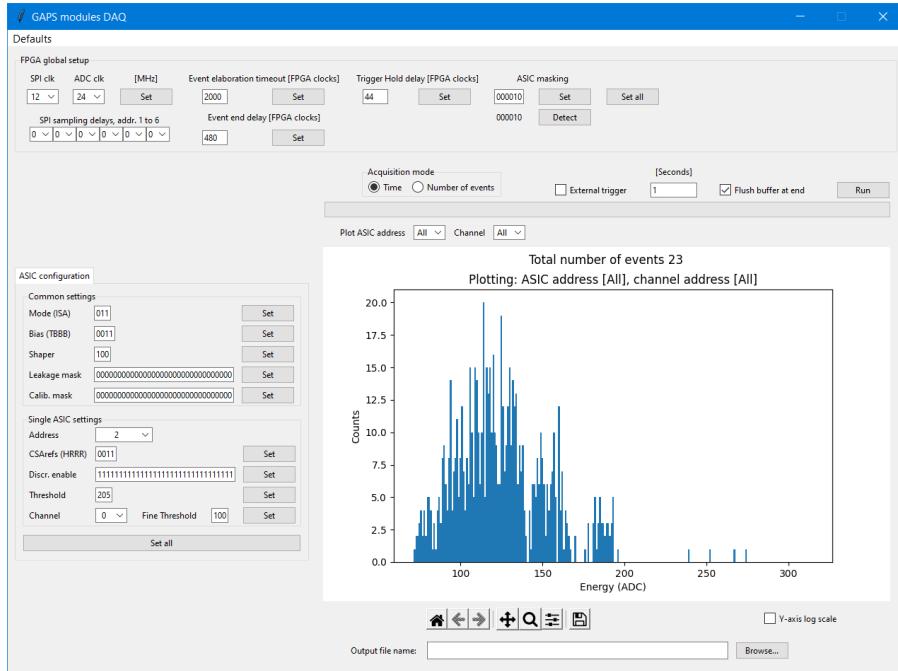


Figure 3.11: GAPS_DAQ Python software GUI used to perform data acquisition from the Si(Li) tracker module.

Data acquisition from the readout electronics of the Si(Li) tracker module was performed via the GAPS_DAQ version 3 application, whose main graphical user interface is shown in Figure 3.11. The software also allows the setting of the electronics and FPGA parameters, summarised in Table 3.1, which were varied for specific data acquisition sessions and subsequently reported, the results of which are shown in Section 3.3.3.

Parameter	Value	Description
Mode (ISA)	010	Self trigger mode with Zero Suppression
	011	Self trigger mode without Zero Suppression
	001	External trigger mode without Zero Suppression
Bias (TBBB)	0110	Gloabal bias regulation
CSArefs (HRRR)	0011	H set to 0, test performed at -40°C
Shaper	100	Peaking time #4 ($\tau_p = 0.98 \mu\text{s}$)

Table 3.1: Main GAPS_DAQ parameters settings used during data acquisition. Other parameters were kept at their default value, provided by the application.

3.3 Experimental results

This Section presents the experimental results obtained during the readout electronics test, reported in Section 3.3.1, and subsequently during the cosmic muon detection experiment, the results of which are reported in Section 3.3.3.

3.3.1 Module characterisation

In this Section, the tests performed on the readout electronics of the Si(Li) tracker module using the *Automated test* of the `GAPS_ModuleTester` software are presented. The purpose of these measurements, which were carried out prior to the muon detection experiment, is to verify the correct functioning of the readout electronics installed inside the assembled module equipped with Si(Li) detectors and it represents the last step in the process of testing the Si(Li) tracker readout electronics illustrated in this thesis work. The Si(Li) detectors were biased with a voltage of -250 V and bit H was set to 0.

Figure 3.12 shows the input-output trans-characteristics of all channels at peak time #6 ($\tau_p = 1.48 \mu\text{s}$). It can be seen that all channels respond correctly and follow the desired trend defined by the dynamic signal compression feature already illustrated in Section 1.3.

Figure 3.13 shows the average input-output trans-characteristics calculated over all 32 channels for each of the 8 selectable peaking times. Also in this case, the trend of the transfer function is comparable to the desired one.

Figure 3.14 shows the measured time response of the time-invariant filter for an emulated input particle energy of 841 keV. The response was derived for all 8

Experimental results

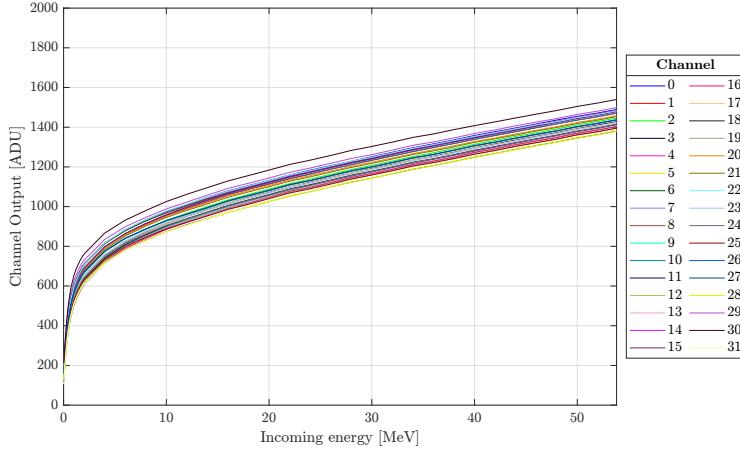


Figure 3.12: Input-output trans-characteristics of all channels at peaking time #6 ($\tau_p = 1.48 \mu\text{s}$) with module at -40°C , Si(Li) detectors biased at -250 V and bit H set to 0.

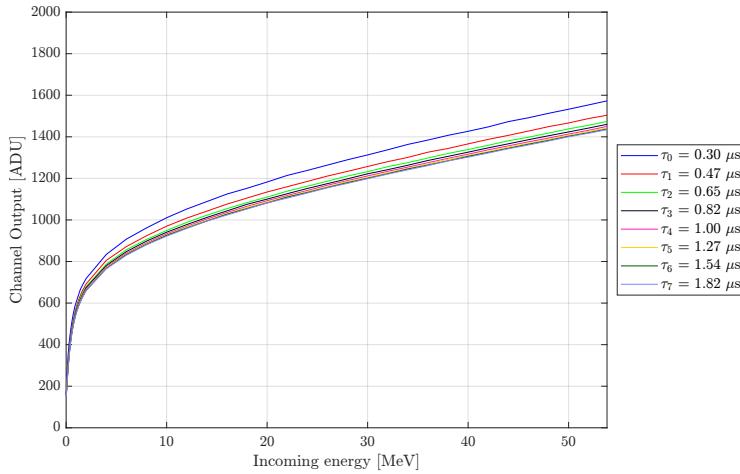


Figure 3.13: Mean input-output trans-characteristics of all channels at all the selectable peaking times with module at -40°C , Si(Li) detectors biased at -250 V and bit H set to 0.

selectable peaking times. Again, the response of the shaper filter is consistent with the simulations and with the measurements carried out first on the ASIC alone via test board, illustrated in Chapter 1, and then on the FEB tested in Chapter 2.

Figure 3.15 shows the ENC graph evaluated for all 32 channels at each of the 8 selectable peaking times. From the measurements made on the ASIC alone and illustrated in Figure 1.20 (on the right), it can be seen that the 8 channels on which an equivalent number of 40 pF capacitors were mounted to simulate the detector strips, demonstrate a lower ENC value than that measured on the assembled module. This could be related to the measurement setup, which for the tests on the ASIC

X-ray and particle detection with an assembled Si(Li) tracker module

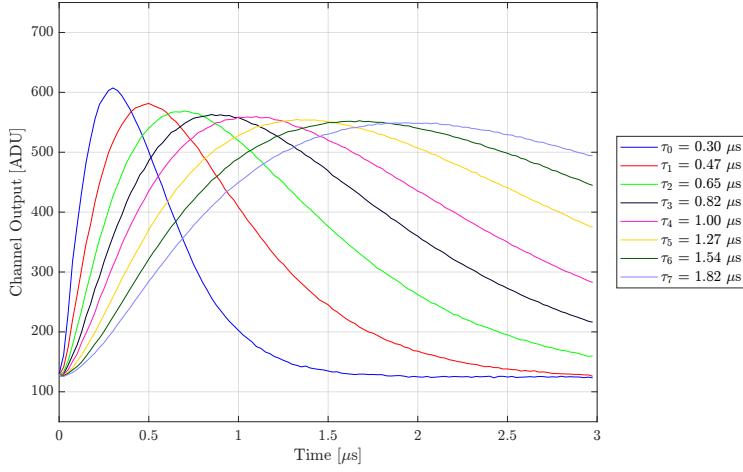


Figure 3.14: Measured time response of the time-invariant filter for an emulated input particle energy of 841 keV and for the 8 selectable peaking times with module at -40°C , Si(Li) detectors biased at -250 V and bit H set to 0.

involved the use of a metal box to shield electromagnetic interference present in the test environment. In contrast, the module was tested by placing it in the climatic chamber without any shielding, as it will be during flight.

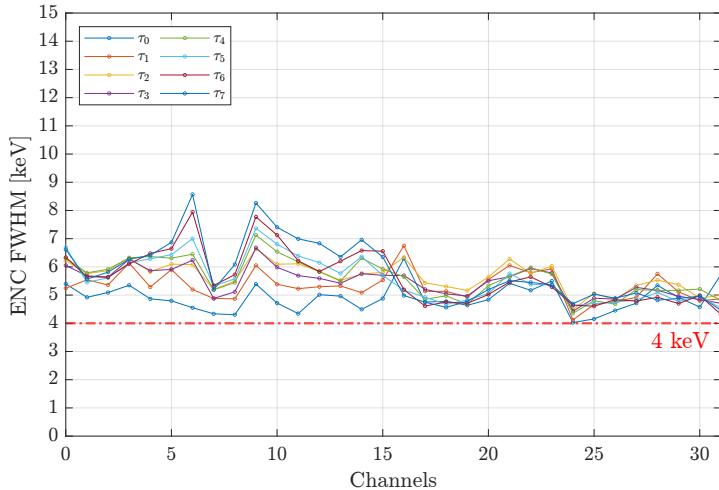


Figure 3.15: ENC without external interference evaluated with module at -40°C , Si(Li) detectors biased at -250 V and bit H set to 0.

The leakage current associated with Si(Li) detectors was also evaluated. The measurement was carried out at a constant temperature of -40°C using the *manual test* provided by the `GAPS_ModuleTester` software already presented in Section 2.1. The software outputs a text file containing 1000 acquisitions of the leakage current value reported in ADU, as obtained at the output of the ADC located in the portion

Experimental results

of the circuit dedicated to both temperature and leakage current measurements. In order to activate the latter mode of operation, bit I of the ISA triplet must be set to 1. The conversion from ADU to Ampere is carried out by means of the following formula, which takes into account the design parameters associated with the circuit used to measure the leakage current:

$$I_{leakage} = \frac{(1024 - ADC_{code}) \cdot 1.72 \text{ mV}}{3.87 \cdot 10 \cdot R} \quad (3.1)$$

where ADC_{code} is comprised between 0 and 2047 ADU, 1.72 mV represents the ADC *Least Significant Bit* (LSB), 3.87 is the gain of the S&H, 10 is the gain of the current mirror implemented in the measuring circuit and R equals to 223.7 k Ω . The latter parameter represents the value of the resistor employed for the conversion from current to voltage that is then sampled by the S&H and later digitised by the ADC.

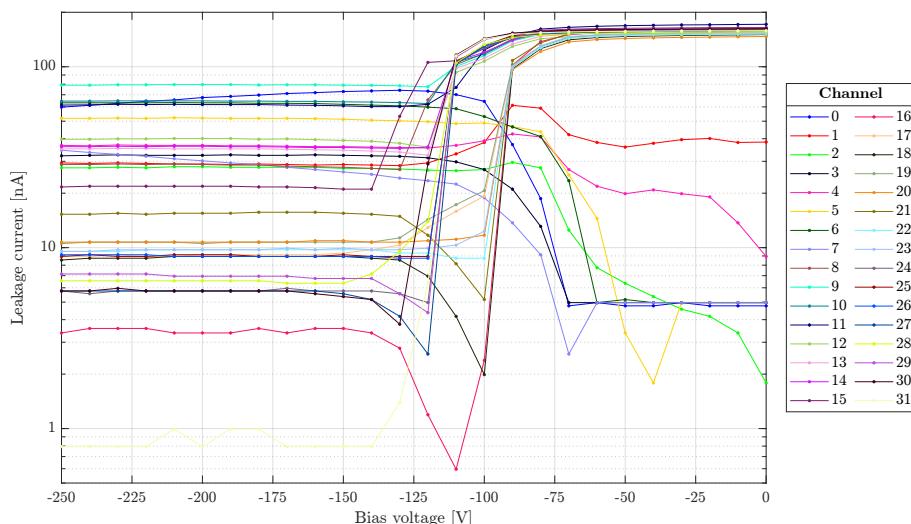


Figure 3.16: Si(Li) detectors leakage current measured for all 32 channels at a constant temperature of -40°C for detector biasing voltage comprised between 0 V and -250 V .

From the graph in Figure 3.16, it can be seen that the leakage current decreases for most channels as the nominal value of the detector bias voltage set at -250 V is reached.

In order to better study the leakage current value of each of the 32 channels at the operating voltage of -250 V , the graph in Figure 3.17 shows its trend as a function of channel. It can be seen that the first 16 channels (between 0 and 15) take on average 10 times more leakage current than the last 16 channels (between 16 and 31). In these channels, the highest leakage current value per individual channel is

also measured, amounting to 71.13 nA for channel 9. In contrast, the lowest leakage current value was measured in channel 31 and evaluated at 1.59 nA.

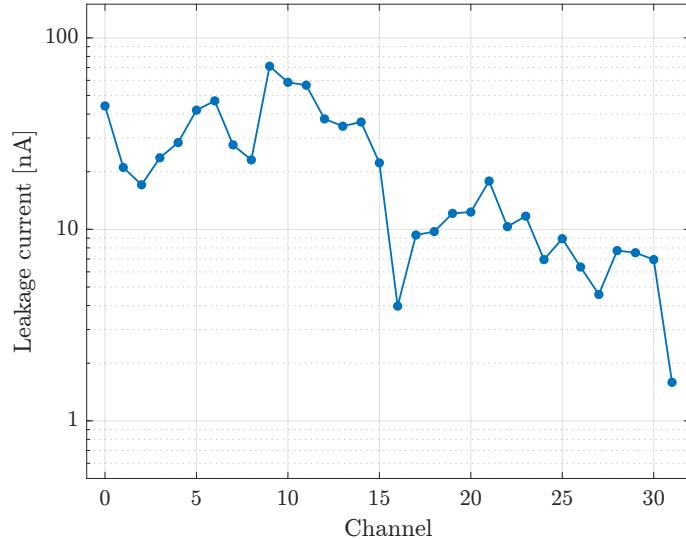


Figure 3.17: Si(Li) detectors leakage current measured for all 32 channels at a constant temperature of -40°C for detector biasing voltage fixed to -250 V .

This behaviour can be explained by taking into account the fact that each of the detectors mounted within the Si(Li) tracker module under investigation has its own peculiar characteristics that can induce quite natural variations in the leakage current value. Overall, the total leakage current on all 32 channels was evaluated at 746.11 nA and is comparable to the value read directly from the high voltage power supply used during the test.

3.3.2 X-ray detection

As a final procedure for characterising the module, an experiment was carried out using a sample of Americium 241, commonly referred to as ^{241}Am . The latter is a man-made radioactive isotope with a half-life of 432.2 years and is usually found in smoke detectors. The source is an alpha emitter, and in the decay process it also kicks out gamma radiation at 59.54 keV and 26.34 keV [16]. A sample of Americium 241 was placed below Si(Li) detector #0 (channels 0 to 7).

In order to determine the best threshold level to be set on these channels with the aim of detecting at least the 59.54 keV peak, a charge scan was first performed and it is presented in Figure 3.18 on the left. During this test, the threshold value is kept constant and the value of the injected charge is varied in order to determine

Experimental results

the channel's trigger profile, expressed in trigger probability from 0 % to 100 %. This test was performed using the *manual test* of the **GAPS_ModuleTester** software already described in Section 2.1, in which the injected charge range and step can be specified. For this specific test, the range was set from a minimum of 0 DAC_{unit} to a maximum of 300 DAC_{unit} with steps of 1 DAC_{unit} . Repeated tests led to the selection of a threshold value of 214, whose equivalent energy value can be seen in Figure 3.18 (on the right) for channels 0 to 7 and is equivalent to 22.65 keV on average. On the same graph, the ENC trend evaluated on the corresponding channels is shown in blue.

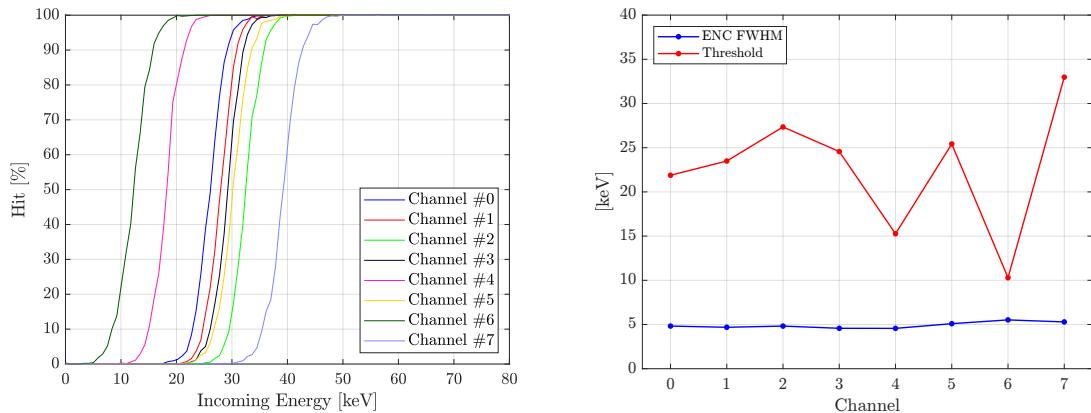


Figure 3.18: Charge scan performed on channels 0 to 7 of detector #0 (on the left) with corresponding ENC and threshold values (on the right).

Both of the previously mentioned parameters were obtained from the charge scan by interpolating the Cumulative Distribution Function (CDF) of the normal distribution reported in Equation (3.2). The mean value (μ) equals to the threshold associated to each channel and corresponds to the charge value that causes the channel to trigger in 50 % of the cases. On the other hand, the FWHM ENC value was obtained by multiplying the corresponding standard deviation (σ) by the *Fano factor*, as reported in Equation (3.3).

$$F(x) = \Phi\left(\frac{x - \mu}{\sigma}\right) = \frac{1}{2} \left[1 + \operatorname{erf}\left(\frac{x - \mu}{\sigma\sqrt{2}}\right) \right] \quad (3.2)$$

$$ENC = \sigma \cdot 2.35 \quad (3.3)$$

The acquisition was carried out for a duration of 1 hour in self-trigger mode with

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peak time no. 4 ($\tau_p = 0.98 \mu\text{s}$) and discriminator enable mask set to 0x0000FF in order to activate only the first 8 channels (channel 0 to 7) belonging to detector #0. As can be seen from the graph in Figure 3.19, in addition to the peak associated with the pedestal, there is first of all a peak at approximately 59 keV. It is also possible to observe the classic *Compton shoulder* (also called *Compton edge*) arranged approximately between the first peak and a second one positioned at about 26 keV. As mentioned above, both peaks can be associated with those present in the emission spectrum of Americium 241 caused by gamma decays.

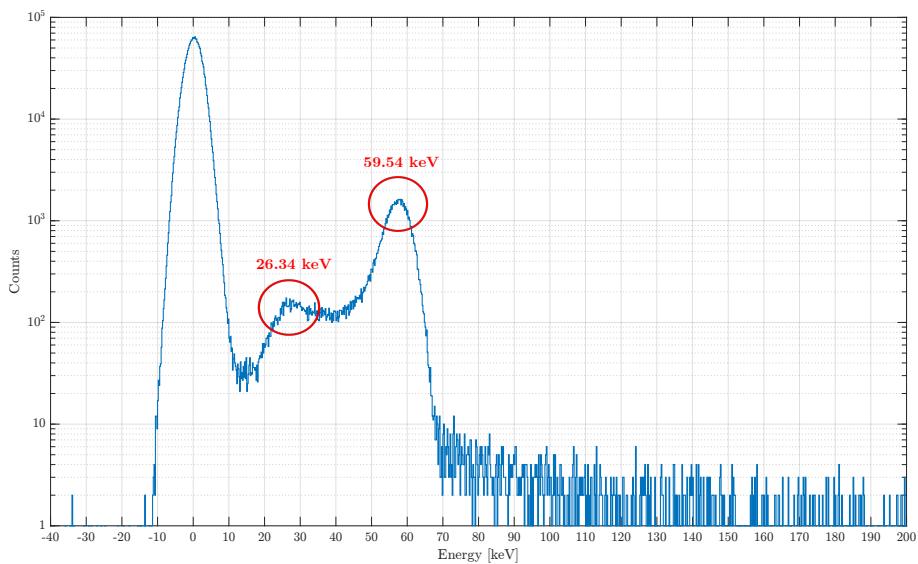


Figure 3.19: Self trigger acquisition carried out using the ^{241}Am sample with global threshold set to 214 and channels 0 to 7 enabled (detector #0).

As highlighted by the estimation of the threshold value associated with channels 0 to 7 (detector #0), it is possible to show how this latter parameter varies around the mean value reaching values higher than the lowest energy peak recorded around 26.34 keV, which would ideally make it impossible to measure. The explanation for this is linked to the presence of channels firing at lower energies, such as channel 6, whose threshold is 10.29 keV, thus making it possible to measure this second peak as well.

This phenomenon can be seen in Figure 3.20, which shows on the left the measurement made on channel 6 alone, in which the peak at 26.34 keV is visible. On the contrary, the energy spectrum recorded on channel 7 is presented on the left, which, having a threshold of 32.98 keV, does not record the lowest energy peak, measuring only that at 59.54 keV.

Experimental results

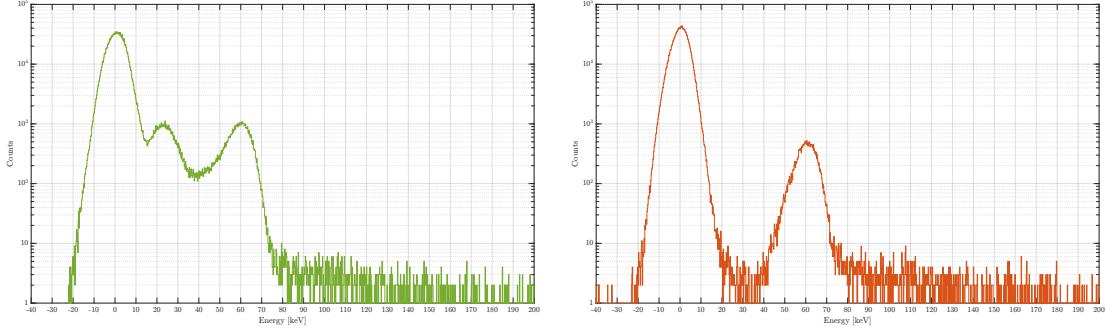


Figure 3.20: Self trigger acquisition carried out using the ^{241}Am sample with global threshold set to 214 on channel 6 (on the left) and on channel 7 (on the right).

3.3.3 Cosmic muon detection

This Section reports the results obtained during the muon detection experiment. Data acquisition was performed with the ASIC operated both in self-trigger mode, in which the sampling signal is generated internally starting from the information provided by the zero-crossing discriminator output signal, and in external trigger mode. In the latter mode, the trigger signal is provided by the *ArduSiPM* device, previously illustrated in Section 3.2.1, at the moment when an interaction event is recorded in the scintillator located below one of the sensors.

Figure 3.21 shows in blue the result of the acquisition performed for a duration of 1 hour in self-trigger mode with global threshold set to 100. The plot also shows a comparison with the measurements carried out by INFN (*Istituto Nazionale di Fisica Nucleare*) Napoli, in red, and MIT (*Massachusetts Institute of Technology*) in green. It can be seen that both the low and high energy peaks, representing noise and muons respectively, are in correspondence with those recorded by the first two measurements.

On the other hand, Figure 3.22 shows the same plot illustrated above (in blue) overlaid in red with the measurement carried out under the same conditions but with the Zero Suppression (ZS) feature activated. The latter represents a channel reading mode where the output of the channel, sampled by the ADC, can be read with the dedicated read procedure only if the SOT comparator output of that channel is 1 (namely, if the shaper output is higher than the set threshold).

The same representation of the acquisition carried out in self trigger mode with zero suppression channel readout mode activated is shown in Figure 3.23, in which it is presented on a linear scale and not logarithmic as previously done. Superimposed

X-ray and particle detection with an assembled Si(Li) tracker module

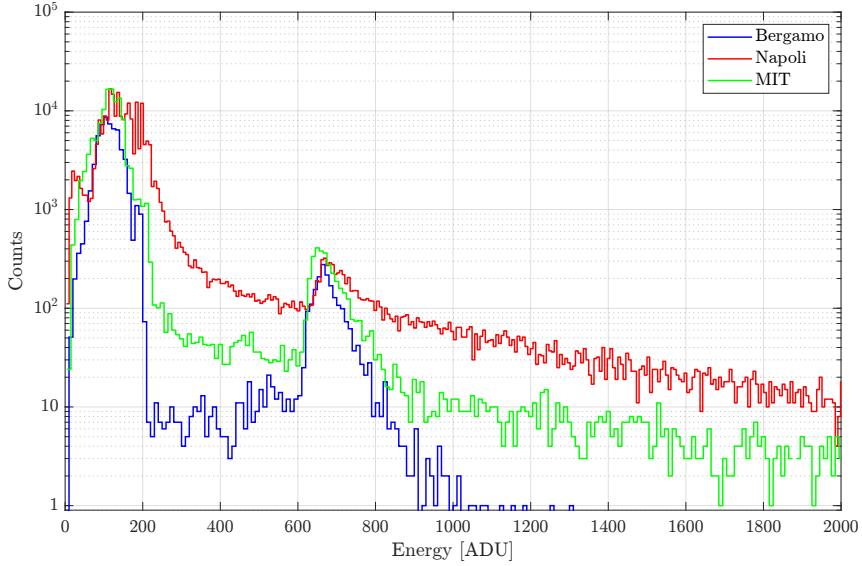


Figure 3.21: Self trigger acquisition with global threshold set to 100 (in blue) compared to acquisitions performed by INFN Napoli (in red) and MIT (in green).

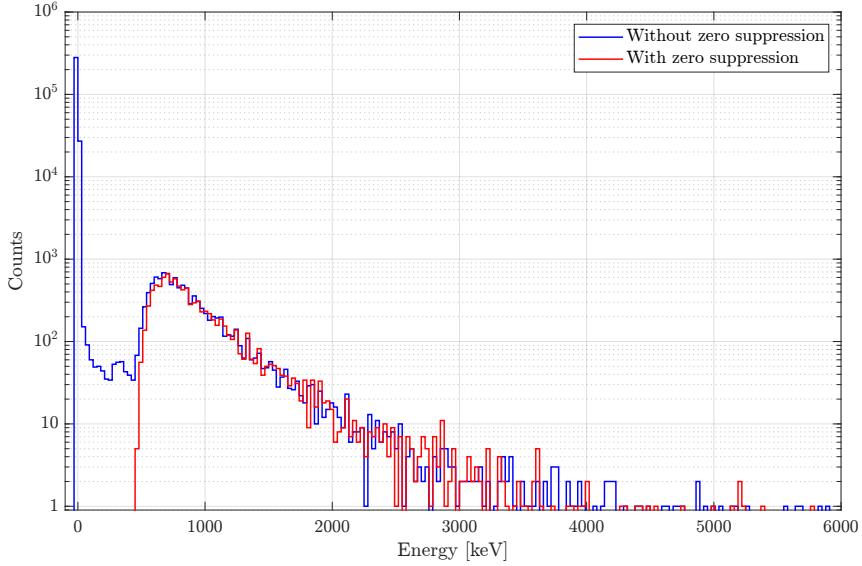


Figure 3.22: Self trigger acquisition with global threshold set to 130 without zero suppression (in blue) and with zero suppression (in red).

on the same plot in green is the profile of the *Landau* distribution, which almost perfectly traces the trend of the underlying data. The latter represents the distribution of energy lost by ionization of a charged particle in a thin layer of matter, that in this case is represented by the Si(Li) detector on which muons impact.

The most interesting result of the entire experiment is represented in Figure 3.24, which depicts the energy spectrum at the input of each of the 4 Si(Li) detectors,

Experimental results

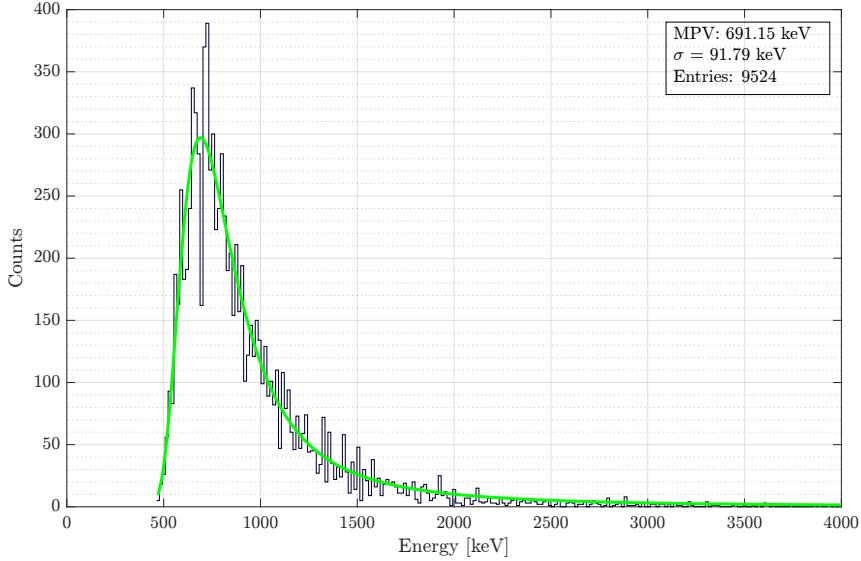


Figure 3.23: Self trigger acquisition with global threshold set to 130 and zero suppression following the Landau distribution highlighted in green.

with detector 2 (channels 16 to 23) highlighted in red, i.e. the Si(Li) detector below which the scintillator was placed.

The acquisition represented by the plot was carried out in external trigger mode and lasted 2 hours. The global threshold was set to 130 and the trigger hold delay was set to 34 FPGA clocks. The latter parameter was estimated experimentally through tests, and is described below. It can be seen that in all 4 detectors there is a low-energy peak representing noise (the pedestal), as the detection was carried out without zero suppression. The interesting result, however, can be seen in channels 16 to 23 highlighted in red. In them, a higher energy peak is visible, roughly between 400 ADU and 800 ADU, representing the energy released by cosmic muons as they pass through the Si(Li) detector strips. This behaviour serves as a proof of concept of the operating principle on which the entire GAPS experiment is based, demonstrating how a scintillator placed at a known distance from the Si(Li) detector is able to intercept cosmic muons, allowing the energy released in the Si(Li) detector to be measured by the readout electronics, as implemented in the experiment with the Time Of Flight (TOF) system, described in Appendix A.2. A 32-channel representation of the same acquisition in which the phenomenon can be observed for each individual channel is available in Appendix C.

The graph in Figure 3.25 shows in pink the histogram associated with the acquisition performed in external trigger mode superimposed on the equivalent acquisition

X-ray and particle detection with an assembled Si(Li) tracker module

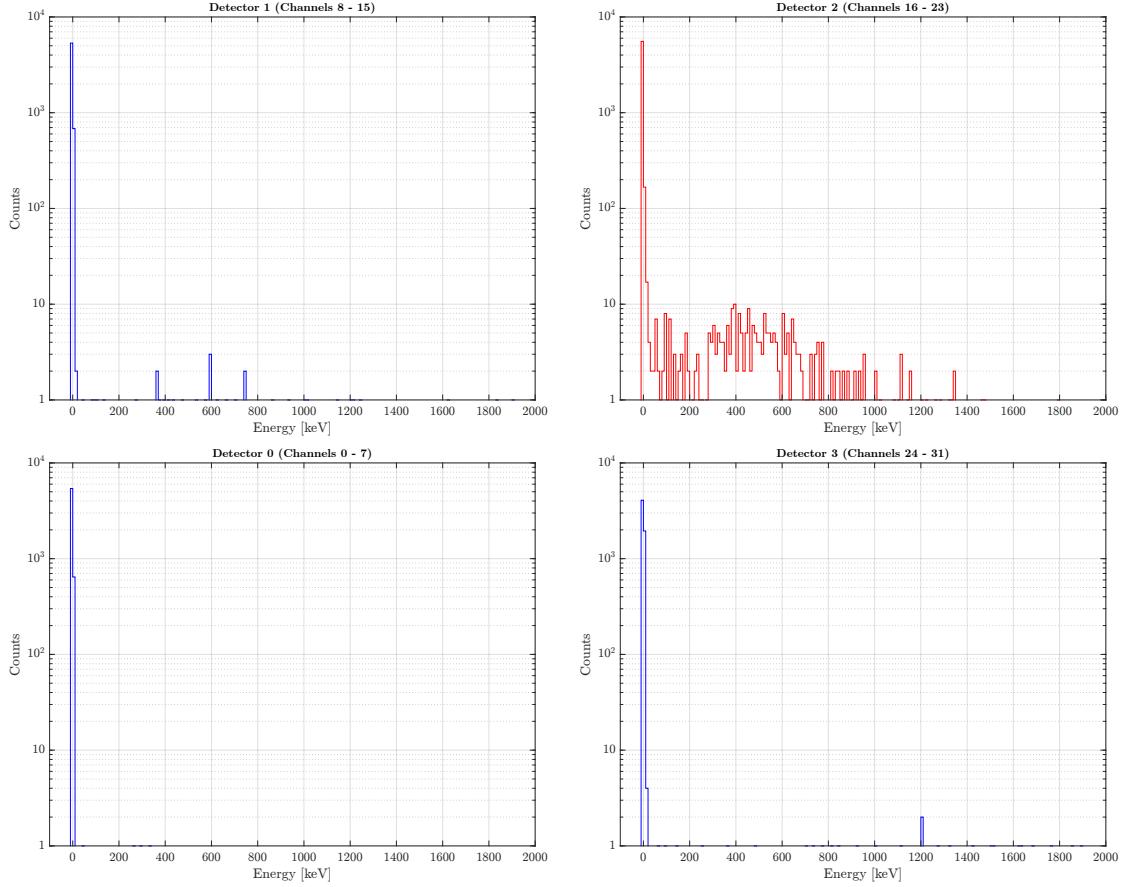


Figure 3.24: 4 Si(Li) detectors view of a two-hour acquisition performed in external trigger mode with global threshold set to 130 and trigger hold delay set to 34 FPGA clocks. Channels from 16 to 23 are highlighted in red.

performed in self-trigger mode, considering in both cases the sum of the interaction events on all 32 channels. It can be seen that the energy peak in the muon region is lower in the external trigger measurement than in the self-trigger one.

This phenomenon can be interpreted in two ways: first, the explanation could be associated therewith a geometrical aspect concerning the positioning of the scintillator with respect to the Si(Li) detector. In fact, the use of a single scintillator positioned below the sensor at a distance of 4 to 5 cm could result in the interaction with the scintillator of incident muons at an angle to the vertical greater than zero. This would result in the release of energy spread over several strips, so that a lower energy per strip is measured. To solve this problem, it would be necessary to use a second scintillator placed at a known distance from the first one, so that the trigger signal would be generated when an interaction event occurs on both scintillators. Such a device, based on the operating principle of a telescope, would make it pos-

Experimental results

sible to uniquely identify the interaction of vertically interacting muons with the Si(Li) detector, thus removing readings from the interaction with muons reaching the sensor at an angle from the vertical greater than zero.

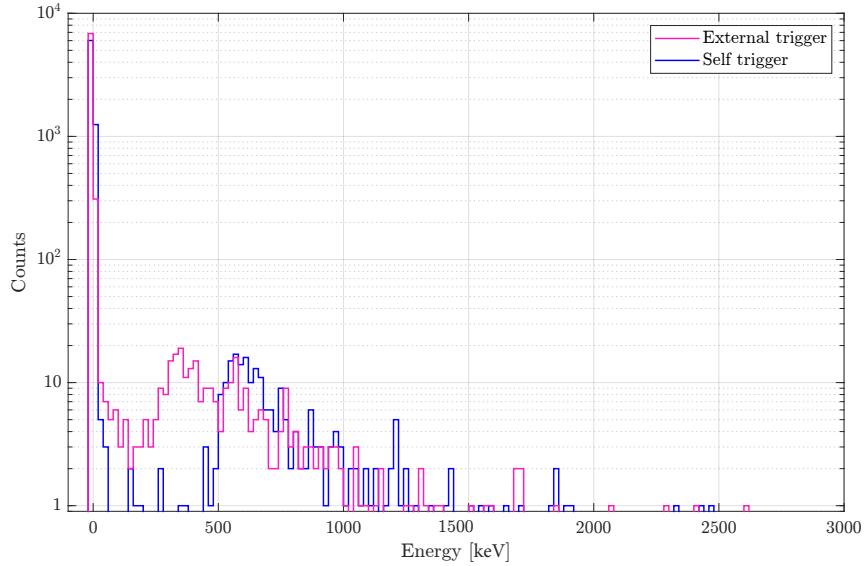


Figure 3.25: Comparison between self trigger mode (in blue) and external trigger mode (in pink); both self and external trigger acquisitions were performed with global threshold set to 130 and trigger hold delay set to 34 FPGA clocks.

A second hypothesis could be related to the time required for the ArduSiPM detector to generate the trigger signal. Indeed, it is possible that the time required for the detector to generate the trigger signal from the interaction event recorded in the scintillator is too long for the sample-and-hold circuit to sample the channel at the point of maximum signal output from the shaper filter. For this purpose, various delay values were evaluated, a parameter known as *trigger hold delay*, which in the specific case of this test was set to 34 FPGA clocks. This parameter can be defined via the `GAPS_DAQ` Python software and represents the delay, measured in FPGA clocks, that elapses from the acquisition of the trigger signal to the moment when the channel is actually sampled. With this trigger hold delay value, sampling may not occur at the maximum point of the signal output from the shaper, resulting in a lower recorded energy value than measured in self-trigger mode.

Unfortunately, it was not possible to measure by means of an oscilloscope the delay between the recording of the interaction event on the scintillator and the moment when the trigger signal is generated by the ArduSiPM device, shown in Figure 3.7. It is also possible that even a zero trigger hold delay value is not sufficient

X-ray and particle detection with an assembled Si(Li) tracker module

to ensure that the channel output is sampled at the correct instant, consistent with the set peak time #4 ($\tau_p = 0.98 \mu\text{s}$), if the trigger generation delay is excessively high.

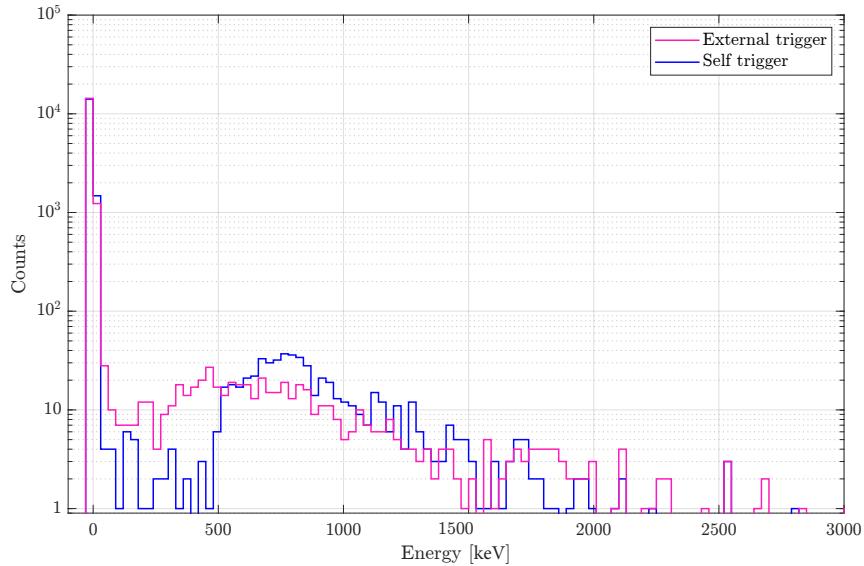


Figure 3.26: Comparison between the measurement made in self-trigger mode (in blue) and that made in external trigger mode by placing the scintillator at a close distance from the Si(Li) detector (in pink).

Further tests showed how the variation of the delay around the value used for the previous measurements varies the position of the muon peak in the external trigger measurements only slightly. On the contrary, it was ascertained how bringing the scintillator closer to the Si(Li) detector, in the order of a few millimetres instead of a few centimetres, resulted in the peak being shifted to higher energy, bringing it closer to that detected in the self-triggered acquisitions, as shown in the histogram presented in Figure 3.26. This leads to the conclusion that the phenomenon is mainly attributable to a geometric rather than a timing issue.

Conclusions

GAPS (General Antiparticle Spectrometer) is an international experiment aimed at detecting antideuterons and other low-energy particles emitted by cosmic rays, since they are considered a promising indirect signature of Dark Matter. The charge released by an incident particle in the GAPS Si(Li) detectors is read out by an Application Specific Integrated Circuit (ASIC) named *SLIDER32*. It is installed on a custom designed Front-End Board (FEB) and it is connected to 4 Si(Li) detectors, housed in a metal frame that comprises the basic module on which the GAPS tracker is based.

The main topics discussed in this thesis work are relevant to the characterisation and experimental evaluation of all flight items that constitute a single Si(Li) tracker module, in order to verify their correct functioning before the final integration of the assembled modules into the flight version of the experiment, that will be completed by the end of 2022.

First, the ASIC in the version intended for flight was successfully tested by means of a custom-designed test board in order to verify its operation at varying temperatures, and the results were consistent with what was predicted by the simulations and observed during the testing of the *pSLIDER32* prototype version of the chip.

The main work was aimed at testing and validating the flight items constituting the tracker, namely FEBs, dummy-1 FEBs, shields, flex-rigid boards and termination connectors. Each of them was tested individually and subjected to validation procedures to verify their correct functioning and adherence to design standards. The validated components were finally shipped to Columbia University in New York and then assembled at the MIT Bates facility in Middleton, Massachusetts.

Finally, an experiment on a complete module equipped with Si(Li) sensors was conducted to validate the operation of the readout electronics using a trigger signal provided by an external scintillator for the purpose of detecting cosmic muons. The results of this last experiment are encouraging and have made it possible to confirm

Conclusions

the soundness of the design choices made at various levels in the development of all components constituting the readout electronics.

Future work includes the implementation of an accurate calibration technique for all Si(Li) tracker modules when the assembly operations currently underway are completed. The calibration procedure will be aimed at precisely defining the correct configuration of the fine threshold values for every channel of each of the tracker modules. In this regard, the measurements carried out in Chapter 3 using both the Americium 241 source and the scintillator for detecting cosmic muons have provided useful information for this purpose and will be extended and studied in greater detail in the future.

Appendix A

The GAPS experiment

A.1 The Dark Matter unsolved issue

The study and understanding of Dark Matter is a broad field of modern physics. Dark Matter is a hypothetical component of matter that, unlike known matter, is unaffected by electromagnetic fields. As a result, it does not absorb, reflect, or emit electromagnetic radiation, making it difficult to detect. This is the origin of the term "Dark Matter". Gravitational effects are the only ones that appear to be related to Dark Matter based on astrophysical observations. In fact, some events are not explainable by the common gravity theories accepted by the scientific community, unless there is more matter than what can be detected through all other physical effects. In the standard Lambda-CDM (Cold Dark Matter) model, based on the Big Bang, Dark Matter has to exist because [17]:

- Galaxies and galaxy clusters could not be created in such a little time starting from the Big Bang calculated instant.
- In the present cosmological scenario (that has only the gravity as a cosmological force) galaxies behaviour cannot be explained considering the visible matter only since it is not able to generate sufficient gravitational force.

Modern measurements indicate that Dark Matter accounts for 86 % of the total mass of the universe. Moreover, in the standard Lambda-CDM model, the total mass-energy of the universe is composed of [18]:

- 5 % ordinary matter and energy,
- 26 % Dark Matter,

- 69 % dark energy.

Dark Matter and dark energy are two different concepts. The sum of the Dark Matter and the dark energy account for 95 % of the total mass–energy content.

Dark Matter identification

Another major issue that researchers are attempting to solve is the identification of Dark Matter. Some experiments seek to directly detect Dark Matter, while others seek to detect the byproducts of its self-annihilation or decay. [18] A brief description of these experiments is presented below.

- **Direct detection experiments:** These experiments attempt to observe the recoils caused by the interaction of Dark Matter passing through the earth with atomic nuclei at very low energies. When Dark Matter passes through special sensitive apparatuses, the particles emit light (scintillators) or phonons (calorimeters). Instruments must be able to differentiate between background particles, which primarily scatter electrons, and Dark Matter particles, which scatter nuclei.
- **Indirect detection experiments:** Experiments of this type attempt to detect the products of self-annihilation or decay of Dark Matter particles in space. In theory, two Dark Matter particles could annihilate in areas with a high density of Dark Matter. In fact, some regions, such as the center of our galaxy, are expected to have a high concentration of Dark Matter. These events are thought to produce gamma rays, Standard Model particle-antiparticle pairs, or Standard Model particles. The main challenge of this type of detection is distinguishing products of Dark Matter annihilation from products of other astrophysical sources [19]. As a result, different types of evidence are required for a conclusive discovery.
- **Collider searches for Dark Matter:** These experiments attempt to recreate Dark Matter particles in special colliders (like the Large Hadron Collider at CERN in Geneva). All collider discoveries must be validated by further direct or indirect tests to prove that the newly discovered particle is indeed Dark Matter.

Because of their unusual sensitivity to annihilating and decaying Dark Matter, cosmic-ray antinuclei (antiprotons, antideuterons, and antihelium) can help researchers

The GAPS experiment

show or reject a variety of Dark Matter ideas. These indirect detections can also be used to avoid or supplement collider, direct, or other cosmic-ray searches. The hunt for cosmic antideuterons is a novel experiment that provides a strong new approach of studying cosmic physics. The antideuteron is distinguished by its extremely low astrophysical backdrop, particularly at low energies. In reality, some Dark Matter theories anticipate antideuteron flow with energies in the order of a few GeV/n [19]. All other sorts of Dark Matter searches often attempt to find other types of particles, such as the positron, at greater energy levels (around 100 GeV). The key challenge for these tests is distinguishing the results of Dark Matter annihilation from other conventional sources of positrons in this energy range.

A.2 The GAPS experiment

The primary goal of the General Antiparticle Spectrometer (GAPS) experiment is the indirect detection of low-energy cosmic-ray antinuclei (below 0.25 GeV) [19]. The experiment consists of 10 layers of semiconducting Si(Li) strip detectors surrounded by a Time Of Flight (TOF) plastic scintillator system on all sides. GAPS is supported by a unique particle identification approach based on exotic atom production and decay [1]. A low-energy antiparticle, slowed by the environment, first travels through the TOF. This enables the collection of preliminary data on particle velocity and energy. When an antiparticle goes through the detector, it loses energy in the Si(Li) detector tracking system and slows down until it stops inside the device. If this occurs, the antiparticle replaces a silicon shell electron, resulting in the formation of an exotic atom in an excited state with a probability close to one. The exotic atom de-excites via auto-ionization and radiative transitions that produce X-rays before annihilating with the silicon nucleus, forming a nuclear star of pions and protons. The antiparticle and silicon decreased mass and atomic numbers determine the X-ray energy in a unique way.

The rejection of the dominating antiproton backdrop is the most difficult challenge in finding antideuterons. The GAPS detector design, on the other hand, allows for the detection of either antiproton or antideuteron cosmic rays. Antihelium signatures can be easily recognised even if the equipment is optimised for antideuteron detection [20]. Because antihelium has a larger charge than antideuterons and antiprotons, its analysis is significantly simpler than the antideuteron-antiproton one.

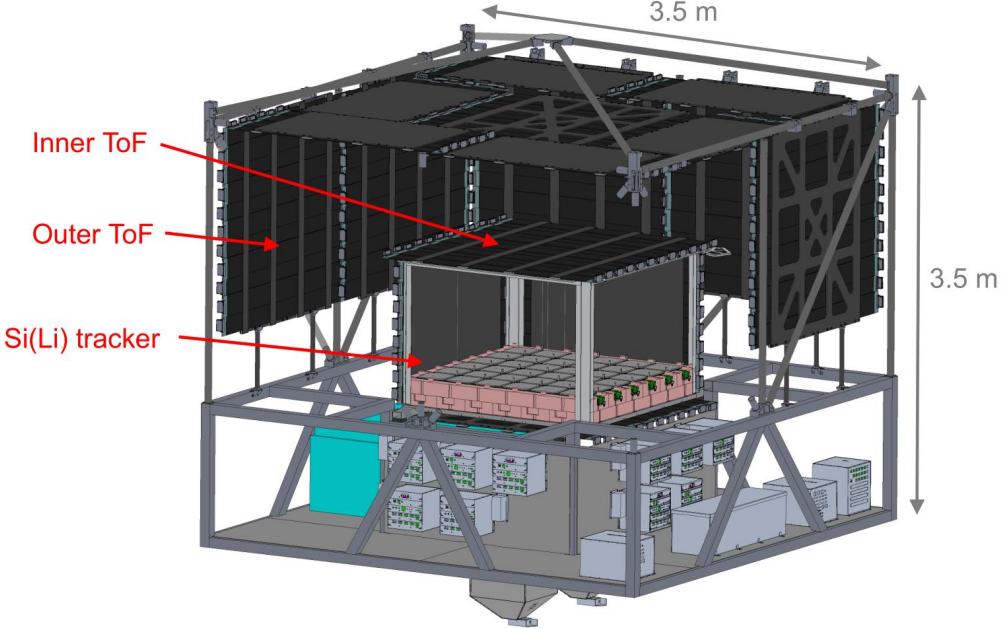


Figure A.1: Complete GAPS tracking system structure.

GAPS tracking system

The GAPS instrument, shown in Figure A.1, is mainly composed of [21]:

- Two external layers of TOF plastic scintillators that surround the inner tracker. The outer TOF dimension are $3.5 \times 3.5 \text{ m}^2$, with an height of 1.5 m. The inner TOF dimension are $1.5 \times 1.5 \text{ m}^2$, with height of 1 m. The distance between the outer TOF and the inner TOF is 1 m. The entire TOF time resolution is about 300 ps [19].
- The inner tracker is subdivided in 10 layers with 10 cm separation in order to achieve 3D particle tracking. Each layer is composed of 12×12 Si(Li) detectors [22]. Each detector has a diameter of 10 cm and a thickness of 2.5 mm. Moreover, each detector is segmented in 8 strips in order to improve the spatial resolution enough to distinguish tracks from incident particles and exotic atom annihilation products. Each strip is then connected to a front-end channel which processes the charge released by the passing particle. The GAPS detectors are capable to detect X-rays ranging from 20 keV to 80 keV and charged particles up to 50 MeV, at an operating temperature of -40°C , with a FWHM energy resolution lower than 4 keV. During flight, the cooling operation will be executed by a passive oscillating heat pipe approach, tested

GAPS front-end

on two prototype test flights [23].

- Each layer of the inner tracker’s circuitry is made up of 6×6 modules. Each module consists of a readout ASIC and a front-end board. Four detectors are linked to a single module. Each ASIC has 32 front-end channels capable of processing signals from 32 strips. The front-end board contains all of the components required to ensure the ASIC’s proper operation. A flex-rigid board, particularly intended for this duty, links two front-end boards for a total of six front-end boards connected on the same line.

A.3 GAPS front-end

SLIDER32 (32 channels Si-LI DEtector Readout) is the final ASIC for the GAPS experiment and contains 32 channels. Each channel is linked to a different detector strip. When an antiparticle goes through one of the GAPS instrument’s strips, it loses energy in each of the Si(Li) detector layers. When it has expended enough energy, it comes to a halt and creates an exotic excited atom. The atom then de-excites and produces X-rays. The nucleus that remains annihilates, producing pions and protons. When an antiparticle travels over a detector strip, it releases a little quantity of charge.

The antiparticle annihilation causes a little quantity of charge to be released in the detector strips. The main purpose of the channel front-end is to analyse the quantity of charge coming from the associated detector strip. This is accomplished by collecting current pulses at the channel’s input and turning them into an analog voltage, which is then digitised using an analog-to-digital converter. It is feasible to deduce which particle travelled through the detector based on these digitised values.

The GAPS front-end channel has been designed with a commercial 180 nm CMOS technology and its block schematic is shown in Figure A.2. The design targets the experiment requirements reported in Table A.1.

A.3.1 Injection circuit

The injection circuit generates a current pulse, whose amplitude is decided by the user, in order to simulate the release of charge due to the passage of particles through the GAPS Si(Li) detector. This block is used only during the test phase, because in the real experiment, the channels will be connected to the detector strips.

Requirement	Value
Temperature	-40 °C
Power consumption	< 10 mW/channel
Input dynamic range	10 keV - 50 MeV
Maximum electronic noise interference	4 keV (FWHM)
Minimum threshold	10 keV
Detector leakage current	max 50 nA @ 27 °C

Table A.1: GAPS ASIC requirements.

An injection capacitor C_{inj} , shown in Figure A.2, is integrated in each channel to generate the current pulse emulating the charge released in the detector.

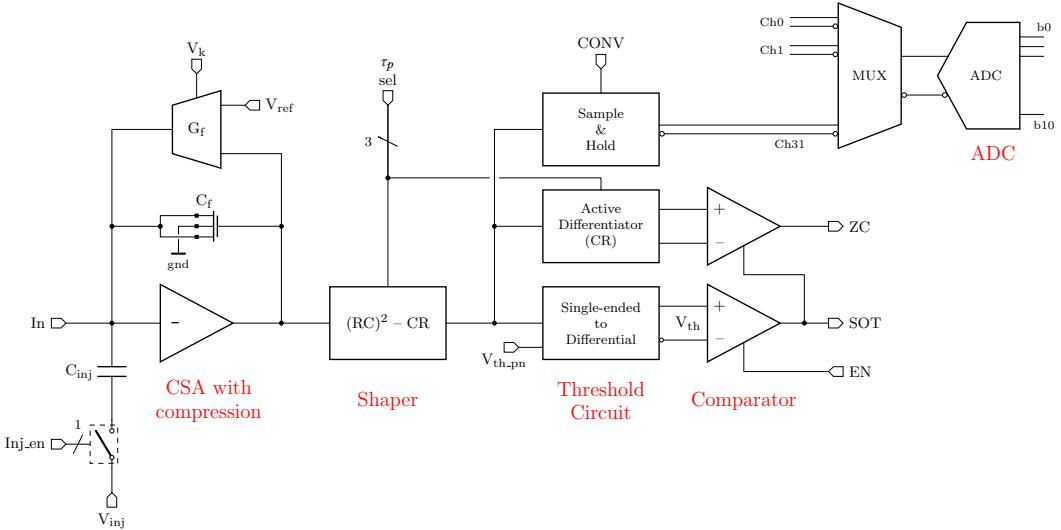


Figure A.2: Front-end channel block schematic.

A.3.2 Charge Sensitive Amplifier with dynamic signal compression

The Charge Sensitive Amplifier is the channel's initial block. The goal of this block is to transform the detector's current pulses into a voltage step whose amplitude is proportional to the area of the current pulse, namely the charge induced by the current pulse. This block's key feature is its input-output trans-characteristic, which is defined by dynamic signal compression. This is a critical feature of the

CSA because, due to the low supply voltage and large number of bits required for this solution, a linear gain was not an option for covering the large energy dynamic range required by the project specifications and maintaining a high resolution in the low energy range.

The CSA is built around an active folded cascode (with local feedback) that is loaded using an active cascode architecture. A continuous time feedback implemented using a Krummenacher network does the reset. The dynamic compression has been performed using the nMOS capacitor C_f .

A.3.3 Time-invariant filter (CR-(RC)²)

The shaper is the second GAPS channel block. The primary purpose of this block is to enhance the Signal-to-Noise ratio in order to achieve the low energy resolution (of 4 keV FWHM). It consists of two stages: One CR (high-pass filter) and two RC (low-pass filters). This block's transfer function is

$$H(s) = \frac{R_2}{R_1} \cdot \frac{1}{1 + s\tau} \cdot \frac{C_2}{C_1} \cdot \frac{s\tau}{(1 + s\tau)^2} \quad (\text{A.1})$$

The shaper output is a unipolar semi-Gaussian waveform, characterized by a peaking time $t_p = 2 \cdot \tau$, where τ is the time constant of the circuit. The peaking time selection (3 bit) is obtained by switching specific capacitors in the architecture. The shaper output introduces a gain of 1.5 almost independent of the peaking time.

A.3.4 Threshold Generator and SOT comparator

The threshold generator is linked to the shaper output. The remaining two inputs are threshold voltages. This block transforms the single-ended signal from the shaping stage's output to a differential signal. To avoid crosstalk, a differential threshold voltage is utilised. The threshold generator's two output signals are:

$$V_{th,out1} = v_{s0} + V_{tp} - \frac{V_{sh}}{2} \quad (\text{A.2})$$

$$V_{th,out2} = v_{s0} + V_{tp} - \frac{V_{sh}}{2} \quad (\text{A.3})$$

where V_{sh} is the shaper output voltage and v_{s0} is a threshold generator bias voltage. The differential signal obtained is

$$\begin{aligned}
V_{th,out1} - V_{th,out2} &= (v_{s0} + V_{tp} - \frac{V_{sh}}{2}) - (v_{s0} + V_{tn} + \frac{V_{sh}}{2}) \\
&= V_{tp} - V_{tn} - V_{sh}
\end{aligned} \tag{A.4}$$

The difference ($V_{tp} - V_{tn}$) can be expressed as V_{th} , which is the SOT comparator differential threshold. The two generated voltages are, in fact, connected to the SOT comparator. Its main goal is to suppress false event caused by noise or disturbances. The comparator fires when

$$V_{th,out2} > V_{th,out1} \tag{A.5}$$

or, more easily, when

$$V_{sh} > V_{th} \tag{A.6}$$

V_{tp} and V_{tn} are created via an 8-bit DAC external to the channels of the SLIDER32 ASIC. These voltages are then routed to each channel's threshold generator. To compensate for process parameter fluctuations in each channel threshold, a 3-bit DAC for fine threshold trimming is added to each of these.

A.3.5 Active CR differentiator and Zero Crossing comparator (ZC)

The differentiator goal is to use a CR filter to extract the shaper output in order to discover the precise shaper peaking moment. When the shaper signal derivative equals zero, the shaper output is at its maximum voltage, i.e. it has reached its peaking time. This block negates the differentiator output and adds a constant voltage of $V_{dd}/2$ to the derivative signal in the process.

This voltage increase avoids the differentiator output from always being 0V if the derivative is less than 0V. This block's output is then connected to the ZC comparator and compared to $V_{dd}/2$ voltage: If it is larger than $V_{dd}/2$, the ZC output becomes a logic 1. This is the point at which the shaper output must be sampled continuously throughout the CONV signal in order to determine the precise injected charge.

The ZC comparator operates only when the SOT comparator voltage is set to logic 1. This is done to readily eliminate erroneous events generated by noise or external disturbances.

A.3.6 Single-ended to differential S&H

When the signal **CONV** changes from logic 0 to logic 1, this block stores the shaper output voltage value. When the front-end is in self-trigger mode, the **CONV** signal is identical to **ZC**; however, when it is not in self-trigger mode, the **CONV** signal must be supplied from an external source.

The sample & hold output is then connected to a multiplexer, and finally to an ADC used to digitise the voltage stored in it. All the blocks signals are shown in Figure A.3 for an incoming energy of 100 keV at -40°C .

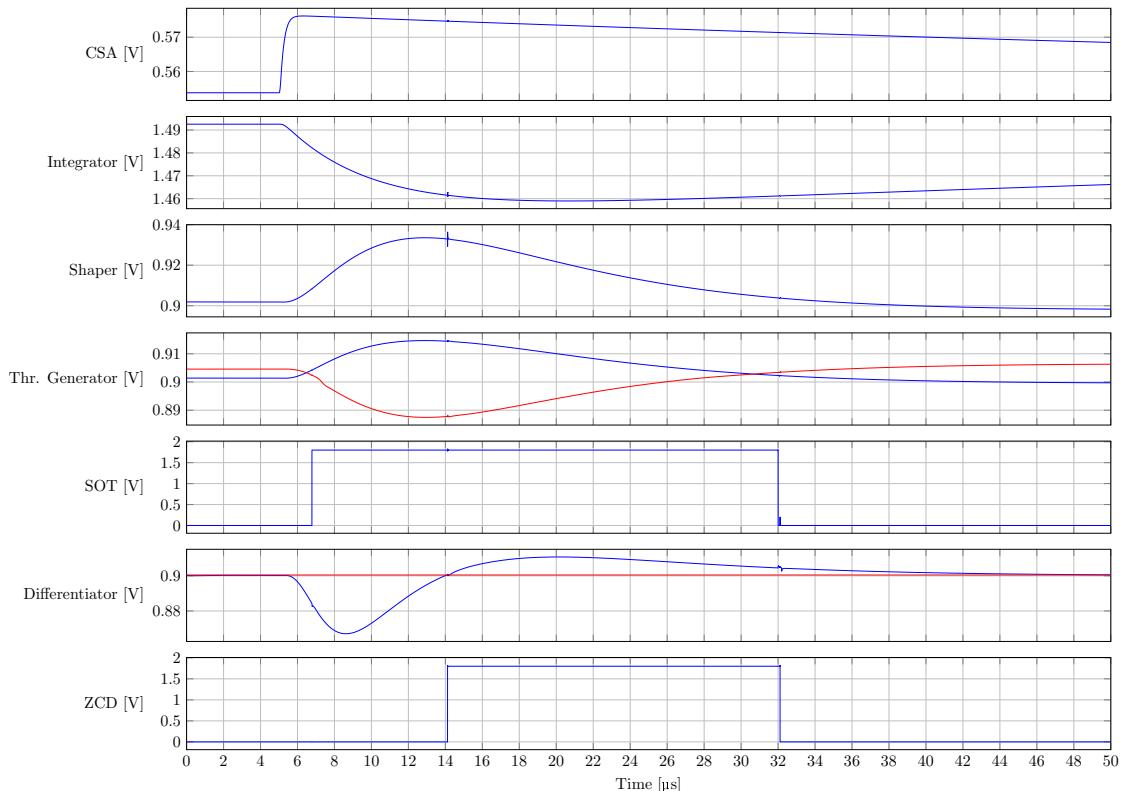


Figure A.3: All channel blocks signals for an incoming energy of 100 keV at -40°C .

Appendix B

Si(Li) tracker flight components test reports

This Appendix shows the test reports generated for each of the flight item categories that were tested. The test reports are listed in the following order:

1. Front-end board
2. Dummy-1 front-end board
3. Flex-rigid board
4. Connector for termination
5. Front-end board shield

Si(Li) tracker flight components test reports

F065I

Board ID	Doc Version	Date	Author	ASIC ID	Production
F065I	0.1	16.04.2022	L. Ghislotti	065	Italian
	#	Test Description	Pass	Note	
Visual	1	Visual inspection	Yes	See notes (if any)	
Bias	2	Analog		Yes	AVDD [V]
				Yes	IVDD [mA]
	Digital			Yes	DVDD [V]
				Yes	IDVDD [mA]
		Calibration		Yes	3V3 [V]
				Yes	I3V3 [mA]
	Bias current			Yes	Ibias [mA]
		Reference Voltages		Yes	VCM SH [V]
				Yes	VCM [V]
				Yes	RVCM [V]
Digital	3	Configuration test	Yes		
		Wrong address test	Yes		
		Temperature Sensor	Yes	ADC	1040
				T [°C]	25.947
Analog	4	Input-output characteristic	Yes	# of non resp. ch	0
	5	Noise ENC FWHM @ tp=6		Yes	Ch 0 [keV]
				Yes	Ch 7 [keV]
				Yes	Ch 15 [keV]
				Yes	Ch 16 [keV]
				Yes	Ch 23 [keV]
				Yes	Ch 31 [keV]
	6	Threshold dispersion @ tp=6		Yes	Before FT [DAC]
				Yes	After FT [DAC]
	7	Pedestal dispersion @ tp=6	Yes	Dispersion [ADC]	

Notes:

solid defect on top
exposed copper on bottom
solid defect on bottom

1/1

Figure B.1: An example of the report that has been generated for every of the FEBs that have been tested. The one shown refers to FEB n. F065I.

DUMMY BOARDS

Doc Version	Date	Author
0.1	28.04.2022	L. Ghislotti

#	Board ID	Thermal cycling	Visual inspection	Communication test	IAVDD [mA]	PAVDD [mW]
1	D01	Yes	Yes	Yes	135.7	379.96
2	D02	Yes	Yes	Yes	135.8	380.24
3	D03	Yes	Yes	Yes	135.7	379.96
4	D04	Yes	Yes	Yes	135.6	379.68
5	D05	Yes	Yes	Yes	135.7	379.96
6	D06	Yes	Yes	Yes	135.8	380.24
7	D07	Yes	Yes	Yes	135.8	380.24
8	D08	Yes	Yes	Yes	135.8	380.24
9	D09	Yes	Yes	Yes	135.7	379.96
10	D10	Yes	Yes	Yes	135.9	380.52
11	D11	Yes	Yes	Yes	135.8	380.24
12	D12	Yes	Yes	Yes	135.6	379.68
13	D13	Yes	Yes	Yes	135.8	380.24
14	D14	Yes	Yes	Yes	135.9	380.52
15	D15	Yes	Yes	Yes	135.8	380.24
16	D16	Yes	Yes	Yes	135.8	380.24
17	D17	Yes	Yes	Yes	135.8	380.24
18	D18	Yes	Yes	Yes	135.7	379.96
19	D19	Yes	Yes	Yes	135.8	380.24
20	D20	Yes	Yes	Yes	135.8	380.24
21	D21	Yes	Yes	Yes	135.9	380.52
22	D22	Yes	Yes	Yes	135.8	380.24
23	D23	Yes	Yes	Yes	135.7	379.96
24	D24	Yes	Yes	Yes	135.8	380.24
25	D26	Yes	Yes	Yes	135.7	379.96
26	D27	Yes	Yes	Yes	135.9	380.52
27	D28	Yes	Yes	Yes	135.8	380.24
28	D29	Yes	Yes	Yes	135.8	380.24
29	D30	Yes	Yes	Yes	135.8	380.24
30	D32	Yes	Yes	Yes	135.7	379.96

1/2

Figure B.2: First page of the report that has been produced for the dummy-1 front-end boards.

FLEX-RIGID BOARDS

Doc Version	Date	Author
0.1	22.04.2022	L. Ghislotti

#	Board ID	Thermal cycling	Visual inspection	Communication test
1	FR001	Yes	Yes	Yes
2	FR002	Yes	Yes	Yes
3	FR003	Yes	Yes	Yes
4	FR004	Yes	Yes	Yes
5	FR005	Yes	Yes	Yes
6	FR006	Yes	Yes	Yes
7	FR007	Yes	Yes	Yes
8	FR008	Yes	Yes	Yes
9	FR009	Yes	Yes	Yes
10	FR010	Yes	Yes	Yes
11	FR011	Yes	Yes	Yes
12	FR012	Yes	Yes	Yes
13	FR013	Yes	Yes	Yes
14	FR014	Yes	Yes	Yes
15	FR015	Yes	Yes	Yes
16	FR016	Yes	Yes	Yes
17	FR017	Yes	Yes	Yes
18	FR018	Yes	Yes	Yes
19	FR019	Yes	Yes	Yes
20	FR020	Yes	Yes	Yes
21	FR021	Yes	Yes	Yes
22	FR022	Yes	Yes	Yes
23	FR023	Yes	Yes	Yes
24	FR024	Yes	Yes	Yes
25	FR025	Yes	Yes	Yes
26	FR026	Yes	Yes	Yes
27	FR027	Yes	Yes	Yes
28	FR028	Yes	Yes	Yes
29	FR029	Yes	Yes	Yes
30	FR030	Yes	Yes	Yes
31	FR031	Yes	Yes	Yes
32	FR032	Yes	Yes	Yes
33	FR033	Yes	Yes	Yes

Figure B.3: First page of the report that has been produced for the flex-rigid boards.

CONNECTORS FOR TERMINATION

Doc Version	Date	Author
0.1	26.04.2022	L. Ghislotti

#	Connector ID	Thermal cycling	Visual inspection	Resistor soldering
1	T01	Yes	Yes	Yes
2	T02	Yes	Yes	Yes
3	T03	Yes	Yes	Yes
4	T04	Yes	Yes	Yes
5	T05	Yes	Yes	Yes
6	T06	Yes	Yes	Yes
7	T07	Yes	Yes	Yes
8	T08	Yes	Yes	Yes
9	T09	Yes	Yes	Yes
10	T10	Yes	Yes	Yes
11	T11	Yes	Yes	Yes
12	T12	Yes	Yes	Yes
13	T13	Yes	Yes	Yes
14	T14	Yes	Yes	Yes
15	T15	Yes	Yes	Yes
16	T16	Yes	Yes	Yes
17	T17	Yes	Yes	Yes
18	T18	Yes	Yes	Yes
19	T19	Yes	Yes	Yes
20	T20	Yes	Yes	Yes
21	T21	Yes	Yes	Yes
22	T22	Yes	Yes	Yes
23	T23	Yes	Yes	Yes
24	T24	Yes	Yes	Yes
25	T25	Yes	Yes	Yes
26	T26	Yes	Yes	Yes
27	T27	Yes	Yes	Yes
28	T28	Yes	Yes	Yes
29	T29	Yes	Yes	Yes
30	T30	Yes	Yes	Yes
31	T31	Yes	Yes	Yes
32	T32	Yes	Yes	Yes
33	T33	Yes	Yes	Yes

1/2

Figure B.4: First page of the report that has been produced for the termination connectors.

Si(Li) tracker flight components test reports

SHIELDS				
#	Board ID	Thermal cycling	Visual inspection	Note
1	S001AP	Yes	Yes	
2	S001BP	Yes	Yes	
3	S002AP	Yes	Yes	
4	S002BP	Yes	Yes	
5	S003AP	Yes	Yes	
6	S003BP	Yes	Yes	
7	S004AP	Yes	Yes	
8	S004BP	Yes	Yes	
9	S005AP	Yes	Yes	
10	S005BP	Yes	Yes	
11	S006AP	Yes	Yes	
12	S006BP	Yes	Yes	
13	S007AP	Yes	Yes	
14	S007BP	Yes	Yes	
15	S008AP	Yes	Yes	
16	S008BP	Yes	Yes	
17	S009AP	Yes	Yes	
18	S009BP	Yes	Yes	
19	S010AP	Yes	Yes	
20	S010BP	Yes	Yes	
21	S011AP	Yes	Yes	
22	S011BP	Yes	Yes	
23	S012AP	Yes	Yes	
24	S012BP	Yes	Yes	
25	S013AP	Yes	Yes	
26	S013BP	Yes	Yes	
27	S014AP	Yes	Yes	
28	S014BP	Yes	Yes	
29	S015AP	Yes	Yes	
30	S015BP	Yes	Yes	
31	S016AP	Yes	Yes	
32	S016BP	Yes	Yes	
33	S017AP	Yes	Yes	

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Figure B.5: First page of the report that has been produced for the front-end board shields.

Appendix C

External trigger data acquisition: 32-channels view

This Appendix provides the 32-channel view of the data acquisition session that has been performed in external trigger mode by using a scintillator placed underneath detector #2 (Channels 16 to 23) already illustrated in Figure 3.24 in Chapter 3. The y-axis reports the number of events from 1 to 10^4 and the x-axis reports the energy of the recorded events expressed in keV.

External trigger data acquisition: 32-channels view

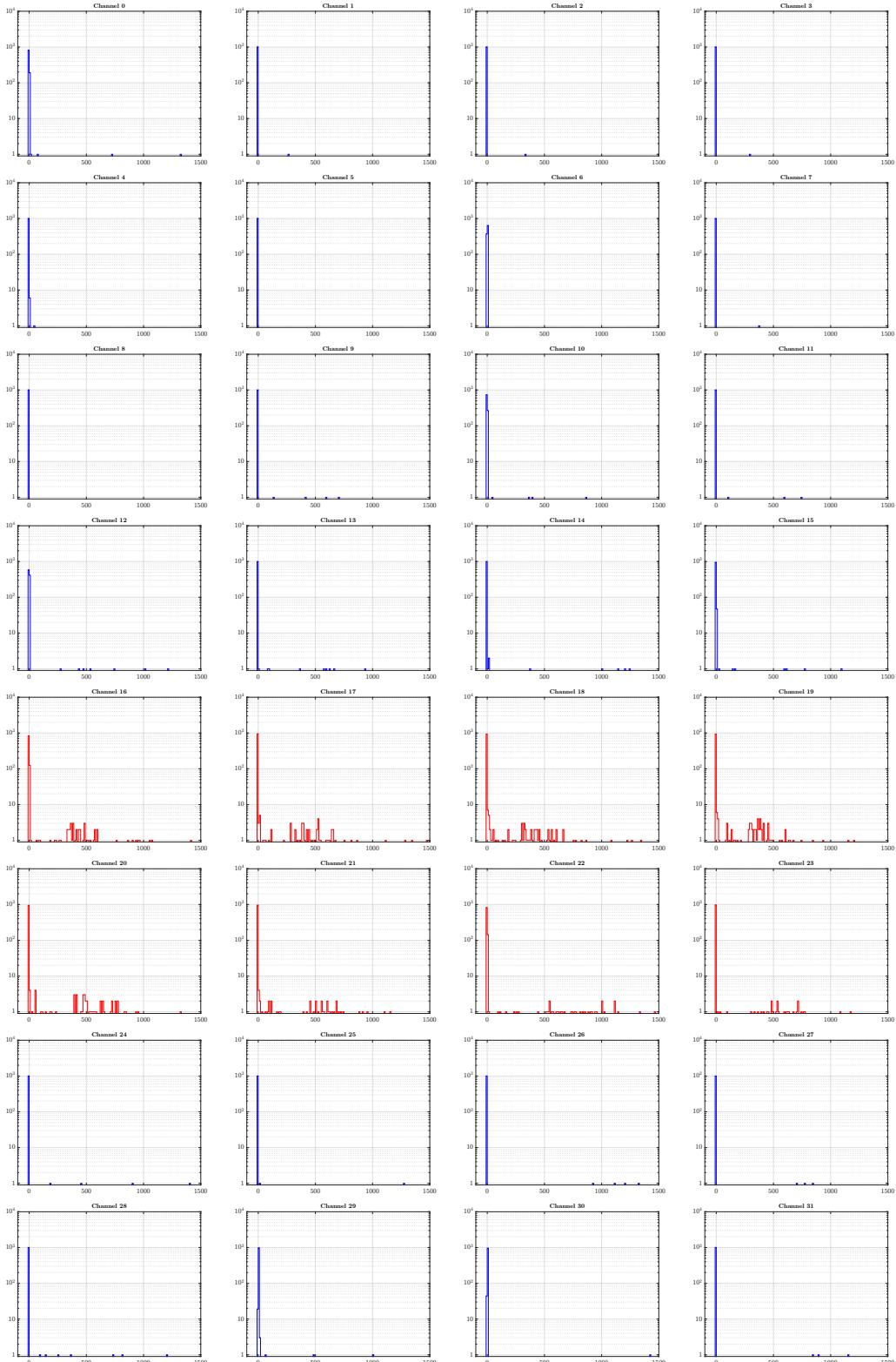
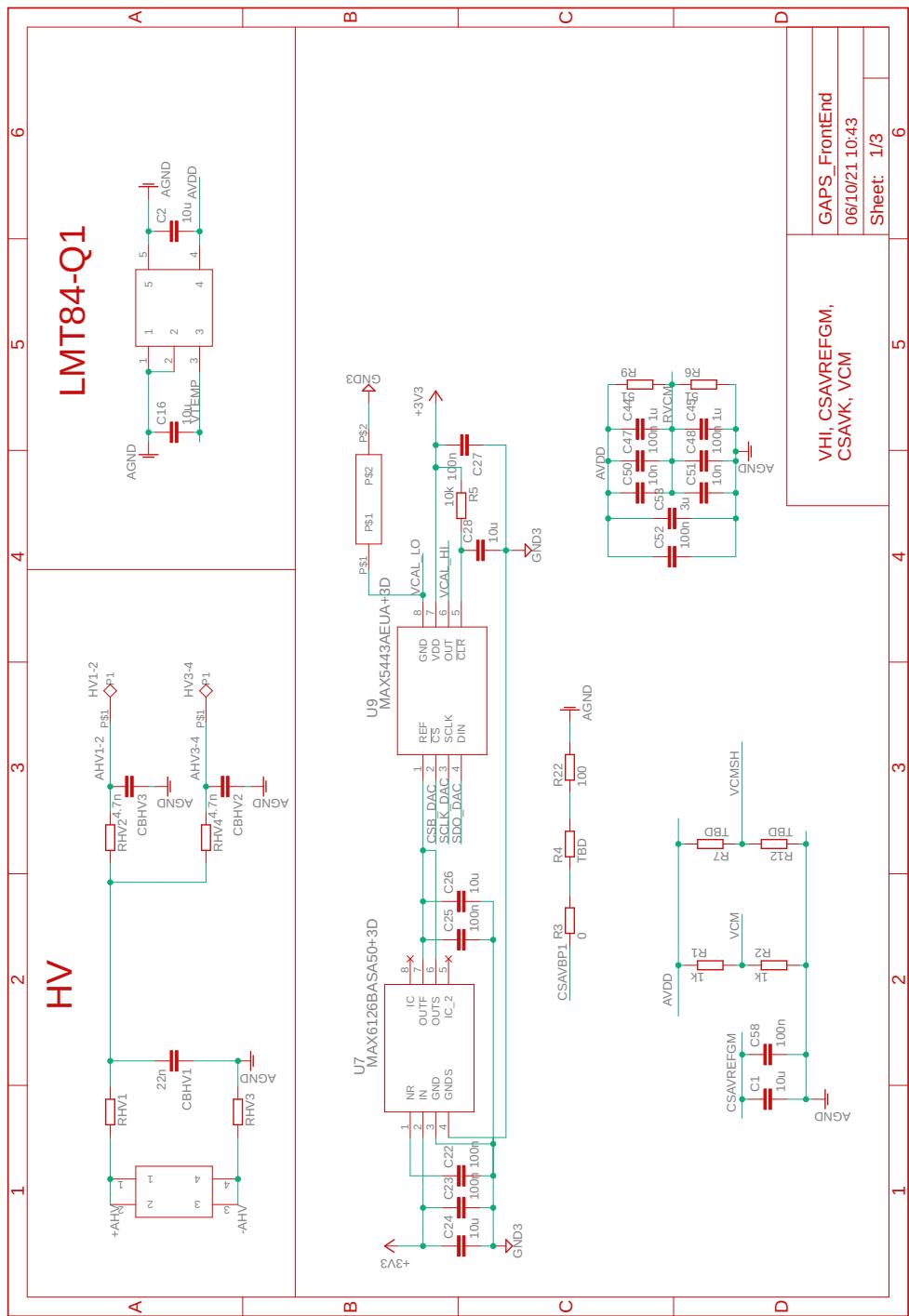


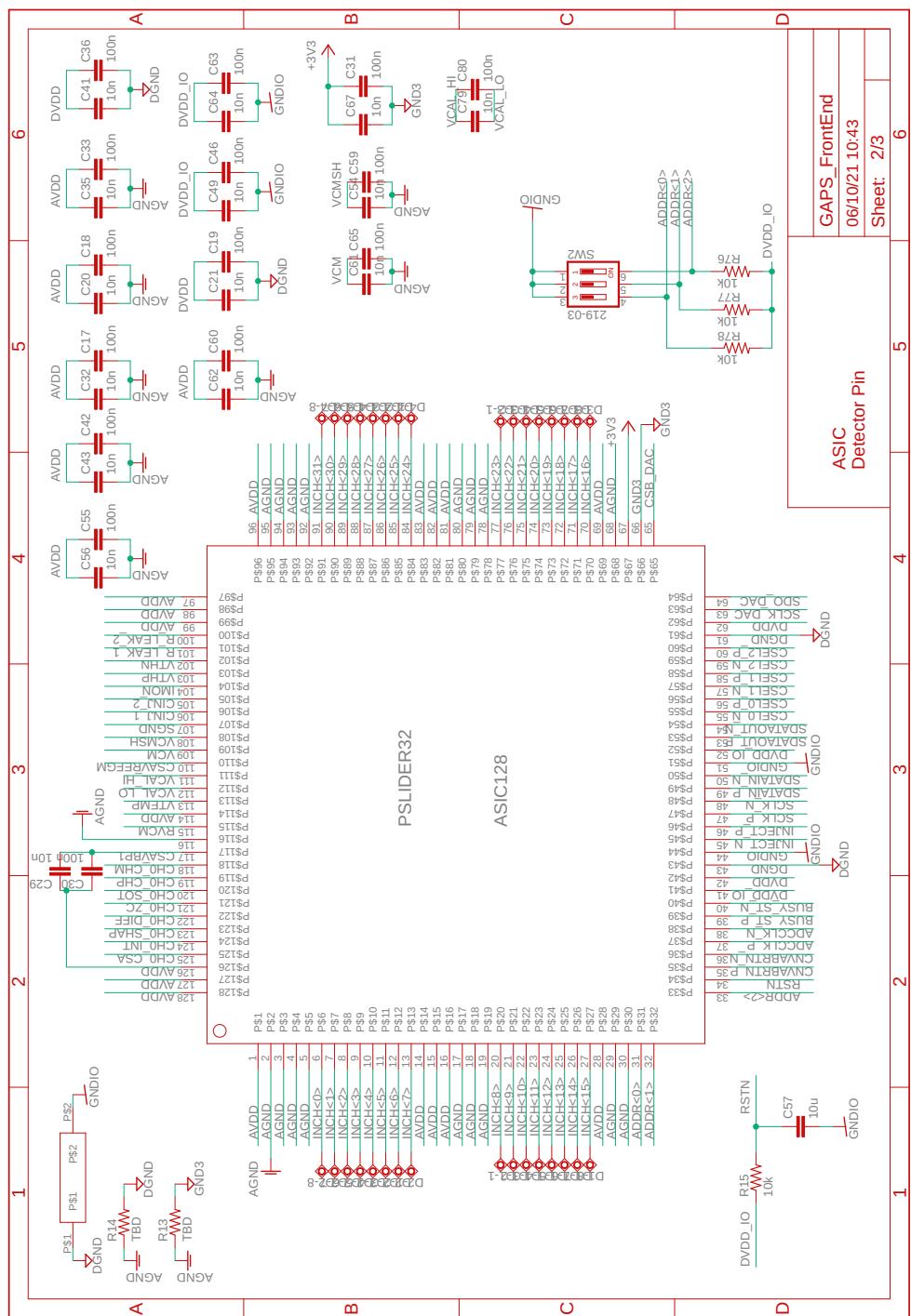
Figure C.1: 32-channel view of a two-hour acquisition performed in external trigger mode with global threshold set to 130 and trigger hold delay set to 34 FPGA clocks. Channels from 16 to 23 (detector #2) are highlighted in red.

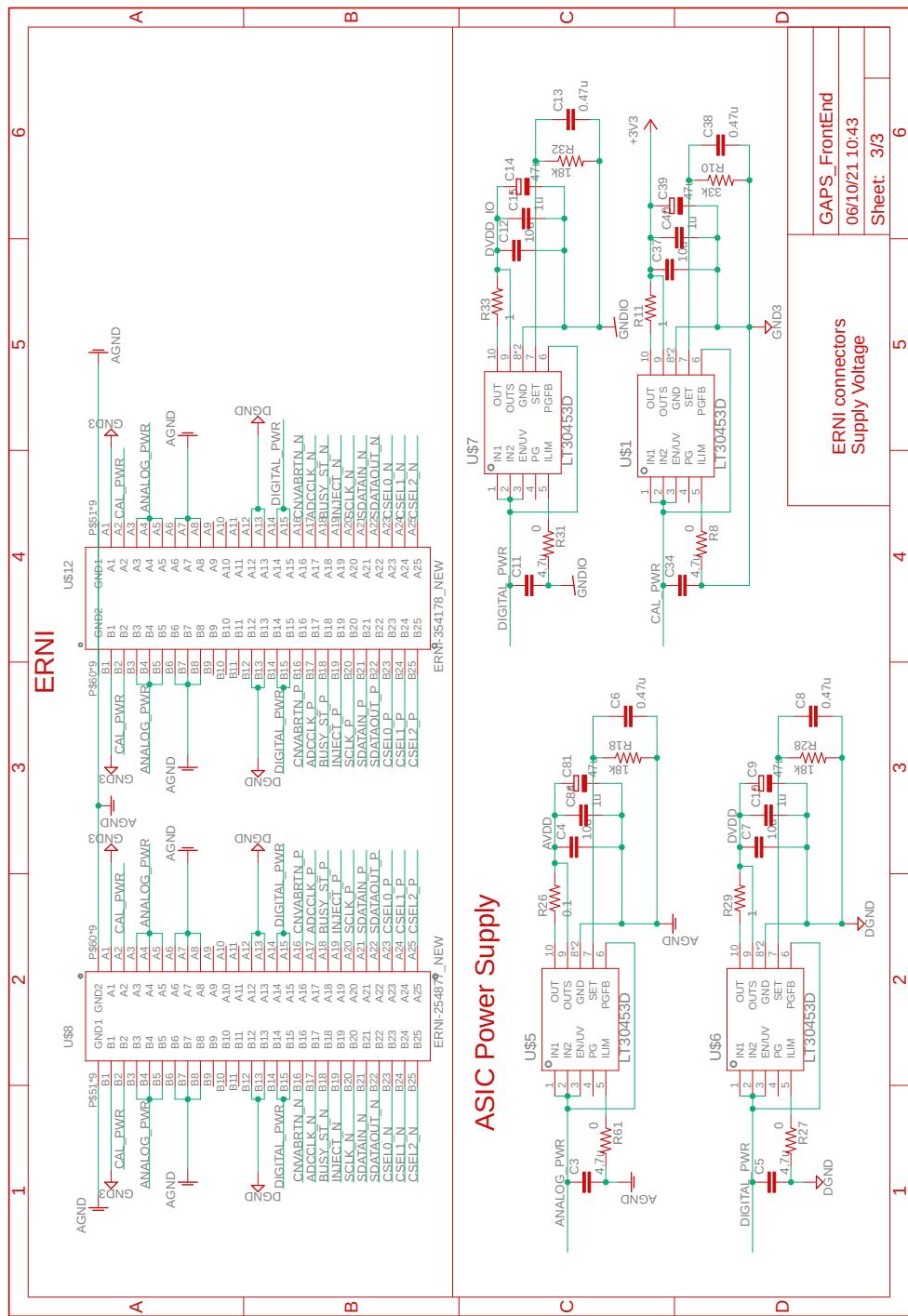
Appendix D

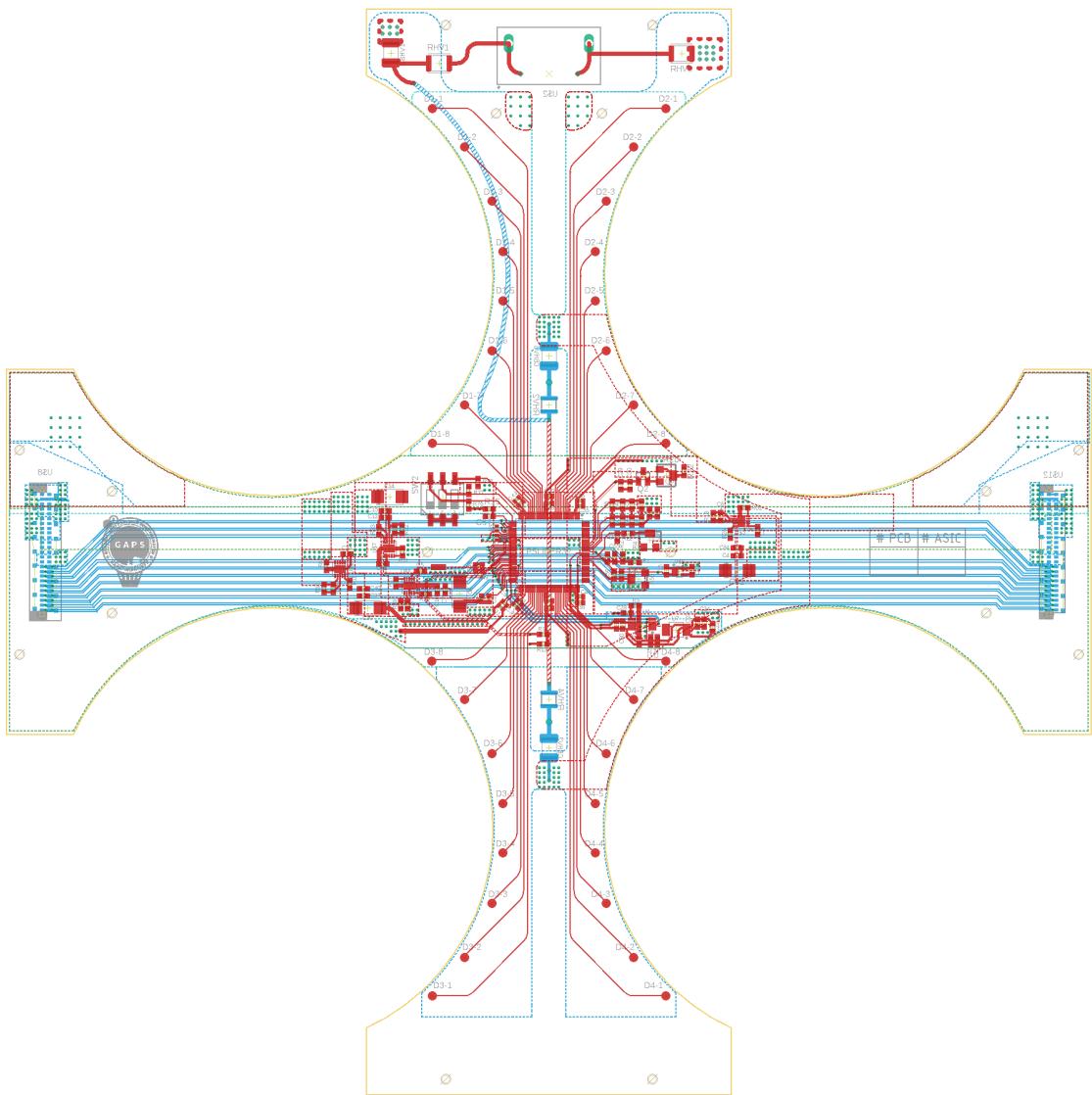
Schematics

This Appendix provides the schematics of the GAPS Front-End Board (FEB).









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