GAPS modules DAQ

Defaults

FPGA global setup

SPI clk: 12 | ADC clk: 24 | [MHz] Set

Event elaboration timeout [FPGA clocks]: 2000 Set

Trigger Hold delay [FPGA clocks]: 44 Set

ASIC masking: 000010 Set | Set all

000010 Detect

SPI sampling delays, addr. 1 to 6: 0 0 0 0 0 0

Event end delay [FPGA clocks]: 480 Set

Acquisition mode: (•) Time ( ) Number of events

[Seconds]: 1

[ ] External trigger

[✓] Flush buffer at end

Run

Plot ASIC address: All | Channel: All

ASIC configuration

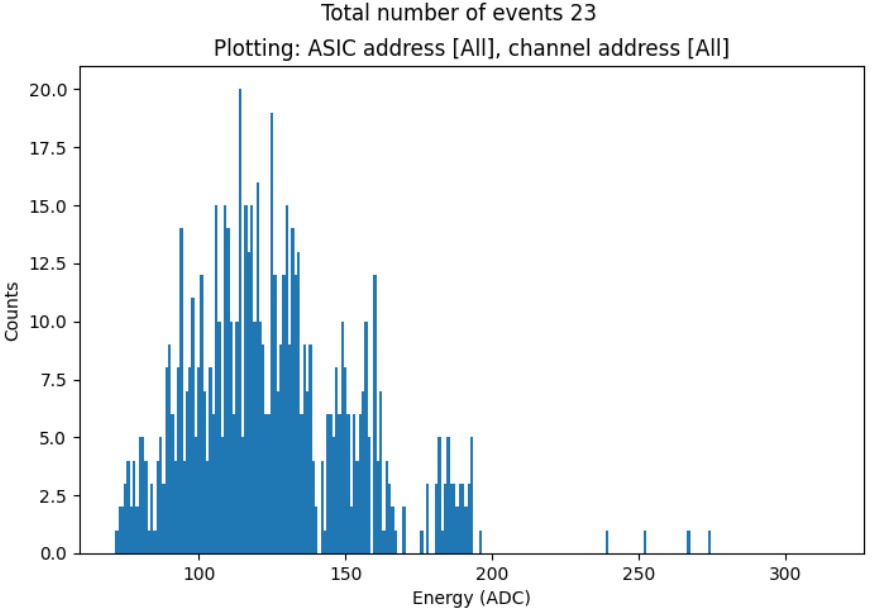
Common settings

Mode (ISA)	011	Set
Bias (TBBB)	0011	Set
Shaper	100	Set
Leakage mask	00000000000000000000000000000000	Set
Calib. mask	00000000000000000000000000000000	Set

Single ASIC settings

Address	2		
CSArefs (HRRR)	0011		Set
Discr. enable	11111111111111111111111111111111		Set
Threshold	205		Set
Channel	0	Fine Threshold 100	Set

Set all



[ ] Y-axis log scale

Output file name: Browse...