

GAPS Module tester v3.0

Defaults

FPGA global setup

SPI clk 8 ADC clk 24 [MHz] Set

Self-trigger timeout [FPGA clocks] 500 Set

Delay between events [FPGA clocks] 2000 Set

Set all

SPI sampling delays, addr. 0 to 5

0 0 0 0 0 0

ASIC configuration Manual test Automated test

Setting

Address Broadcast

Mode (ISA) 000 Set

Bias (TBBB) 0101 Set

CSArefs (HRRR) 1011 Set

Shaper 100 Set

Leakage mask 00000000000000000000000000000000 Set

Discr. enable 11111111111111111111111111111111 Set

Calib. mask 11111111111111111111111111111111 Set

Threshold 212 Set

Ch. 0 Ch. 1 Ch. 2 Ch. 3 >>>>

Fine THR 011 Set

Set all

ASIC

Address 2

Mode (ISA) Get

Bias (TBBB) Get

CSArefs (HRRR) Get

Shaper Get

Leakage mask Get

Discr. enable Get

Calib. mask Get

Threshold Get

Ch. 0 Ch. 1 Ch. 2 Ch. 3 >>>>

Fine THR Get

Get all

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SPI clk 8 ADC clk 24 [MHz] Set

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0 0 0 0 0 0

ASIC configuration Manual test Automated test

☒ Inject ☒ Count triggered events

DAC (min) value 0 Set DAC max value 300 step 1 ☒ Sweep DAC

Hold delay (max) 48 ☐ Sweep hold delay

THR (max) value 200 THR min value 100 THR step 1 ☐ Sweep THR

Events to acquire 1000

File name Browse

Acquire events Acquire HK

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Address 2 ☒ Fast test

☒ Pedestal run Events 1000

☒ Waveform scan Events 100 DAC value 1000 Max delay 120

☒ Transfer function Events 100

Range #1: DAC min 10 DAC max 100 step 10

Range #2: DAC min 200 DAC max 1000 step 100 ☒ Enable

Range #3: DAC min 1200 DAC max 2000 step 200 ☒ Enable

Range #4: DAC min 4000 DAC max 64000 step 2000 ☒ Enable

☒ Threshold scan Events 1000 THR min 200 THR max 255 step 1

☒ Self-trigger Events 100 DAC value 1000 Threshold 200 Shaper 4

☒ HK test Events 100

MODULE # Leaf dir. Database dir. Browse Start test