Politecnico di Torino

System-on-chip Architecture

Laboratory 1

Report

Master degree in Computer Engineering

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December 23, 2016

Summary

In this laboratory we have handled with low-power states of the STM32F05138 board. The lab has three main phases:

- Using datasheets in order to learn the configuration of the different low-power states;
- Providing a C code for handling and swichting among these states, using LEDs and User Button to highlighting the transitions among states;
- Measuring current in the different low-power states and comparing results with the ones in datasheets

Low-Power states description

In this phase we describe the different settings and configurations of the board according to a given power state.

Sleep mode

In this mode we have the following configuration:

- System Running at PLL (48MHz);
- All GPIOs are disabled by default. Moreover, we the option to disable also: *DMA*, SRAM clock,*CRC* (Cyclic Redundancy Check) calculation unit, Flash memory programming interface (not advisable since code run from internal Flash);
- Entry point for Sleep mode: WFI (Wait For Interrupt) or WFE (Wait for Event) instructions;
- Exit point for Sleep mode: enabling an interrupt in the peripheral control register but not in the NVIC, and enabling the SEVONPEND bit in the Cortex-M0 System Control register or configuring an external or internal EXTI line in event mode. In our case use the second option, an EXTI line linked to user button PA.00

Stop mode

The Stop mode is based on the Cortex-M0 deepsleep mode combined with peripheral clock gating.In this mode we have the following configuration:

- RTC Clocked by LSI (low-power clock source around 40kHz).The HSI and the HSE oscillators are disabled;
- Using a RTC clock by LSI to resume from this mode (in our case it is setted to 5s);
- Voltage regulator supplies low-power to the 1.8 V domain, preserving contents of registers and SRAM;
- Independent watchdog (IWDG) is clocked;
- FLASH in deep power down mode
- All GPIOs are disabled by default. Moreover, we the option to disable also: *DMA*, SRAM clock,*CRC* (Cyclic Redundancy Check) calculation unit, Flash memory programming interface (not advisable since code run from internal Flash);
- ADC or DAC consume power, unless disabled in this mode;
- No DEBUG available since Cortex-M0 is no longer clocked

Standby mode

The Standby mode allows to achieve the lowest power consumption. There are two different types of standby mode depending on the mode to resume: using RTC or with external interruption. In the former RCT is clocked by LSI, in the latter RTC is off. In this mode we have the following configuration:

- RTC Clocked by LSI (low-power clock source around 40kHz).The HSI and the HSE oscillators are disabled;
- All peripherals are disabled;
- No DEBUG available since Cortex-M0 is no longer clocked;
- All I/O pins are high impedance except:reset pad, PC13, PC14 and PC15 if configured by RTC or LSE and WKUPx pins;
- After waking up from Standby mode, program execution restarts in the same way as after a Reset (boot pin sampling, option bytes loading, reset vector is fetched, etc.).

Measurements

The purpose of this section is to compare the values of current in the different low-power states.

Mode	Conditions	I_{DD} current measured (mA)	I_{DD} current datasheet (mA)
RUN	Code executing from FLASH, PLL on, HIS 48MHz clock	12.2	22.0 - 11.8
SLEEP	HIS clock 8MHz, PLL on	0.820	0.6-0.8
STOP	Regulator in low-power mode; all oscillators off at 3.6V	8.6 [μA]	16 -1.3 [μA]
STANDBY	LSI on, IWDG off	0.6 [μA]	1.5 -1.3 [μA]

Table 1: Comparing currents

The result of the comparison is just what it was expected. So values of current measured respetc the ones in the datasheet. Moreover, some modification in the configurations of the different states have been done. For SLEEP and STOP mode we use the lowest power consuming configuration possible disabling *DMA*, SRAM clock,*CRC* (Cyclic Redundancy Check) calculation unit.We tryed to enable the configuration descibed before,we never enabled that kind of peripherals, so the lowest current values posssibles are the ones in the previous Table, to advantades disables those kind of peripherals.