Note: I added this here because I noticed that the assignment submissions between groups were connected and I didn't want to upload over my group members. Should we be writing the lab report together?

Lab 02 - First Verilog

In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

Rubric

Item	**Description**	**Value**
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

I learned how to build a Verilog project in Vivado. The only problem our group had was after pressing autoconnect under the hardware section it didn't connect. I think it was because the board we connected hadn't finished connecting properly yet. After pressing autoconnect again it worked. There were no more problems and we got the switch turning a light on and off.

Lab Questions

1 - Describe the stages of building a Verilog project in Vivado.

First start up the software. Then create a project filling in the necessary details including adding the code files from the computer's filing system. Then select the input under boards and search for Basys3. Check the information and then hit finish and your project is created.

2 - What is the value in looking at the elaborated design schematic?

It allows you to verify whether your design will work. Seeing the actual circuit laid out from your input can make it easier to identify if you've made any silly mistakes.

3 - Why should we simulate our designs frequently? What does the simulation do?

Simulating can help find errors and it takes less time and hassle compared to running the program on the board. A simulation mimics what the board will probably do in software, so it can be used to predict what exactly your code will do.

Code Submission

https://github.com/lucascoltrin/ECE230LAB