Relatório

Trabalho 2 – Arquitetura de Computadores

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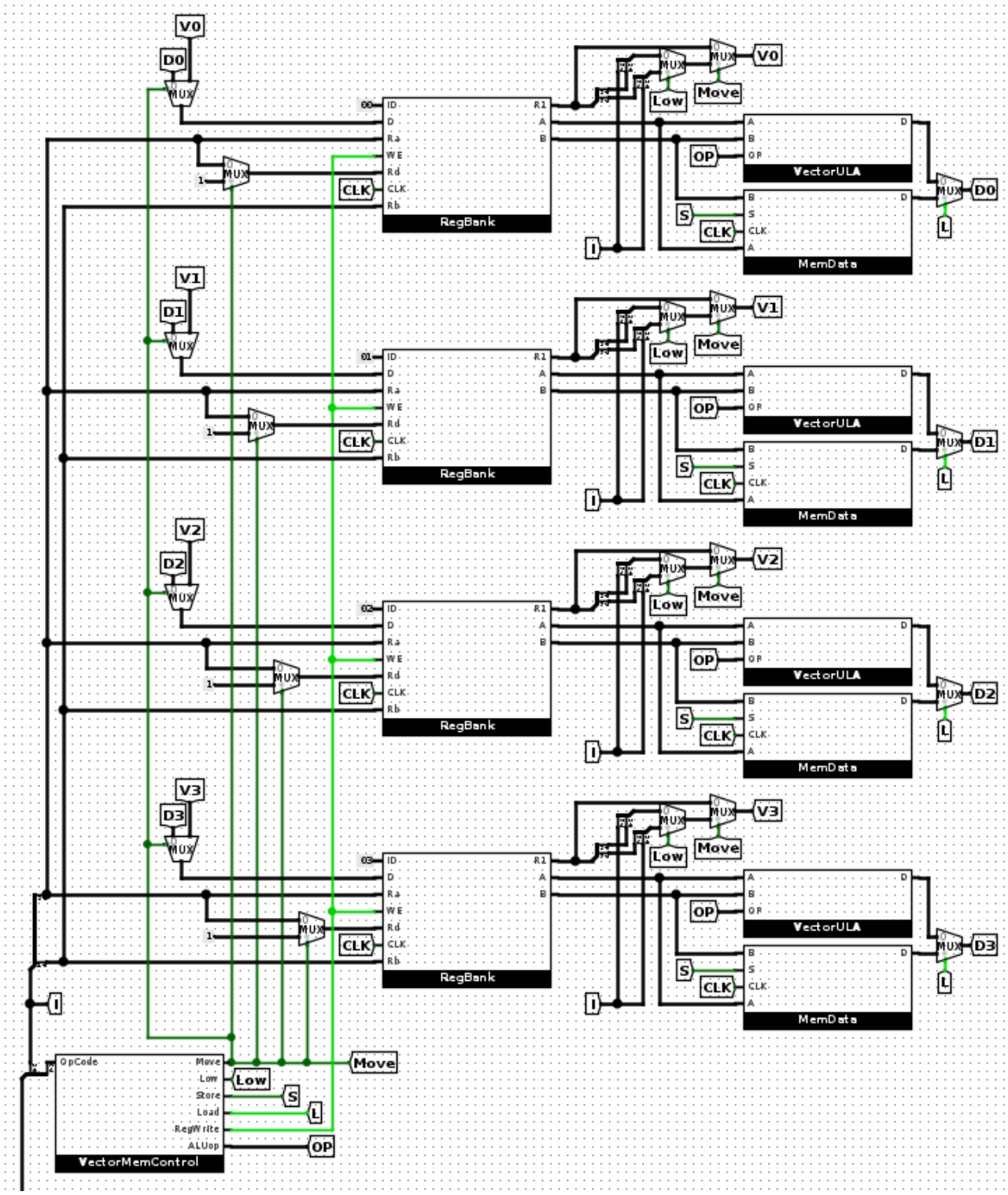
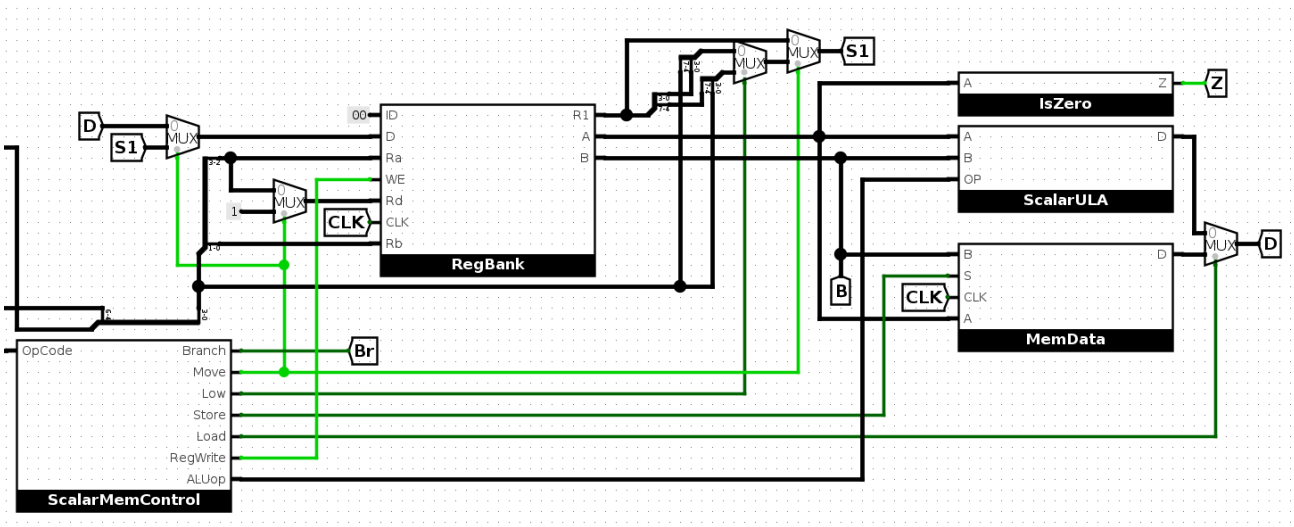
I. Diagrama Sagui Vetorial



II. Diagrama Sagui Vetorial



III. Código de teste

N°	Instrução	Descrição	Binário	Hexa
0.	S movh 1111	# R1 = 240	00101111	2F
1.	S movl 1111	# R1 = 255	00111111	3F
2.	S and $R1 $R2	# R1 = R1 & R2	01100110	66
3.	S movl 0001	# R1 = 1	00110001	31
4.	S add $R3 $R1	# R3 = R3 + R1	01001101	4D
5.	S st $R1 $R1	# M[R1] = R1	00010101	15
6.	S ld $R2 $R1	# R2 = M[R1]	00001001	09
7.	S sub $R1 $R2	# R1 = R1 - R2	01010110	56
8.	V movh 1111	# R1 = 240	10101111	AF
9.	V movl 1111	# R1 = 255	10111111	BF
10.	V and $R1 $R2	# R1 = R1 & R2	11100110	E6
11.	V movl 0001	#R1 = 1	10110001	B1
12.	V st $R1 $R1	# M[R1] = R1	10010101	95
13.	V ld $R2 $R1	# R2 = M[R1]	10001001	89
14.	V add $R1 $R2	# R1 = R1 + R2	11000110	C6
15.	V sub $R1 $R2	# R1 = R1 - R2	11010110	D6
16.	V or $R1 $R2	# R1 = R1 || R2	11110110	F6
17.	S brzr $R1 $R1	# goto 0	01110101	75