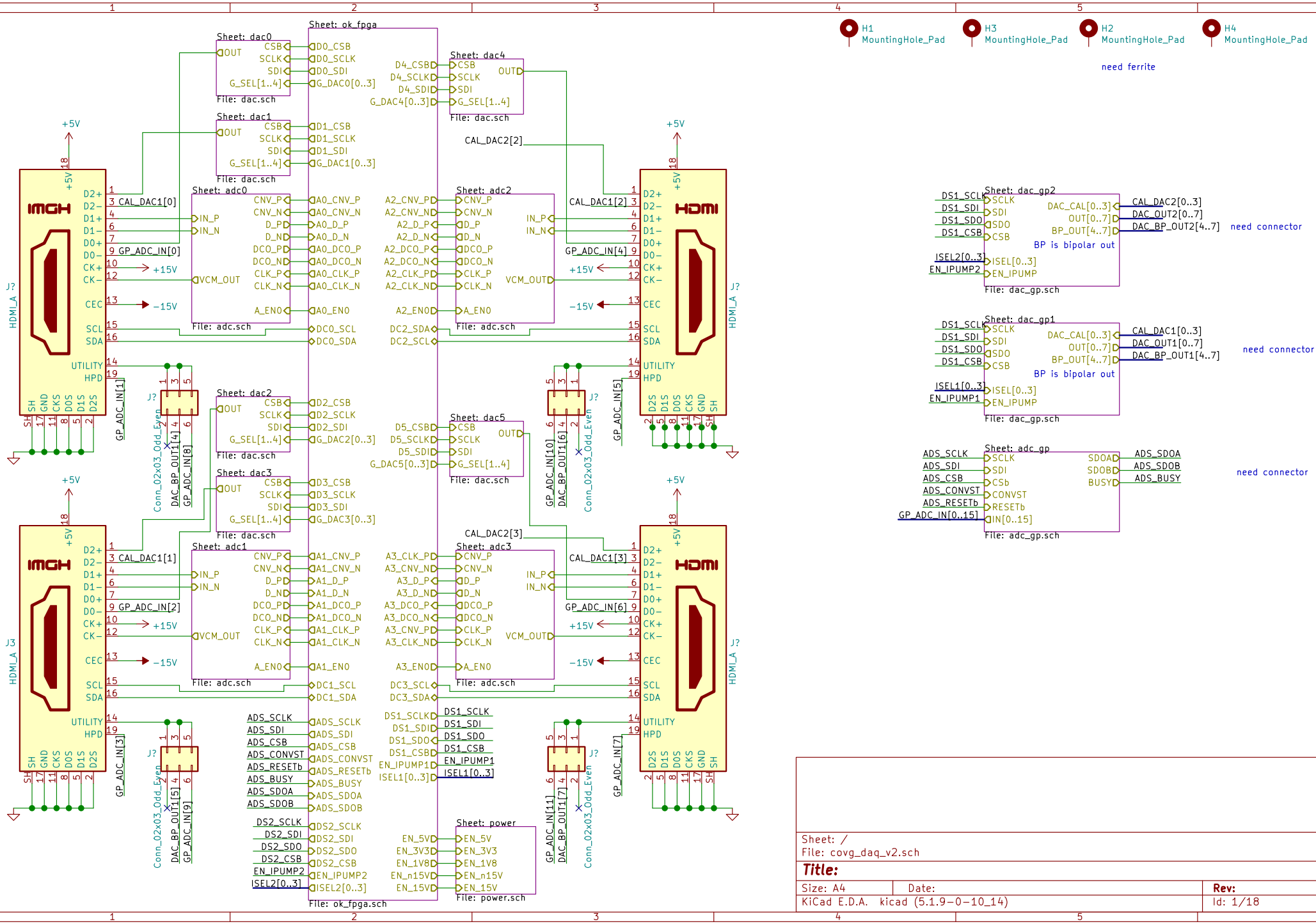
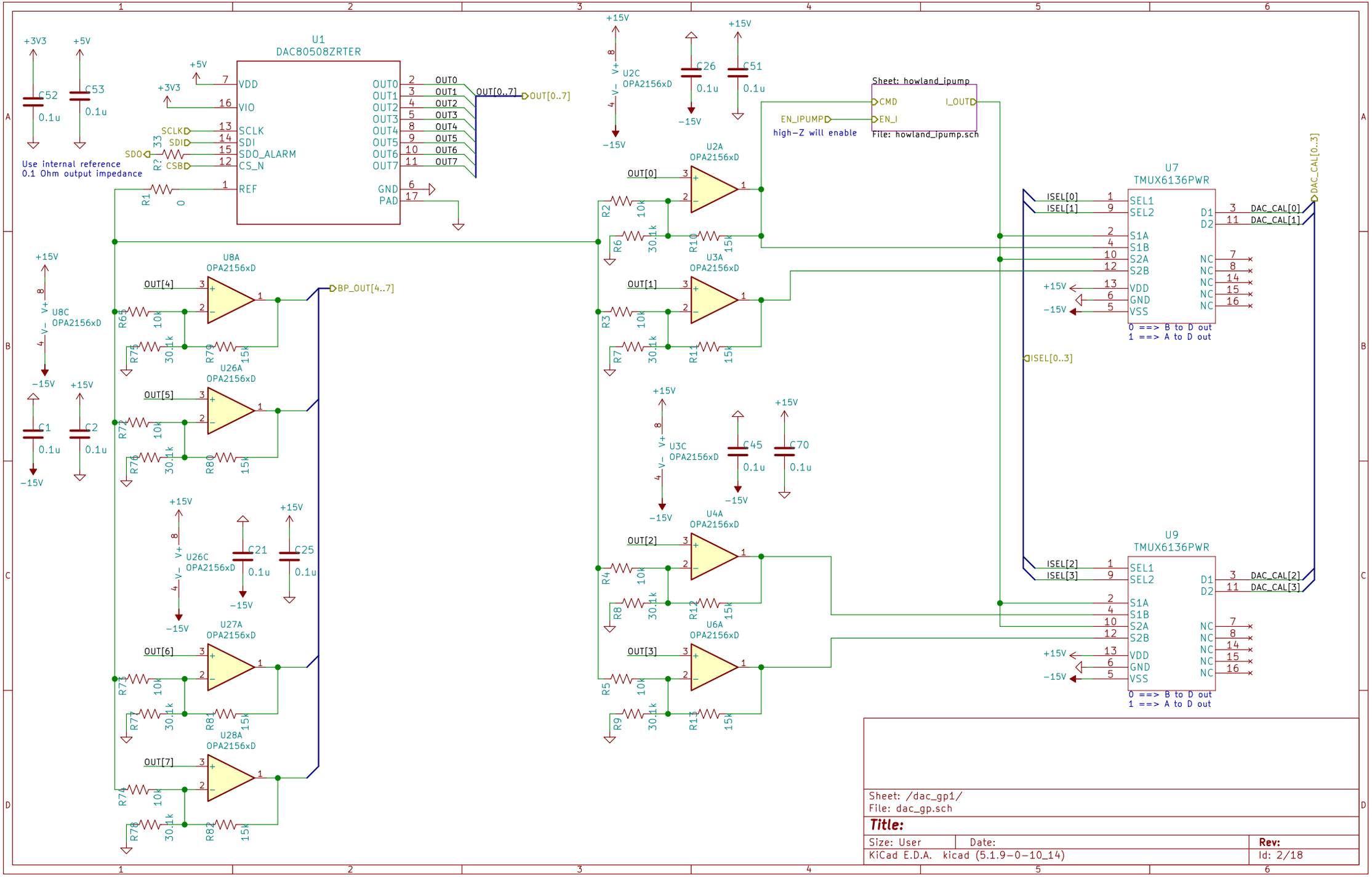
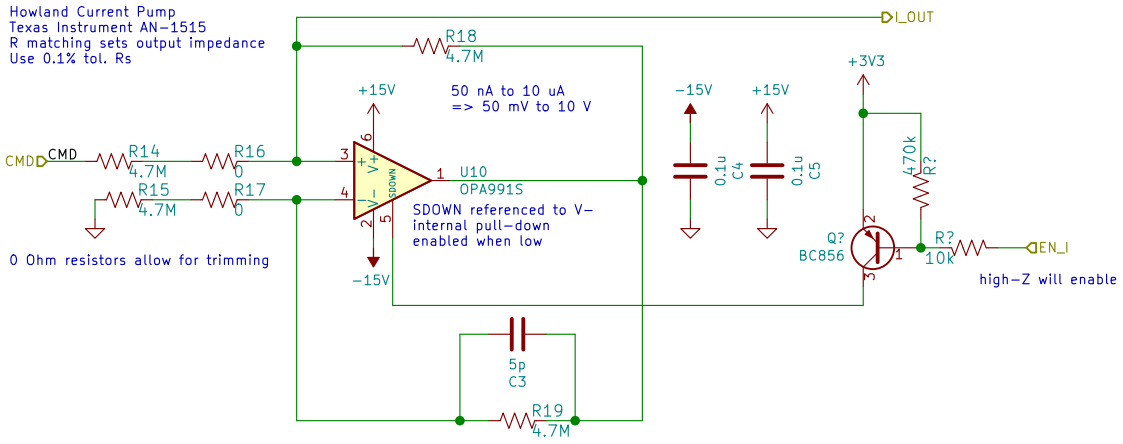
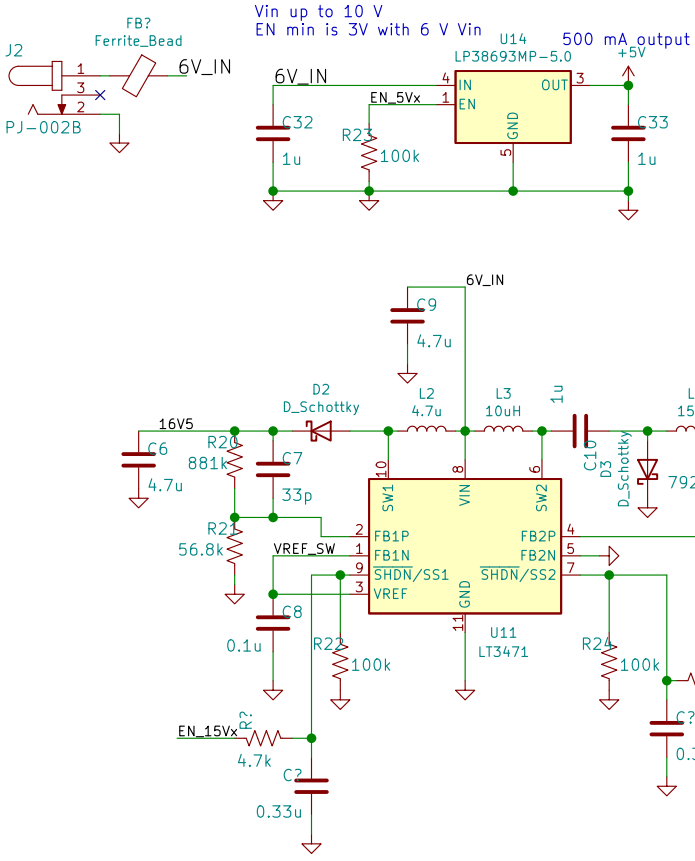

Sheet: ok_fpga
Sheet: dac0
Sheet: dac1
Sheet: dac2
Sheet: dac3
Sheet: dac4
Sheet: dac5
Sheet: adc0
Sheet: adc1
Sheet: adc2
Sheet: adc3
Sheet: power
Sheet: dac_gp2
Sheet: dac_gp1
Sheet: adc_gp
H1 MountingHole_Pad
H3 MountingHole_Pad
H2 MountingHole_Pad
H4 MountingHole_Pad
need ferrite
need connector
BP is bipolar out
Sheet: /
File: covg_daq_v2.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 1/18


U1
DAC80508ZRTER
VDD
VIO
SCLK
SDI
SDO_ALARM
CS_N
REF
GND
PAD
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT[0..7]
Use internal reference
0.1 Ohm output impedance
U2A
U2C
U3A
U3C
U4A
U6A
U8A
U8C
U26A
U26C
U27A
U28A
OPA2156xD
Sheet: howland_ipump
File: howland_ipump.sch
CMD
I_OUT
EN_I
EN_IPUMP
high-Z will enable
U7
U9
TMUX6136PWR
SEL1
SEL2
S1A
S1B
S2A
S2B
D1
D2
NC
VDD
GND
VSS
ISEL[0]
ISEL[1]
ISEL[2]
ISEL[3]
ISEL[0..3]
DAC_CAL[0]
DAC_CAL[1]
DAC_CAL[2]
DAC_CAL[3]
DAC_CAL[0..3]
0 ==> B to D out
1 ==> A to D out
BP_OUT[4..7]
+3V3
+5V
+15V
-15V
Sheet: /dac_gp1/
File: dac_gp.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 2/18



Sheet: /dac_gp1/howland_ipump/		
File: howland_ipump.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 3/18



Sheet: /power/		
File: power.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 4/18

What is VCCBATT?

Do a check of skew matching between DCO and D
for high-speed ADC

Bank 13: 3.3V always
MC1 64 and 66-76 MC2 64 and 66-76
(24 total)

Bank 34: default 3.3V,
change by ferrite bead (FB8)
on MC1
(total of 48)

Bank 35: default 3.3V,
change by ferrite bead (FB9)
MC2 2
(total of 50)

OK1A

SYS_CLK not special
other than name

IO voltage for bank 35
3.3 V (leave open)

IO voltage for bank 35
3.3 V (leave open)

OK1B

ADS8686
16-chan ADC

DAC80508
8-chan

DAC80508
8-chan

OK1C

OK1D

IO voltage for bank 34

IO voltage for bank 34

Ok for 2.5 V
to TMUX since
ref to Gnd

SparkFun qwiic connector
SM04B-SRSS-TB
3.3 V VCC

U?
PCA9306

U?
TXS0108EPW

U?
TXS0108EPW

U?
TCA9555DBR

U?
TCA9555DBR

U?
NLSX3018DTR2G

Bidirectional translator
Level shifter is not for I2C

Vcc = 1.3 - 4.5 V

VL = 0.9 to VCC-0.4

These are global (for all ADC channels)
EN0 is the only signal that needs
FPGA control per ADC channel.
Default settings:
EN3,EN2,EN1,EN0
0,0,0,FPGA (A_EN2_HV is high-Z)

driving EN2 high outputs test
patterns on the LVDS interface

VREF: needed for single-ended IO standards that use a diff. input buffer.
We do not need VREF. The FPGA also has an internal VREF which can be used if running at or below 400 MHz.
Most relevant to memory interfaces.

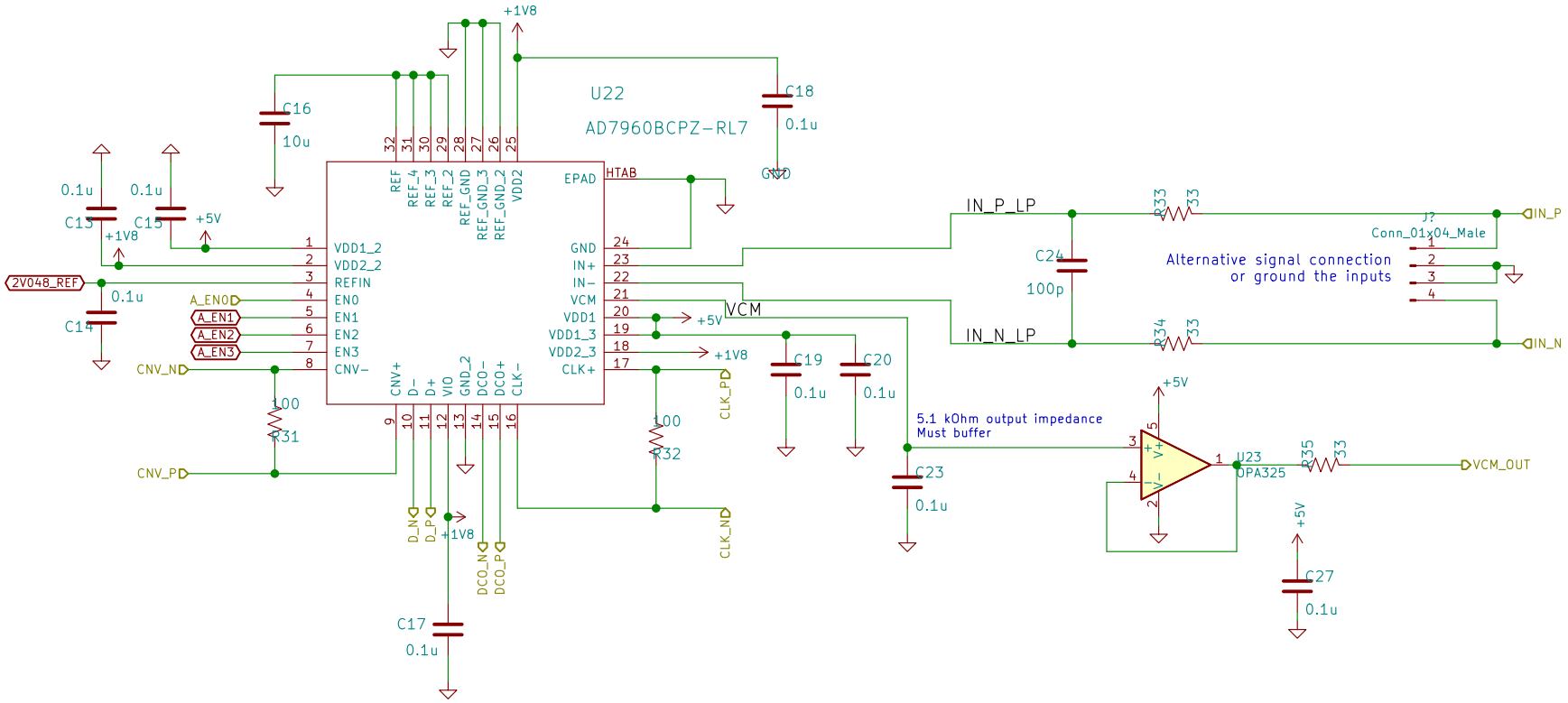
Sheet: /ok_fpga/
File: ok_fpga.sch

Title:

Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 5/18

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

VDD2 and VIO can come from the same supply.
But route and decouple separately.



Sheet: /adc1/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 6/18

AGND_IN must be within +/−0.3 V of GND

AVDD bypass (1x 10uF, 1x 0.1uF per pin)

IC3
ADS8686SIPZAR

Board edge

J?
Conn_02x16_Odd_Even

Some inputs will come from other wires and connectors

REFIO: most guidance is 0.1uF bypass (including EVM schematics), but datasheet layout section suggests 10 uF.

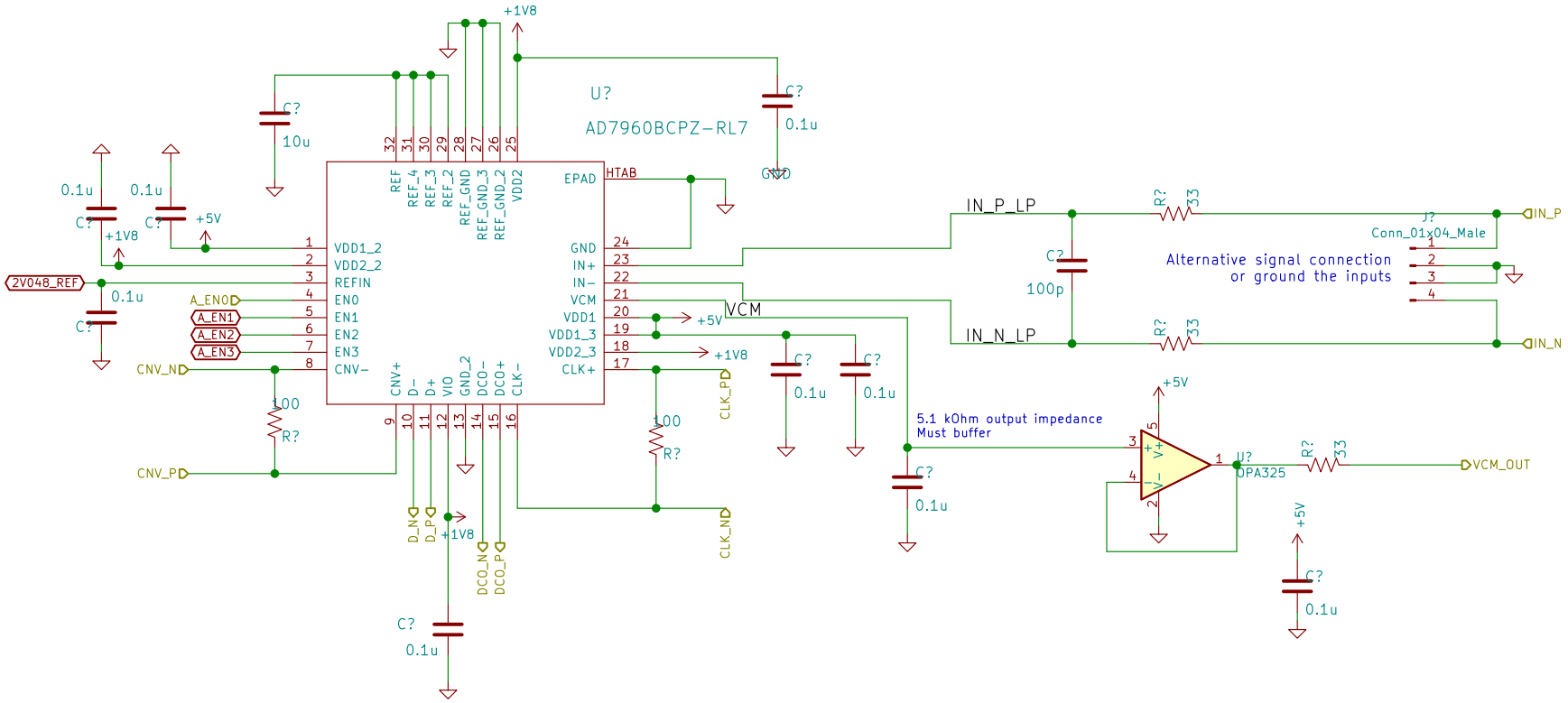
Must by pulled up by FPGA to enable. 3.3 V level.

The dual SPI interface has sufficient BW to clock the data out at the 1 MSPS (just need 16 MHz clock rate)

Sheet: /adc_gp/		
File: adc_gp.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9−0−10_14)		Id: 7/18

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

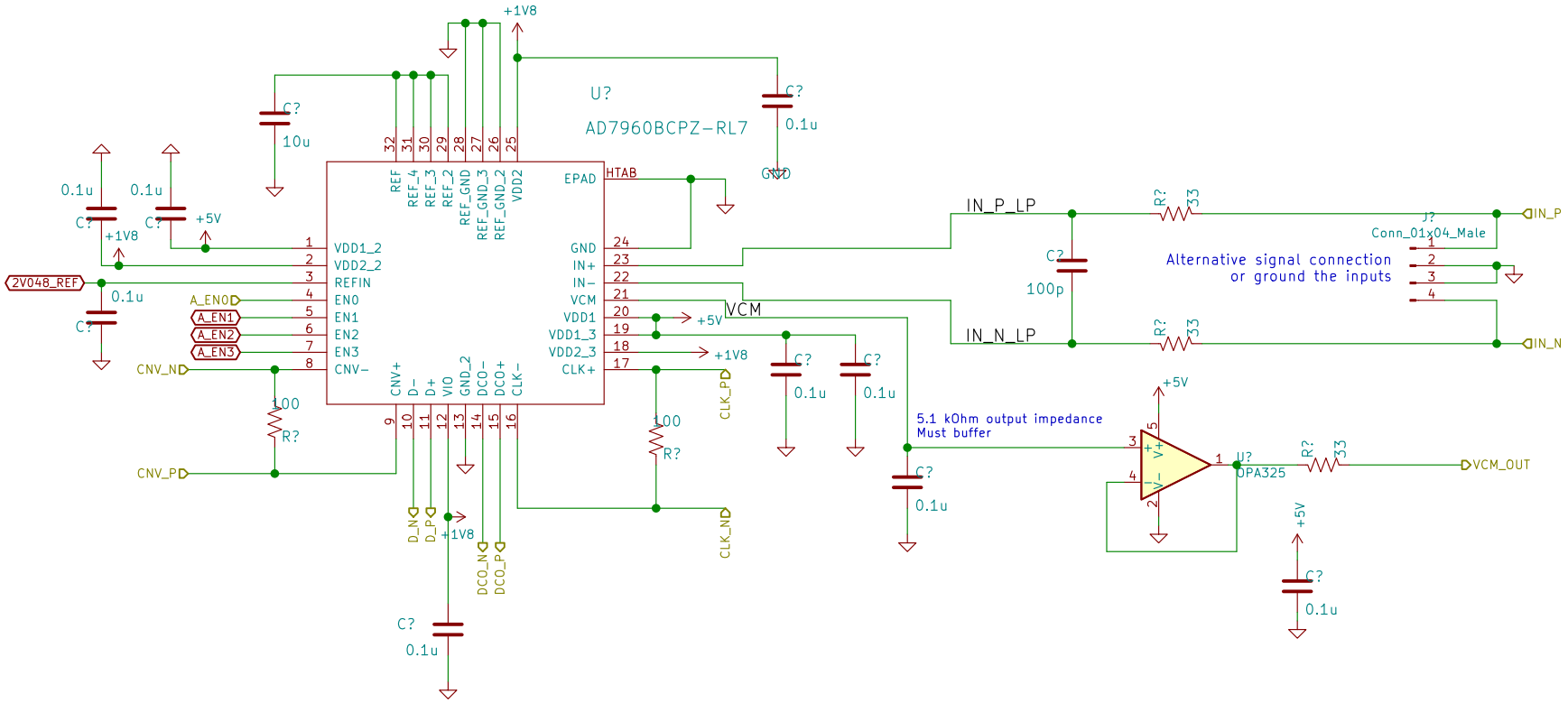
VDD2 and VIO can come from the same supply.
But route and decouple separately.



Sheet: /adc0/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 8/18

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

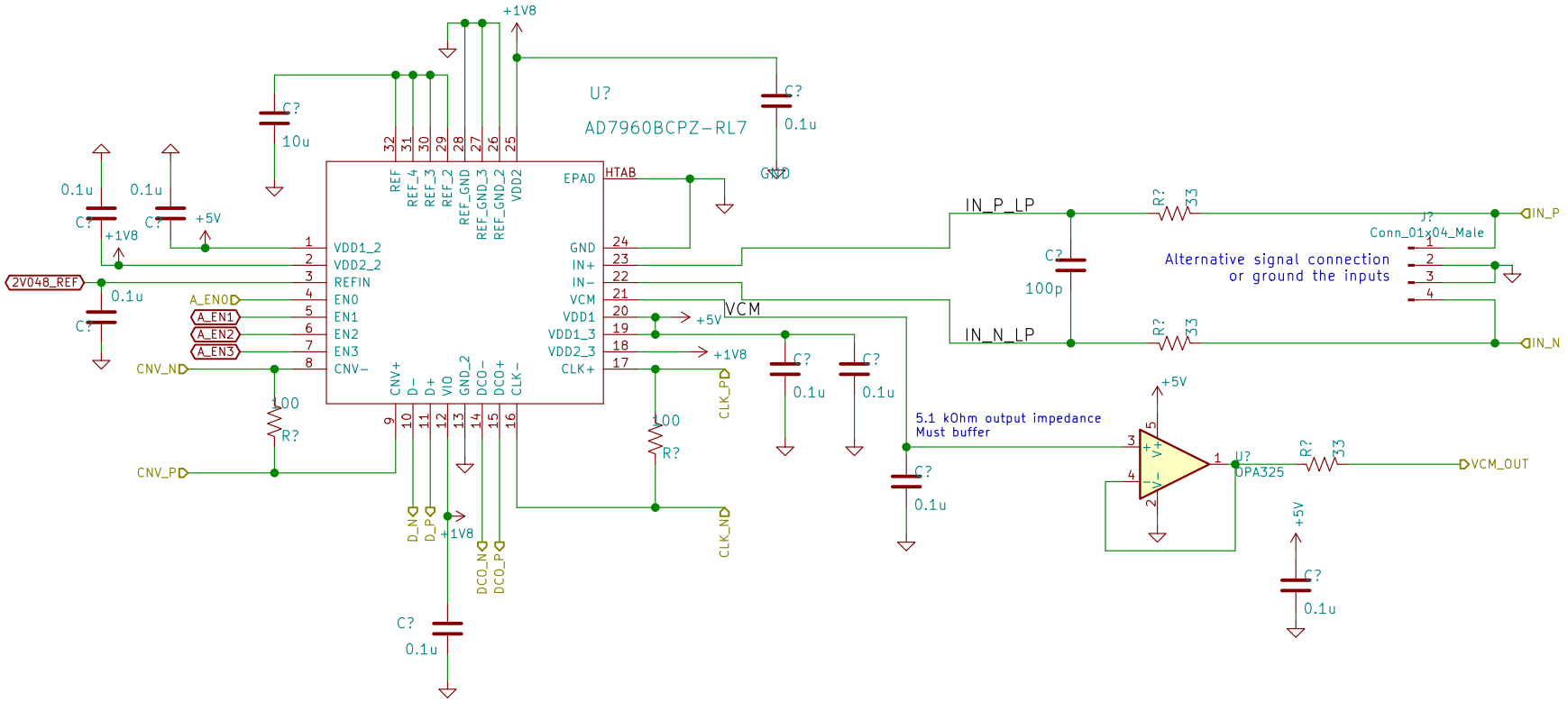
VDD2 and VIO can come from the same supply.
But route and decouple separately.



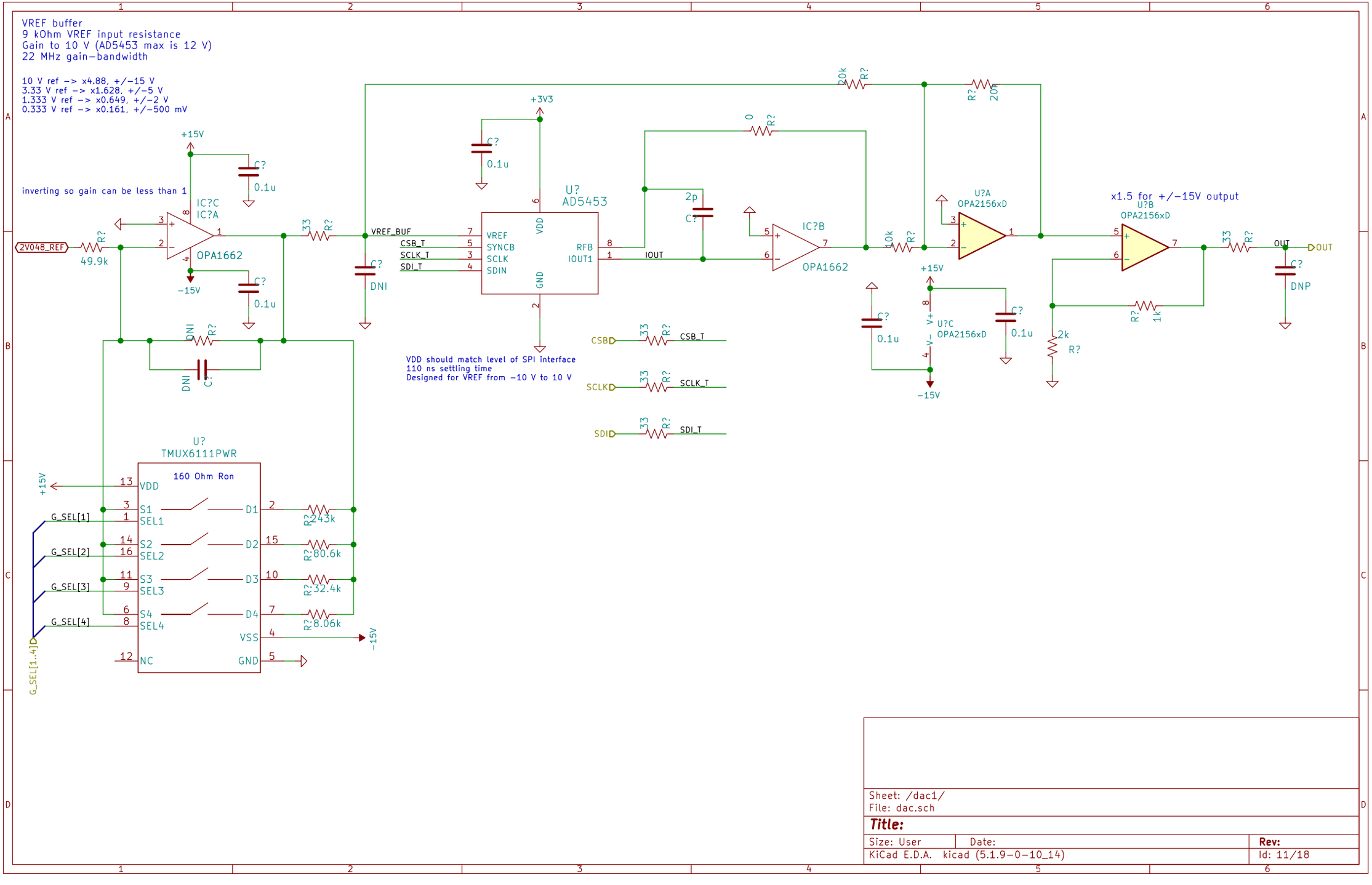
Sheet: /adc2/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 9/18

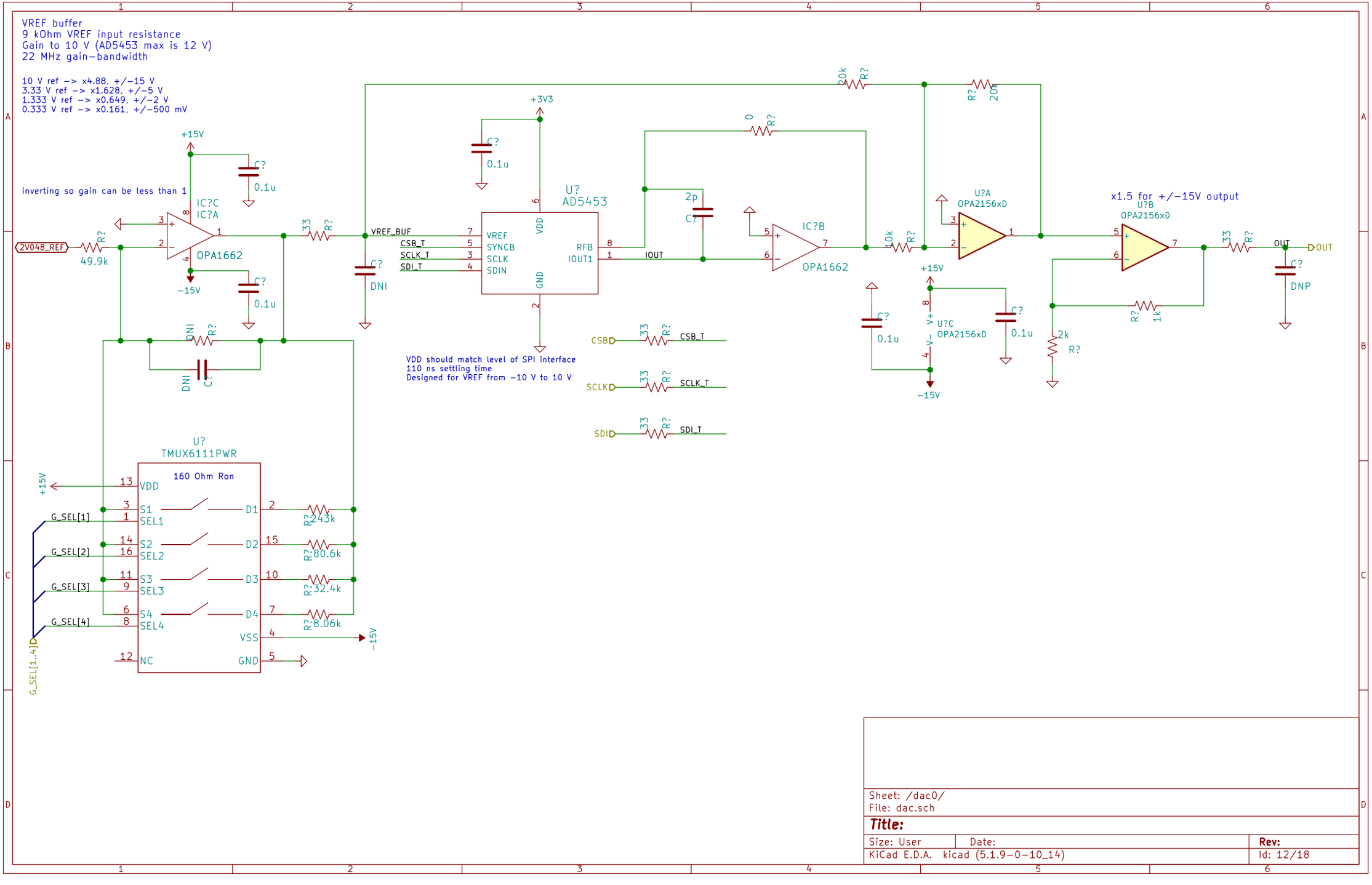
Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

VDD2 and VIO can come from the same supply.
But route and decouple separately.

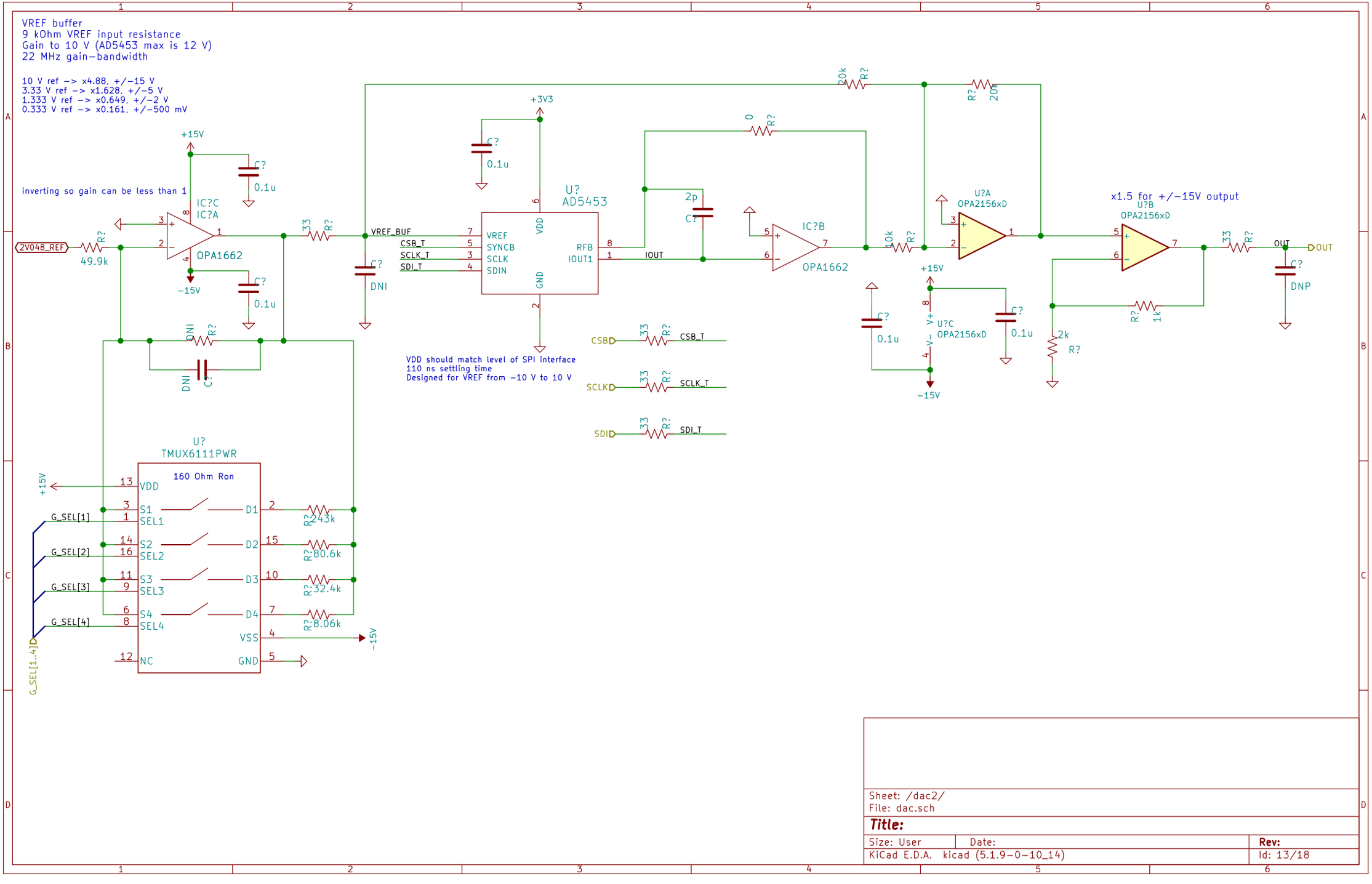


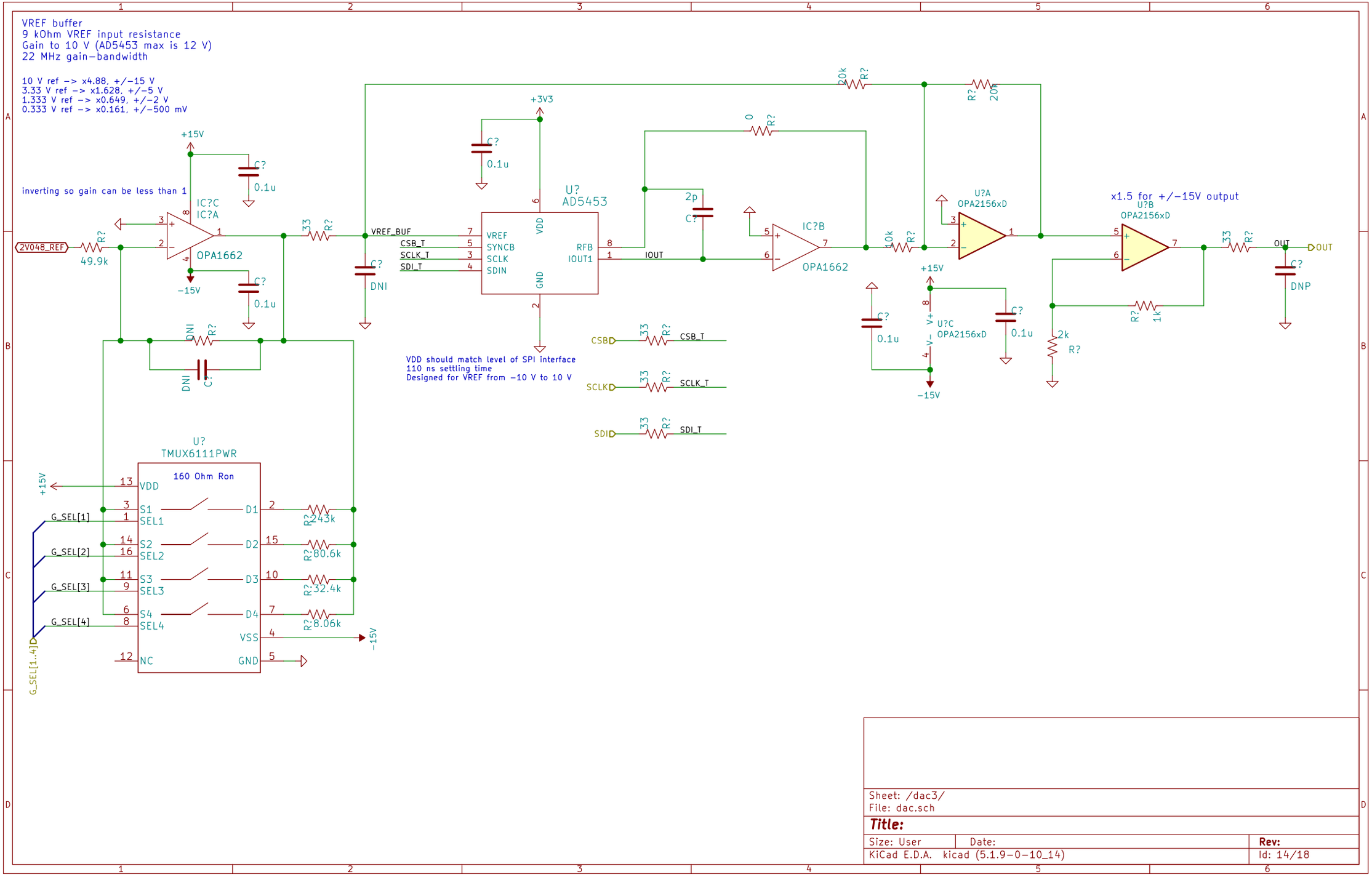
Sheet: /adc3/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 10/18


VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
+15V
-15V
IC?C
IC?A
OPA1662
2V048_REF
49.9k
33
VREF_BUF
CSB_T
SCLK_T
SDI_T
+3V3
U?
AD5453
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
2p
0
20k
10k
IC?B
OPA1662
U?A
OPA2156xD
U?B
OPA2156xD
U?C
OPA2156xD
x1.5 for +/-15V output
OUT
DNP
0.1u
DNI
2k
1k
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
CSB
SCLK
SDI
U?
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
NC
GND
G_SEL[1]
G_SEL[2]
G_SEL[3]
G_SEL[4]
G_SEL[1..4]
243k
80.6k
32.4k
8.06k
Sheet: /dac1/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 11/18



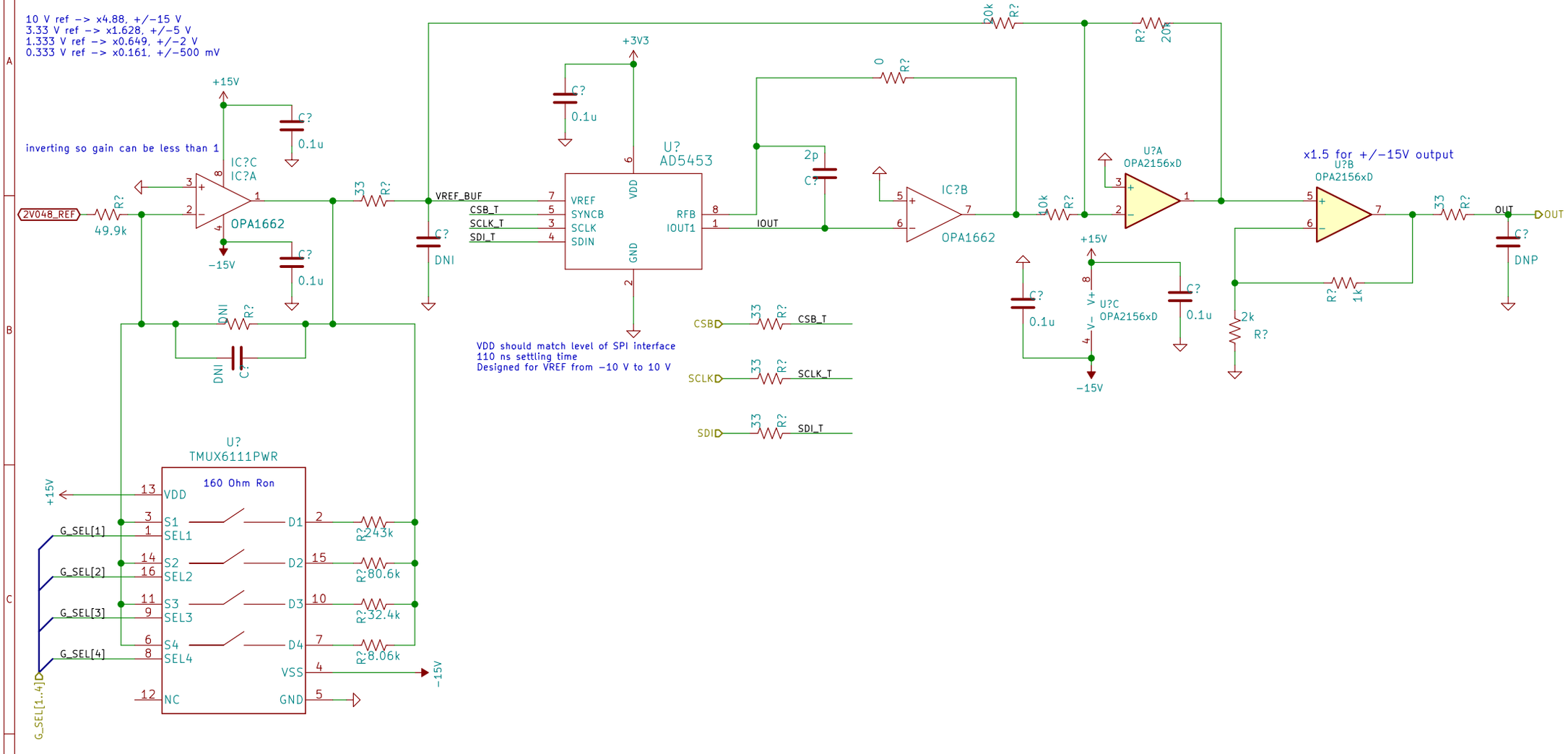
Sheet: /dac0/		
File: dac.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 12/18


VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
+15V
-15V
IC?C
IC?A
OPA1662
2V048_REF
49.9k
33
VREF_BUF
CSB_T
SCLK_T
SDI_T
+3V3
U?
AD5453
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
2p
0
20k
10k
IC?B
OPA1662
U?A
OPA2156xD
U?B
OPA2156xD
x1.5 for +/-15V output
U?C
OPA2156xD
2k
1k
OUT
DNP
DNI
0.1u
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
CSB
SCLK
SDI
U?
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
NC
GND
G_SEL[1]
G_SEL[2]
G_SEL[3]
G_SEL[4]
G_SEL[1..4]
243k
80.6k
32.4k
8.06k
Sheet: /dac2/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 13/18

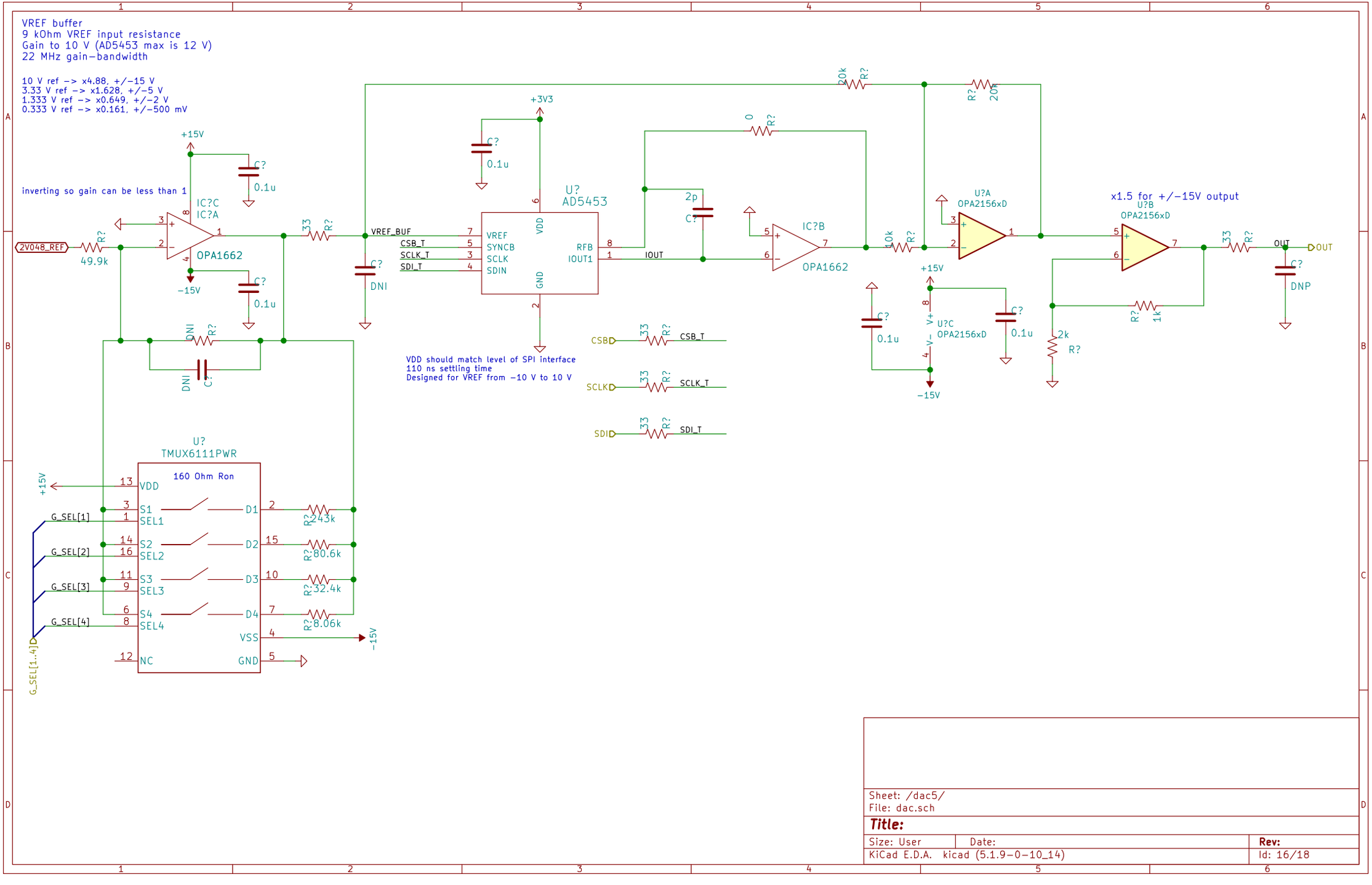

VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
+15V
-15V
IC?C
IC?A
OPA1662
2V048_REF
49.9k
R?
C?
0.1u
33
VREF_BUF
DNI
+3V3
U?
AD5453
CSB_T
SCLK_T
SDI_T
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
IOUT
2p
0
20k
10k
IC?B
U?A
OPA2156xD
U?B
U?C
x1.5 for +/-15V output
OUT
DNP
2k
1k
CSB
SCLK
SDI
U?
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
NC
GND
243k
80.6k
32.4k
8.06k
G_SEL[1]
G_SEL[2]
G_SEL[3]
G_SEL[4]
G_SEL[1..4]
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
Sheet: /dac3/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 14/18

VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth

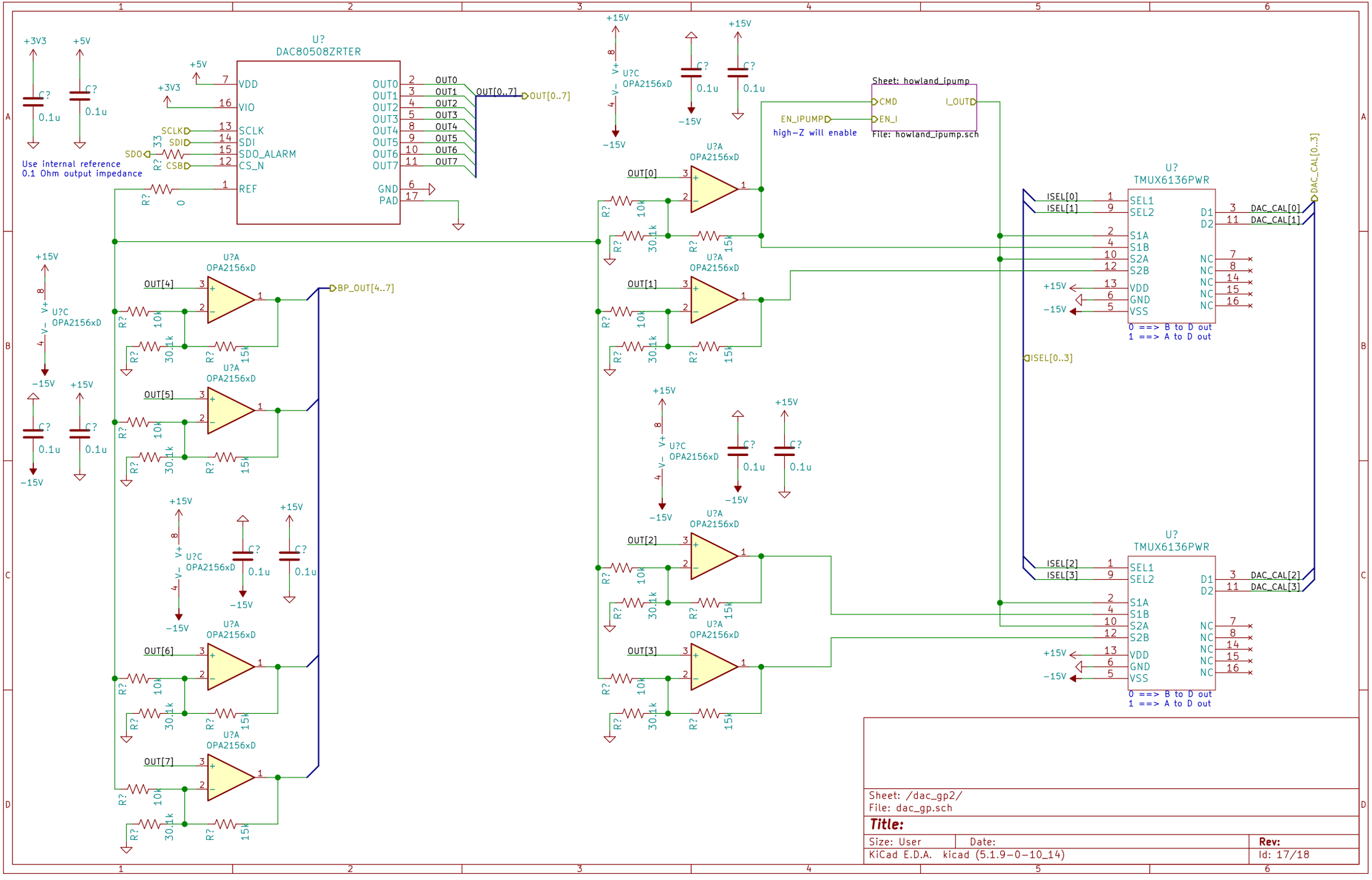
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV

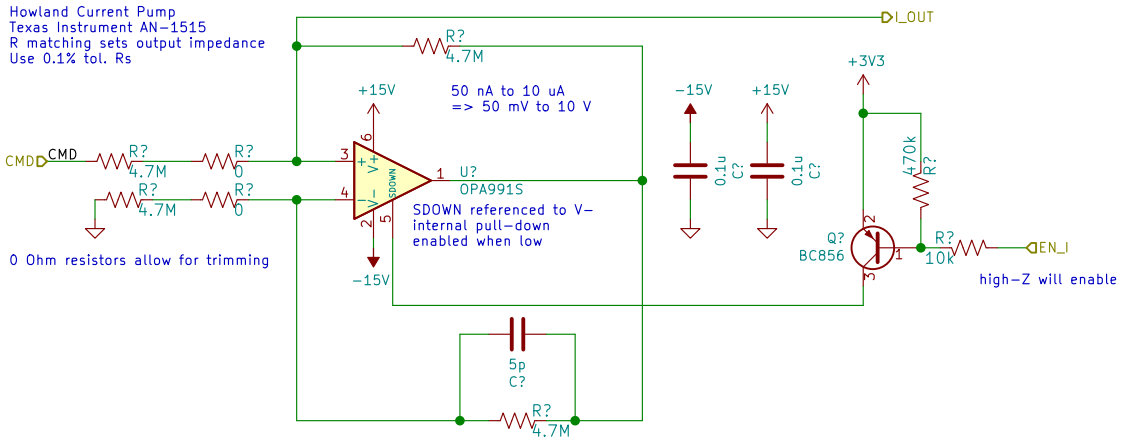


Sheet: /dac4/		
File: dac.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 15/18



Sheet: /dac5/		
File: dac.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 16/18


U?
DAC80508ZRTER
VDD
VIO
SCLK
SDI
SDO_ALARM
CS_N
REF
GND
PAD
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT[0..7]
Use internal reference
0.1 Ohm output impedance
U?A
OPA2156xD
U?C
OPA2156xD
Sheet: howland_ipump
CMD
I_OUT
EN_IPUMP
EN_I
high-Z will enable
File: howland_ipump.sch
BP_OUT[4..7]
U?
TMUX6136PWR
SEL1
SEL2
S1A
S1B
S2A
S2B
VDD
GND
VSS
D1
D2
NC
ISEL[0]
ISEL[1]
ISEL[2]
ISEL[3]
ISEL[0..3]
DAC_CAL[0..3]
DAC_CAL[0]
DAC_CAL[1]
DAC_CAL[2]
DAC_CAL[3]
0 ==> B to D out
1 ==> A to D out
Sheet: /dac_gp2/
File: dac_gp.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 17/18



Sheet: /dac_gp2/howland_ipump/		
File: howland_ipump.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 18/18