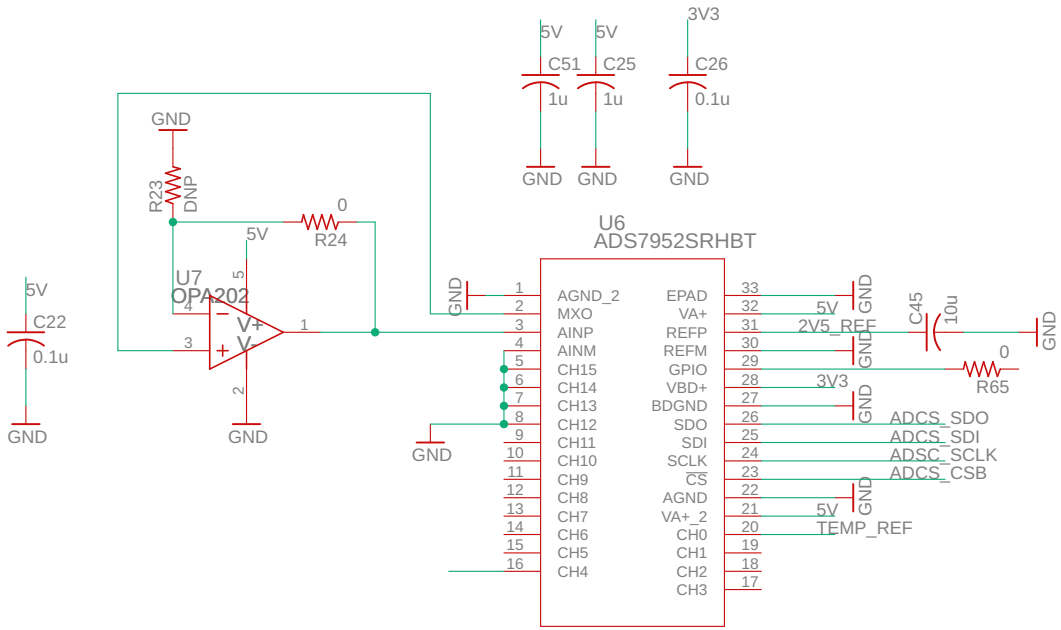
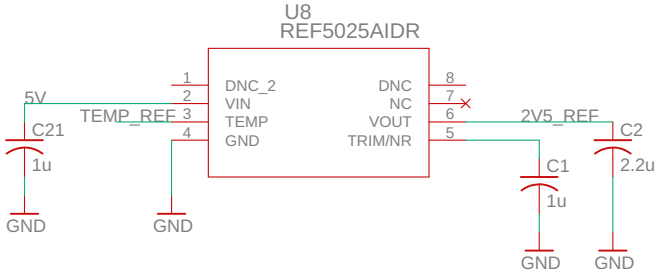


VA+ analog supply.
5V allows Range 2: VREF*2
VBD+ is digital I/O supply = 3.3V
REF from 2V-3V



H1 MOUNT-HOLE3.0
H2 MOUNT-HOLE3.0
H3 MOUNT-HOLE3.0
H4 MOUNT-HOLE3.0

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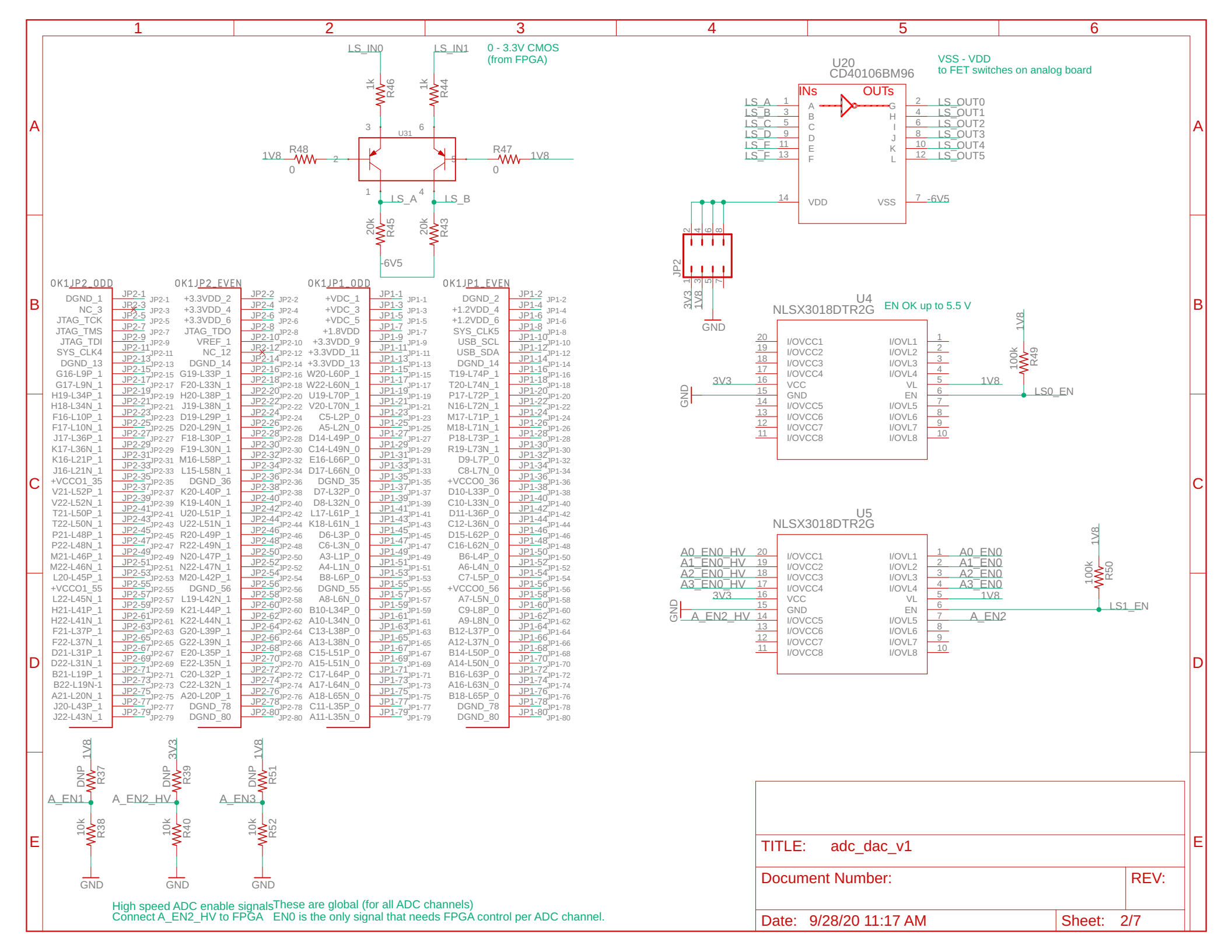
LS_IN0
LS_IN1
0 - 3.3V CMOS
(from FPGA)
1k
R46
1k
R44
U31
1V8
R48
0
R47
1V8
0
LS_A
LS_B
20k
R45
20k
R43
-6V5
U20
CD40106BM96
VSS - VDD
to FET switches on analog board
INs
OUTs
LS_A
LS_B
LS_C
LS_D
LS_E
LS_F
LS_OUT0
LS_OUT1
LS_OUT2
LS_OUT3
LS_OUT4
LS_OUT5
VDD
VSS
-6V5
JP2
3V3
1V8
GND
U4
NLSX3018DTR2G
EN OK up to 5.5 V
I/OVCC1
I/OVCC2
I/OVCC3
I/OVCC4
VCC
GND
I/OVCC5
I/OVCC6
I/OVCC7
I/OVCC8
I/OVL1
I/OVL2
I/OVL3
I/OVL4
VL
EN
I/OVL5
I/OVL6
I/OVL7
I/OVL8
100k
R49
LS0_EN
U5
NLSX3018DTR2G
A0_EN0_HV
A1_EN0_HV
A2_EN0_HV
A3_EN0_HV
A_EN2_HV
A0_EN0
A1_EN0
A2_EN0
A3_EN0
A_EN2
100k
R50
LS1_EN
OK1JP2_ODD
OK1JP2_EVEN
OK1JP1_ODD
OK1JP1_EVEN
DNP
R37
R39
R51
A_EN1
A_EN2_HV
A_EN3
10k
R38
R40
R52
GND
High speed ADC enable signals
Connect A_EN2_HV to FPGA
These are global (for all ADC channels)
EN0 is the only signal that needs FPGA control per ADC channel.
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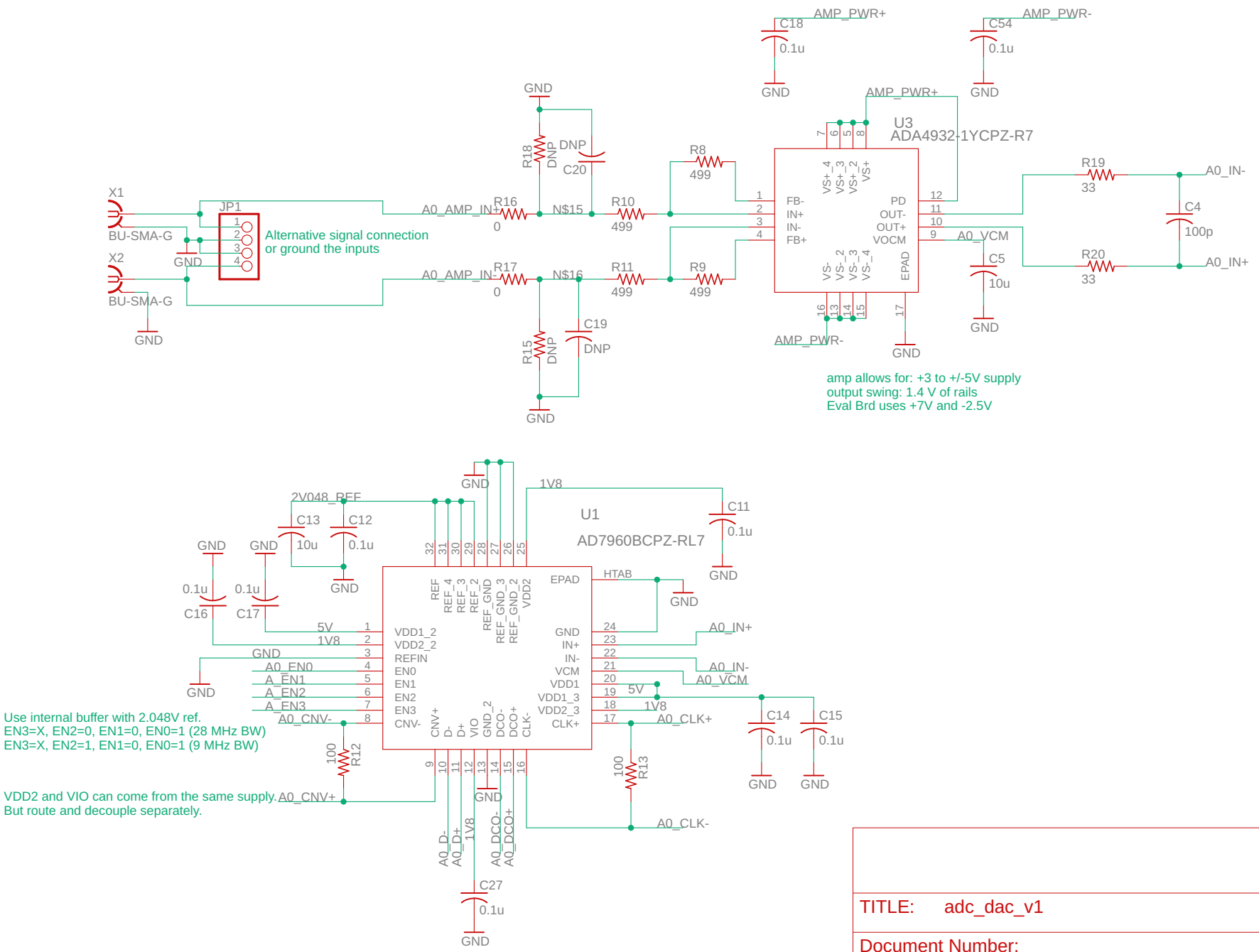

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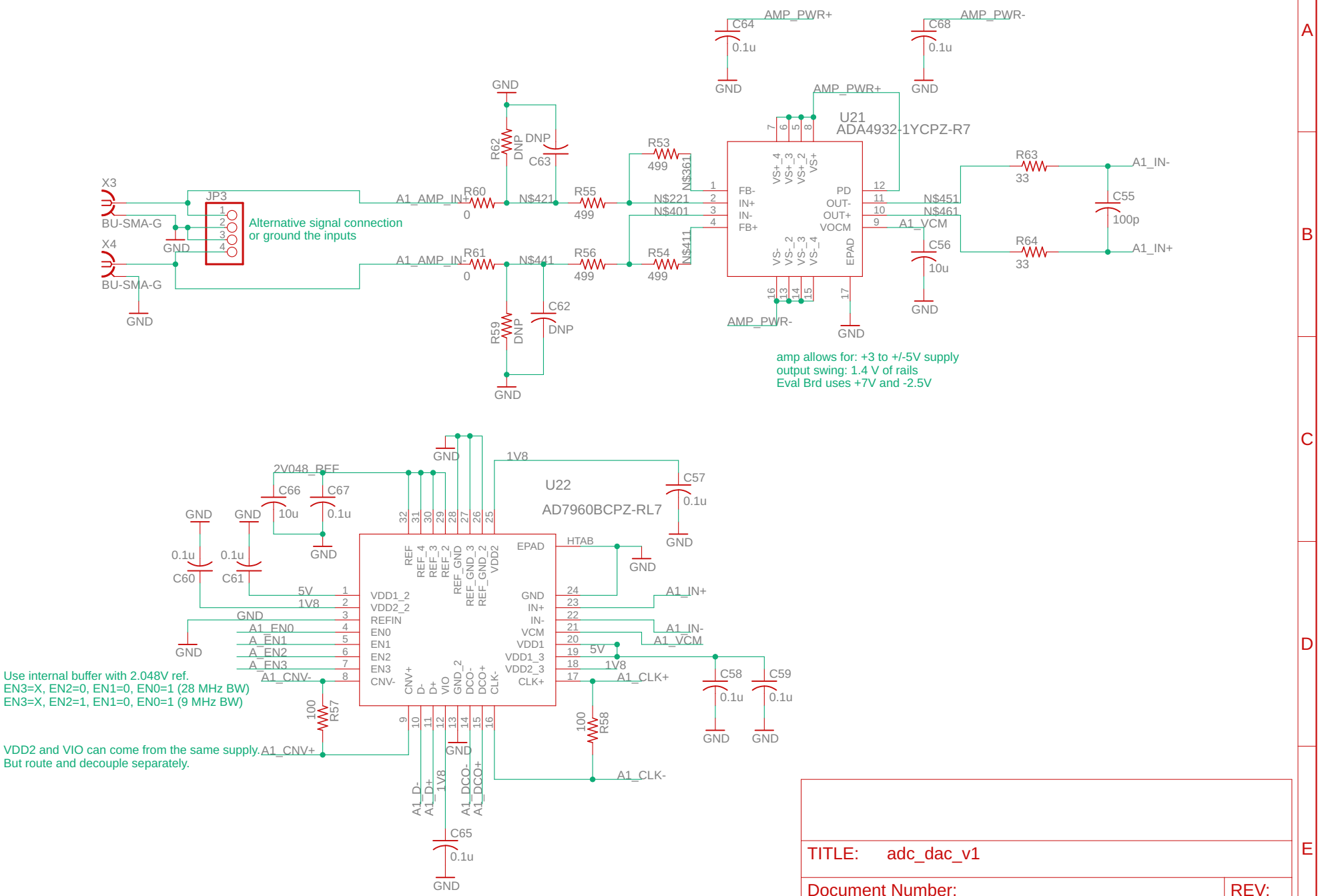

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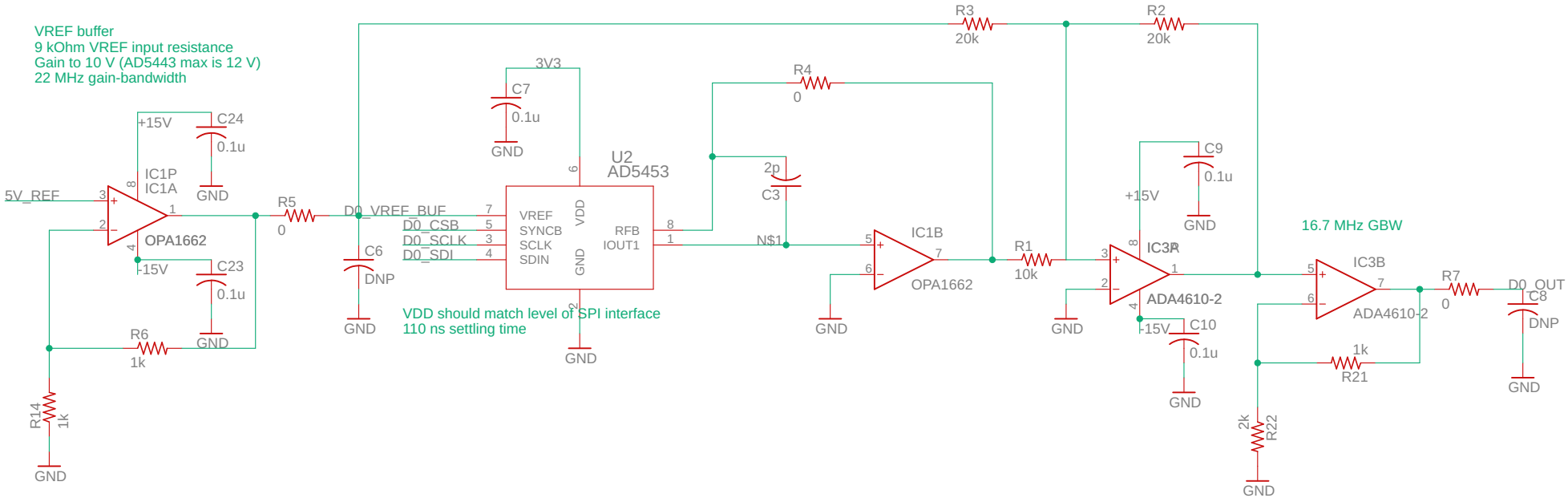

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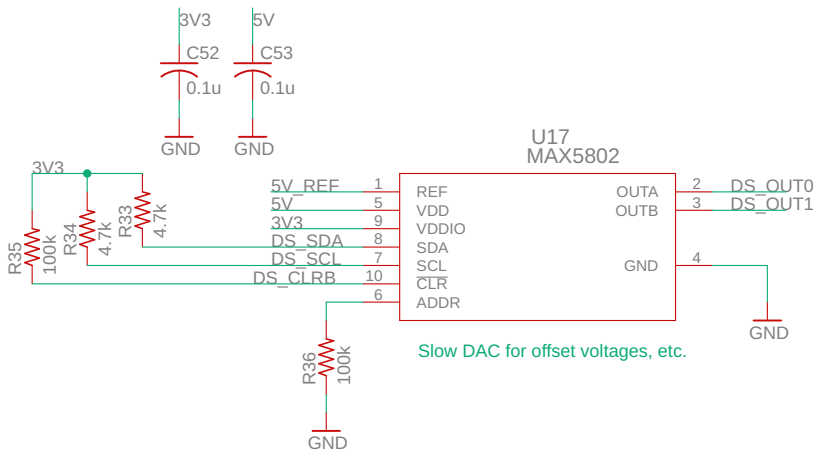

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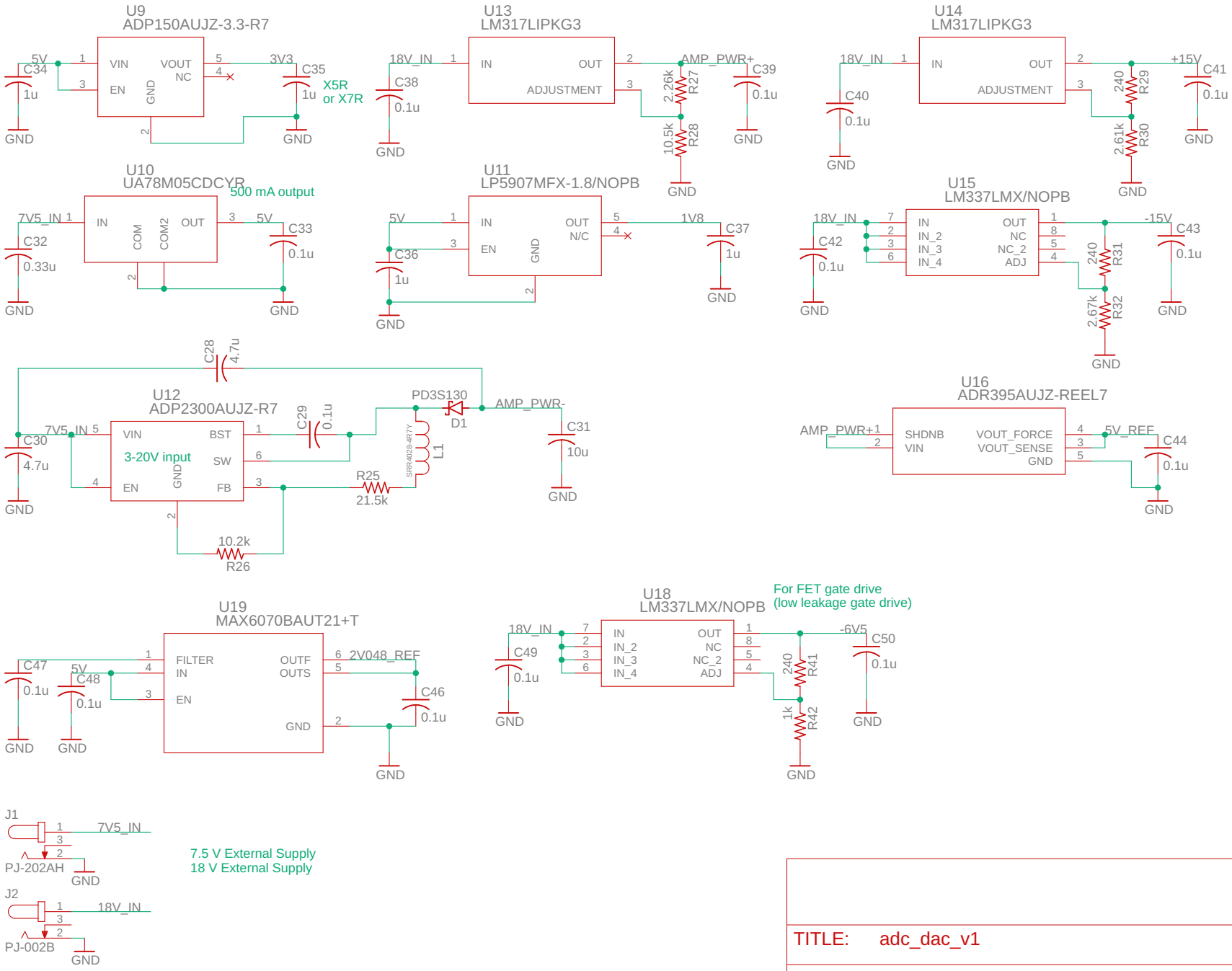

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