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OK1JP2_ODD

DGND_1	JP2-1	GND
NC_3	JP2-3	
JTAG_TCK	JP2-5	JP2-5
JTAG_TMS	JP2-7	JP2-7
JTAG_TDI	JP2-9	JP2-9
SYS_CLK4	JP2-11	JP2-11
DGND_13	JP2-13	A_EN3
G16-L9P_1	JP2-15	GND
G17-L9N_1	JP2-17	JP2-15
H19-L34P_1	JP2-19	LS_IN0
H18-L34N_1	JP2-21	LS_IN1
F16-L10P_1	JP2-23	LS_IN2
F17-L10N_1	JP2-25	LS_IN3
J17-L36P_1	JP2-27	LS_IN5
K17-L36N_1	JP2-29	D3_CSB
K16-L21P_1	JP2-31	D3_SDI
J16-L21N_1	JP2-33	D3_SCLK
+VCCO1_35	JP2-35	D2_CSB
V21-L52P_1	JP2-37	JP2-35
V22-L52N_1	JP2-39	D2_SDI
T21-L50P_1	JP2-41	D2_SCLK
T22-L50N_1	JP2-43	D0_CSB
P21-L48P_1	JP2-45	D0_SDI
P22-L48N_1	JP2-47	D0_SCLK
M21-L46P_1	JP2-49	D1_CSB
M22-L46N_1	JP2-51	D1_SDI
L20-L45P_1	JP2-53	D1_SCLK
+VCCO1_55	JP2-55	JP2-53
L22-L45N_1	JP2-57	JP2-55
H21-L41P_1	JP2-59	GPIO_3V3_0
H22-L41N_1	JP2-61	GPIO_3V3_2
F21-L37P_1	JP2-63	GP_1
F22-L37N_1	JP2-65	GP_3
D21-L31P_1	JP2-67	GP_5
D22-L31N_1	JP2-69	GP_7
B21-L19P_1	JP2-71	GP_9
B22-L19N_1	JP2-73	GP_11
A21-L20N_1	JP2-75	GP_SCL
J20-L43P_1	JP2-77	GP_17
J22-L43N_1	JP2-79	JP2-77

OK1JP2_EVEN

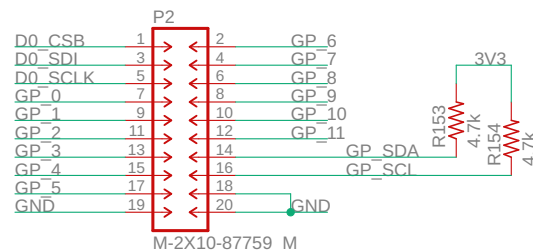
+3.3VDD_2	JP2-2	JP2-2
+3.3VDD_4	JP2-4	JP2-4
+3.3VDD_6	JP2-6	JP2-6
JTAG_TDO	JP2-8	JP2-8
VREF_1	JP2-10	JP2-10
NC_12	JP2-12	
DGND_14	JP2-14	GND
G19-L33P_1	JP2-16	ADCS_SDO
F20-L33N_1	JP2-18	ADCS_SDI
H20-L38P_1	JP2-20	ADCS_SCLK
J19-L38N_1	JP2-22	ADCS_CSB
D19-L29P_1	JP2-24	LS_IN4
D20-L29N_1	JP2-26	JP2-26
F18-L30P_1	JP2-28	DS_SDA
F19-L30N_1	JP2-30	DS_SCL
M16-L58P_1	JP2-32	DS_CLRFB
L15-L58N_1	JP2-34	JP2-34
DGND_36	JP2-36	GND
K20-L40P_1	JP2-38	JP2-38
K19-L40N_1	JP2-40	JP2-40
U20-L51P_1	JP2-42	JP2-42
U22-L51N_1	JP2-44	JP2-44
R20-L49P_1	JP2-46	JP2-46
R22-L49N_1	JP2-48	JP2-48
N20-L47P_1	JP2-50	JP2-50
N22-L47N_1	JP2-52	JP2-52
M20-L42P_1	JP2-54	JP2-54
DGND_56	JP2-56	GND
L19-L42N_1	JP2-58	GPIO_3V3_1
K21-L44P_1	JP2-60	GP_0
K22-L44N_1	JP2-62	GP_2
G20-L39P_1	JP2-64	GP_4
G22-L39N_1	JP2-66	GP_6
E20-L35P_1	JP2-68	GP_8
E22-L35N_1	JP2-70	GP_10
C20-L32P_1	JP2-72	GP_SDA
C22-L32N_1	JP2-74	GP_SCL
A20-L20P_1	JP2-76	JP2-76
DGND_78	JP2-78	JP2-78
DGND_80	JP2-80	GND

OK1JP1_ODD

+VDC_1	JP1-1	JP1-1
+VDC_3	JP1-3	JP1-3
+VDC_5	JP1-5	JP1-5
+1.8VDD	JP1-7	JP1-7
+3.3VDD_9	JP1-9	JP1-9
+3.3VDD_11	JP1-11	JP1-11
+3.3VDD_13	JP1-13	JP1-13
W20-L60P_1	JP1-15	JP1-15
W22-L60N_1	JP1-17	JP1-17
U19-L70P_1	JP1-19	JP1-19
V20-L70N_1	JP1-21	JP1-21
C5-L2P_0	JP1-23	A0_CNV_P
A5-L2N_0	JP1-25	A0_CNV_N
D14-L49P_0	JP1-27	A0_D_P
C14-L49N_0	JP1-29	A0_D_N
E16-L66P_0	JP1-31	A0_DCO_P
D17-L66N_0	JP1-33	A0_DCO_N
DGND_35	JP1-35	JP1-35
D7-L32P_0	JP1-37	A0_CLK_P
D8-L32N_0	JP1-39	A0_CLK_N
L17-L61P_1	JP1-41	JP1-41
K18-L61N_1	JP1-43	JP1-43
D6-L3P_0	JP1-45	JP1-45
C6-L3N_0	JP1-47	JP1-47
A3-L1P_0	JP1-49	JP1-49
A4-L1N_0	JP1-51	JP1-51
B8-L6P_0	JP1-53	A3_EN0_HV
DGND_55	JP1-55	JP1-55
A8-L6N_0	JP1-57	A1_EN0_HV
B10-L34P_0	JP1-59	A1_CLK_P
A10-L34N_0	JP1-61	A1_CLK_N
C13-L38P_0	JP1-63	A2_CNV_P
A13-L38N_0	JP1-65	A2_CNV_N
C15-L51P_0	JP1-67	A2_D_P
A15-L51N_0	JP1-69	A2_D_N
C17-L64P_0	JP1-71	A2_DCO_P
A17-L64N_0	JP1-73	A2_DCO_N
A18-L65N_0	JP1-75	A2_CLK_N
C11-L35P_0	JP1-77	A3_CLK_P
A11-L35N_0	JP1-79	A3_CLK_N

OK1JP1_EVEN

DGND_2	JP1-2	GND
+1.2VDD_4	JP1-4	JP1-4
+1.2VDD_6	JP1-6	JP1-6
SYS_CLK5	JP1-8	LSO_EN
USB_SCL	JP1-10	JP1-10
USB_SDA	JP1-12	A_EN1
DGND_14	JP1-14	JP1-14
T19-L74P_1	JP1-16	JP1-16
T20-L74N_1	JP1-18	JP1-18
P17-L72P_1	JP1-20	JP1-20
N16-L72N_1	JP1-22	JP1-22
M17-L71P_1	JP1-24	JP1-24
M18-L71N_1	JP1-26	JP1-26
P18-L73P_1	JP1-28	JP1-28
R19-L73N_1	JP1-30	JP1-30
D9-L7P_0	JP1-32	A0_EN0_HV
C8-L7N_0	JP1-34	A_EN2_HV
+VCCO0_36	JP1-36	JP1-36
D10-L33P_0	JP1-38	JP1-38
C10-L33N_0	JP1-40	JP1-40
D11-L36P_0	JP1-42	JP1-42
C12-L36N_0	JP1-44	JP1-44
D15-L62P_0	JP1-46	A1_CNV_P
C16-L62N_0	JP1-48	A1_CNV_N
B6-L4P_0	JP1-50	A1_D_P
A6-L4N_0	JP1-52	A1_D_N
C7-L5P_0	JP1-54	A1_DCO_P
+VCCO0_56	JP1-56	JP1-56
A7-L5N_0	JP1-58	A1_DCO_N
C9-L8P_0	JP1-60	A3_CNV_P
A9-L8N_0	JP1-62	A3_CNV_N
B12-L37P_0	JP1-64	A3_D_P
A12-L37N_0	JP1-66	A3_D_N
B14-L50P_0	JP1-68	A3_DCO_P
A14-L50N_0	JP1-70	A3_DCO_N
B16-L63P_0	JP1-72	A2_EN0_HV
A16-L63N_0	JP1-74	A3_EN0_HV
B18-L65P_0	JP1-76	A2_CLK_P
DGND_78	JP1-78	GND
DGND_80	JP1-80	GND



TITLE: adc_dac_v1

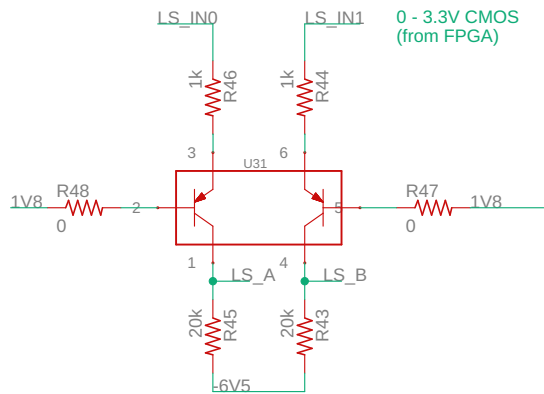
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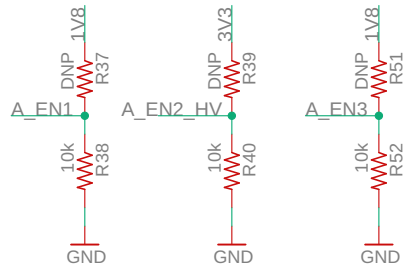
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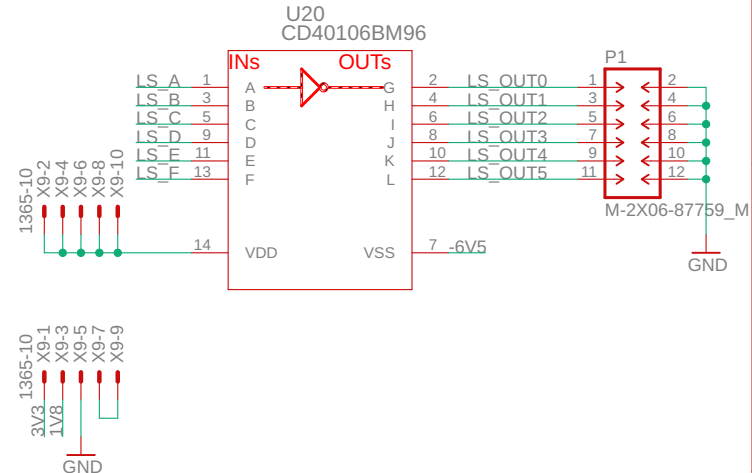
0 - 3.3V CMOS
(from FPGA)



High speed ADC enable signals
Connect A_EN2_HV to FPGA

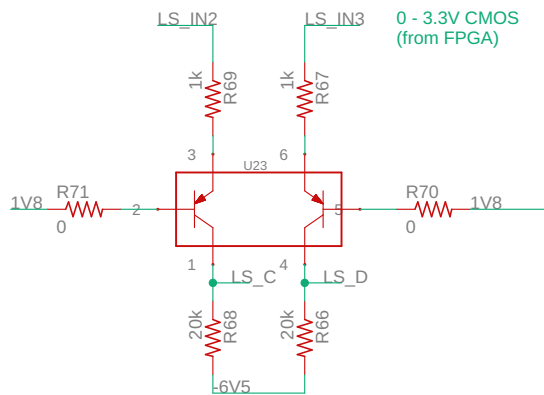
These are global (for all ADC channels)
EN0 is the only signal that needs FPGA control per ADC channel.

B



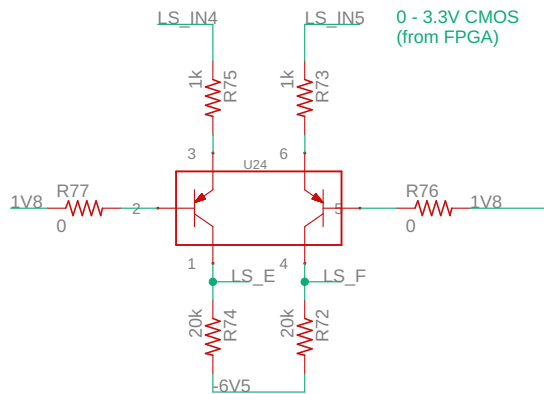
VSS - VDD
to FET switches on analog board

B



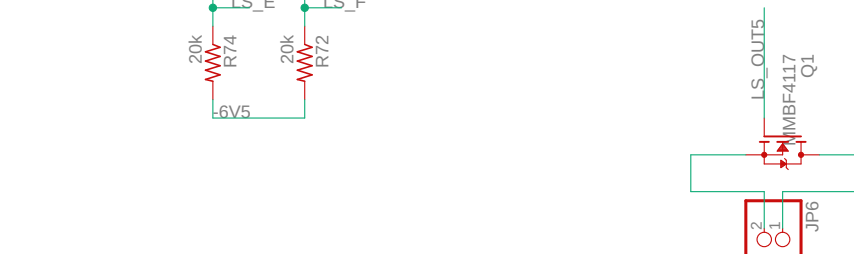
0 - 3.3V CMOS
(from FPGA)

C



0 - 3.3V CMOS
(from FPGA)

D

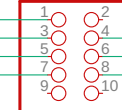


U5
NLSX3018DTR2G

A0_EN0_HV	20	I/OVCC1
A1_EN0_HV	19	I/OVCC2
A2_EN0_HV	18	I/OVCC3
A3_EN0_HV	17	I/OVCC4
3V3	16	VCC
GND	15	GND
A_EN2_HV	14	I/OVCC5
GPIO_3V3_0	13	I/OVCC6
GPIO_3V3_1	12	I/OVCC7
GPIO_3V3_2	11	I/OVCC8

1	A0_EN0
2	A1_EN0
3	A2_EN0
4	A3_EN0
5	1V8
6	LS0_EN
7	A_EN2
8	GPIO_1V8_0
9	GPIO_1V8_1
10	GPIO_1V8_2

JP8



E

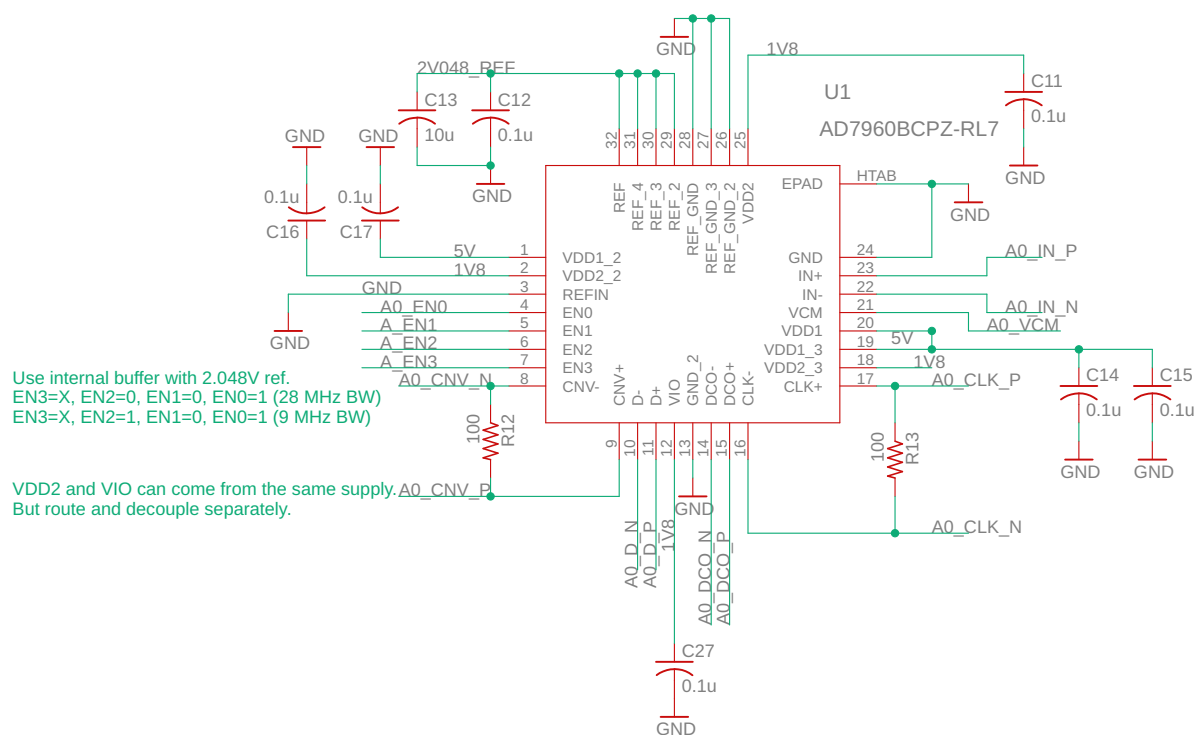
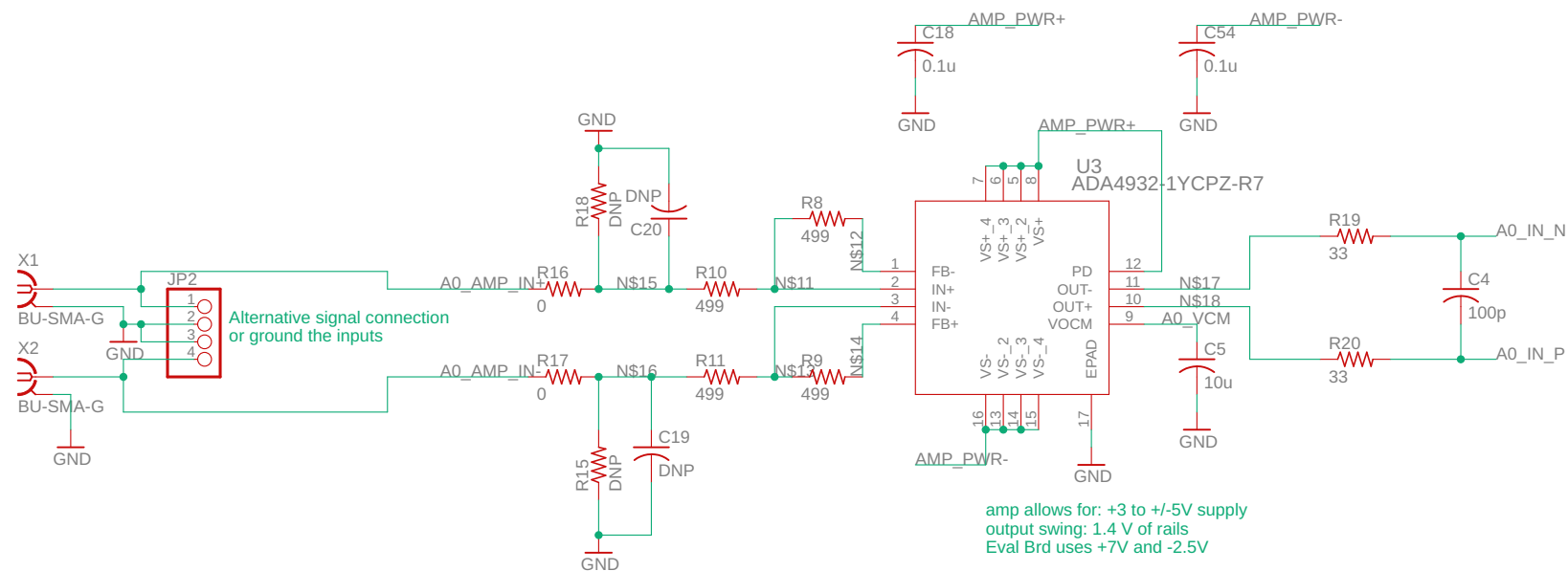
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TITLE: adc_dac_v1	
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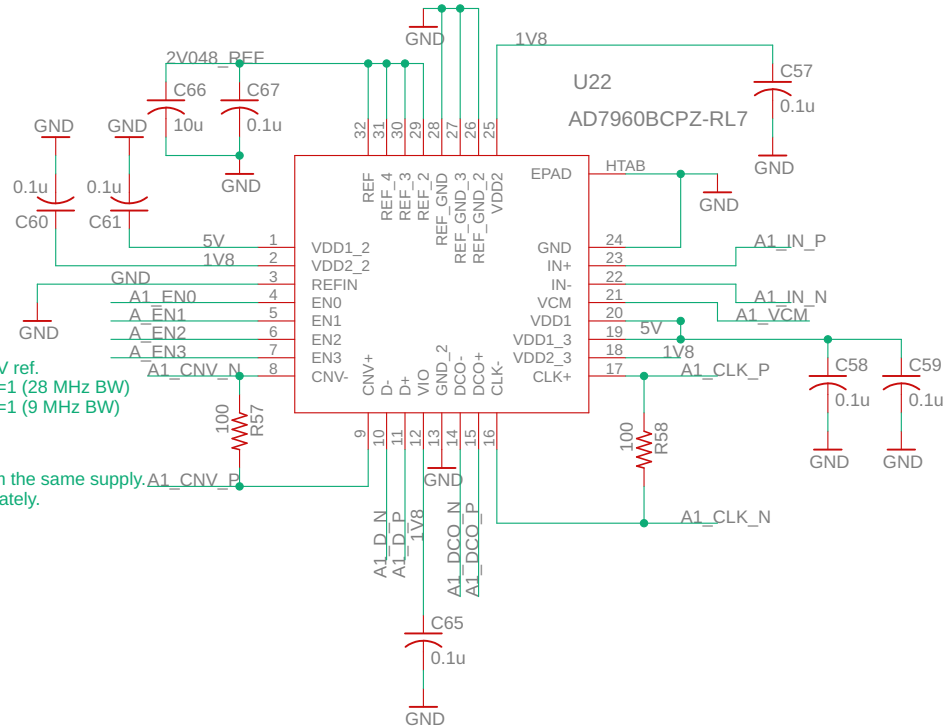
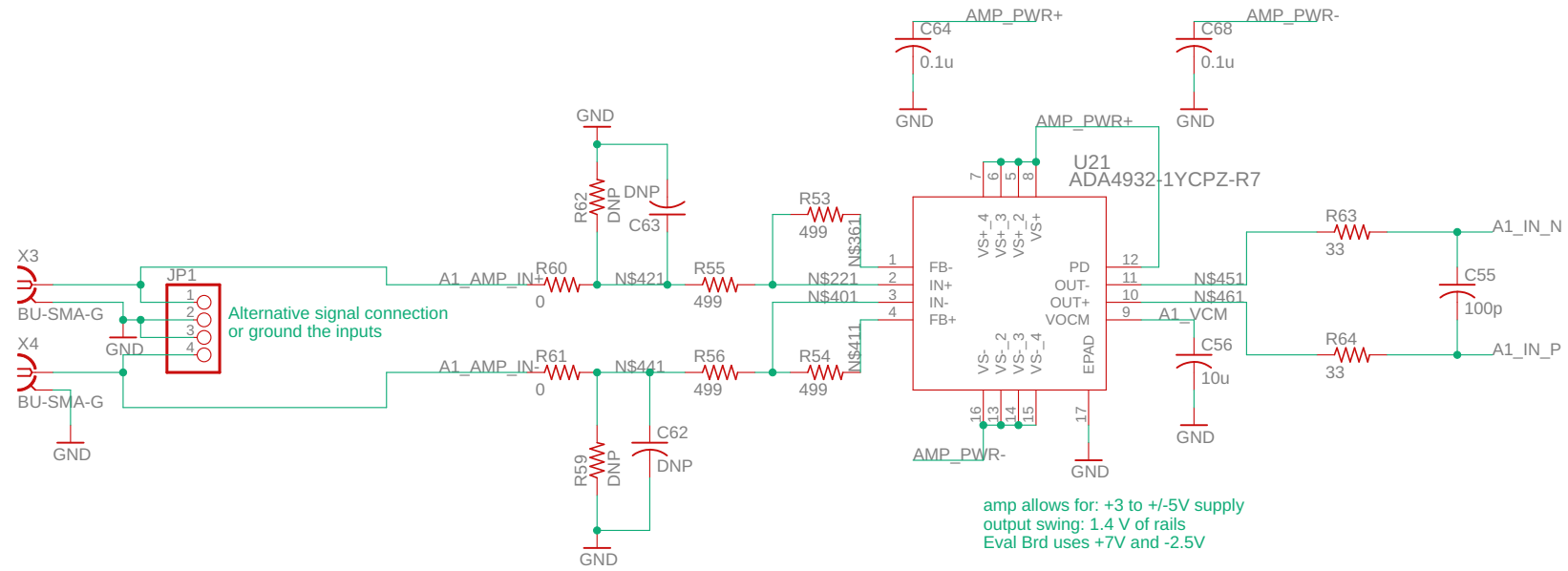
C

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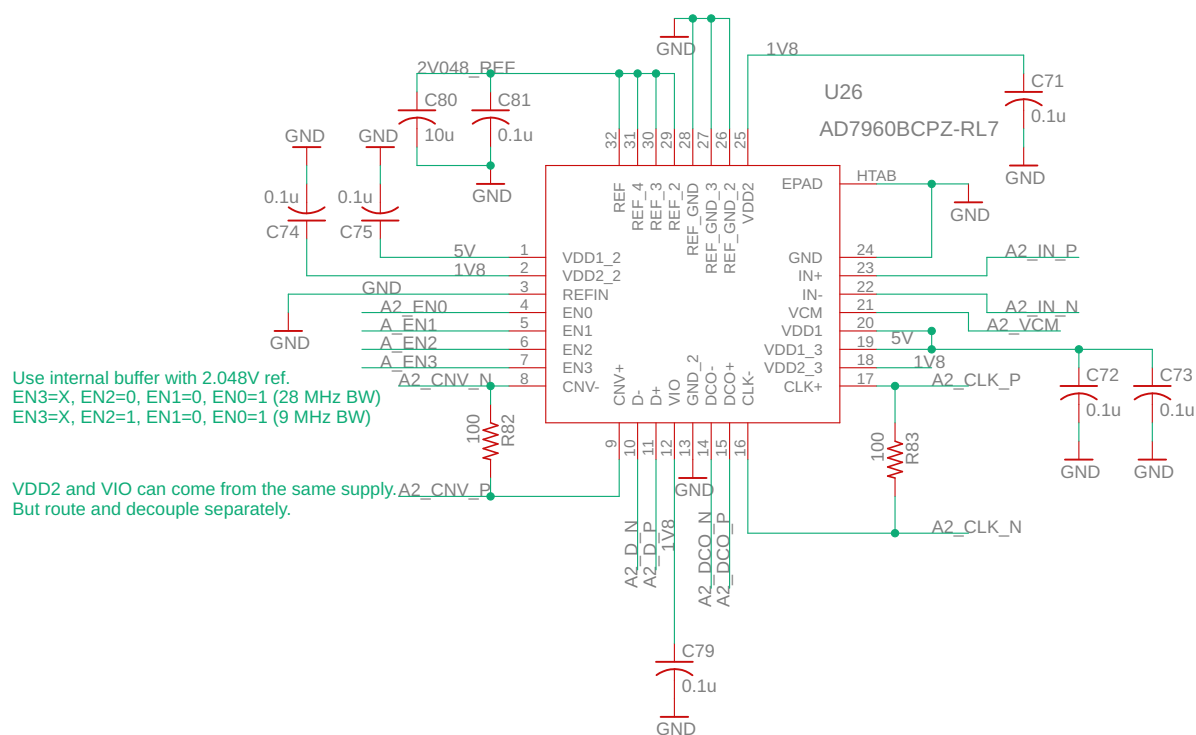
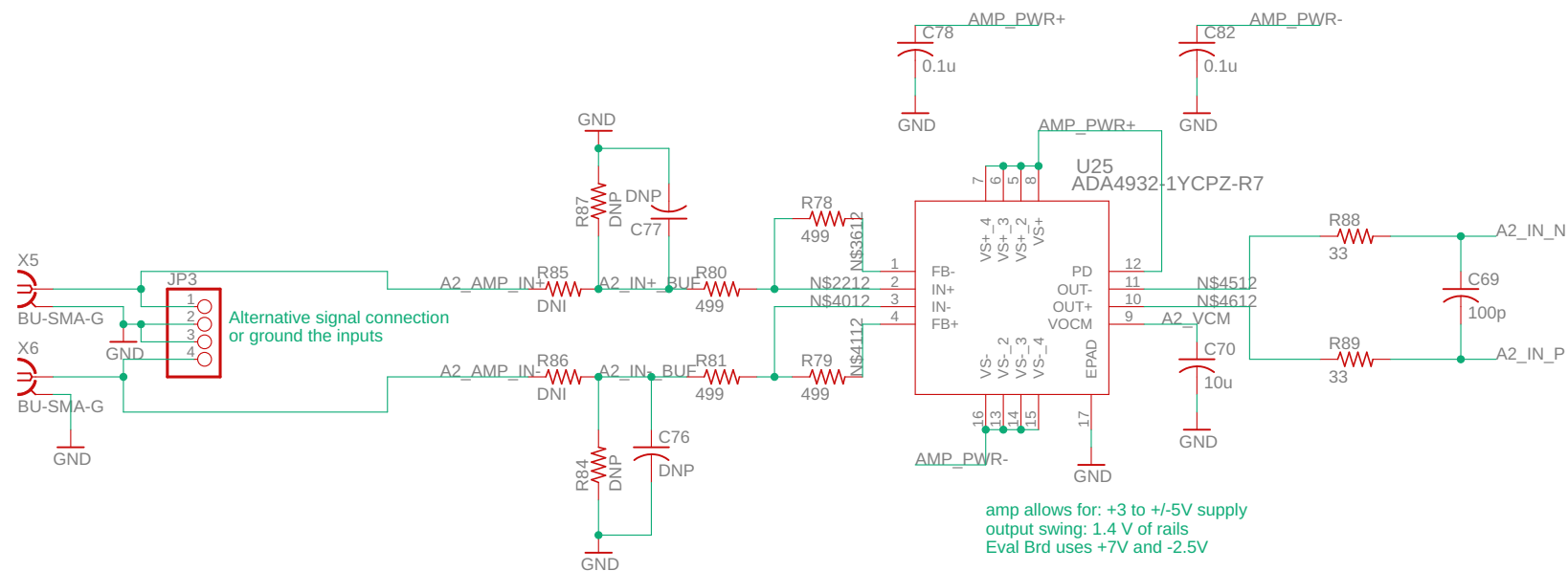
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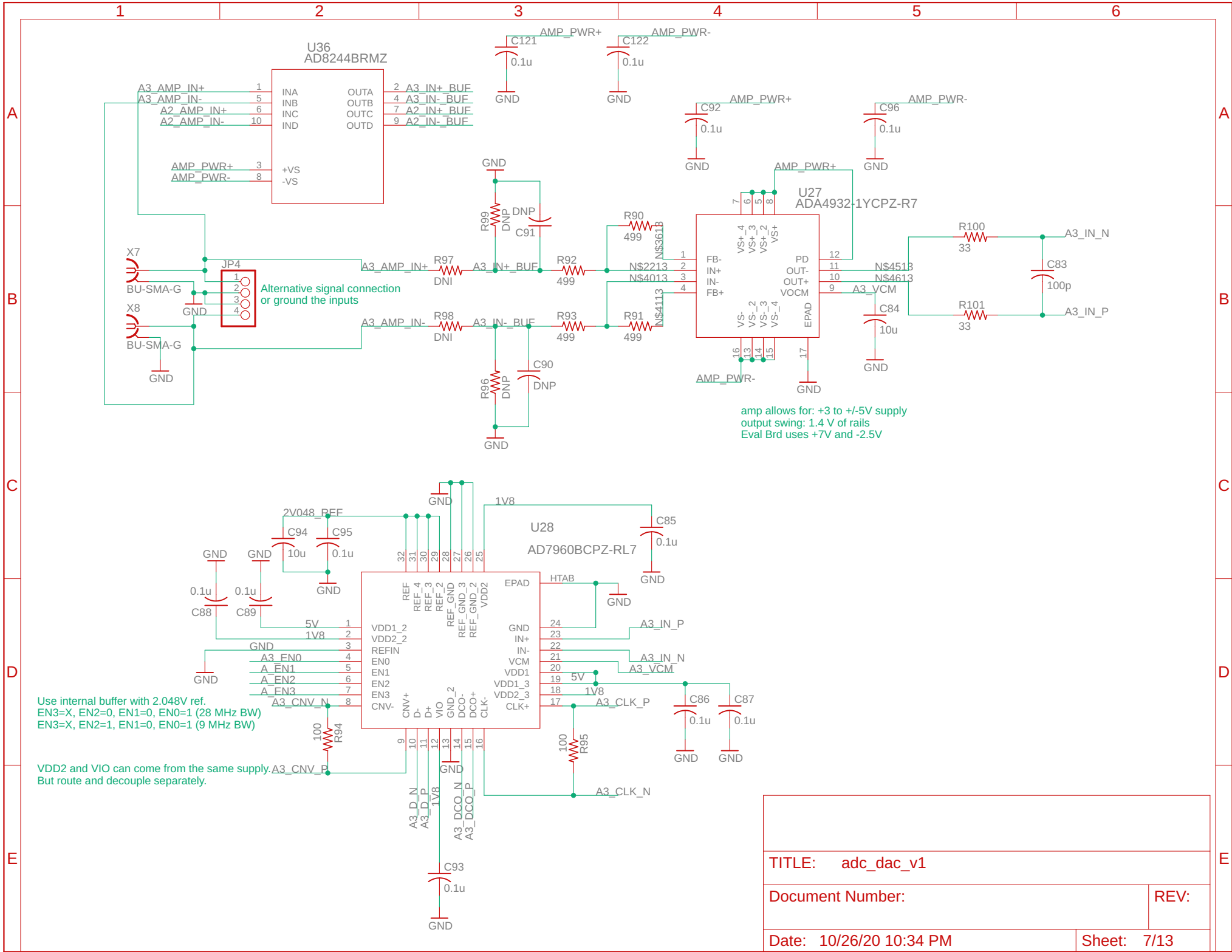
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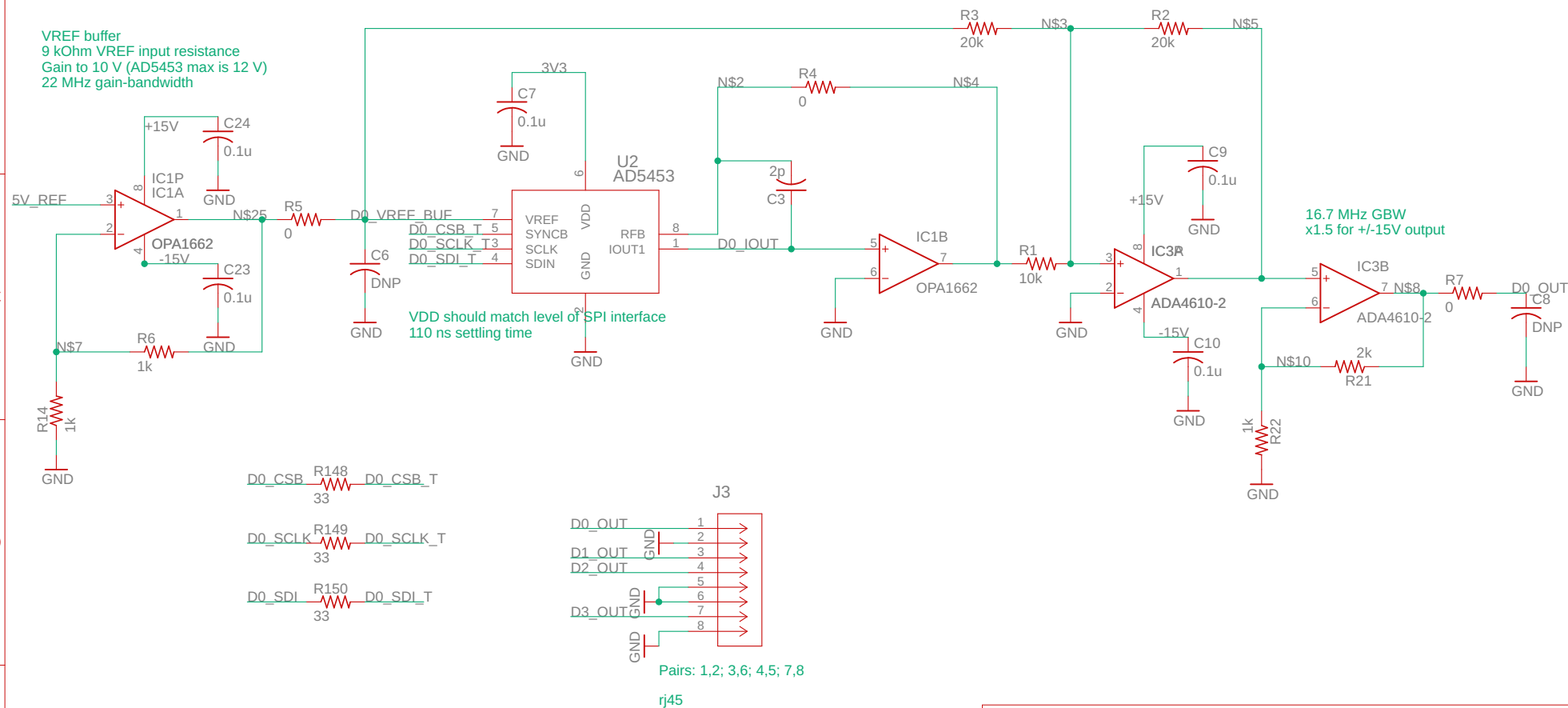
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TITLE: adc_dac_v1

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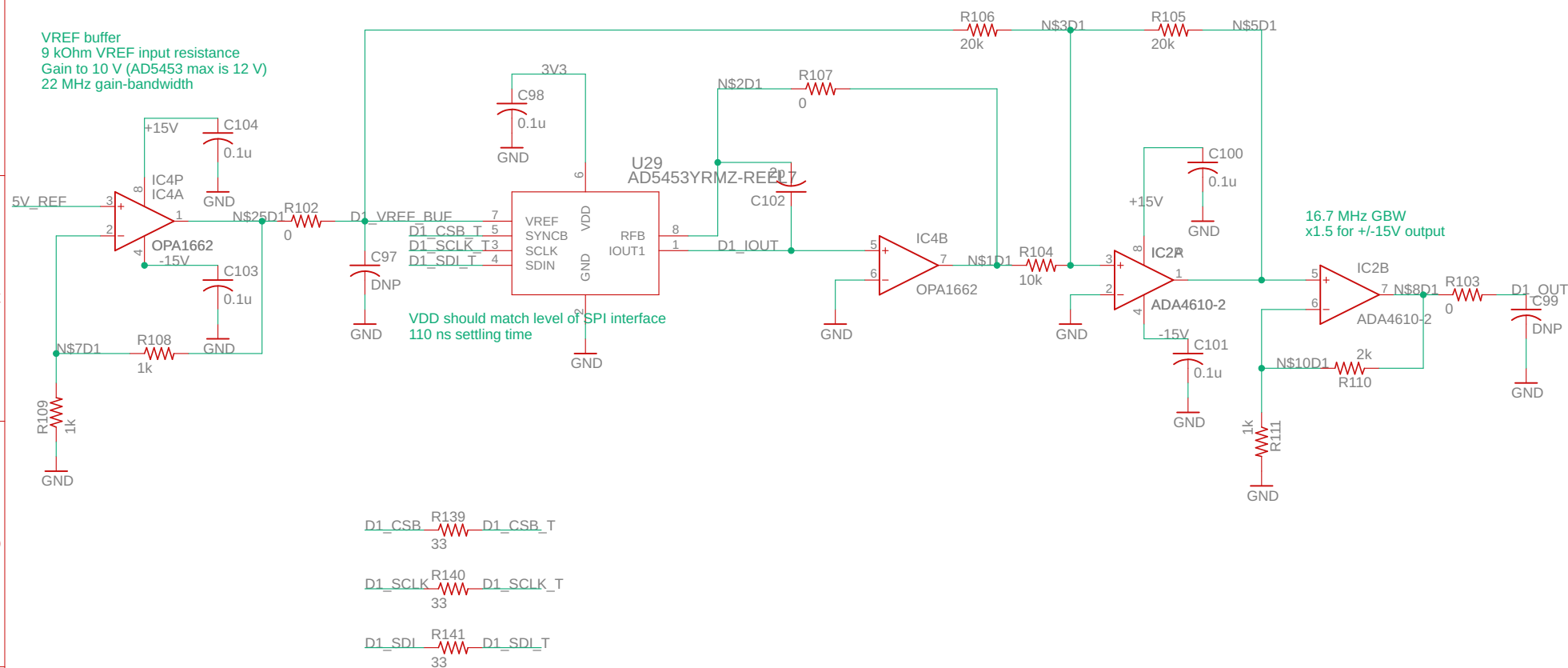
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TITLE: adc_dac_v1

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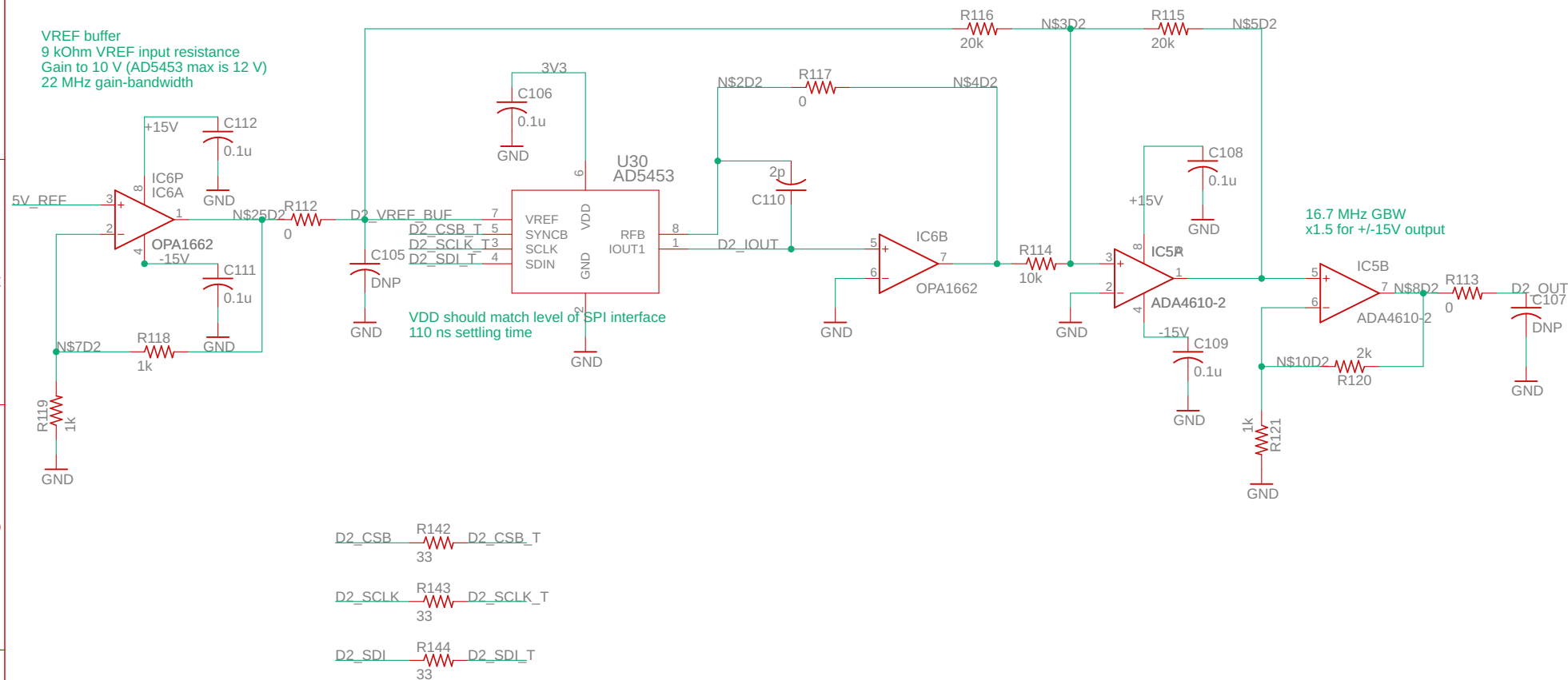
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TITLE: adc_dac_v1

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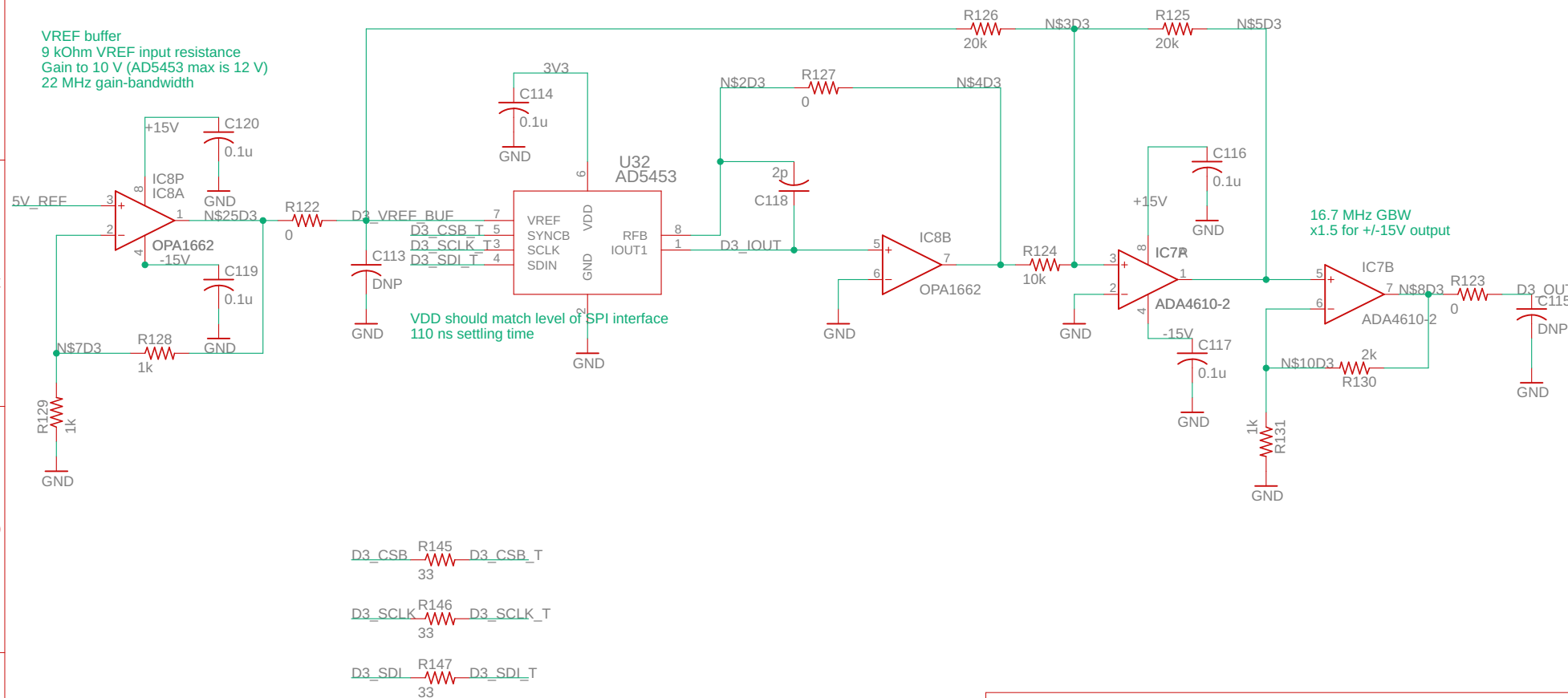
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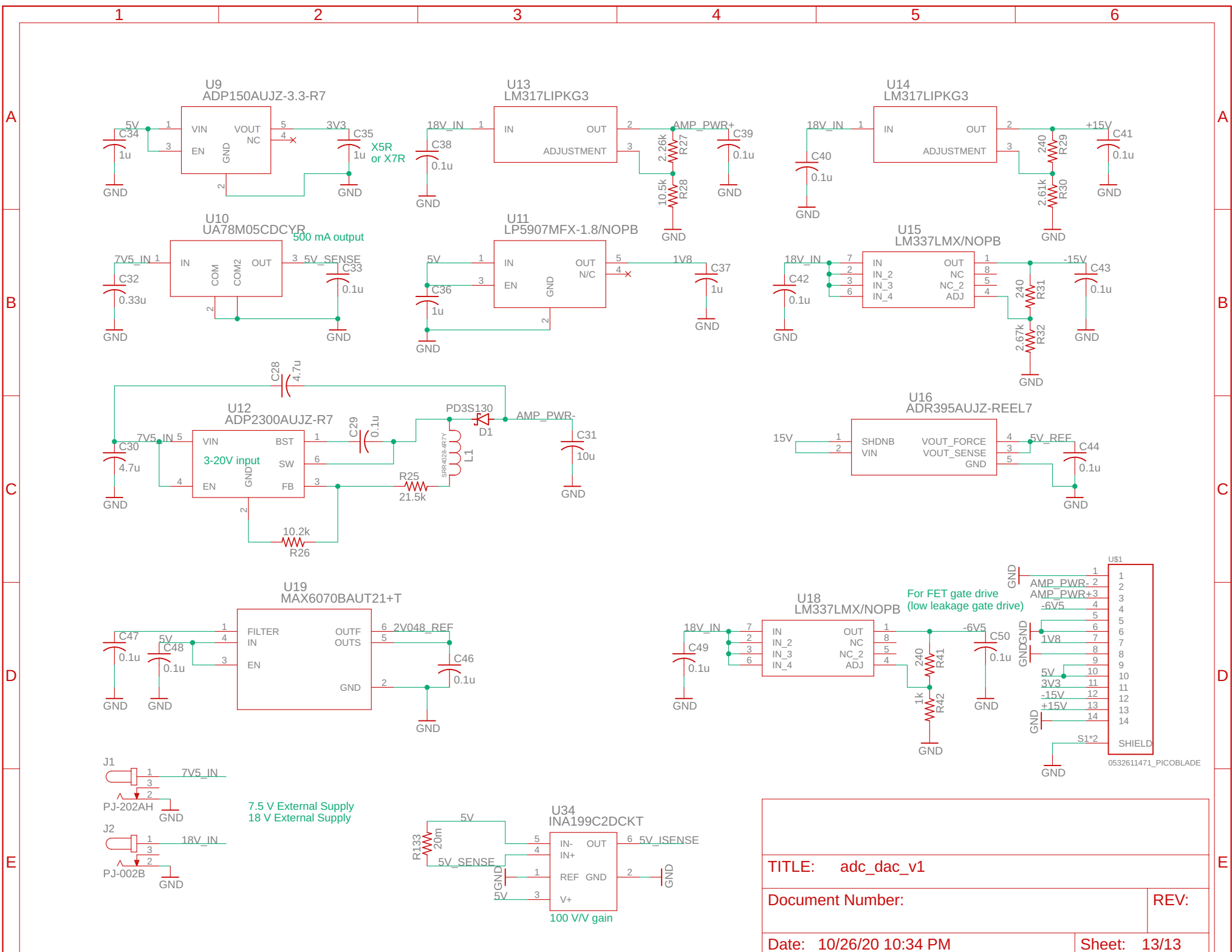
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