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File: howland_ipump.sch

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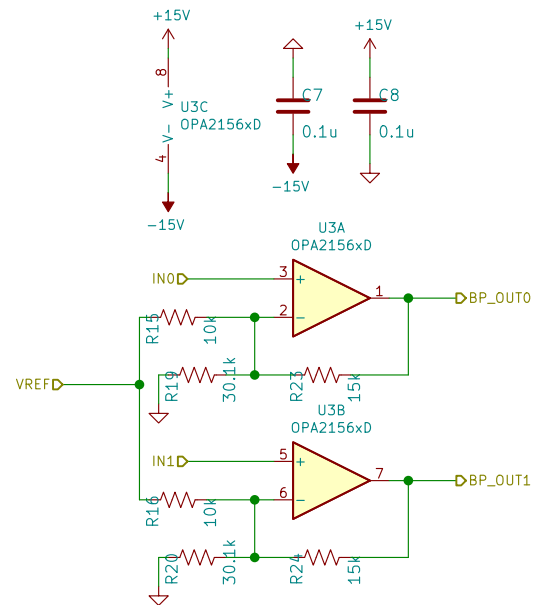
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Rev:

Id: 3/26



Sheet: /dac_gp1/dual_biploar0/
File: dual_bipolar_amp.sch

Title:

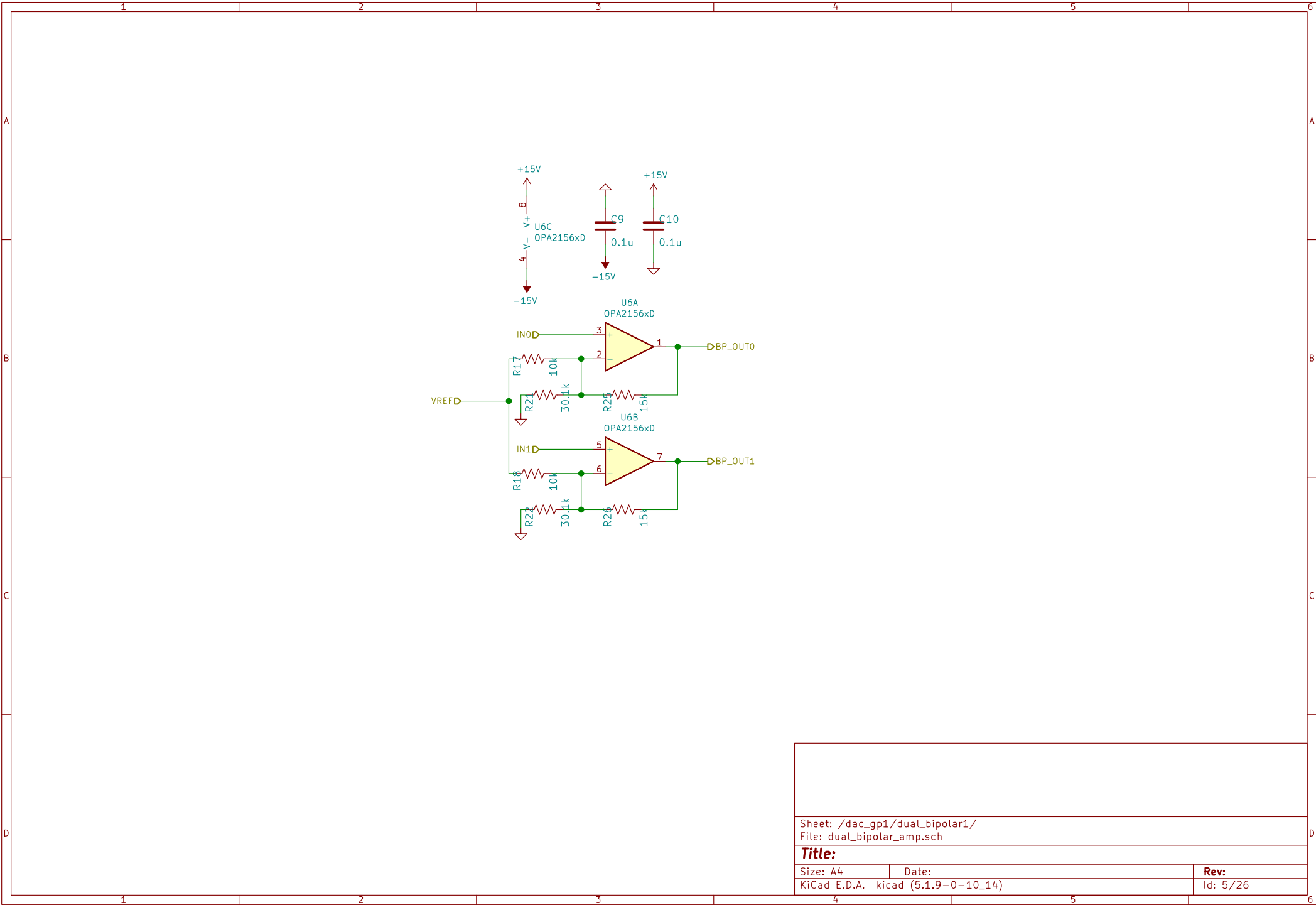
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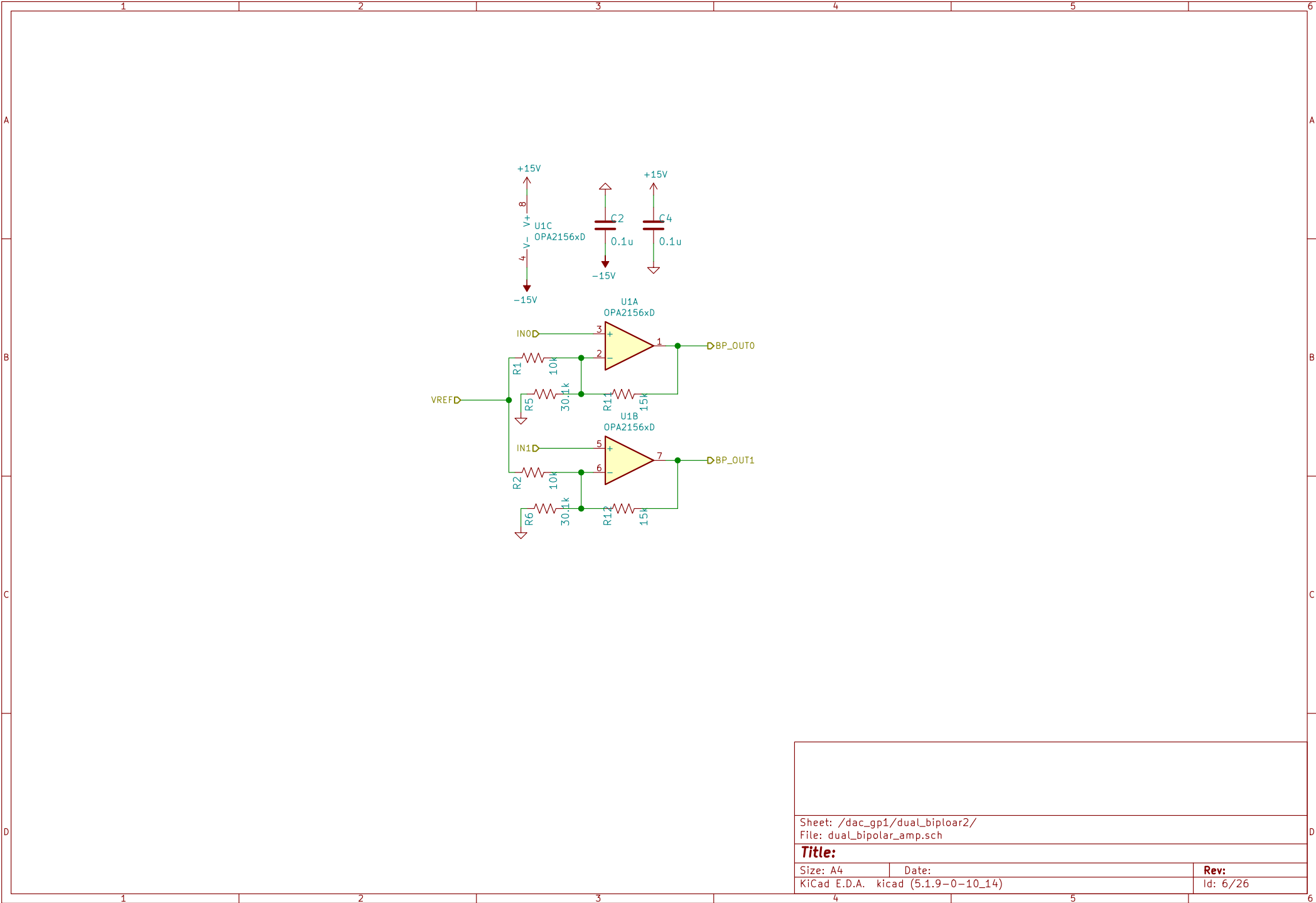
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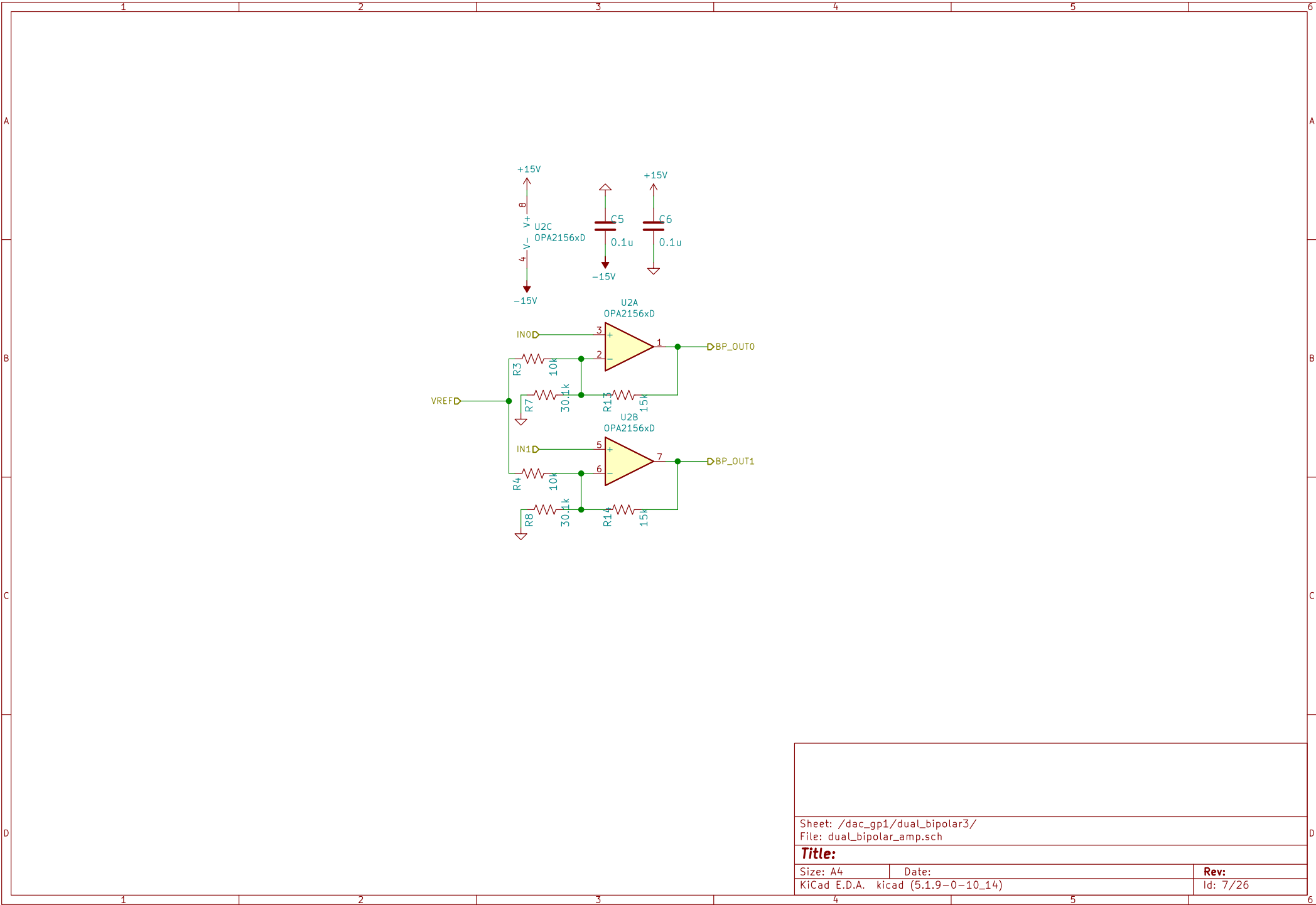
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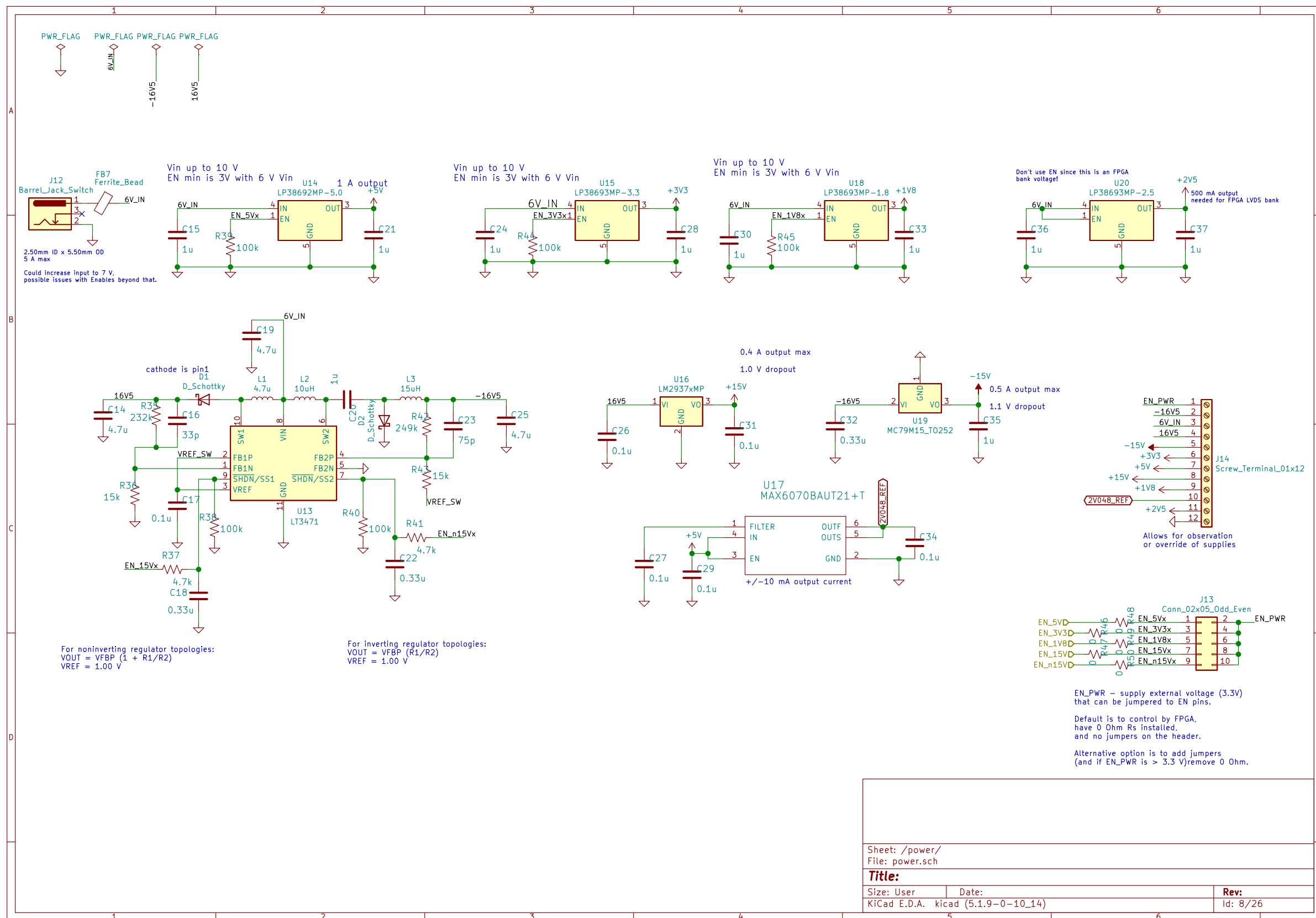
Rev:

Id: 4/26



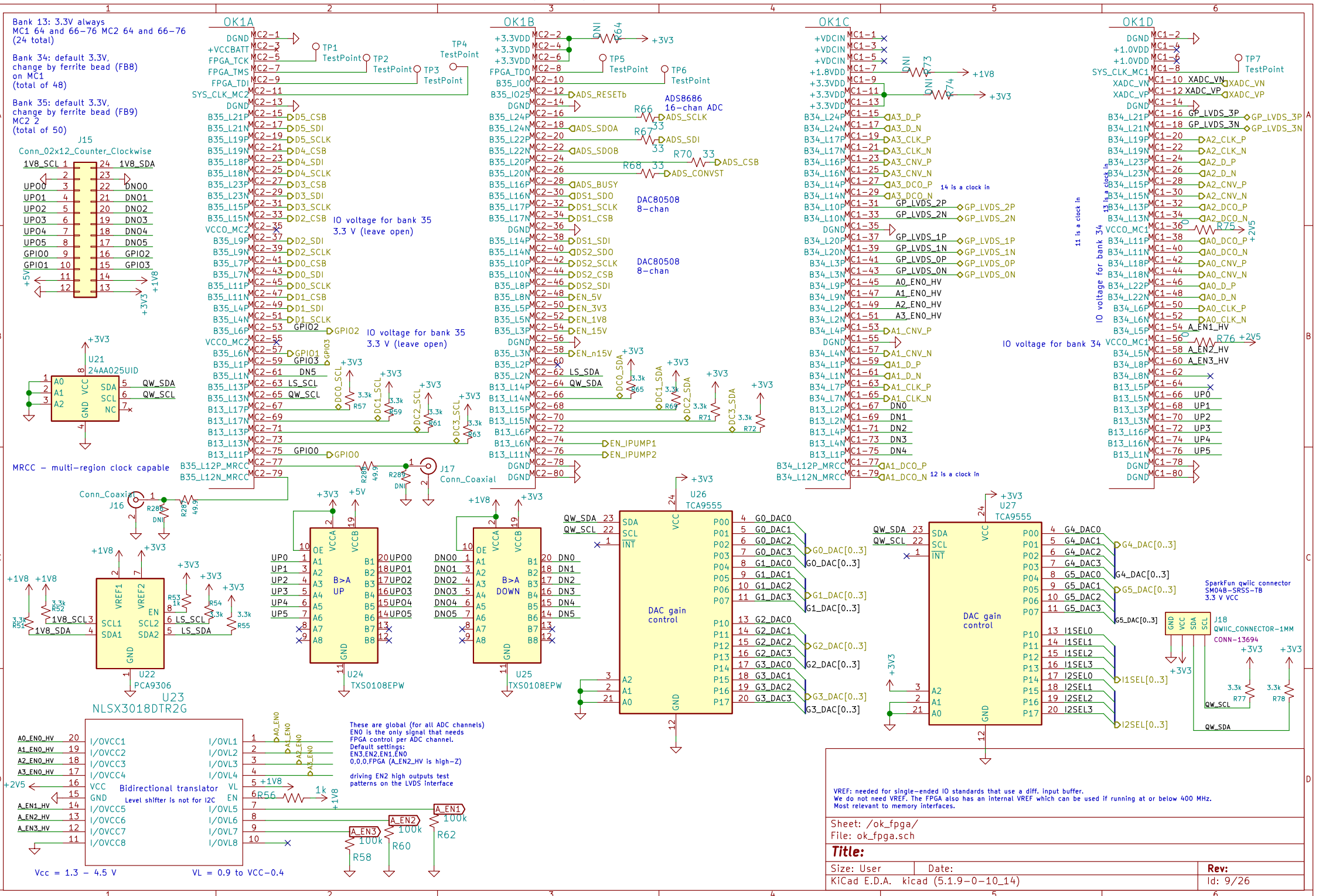






VCCBATT is the battery backup supply for the FPGA's internal volatile memory that stores the key for the AES decryptor (not needed)

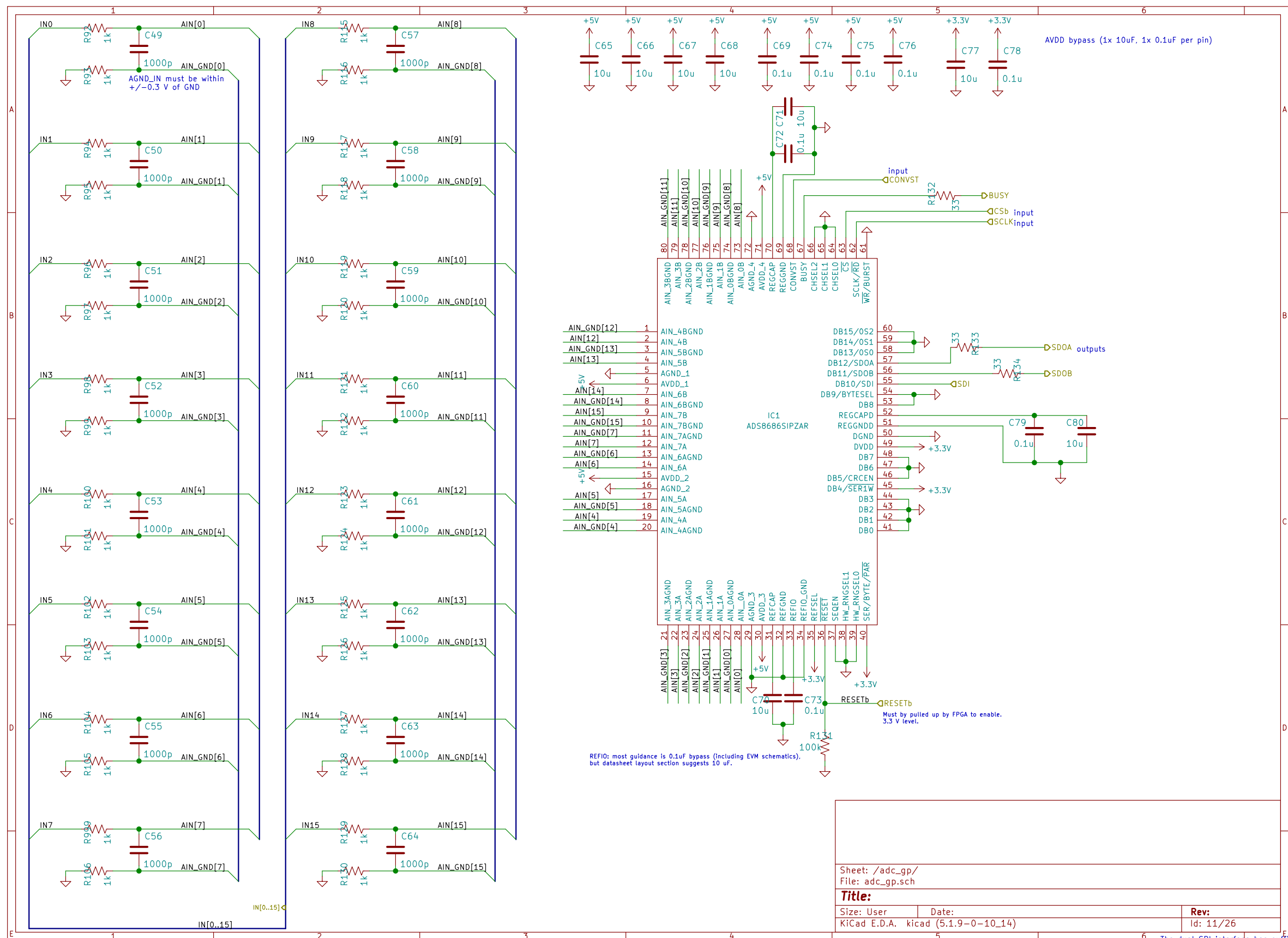
FPGA power: standard "canon-style" 2.1mm / 5.5mm jack. The outer ring is connected to DGND. The center pin is connected to +VDC.



A



Rev:
Id: 10/26



AVDD bypass (1x 10uF, 1x 0.1uF per pin)

AIN_GND[12] 1 AIN_4BGND
AIN[12] 2 AIN_4B
AIN_GND[13] 3 AIN_5BGND
AIN[13] 4 AIN_5B
5 AGND_1
6 AVDD_1
AIN[14] 7 AIN_6B
AIN_GND[14] 8 AIN_6BGND
AIN[15] 9 AIN_7B
AIN_GND[15] 10 AIN_7BGND
AIN_GND[7] 11 AIN_7AGND
AIN[7] 12 AIN_7A
AIN_GND[6] 13 AIN_6AGND
AIN[6] 14 AIN_6A
5V 15 AVDD_2
16 AGND_2
AIN[5] 17 AIN_5A
AIN_GND[5] 18 AIN_5AGND
AIN[4] 19 AIN_4A
AIN_GND[4] 20 AIN_4AGND

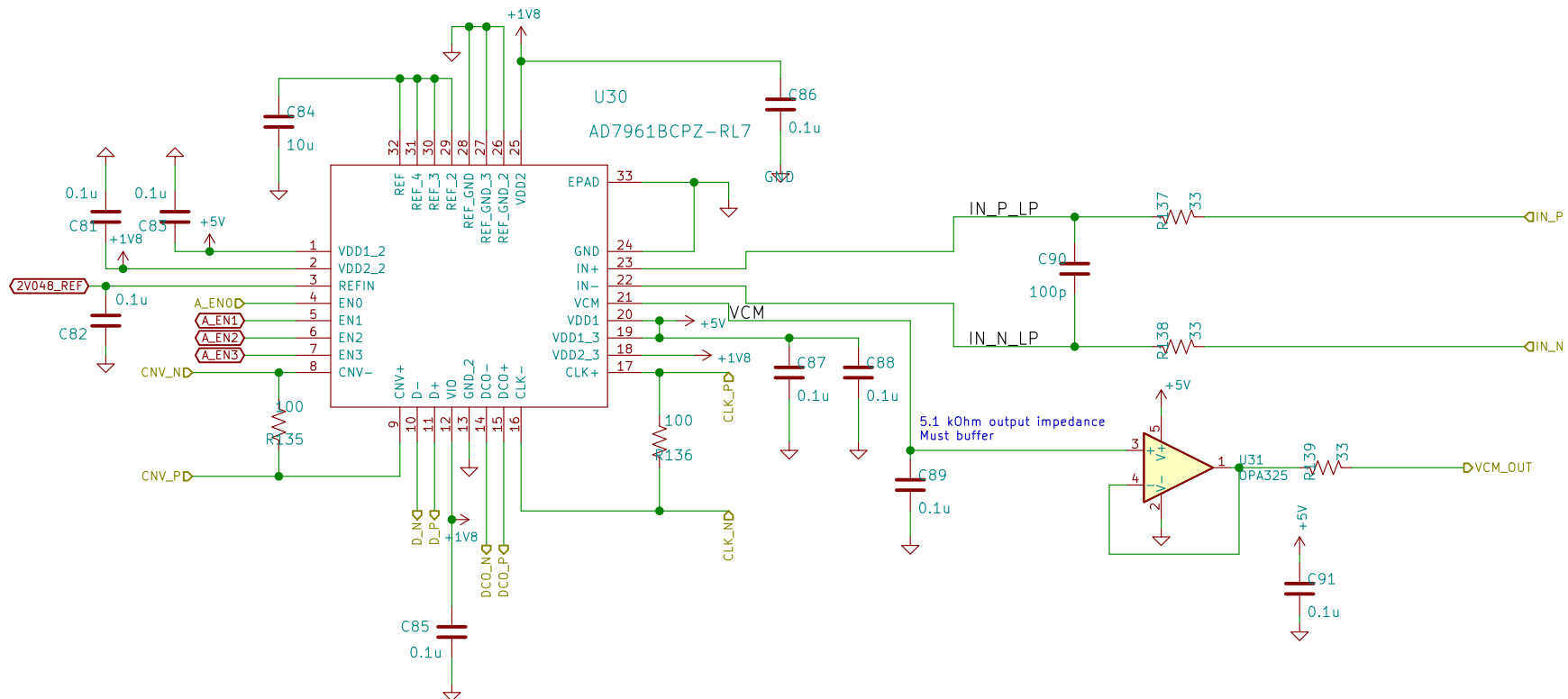
IC1
ADS8686SIPZAR

REFIO: most guidance is 0.1uF bypass (including EVM schematics),
but datasheet layout section suggests 10 uF.

RESEtb
Must be pulled up by FPGA to enable.
3.3 V level.

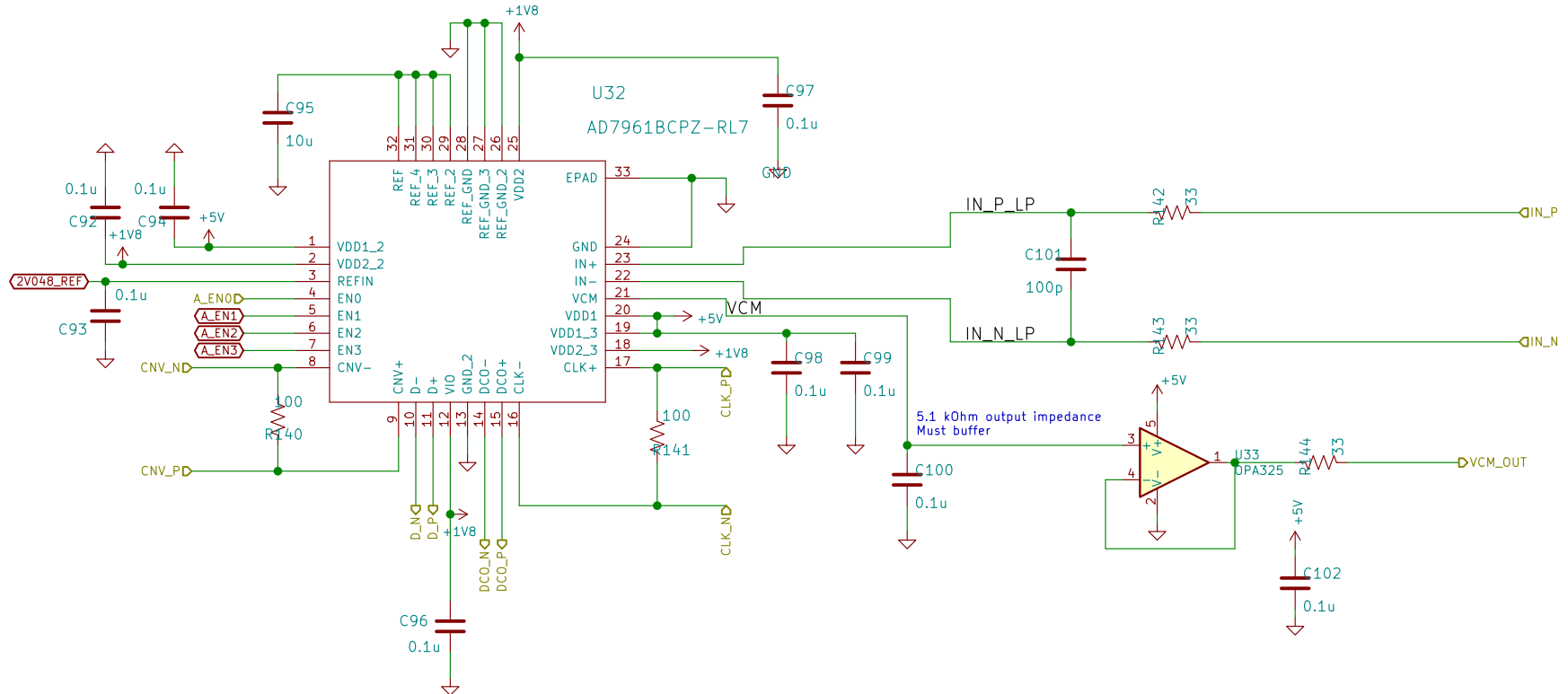
The dual SPI interface has sufficient BW
to clock the data out at the 1 MSPS
(just need 16 MHz clock rate)

Use internal buffer (x2) with 2.048V ref.
 "External reference of 2.048 V applied to the REFIN pin
 (high impedance input). The on-chip buffer gains this by 2
 and drives the REF pin with 4.096 V"
 EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
 EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)
 VDD2 and VIO can come from the same supply.
 But route and decouple separately.



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Use internal buffer (x2) with 2.048V ref.
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 EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
 EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)
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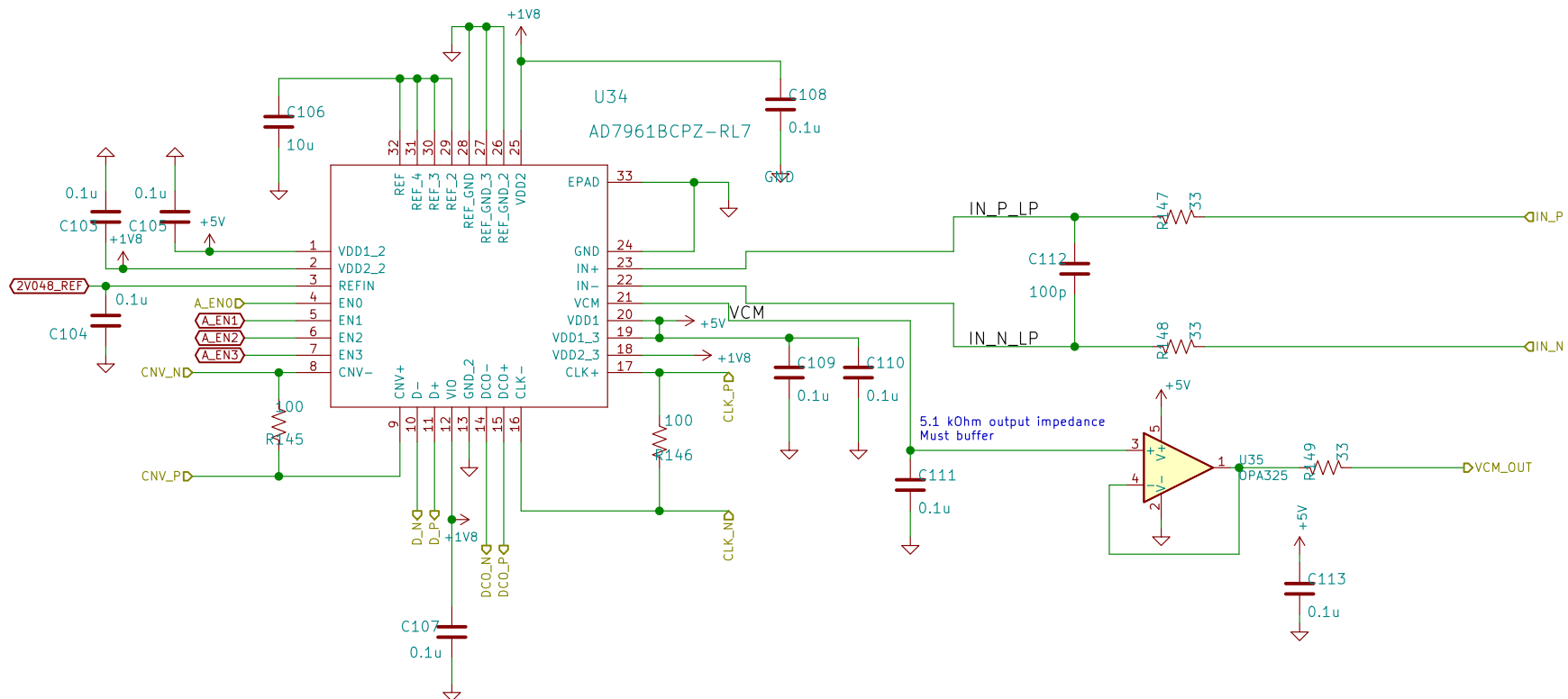
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 KiCad E.D.A. kicad (5.1.9-0-10_14)

Rev:
 Id: 13/26

Use internal buffer (x2) with 2.048V ref.
 "External reference of 2.048 V applied to the REFIN pin
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 and drives the REF pin with 4.096 V"
 EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
 EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)
 VDD2 and VIO can come from the same supply.
 But route and decouple separately.



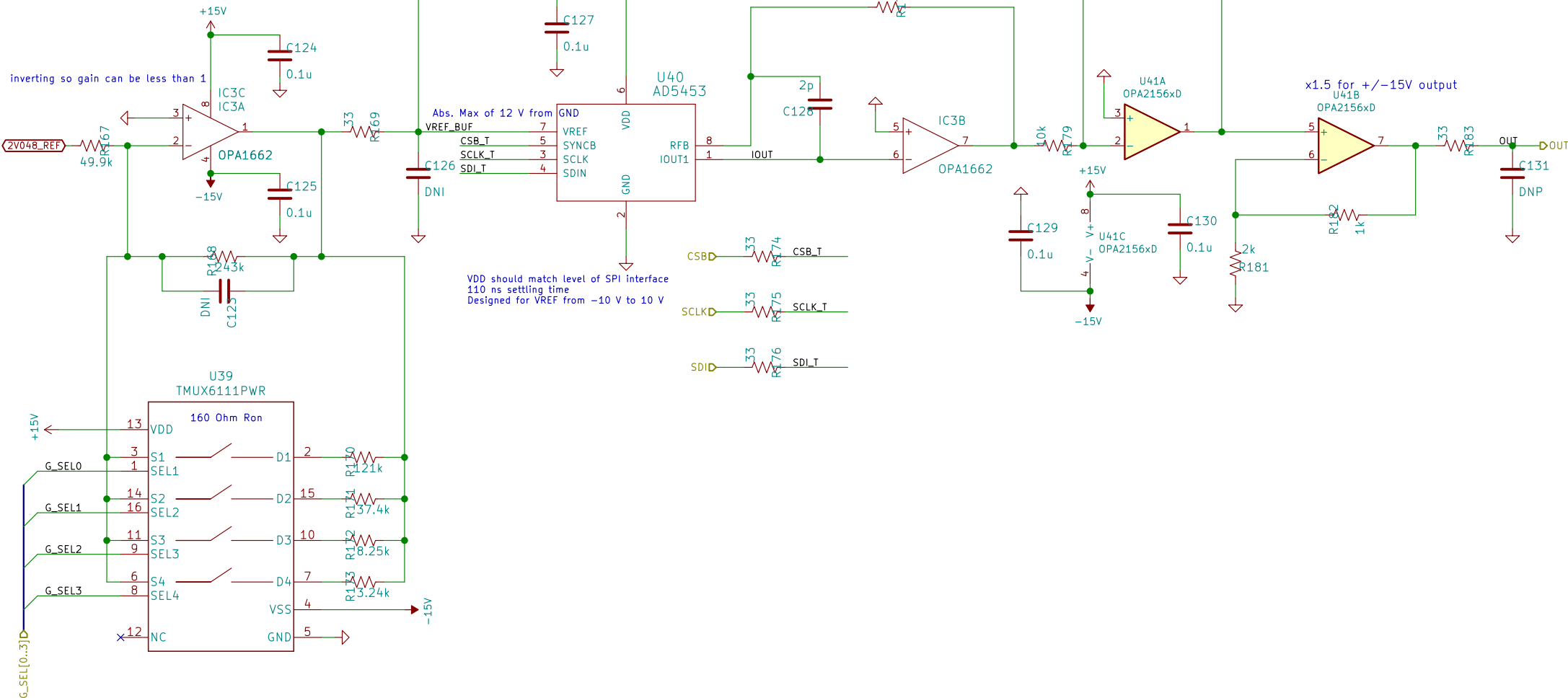
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Rev:
 Id: 14/26

VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
0.133 V ref -> x0.0651, +/- 200 mV

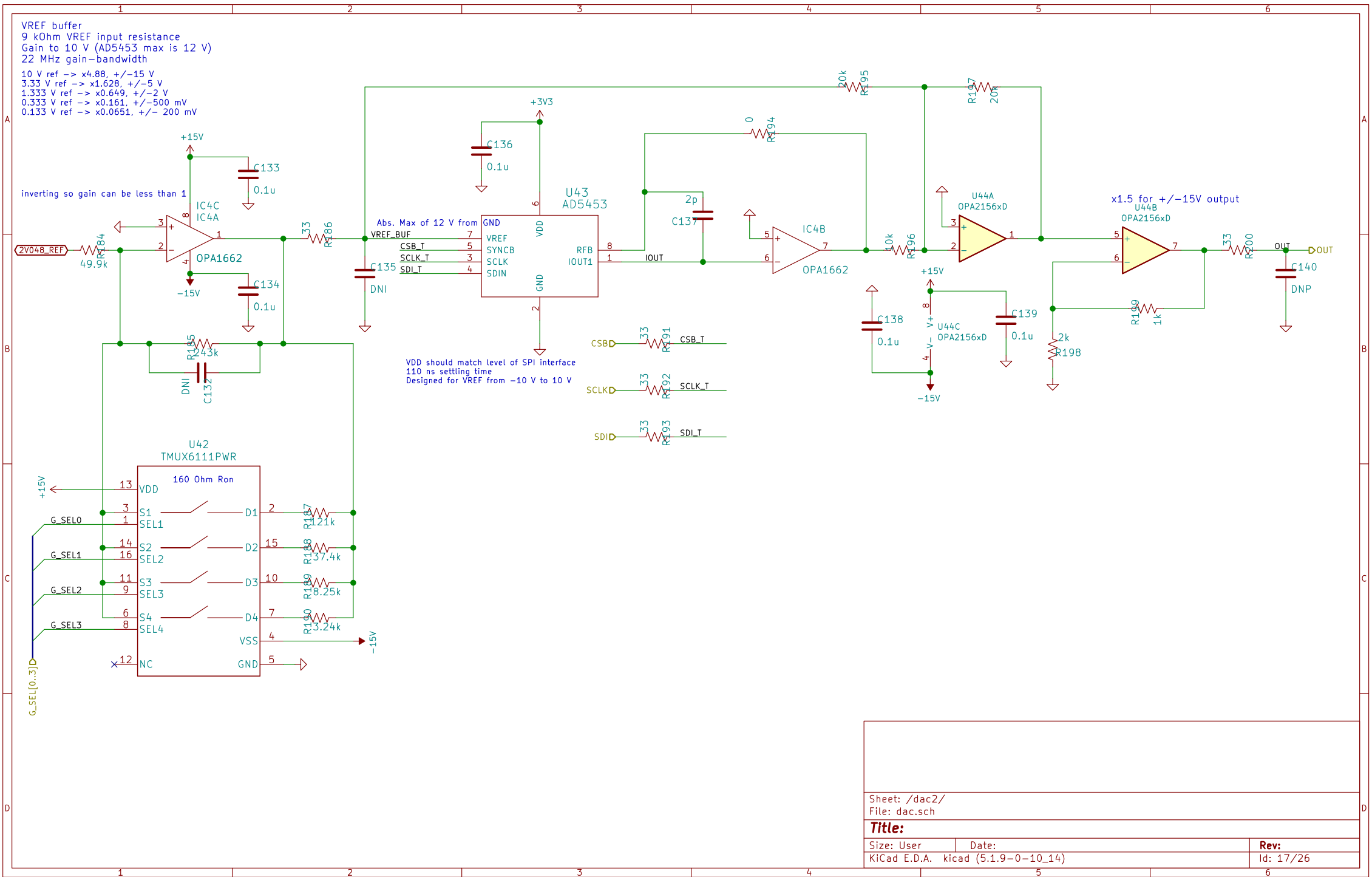


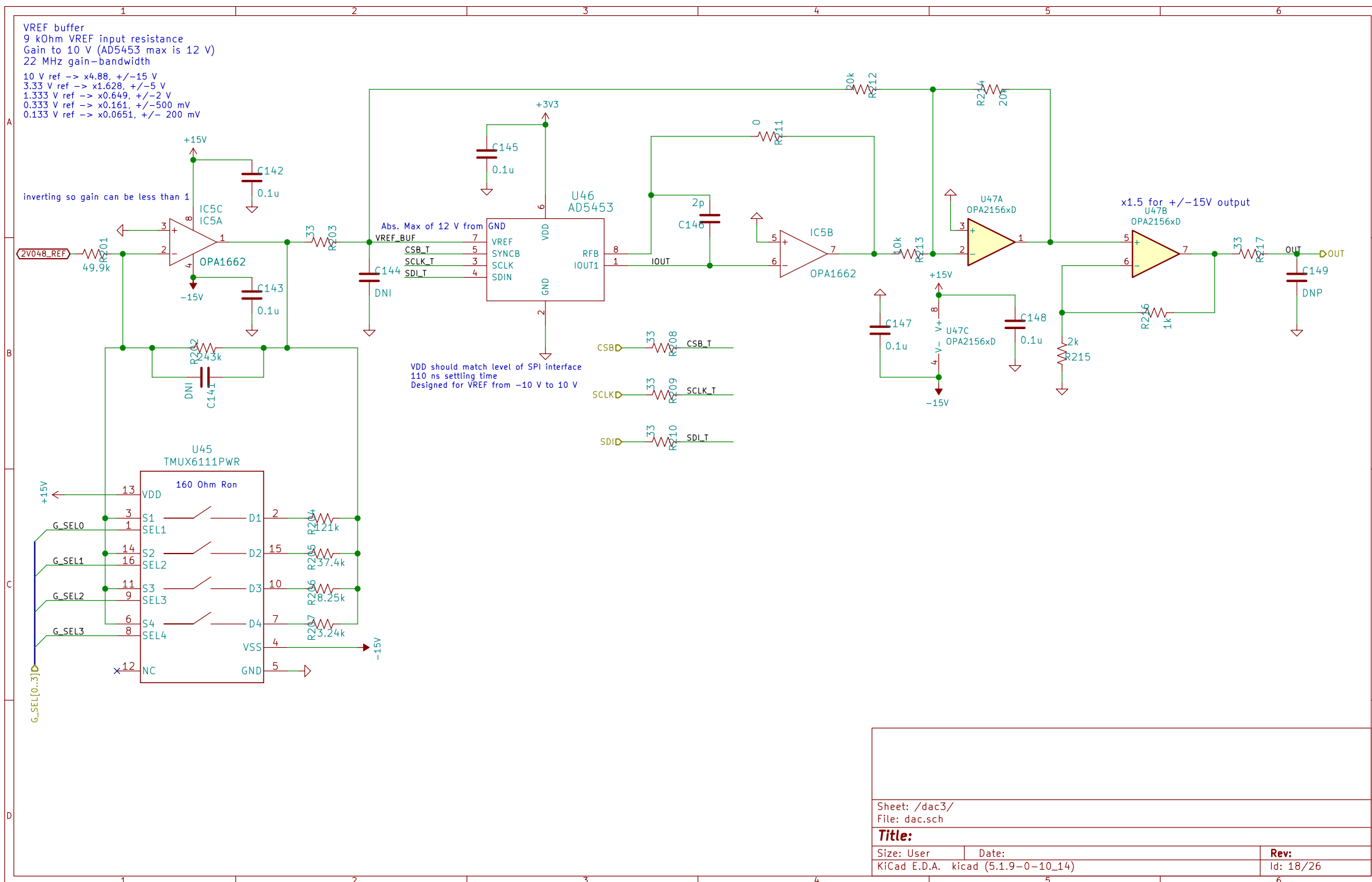
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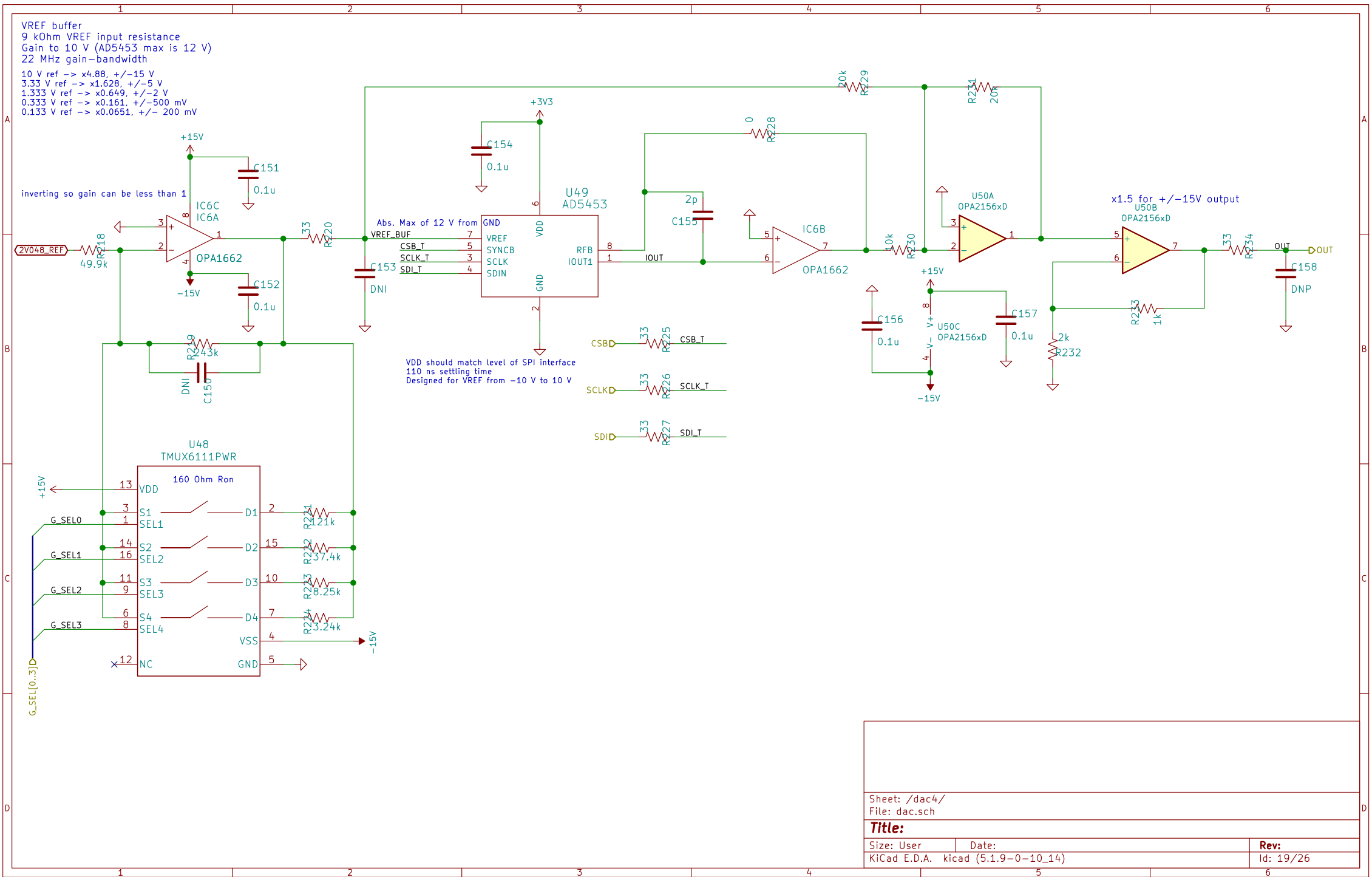
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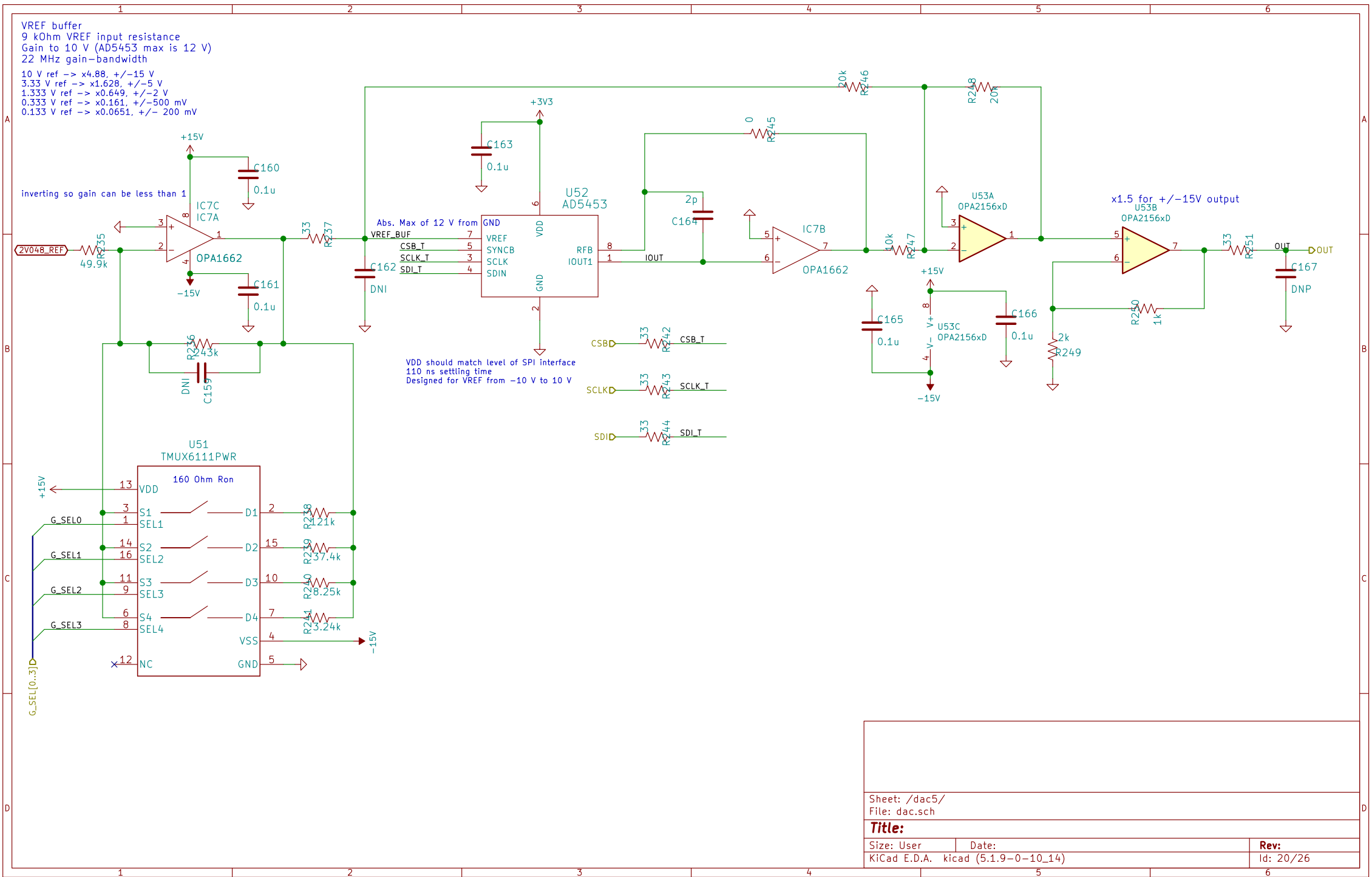
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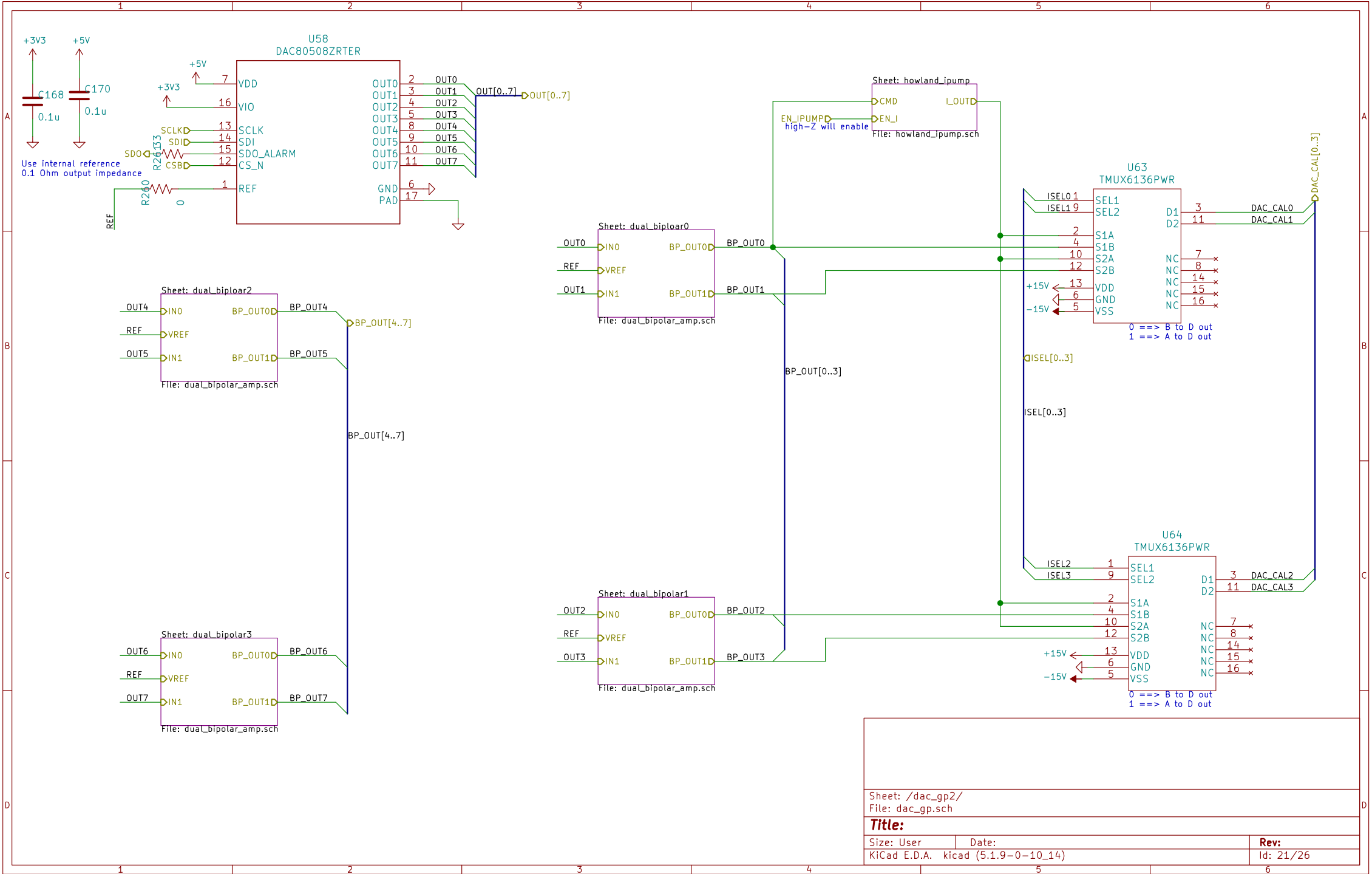
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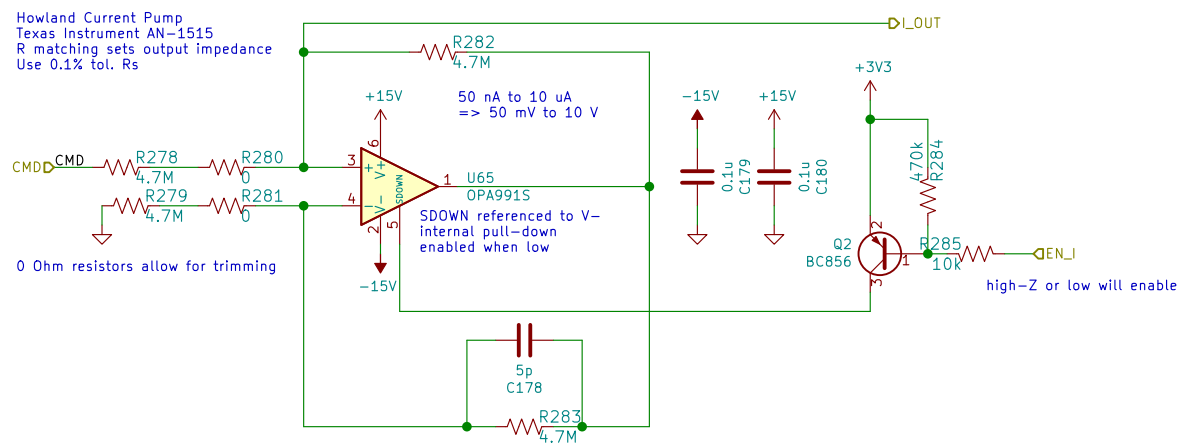












Sheet: /dac_gp2/howland_ipump/
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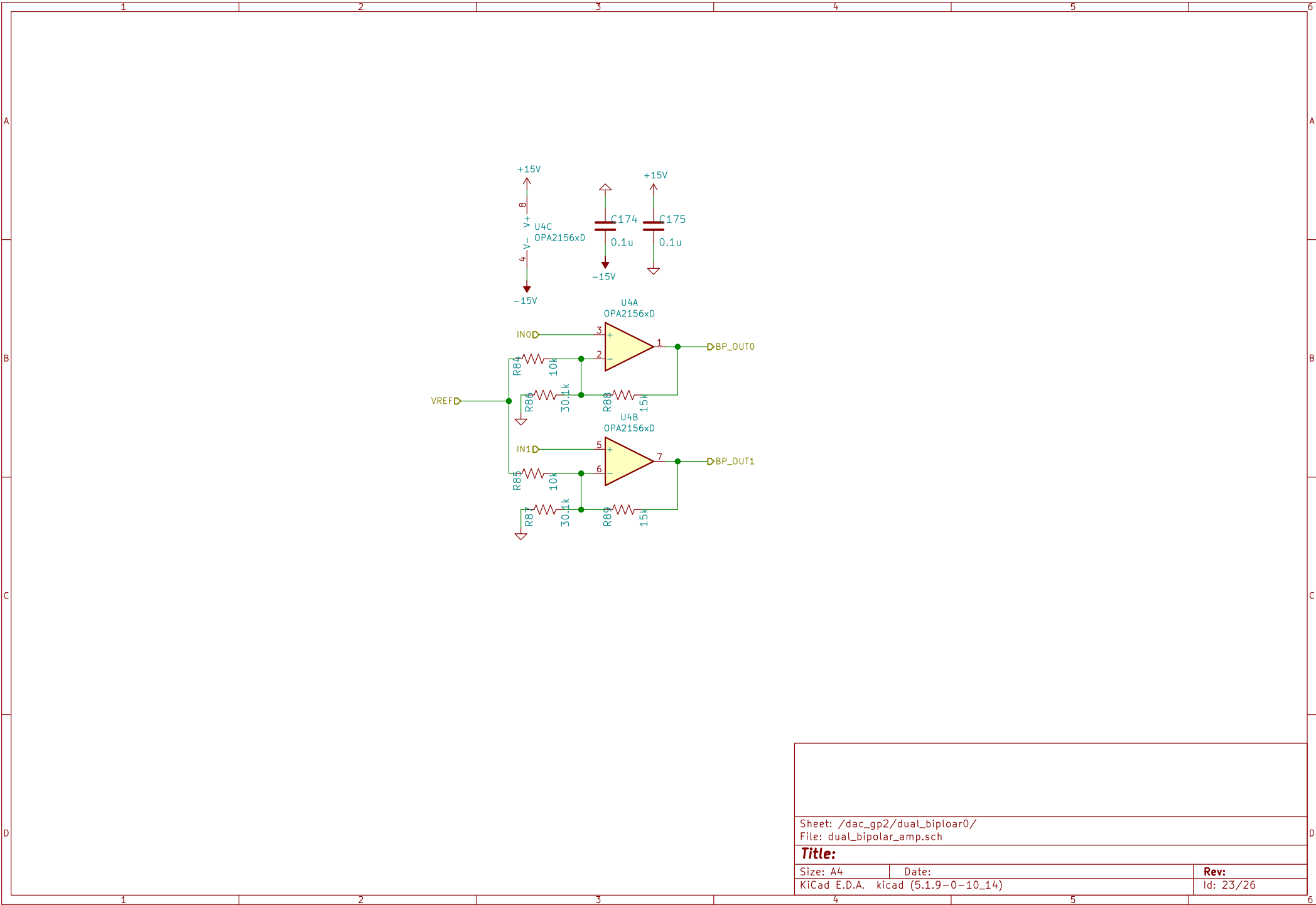
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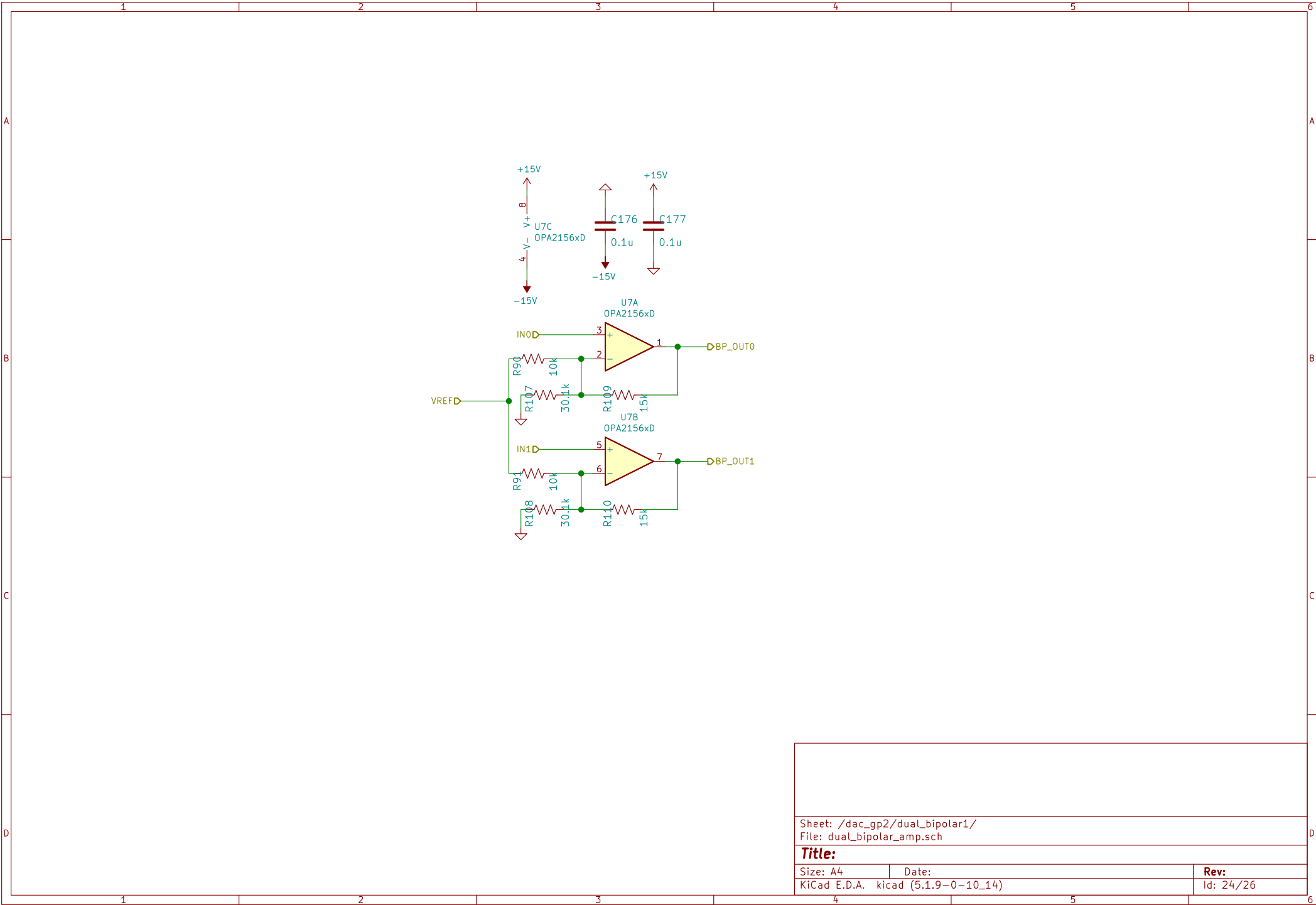
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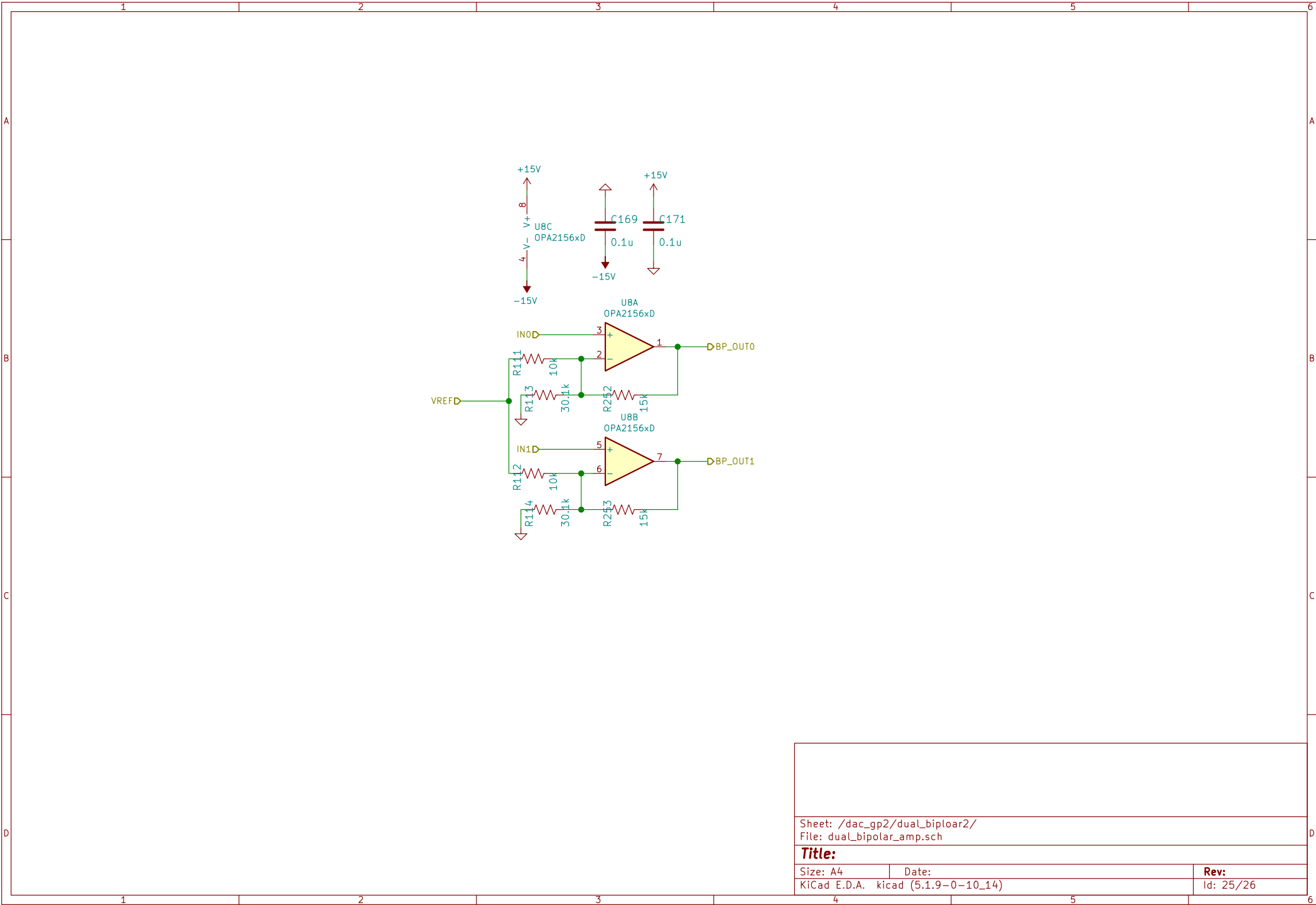
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Rev:

Id: 22/26







Sheet: /dac_gp2/dual_biploar2/
File: dual_bipolar_amp.sch

Title:

Size: A4
KiCad E.D.A. kicad (5.1.9-0-10_14)

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Id: 25/26

