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1

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A

B

C

D

E

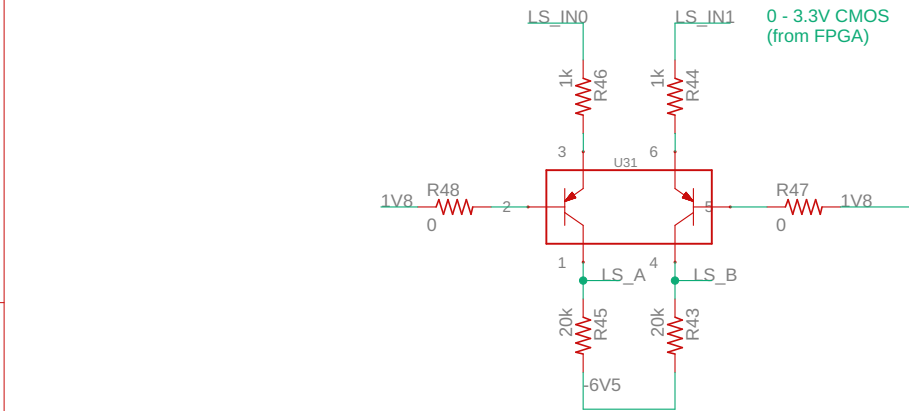
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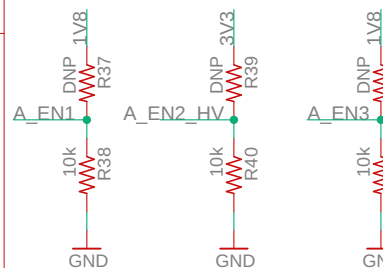
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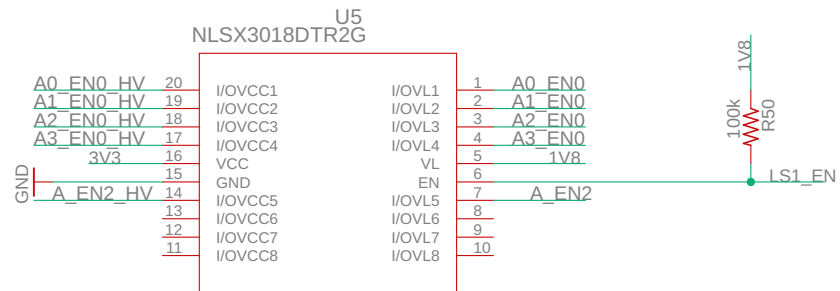
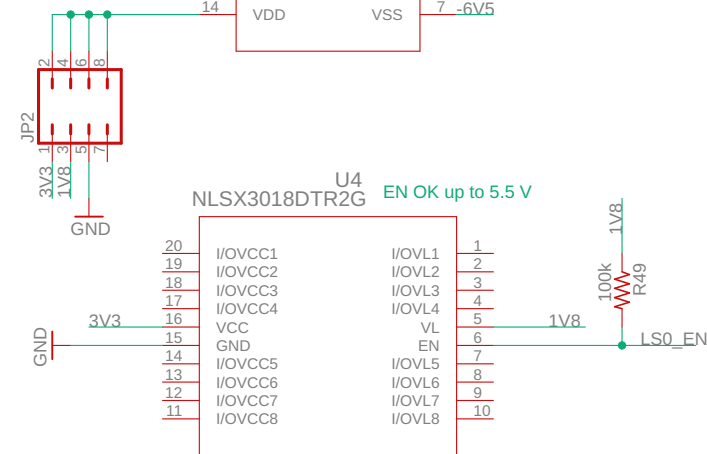
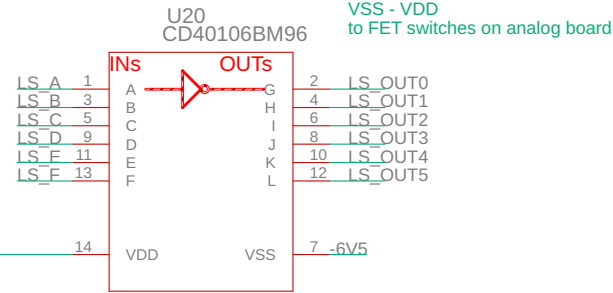
E



0K1JP2_ODD	0K1JP2_EVEN	0K1JP1_ODD	0K1JP1_EVEN
DGND_1	JP2-1	JP2-2	JP1-1
NC_3	JP2-3	JP2-4	JP1-3
JTAG_TCK	JP2-5	JP2-6	JP1-5
JTAG_TMS	JP2-7	JP2-8	JP1-7
JTAG_TDI	JP2-9	JP2-10	JP1-9
SYS_CLK4	JP2-11	JP2-12	JP1-11
DGND_13	JP2-13	JP2-14	JP1-13
G16-L9P_1	JP2-15	JP2-16	JP1-15
G17-L9N_1	JP2-17	JP2-18	JP1-17
H19-L34P_1	JP2-19	JP2-20	JP1-19
H18-L34N_1	JP2-21	JP2-22	JP1-21
F16-L10P_1	JP2-23	JP2-24	JP1-23
F17-L10N_1	JP2-25	JP2-26	JP1-25
J17-L36P_1	JP2-27	JP2-28	JP1-27
K17-L36N_1	JP2-29	JP2-30	JP1-29
K16-L21P_1	JP2-31	JP2-32	JP1-31
J16-L21N_1	JP2-33	JP2-34	JP1-33
+VCCO1_35	JP2-35	JP2-36	JP1-35
V21-L52P_1	JP2-37	JP2-38	JP1-37
V22-L52N_1	JP2-39	JP2-40	JP1-39
T21-L50P_1	JP2-41	JP2-42	JP1-41
T22-L50N_1	JP2-43	JP2-44	JP1-43
P21-L48P_1	JP2-45	JP2-46	JP1-45
P22-L48N_1	JP2-47	JP2-48	JP1-47
M21-L46P_1	JP2-49	JP2-50	JP1-49
M22-L46N_1	JP2-51	JP2-52	JP1-51
L20-L45P_1	JP2-53	JP2-54	JP1-53
+VCCO1_55	JP2-55	JP2-56	JP1-55
L22-L45N_1	JP2-57	JP2-58	JP1-57
H21-L41P_1	JP2-59	JP2-60	JP1-59
H22-L41N_1	JP2-61	JP2-62	JP1-61
F21-L37P_1	JP2-63	JP2-64	JP1-63
F22-L37N_1	JP2-65	JP2-66	JP1-65
D21-L31P_1	JP2-67	JP2-68	JP1-67
D22-L31N_1	JP2-69	JP2-70	JP1-69
B21-L19P_1	JP2-71	JP2-72	JP1-71
B22-L19N_1	JP2-73	JP2-74	JP1-73
A21-L20N_1	JP2-75	JP2-76	JP1-75
J20-L43P_1	JP2-77	JP2-78	JP1-77
J22-L43N_1	JP2-79	JP2-80	JP1-79
			JP1-80



High speed ADC enable signalsThese are global (for all ADC channels)  
Connect A\_EN2\_HV to FPGA EN0 is the only signal that needs FPGA control per ADC channel.



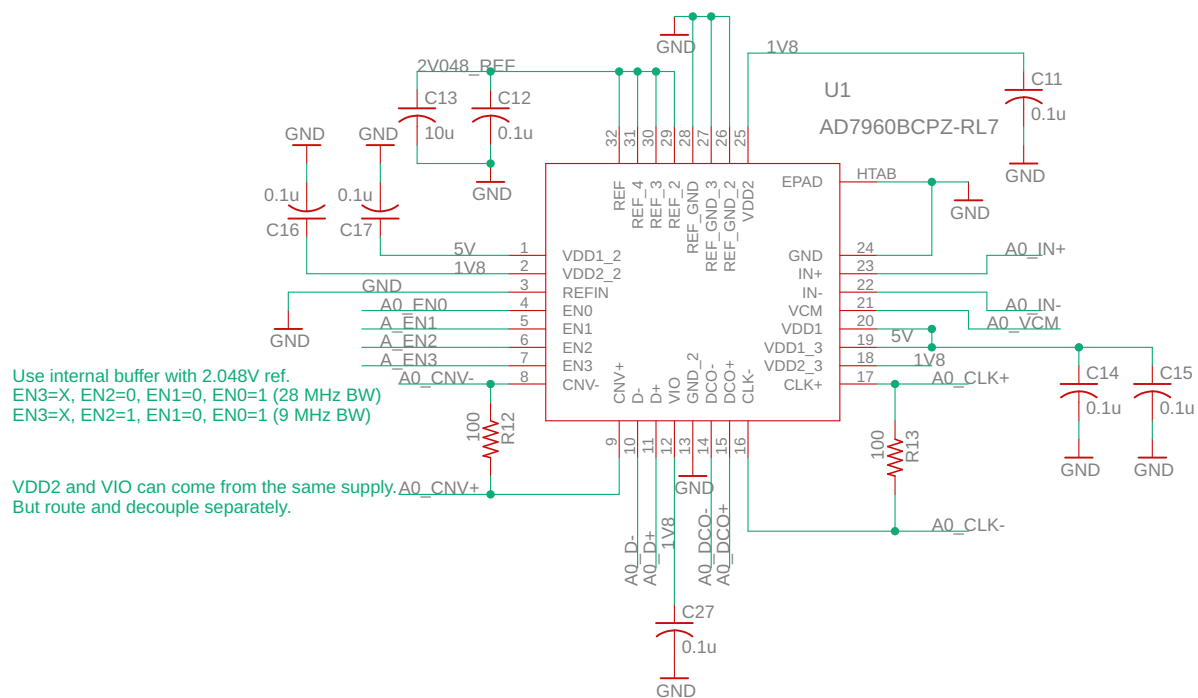
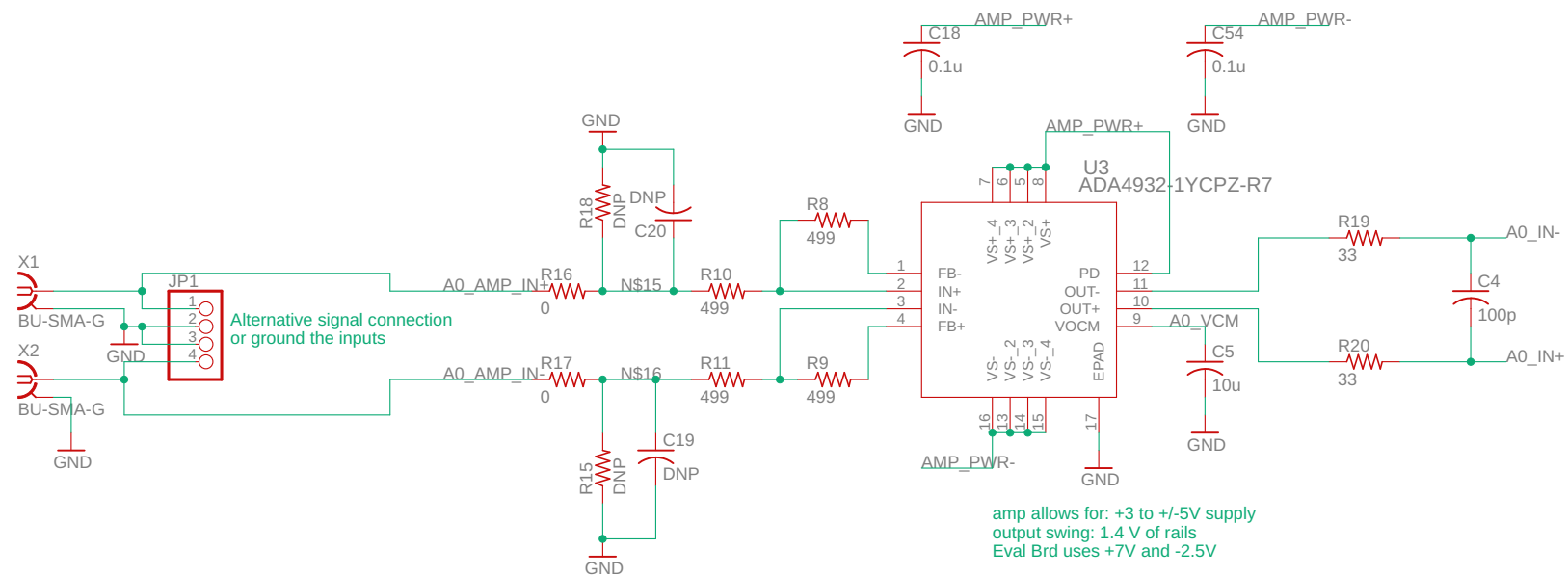
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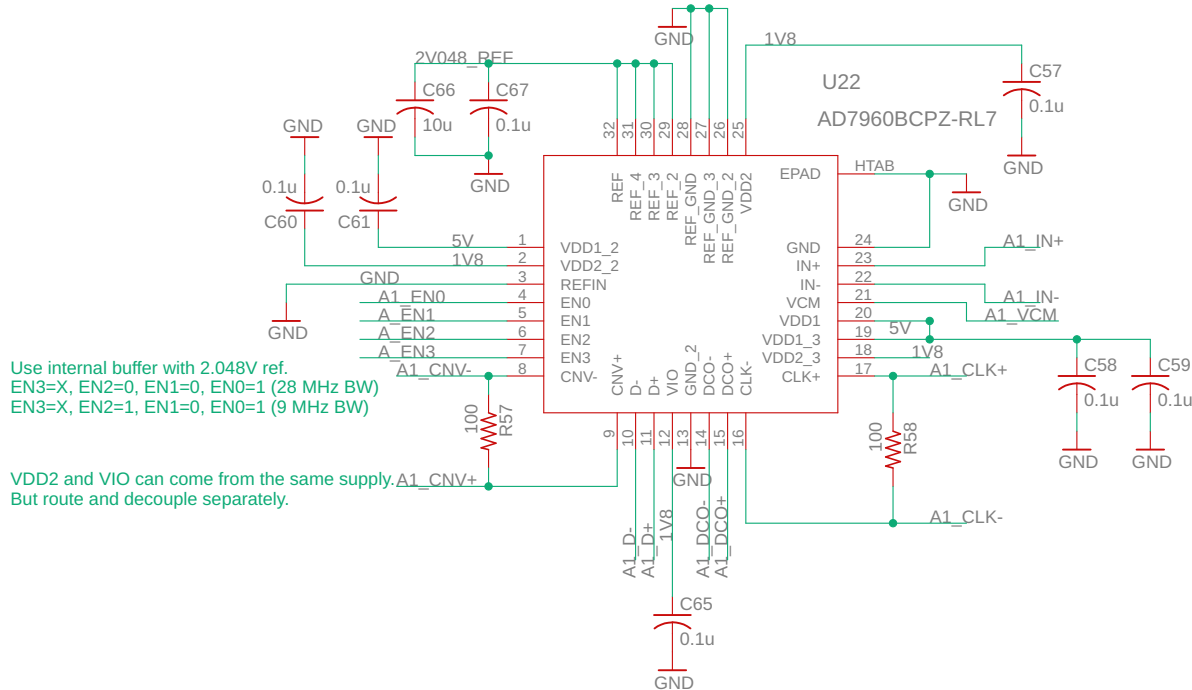
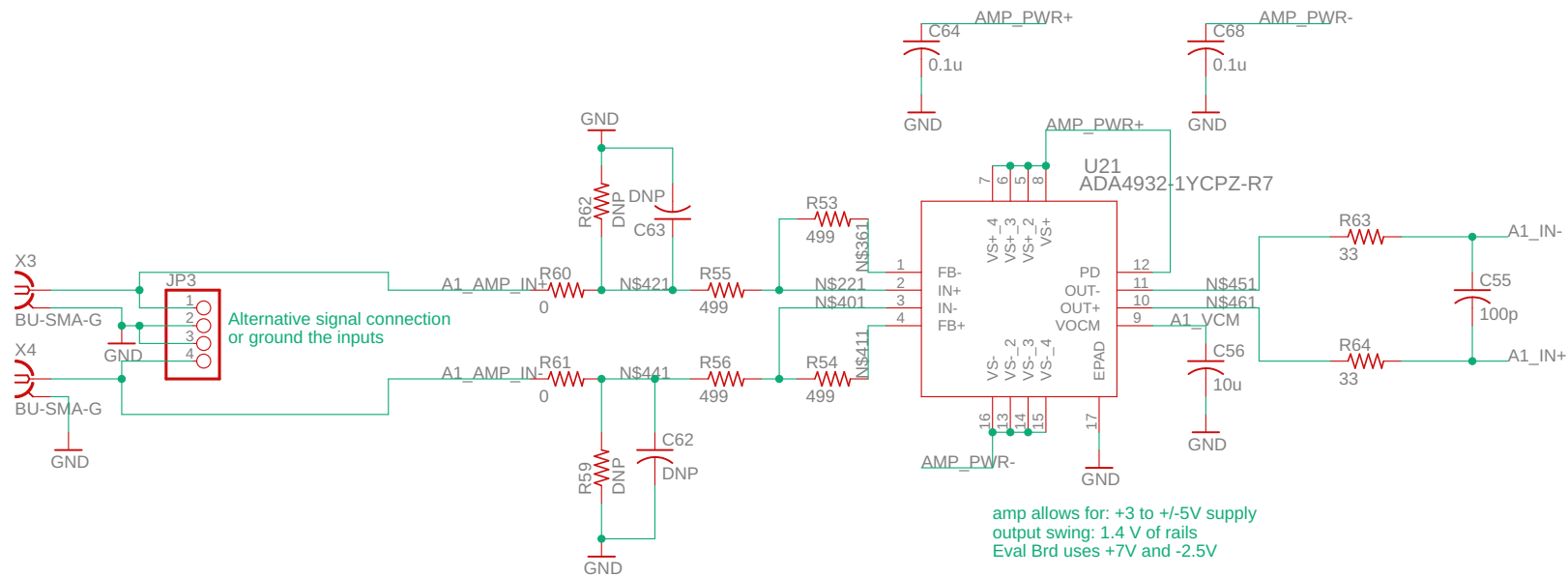
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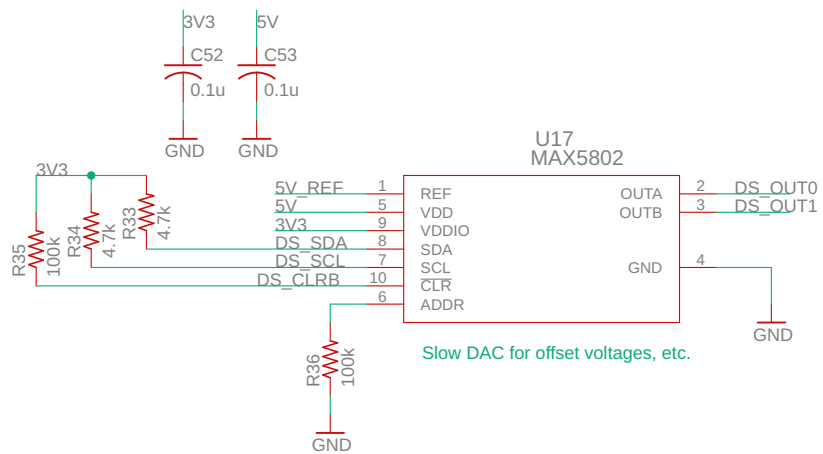


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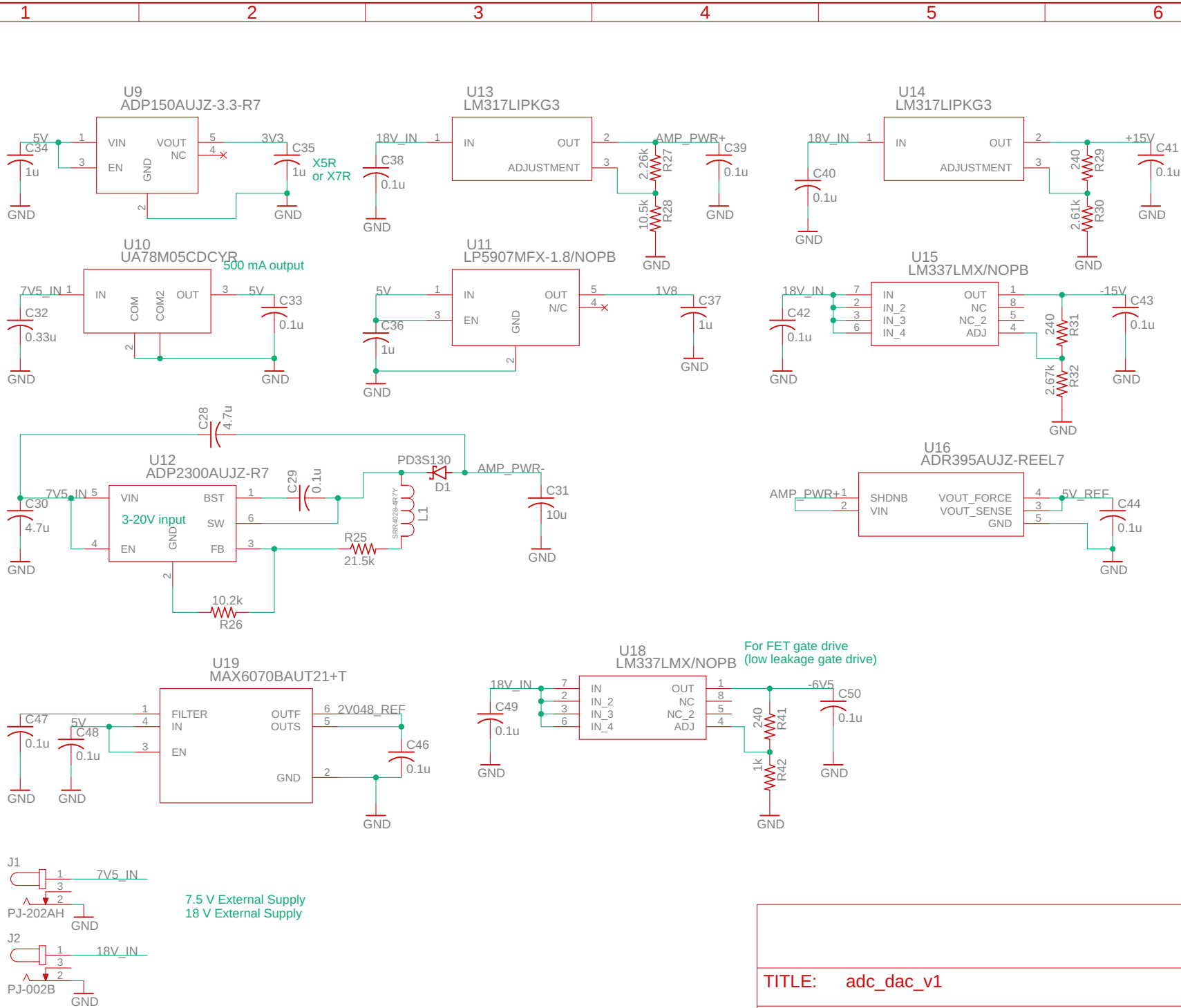
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