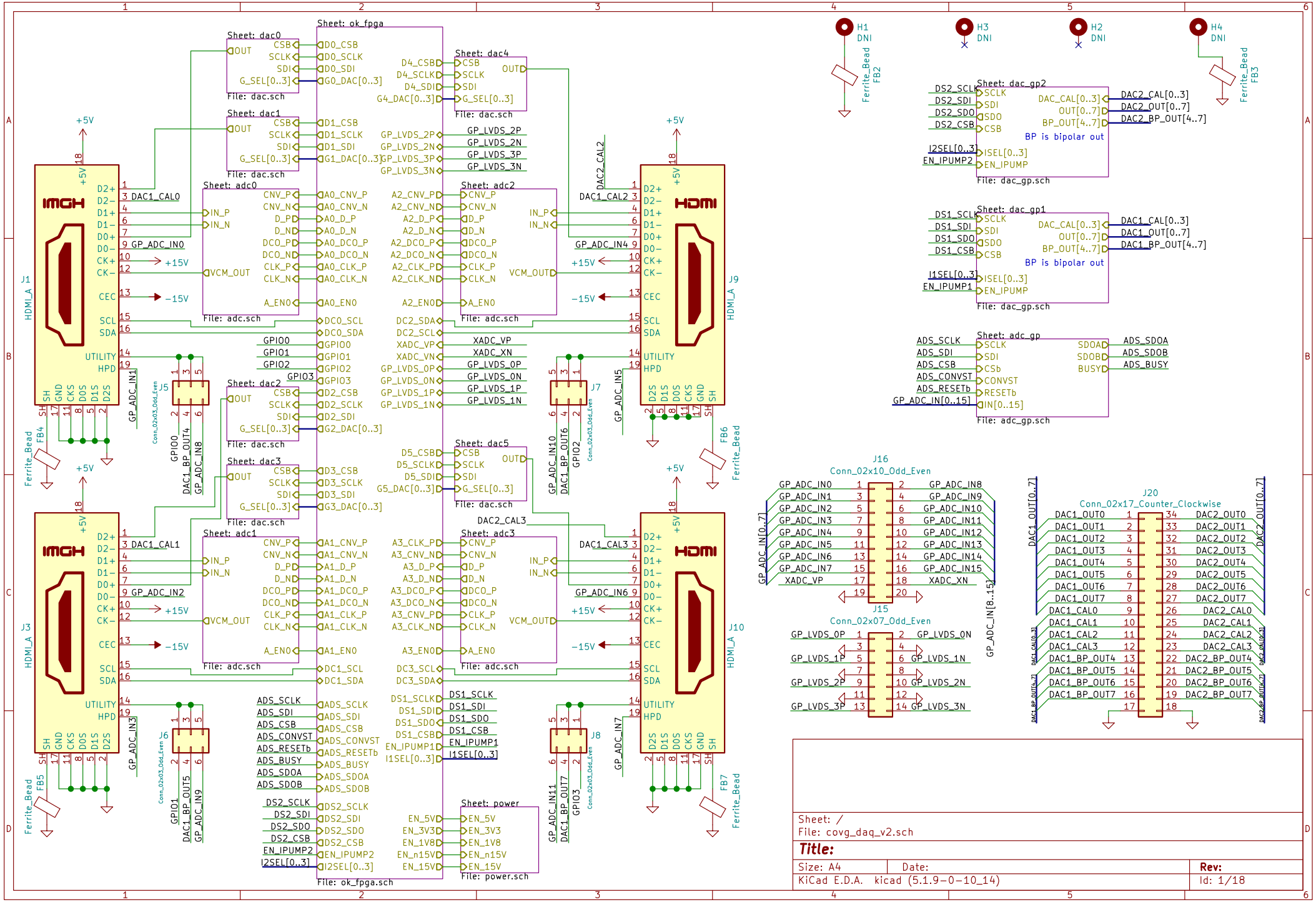
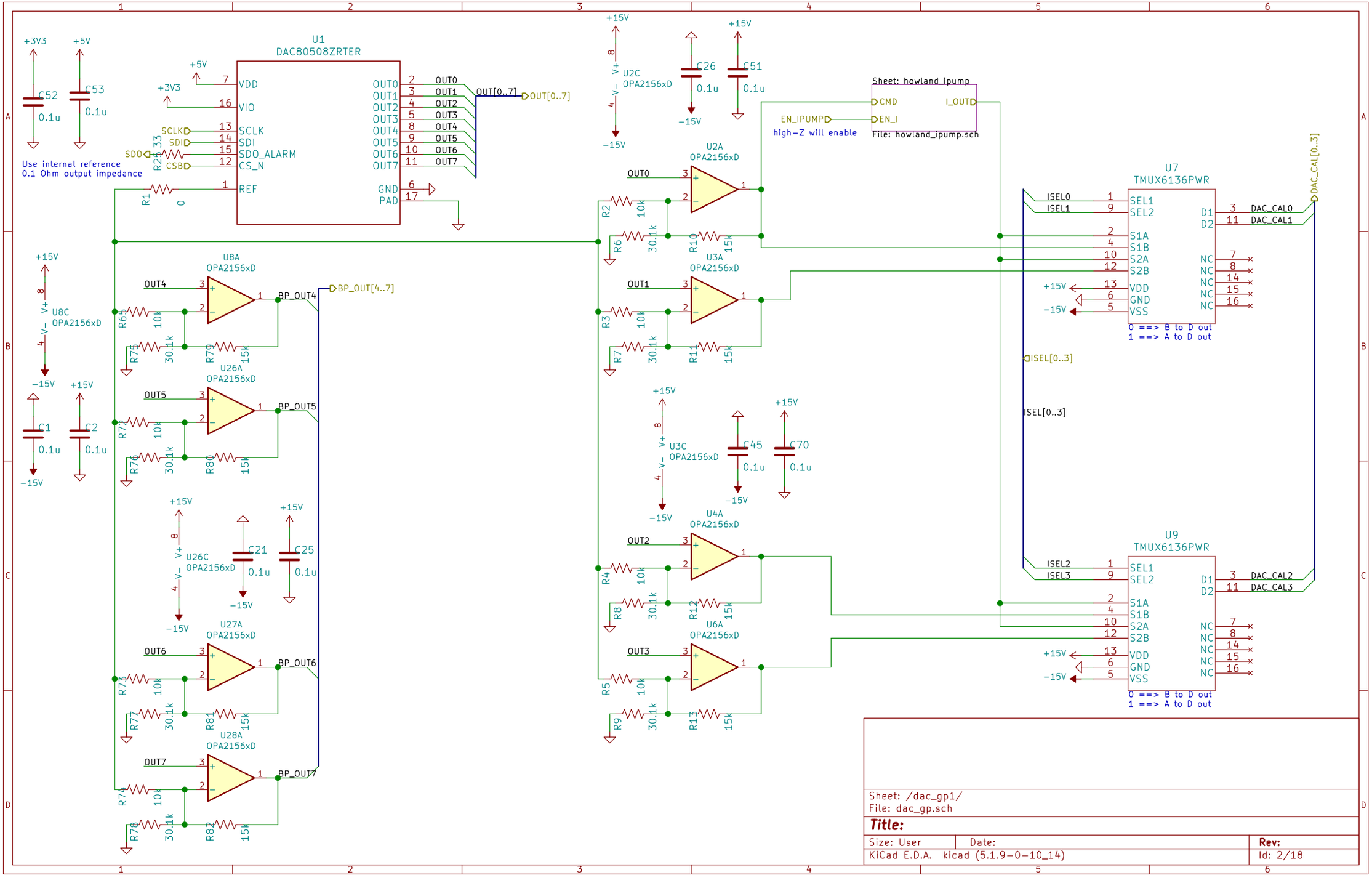
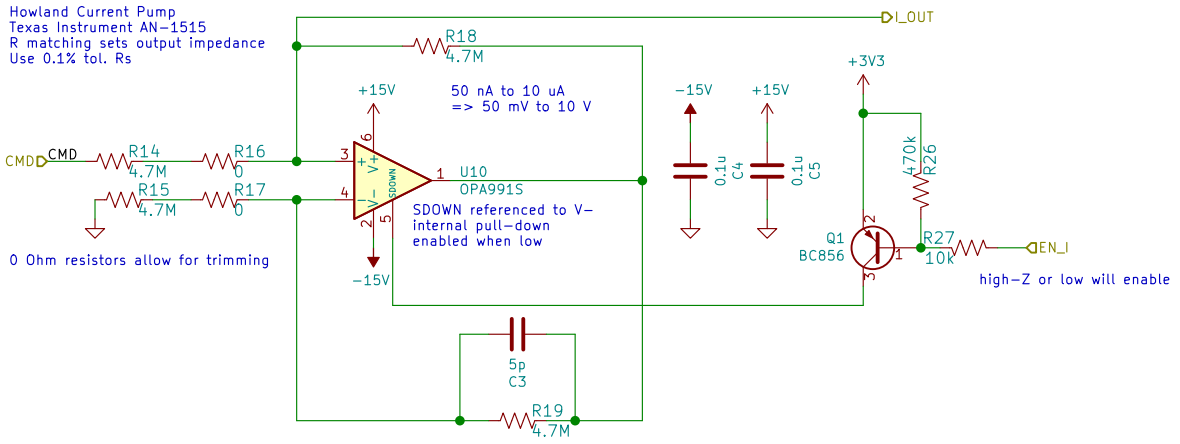

Sheet: ok_fpga
Sheet: dac0
Sheet: dac1
Sheet: dac2
Sheet: dac3
Sheet: dac4
Sheet: dac5
Sheet: adc0
Sheet: adc1
Sheet: adc2
Sheet: adc3
Sheet: power
Sheet: dac_gp2
Sheet: dac_gp1
Sheet: adc_gp
File: dac.sch
File: adc.sch
File: ok_fpga.sch
File: power.sch
File: dac_gp.sch
File: adc_gp.sch
H1 DNI
H3 DNI
H2 DNI
H4 DNI
Ferrite_Bead FB2
Ferrite_Bead FB3
Ferrite_Bead FB4
Ferrite_Bead FB5
Ferrite_Bead FB6
Ferrite_Bead FB7
J1 HDMI_A
J3 HDMI_A
J9 HDMI_A
J10 HDMI_A
J5 Conn_02x03_Odd_Even
J6 Conn_02x03_Odd_Even
J7 Conn_02x03_Odd_Even
J8 Conn_02x03_Odd_Even
J15 Conn_02x07_Odd_Even
J16 Conn_02x10_Odd_Even
J20 Conn_02x17_Counter_Clockwise
BP is bipolar out
BP is bipolar out
+5V
+15V
−15V
Sheet: /
File: covg_daq_v2.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.9−0−10_14)
Id: 1/18


U1
DAC80508ZRTER
VDD
VIO
SCLK
SDI
SDO_ALARM
CS_N
REF
GND
PAD
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT[0..7]
Use internal reference
0.1 Ohm output impedance
U2A
U2C
OPA2156xD
U3A
U3C
U4A
U6A
U8A
U8C
U26A
U26C
U27A
U28A
Sheet: howland_ipump
CMD
I_OUT
EN_I
EN_IPUMP
high-Z will enable
File: howland_ipump.sch
U7
U9
TMUX6136PWR
SEL1
SEL2
S1A
S1B
S2A
S2B
D1
D2
VDD
GND
VSS
NC
ISEL0
ISEL1
ISEL2
ISEL3
ISEL[0..3]
DAC_CAL0
DAC_CAL1
DAC_CAL2
DAC_CAL3
DAC_CAL[0..3]
0 ==> B to D out
1 ==> A to D out
BP_OUT[4..7]
BP_OUT4
BP_OUT5
BP_OUT6
BP_OUT7
+3V3
+5V
+15V
-15V
Sheet: /dac_gp1/
File: dac_gp.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 2/18



Sheet: /dac_gp1/howland_ipump/		
File: howland_ipump.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9−0−10_14)		Id: 3/18

PWR_FLAG PWR_FLAG PWR_FLAG PWR_FLAG

6V_IN −16V5 16V5

J2 Barrel_Jack_Switch

FB1 Ferrite_Bead

6V_IN

2.50mm ID x 5.50mm OD
5 A max

Could increase input to 7 V,
possible issues with Enables beyond that.

Vin up to 10 V
EN min is 3V with 6 V Vin

U14 LP38692MP−5.0 1 A output

6V_IN EN_5Vx R23 100k C32 1u C30 1u +5V

Vin up to 10 V
EN min is 3V with 6 V Vin

U5 LP38693MP−3.3

6V_IN EN_3V3x R37 100k C31 1u C33 1u +3V3

Vin up to 10 V
EN min is 3V with 6 V Vin

U12 LP38693MP−1.8

6V_IN EN_1V8x R38 100k C34 1u C35 1u +1V8

Don't use EN since this is an FPGA
bank voltage!

U13 LP38693MP−2.5 500 mA output
needed for FPGA LVDS bank

6V_IN C36 1u C37 1u +2V5

6V_IN C9 4.7u

cathode is pin1
D2 D_Schottky

16V5 C6 4.7u R20 232k C7 33p R21 15k

L2 4.7u L3 10uH 1u C10 D3 D_Schottky L4 15uH

−16V5 C12 4.7u C11 75p R29 249k R30 15k VREF_SW

U11 LT3471
SW1 VIN SW2 FB1P FB1N SHDN/SS1 VREF FB2P FB2N SHDN/SS2 GND

VREF_SW C8 0.1u R22 100k

R24 100k R36 4.7k EN_n15Vx C29 0.33u

EN_15Vx R28 4.7k C28 0.33u

For noninverting regulator topologies:
VOUT = VFBP (1 + R1/R2)
VREF = 1.00 V

For inverting regulator topologies:
VOUT = VFBP (R1/R2)
VREF = 1.00 V

0.4 A output max
1.0 V dropout

U17 LM2937xMP

16V5 C40 0.1u +15V C41 0.1u

−16V5 C42 0.33u U21 MC79M15_TO252 −15V C43 1u

0.5 A output max
1.1 V dropout

U19 MAX6070BAUT21+T

+5V C47 0.1u C48 0.1u FILTER IN EN OUTF OUTS GND 2V048_REF C46 0.1u

+/−10 mA output current

+1V8 2V048_REF +2V5 +3V3 +5V −15V +15V −16V5 16V5 6V_IN EN_PWR

J4 Screw_Terminal_01x12

Allows for observation
or override of supplies

J11 Conn_02x05_Odd_Even

EN_5V EN_3V3 EN_1V8 EN_15V EN_n15V
R39 R40 R41 R42 R43 0
EN_5Vx EN_3V3x EN_1V8x EN_15Vx EN_n15Vx EN_PWR

EN_PWR − supply external voltage (3.3V)
that can be jumpered to EN pins.

Default is to control by FPGA,
have 0 Ohm Rs installed,
and no jumpers on the header.

Alternative option is to add jumpers
(and if EN_PWR is > 3.3 V)remove 0 Ohm.

Sheet: /power/
File: power.sch

Title:

Size: User | Date: | **Rev:**
KiCad E.D.A. kicad (5.1.9−0−10_14) | Id: 4/18

VCCBATT is the battery backup supply for the FPGA's internal volatile memory that stores the key for the AES decryptor (not needed)

FPGA power: standard "canon-style" 2.1mm / 5.5mm jack. The outer ring is connected to DGND. The center pin is connected to +VDC.

Bank 13: 3.3V always
MC1 64 and 66-76 MC2 64 and 66-76
(24 total)

Bank 34: default 3.3V,
change by ferrite bead (FB8)
on MC1
(total of 48)

Bank 35: default 3.3V,
change by ferrite bead (FB9)
MC2 2
(total of 50)

OK1A

OK1B

OK1C

OK1D

ADS8686
16-chan ADC

DAC80508
8-chan

DAC80508
8-chan

IO voltage for bank 35
3.3 V (leave open)

IO voltage for bank 35
3.3 V (leave open)

IO voltage for bank 34

MRCC - multi-region clock capable

U65
24AA025UID

U15
PCA9306

U16
NLSX3018DTR2
Bidirectional translator
Level shifter is not for I2C

U18
TXS0108EPW

U20
TXS0108EPW

U24
TCA9555
DAC gain control

U25
TCA9555
DAC gain control

J22
Conn_02x10_Counter_Clockwise

J12
Conn_Coaxial

J14
Conn_Coaxial

J13
QWIIC_CONNECTOR-1MM
CONN-13694
SparkFun qwiic connector
SM04B-SRSS-TB
3.3 V VCC

These are global (for all ADC channels)
EN0 is the only signal that needs
FPGA control per ADC channel.
Default settings:
EN3,EN2,EN1,EN0
0,0,0,FPGA (A_EN2_HV is high-Z)

driving EN2 high outputs test
patterns on the LVDS interface

Vcc = 1.3 - 4.5 V

VL = 0.9 to VCC-0.4

VREF: needed for single-ended IO standards that use a diff. input buffer.
We do not need VREF. The FPGA also has an internal VREF which can be used if running at or below 400 MHz.
Most relevant to memory interfaces.

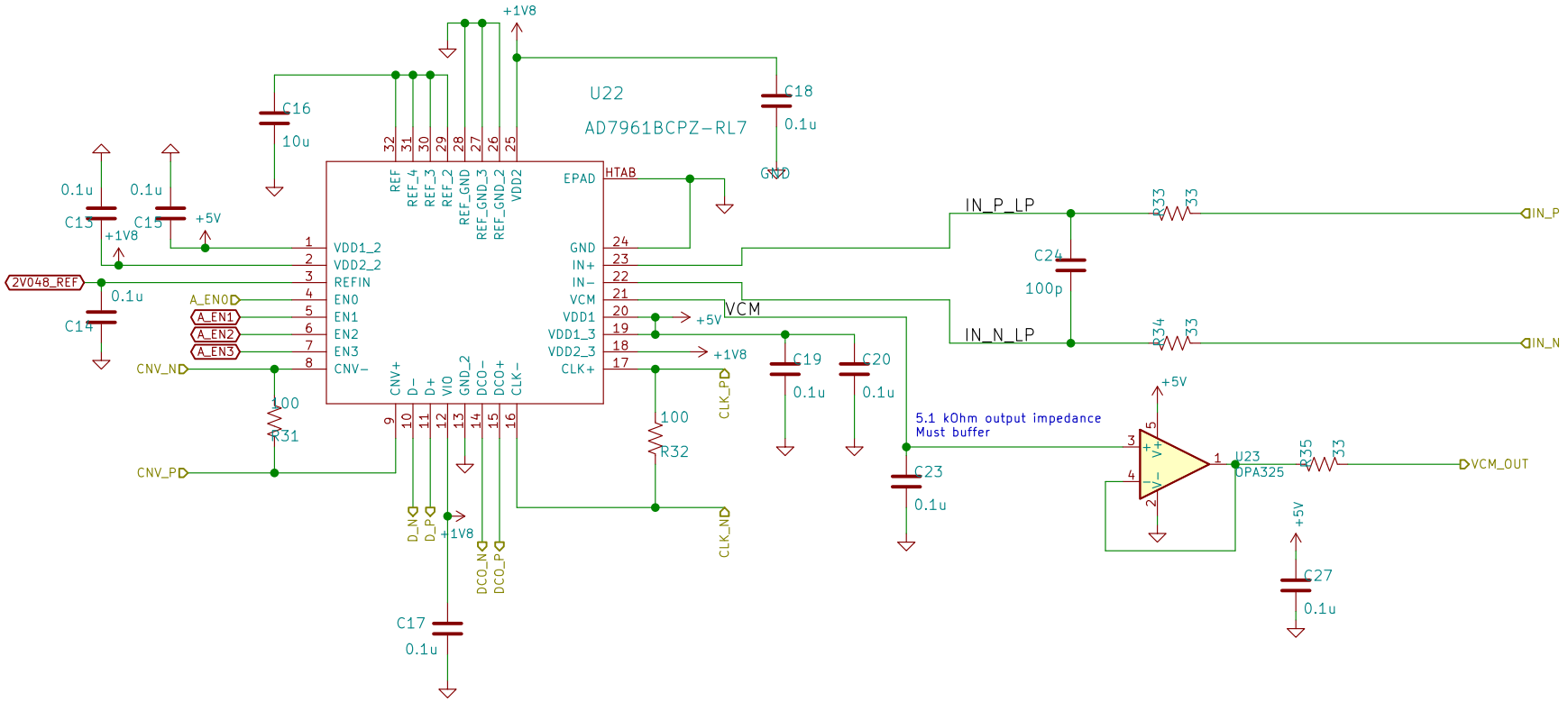
Sheet: /ok_fpga/
File: ok_fpga.sch

Title:

Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 5/18

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

VDD2 and VIO can come from the same supply.
But route and decouple separately.



Sheet: /adc1/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 6/18

AVDD bypass (1x 10uF, 1x 0.1uF per pin)

AGND_IN must be within +/−0.3 V of GND

IC3
ADS8686SIPZAR

REFIO: most guidance is 0.1uF bypass (including EVM schematics), but datasheet layout section suggests 10 uF.

Must by pulled up by FPGA to enable. 3.3 V level.

The dual SPI interface has sufficient BW to clock the data out at the 1 MSPS (just need 16 MHz clock rate)

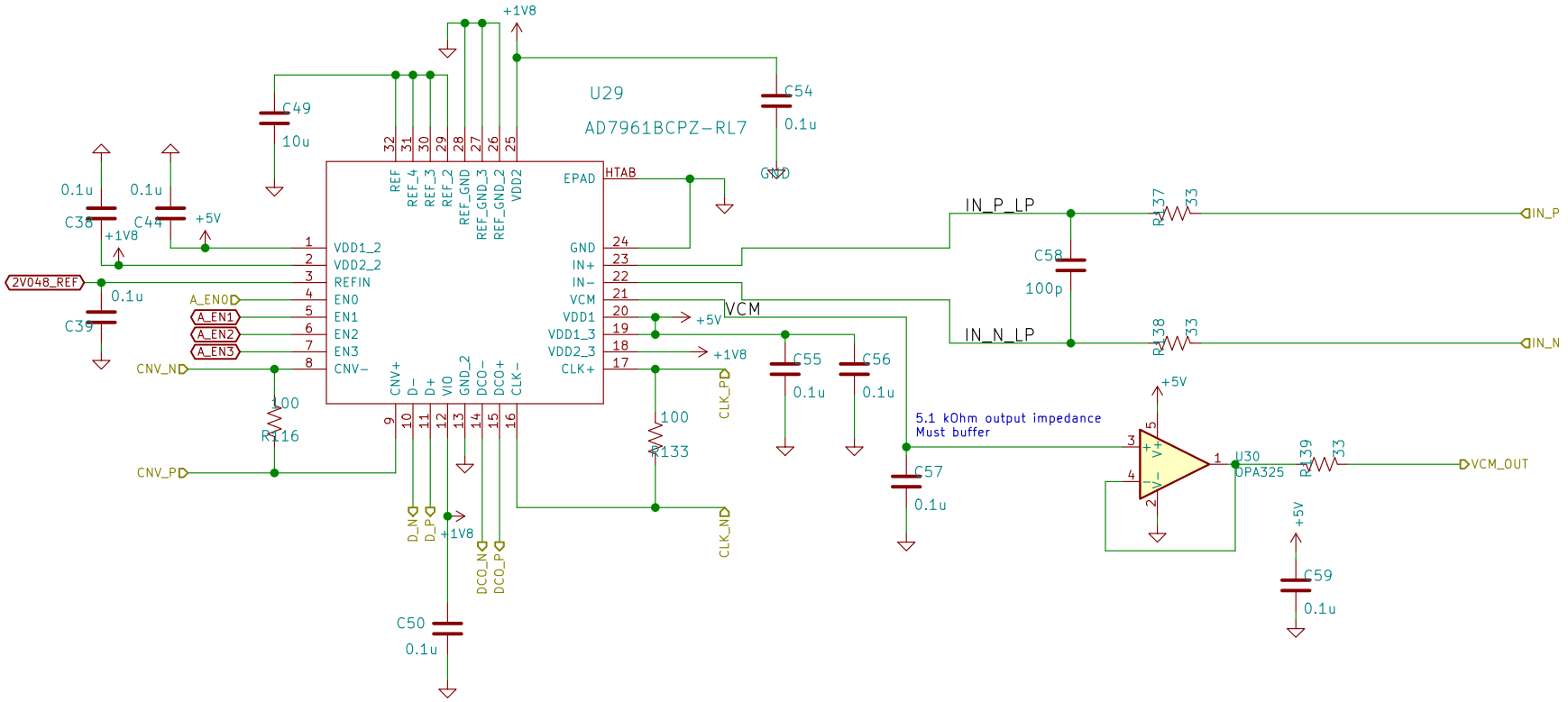
Sheet: /adc_gp/
File: adc_gp.sch

Title:

Size: User | Date: | **Rev:**
KiCad E.D.A. kicad (5.1.9−0−10_14) | Id: 7/18

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

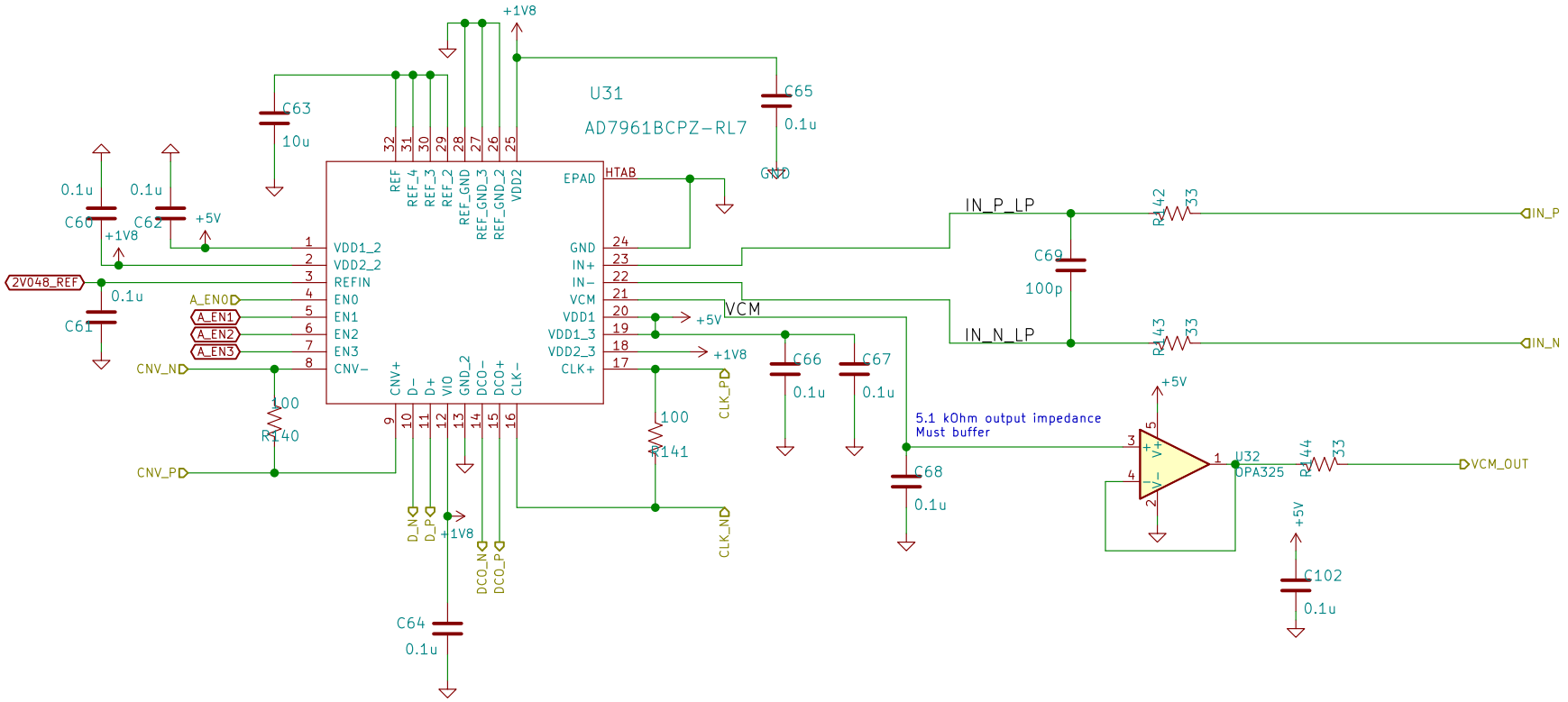
VDD2 and VIO can come from the same supply.
But route and decouple separately.



Sheet: /adc0/ File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 8/18

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

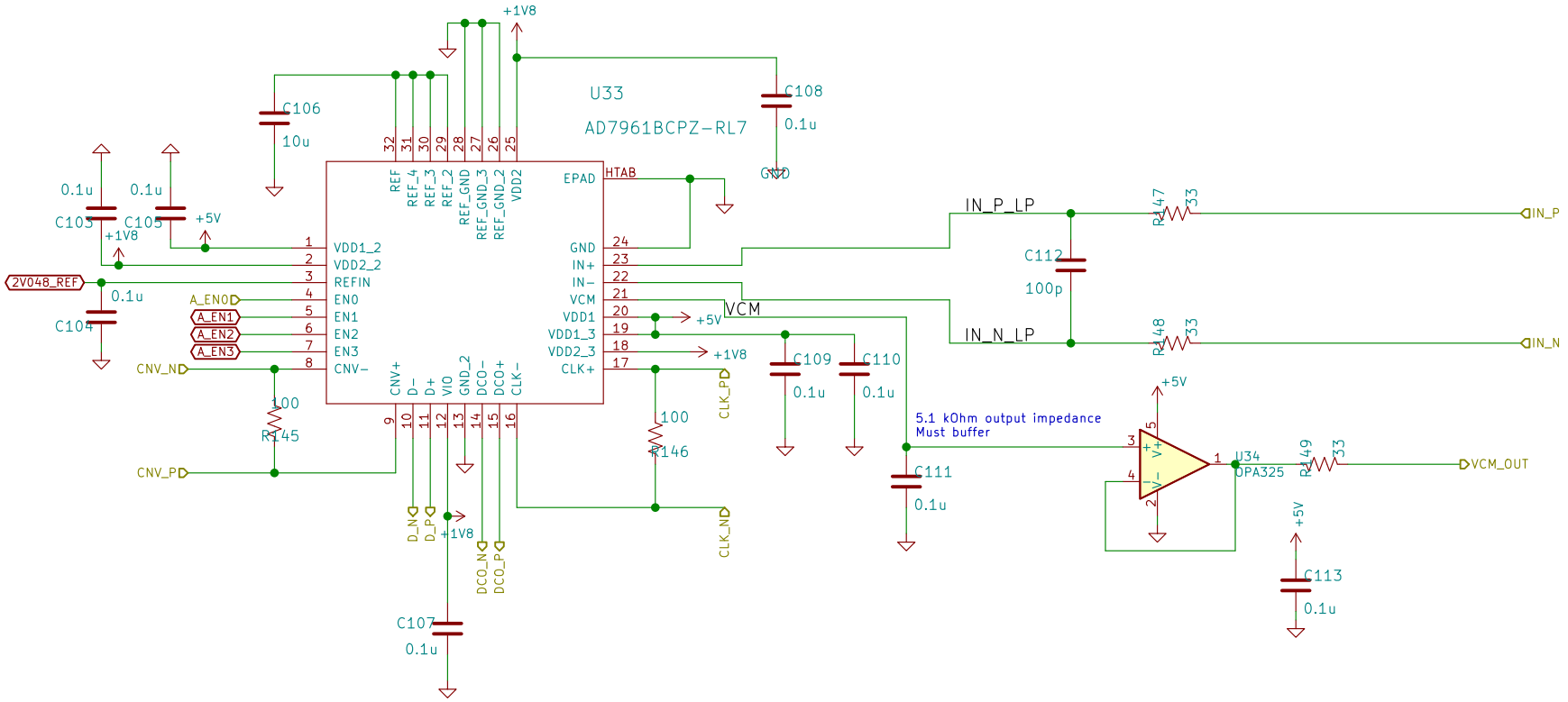
VDD2 and VIO can come from the same supply.
But route and decouple separately.



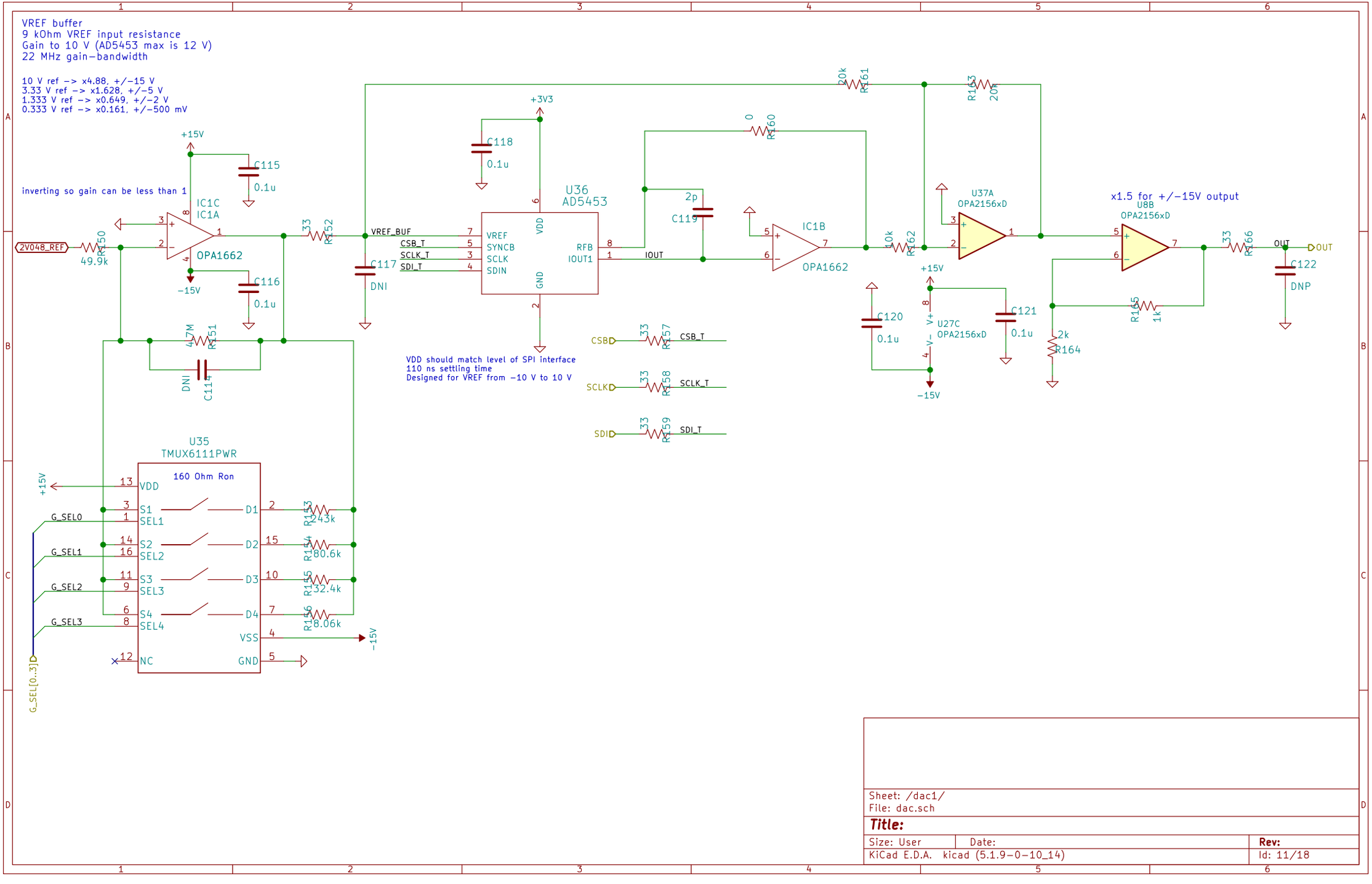
Sheet: /adc2/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 9/18

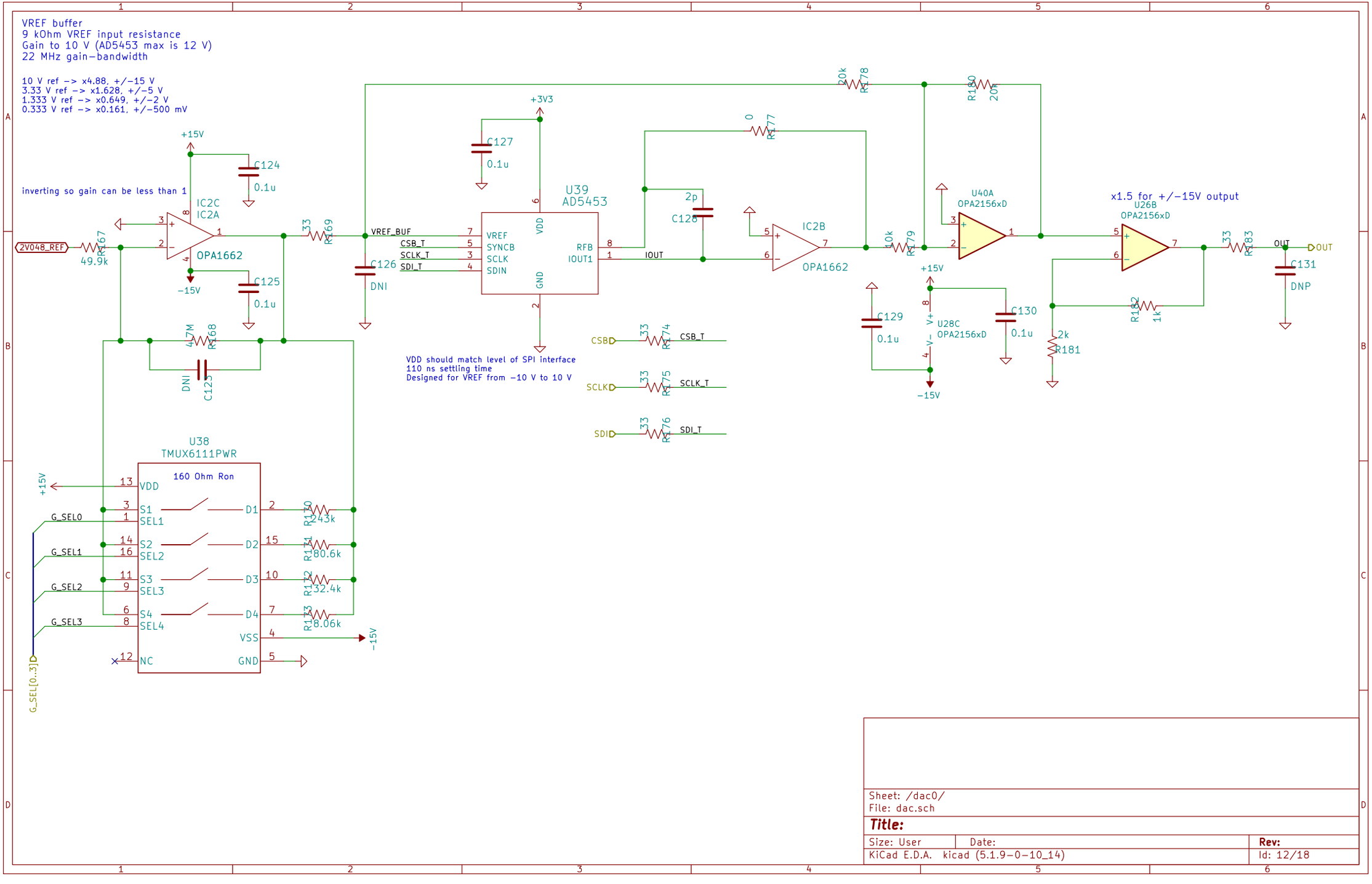
Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

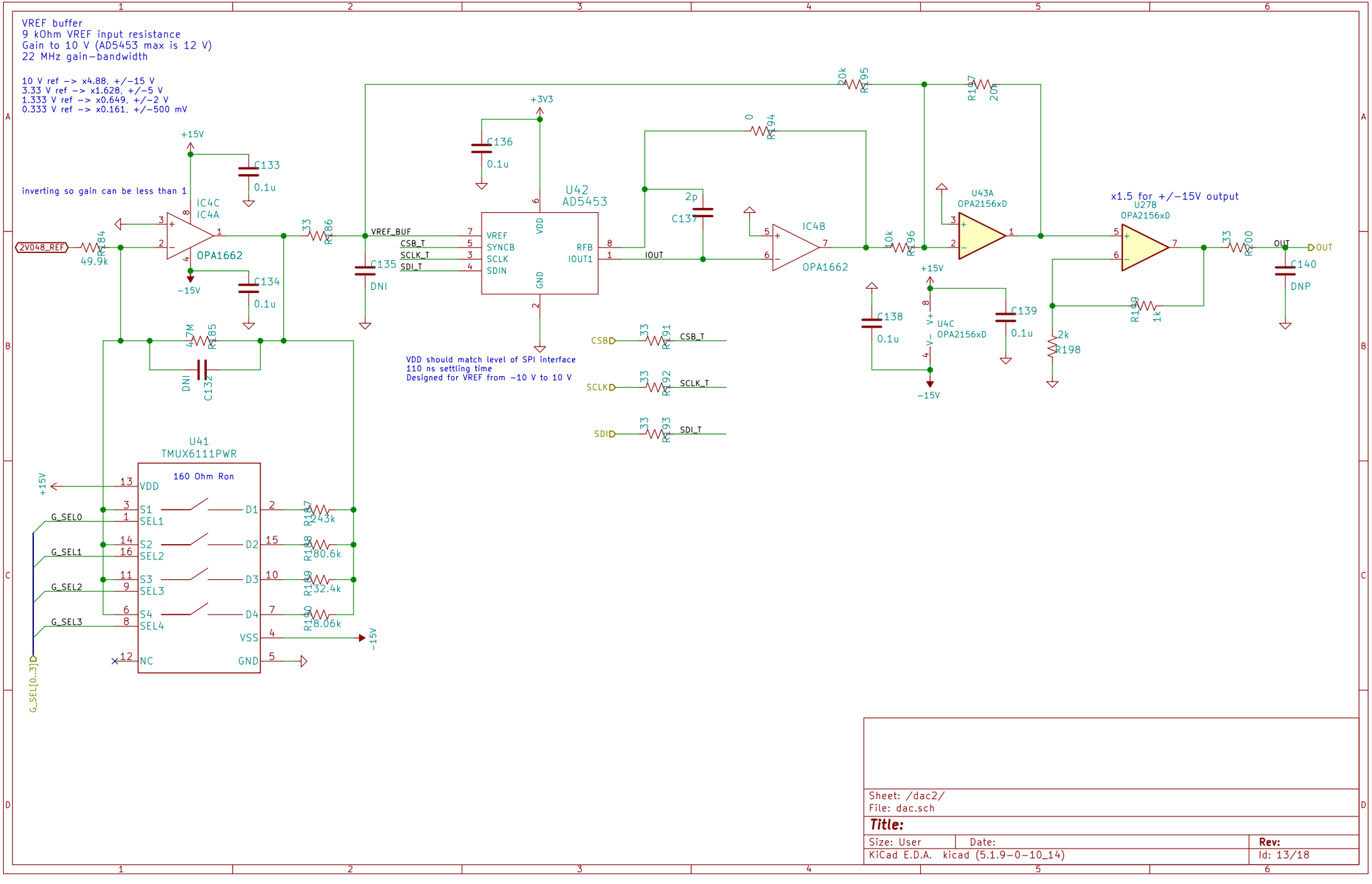
VDD2 and VIO can come from the same supply.
But route and decouple separately.

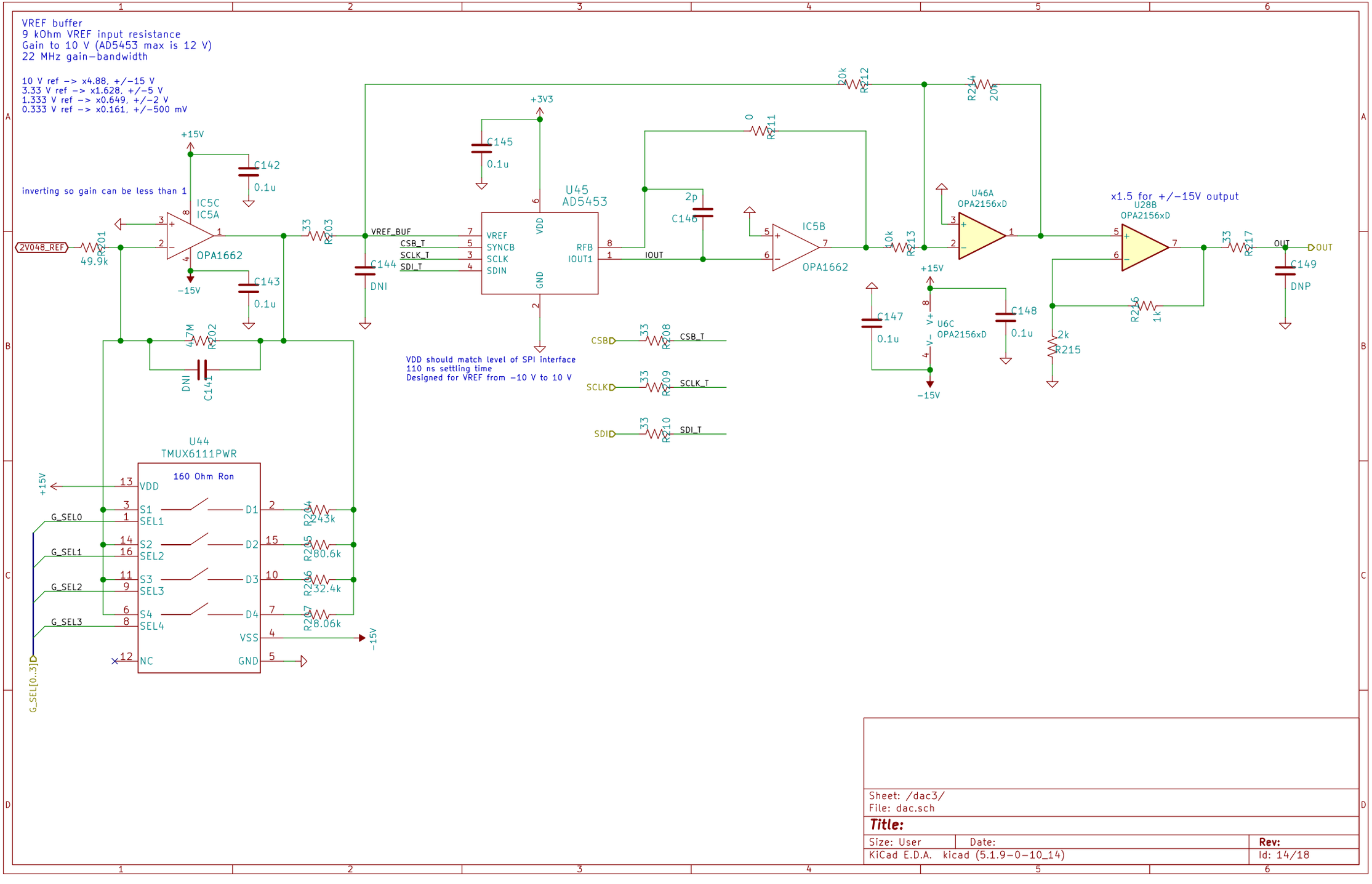


Sheet: /adc3/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 10/18

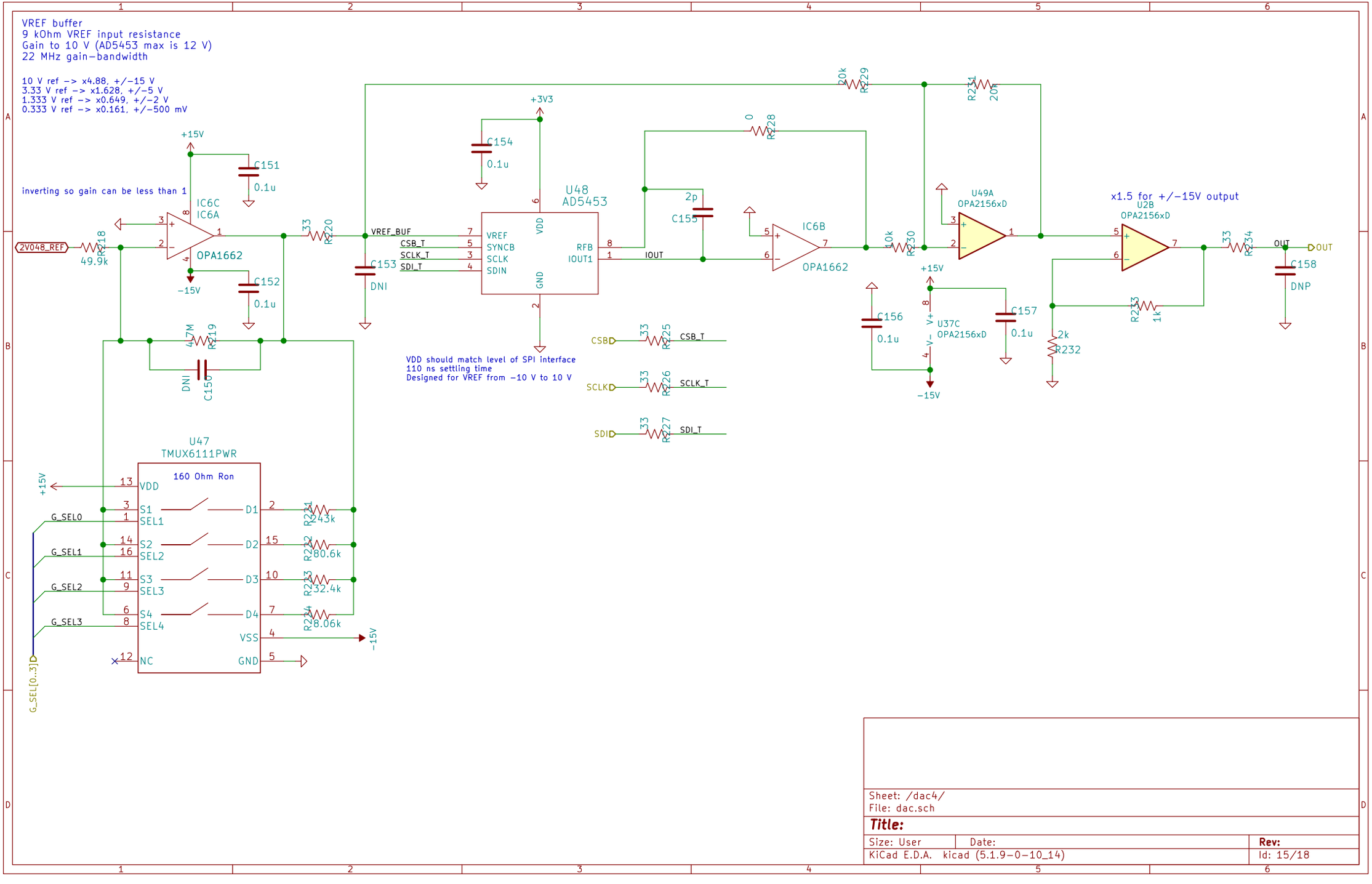

VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
IC1C
IC1A
OPA1662
2V048_REF
R150
49.9k
+15V
-15V
C115
0.1u
C116
0.1u
R151
47M
DNI
C114
R152
33
VREF_BUF
C117
DNI
+3V3
C118
0.1u
U36
AD5453
CSB_T
SCLK_T
SDI_T
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
2p
C119
IOUT
0
R160
IC1B
OPA1662
20k
R161
20k
R163
10k
R162
C120
0.1u
U27C
OPA2156xD
C121
0.1u
U37A
OPA2156xD
x1.5 for +/-15V output
U8B
OPA2156xD
2k
R164
1k
R165
33
R166
OUT
C122
DNP
CSB
SCLK
SDI
R157
R158
R159
33
U35
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
NC
GND
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
R153
243k
R154
80.6k
R155
32.4k
R156
8.06k
Sheet: /dac1/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 11/18

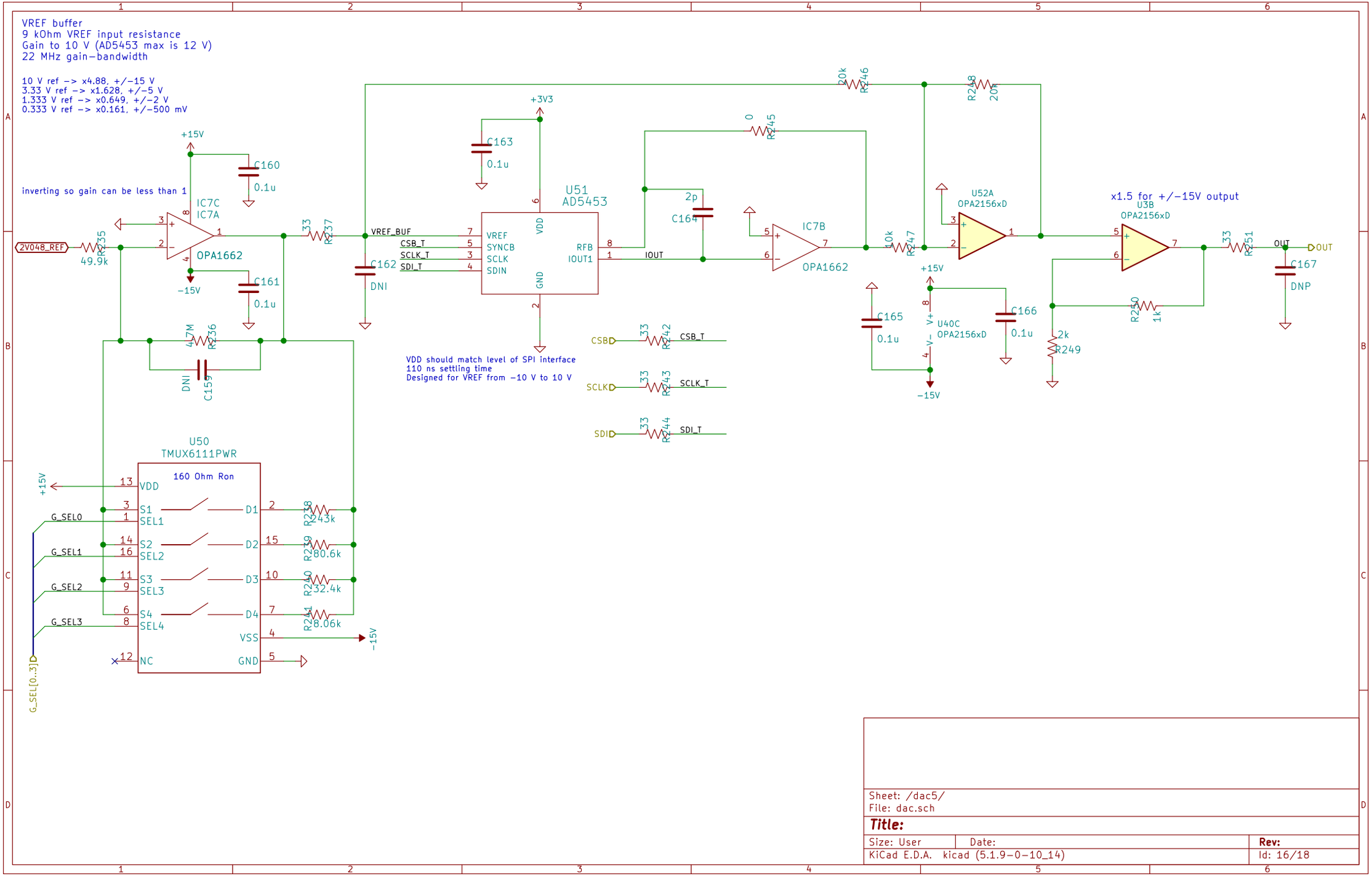

VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
IC2C
IC2A
OPA1662
2V048_REF
R167
49.9k
+15V
-15V
C124
0.1u
C125
0.1u
47M
R168
DNI
C123
33
R169
C127
0.1u
+3V3
U39
AD5453
VREF_BUF
CSB_T
SCLK_T
SDI_T
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
C126
DNI
2p
C128
IOUT
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
CSB
SCLK
SDI
33
R174
R175
R176
CSB_T
SCLK_T
SDI_T
0
R177
IC2B
OPA1662
20k
R178
R180
20k
10k
R179
C129
0.1u
U28C
OPA2156xD
C130
0.1u
U40A
OPA2156xD
x1.5 for +/-15V output
U26B
OPA2156xD
2k
R181
1k
R182
33
R183
OUT
C131
DNP
U38
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
GND
NC
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
R170
243k
R171
80.6k
R172
32.4k
R173
8.06k
Sheet: /dac0/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 12/18

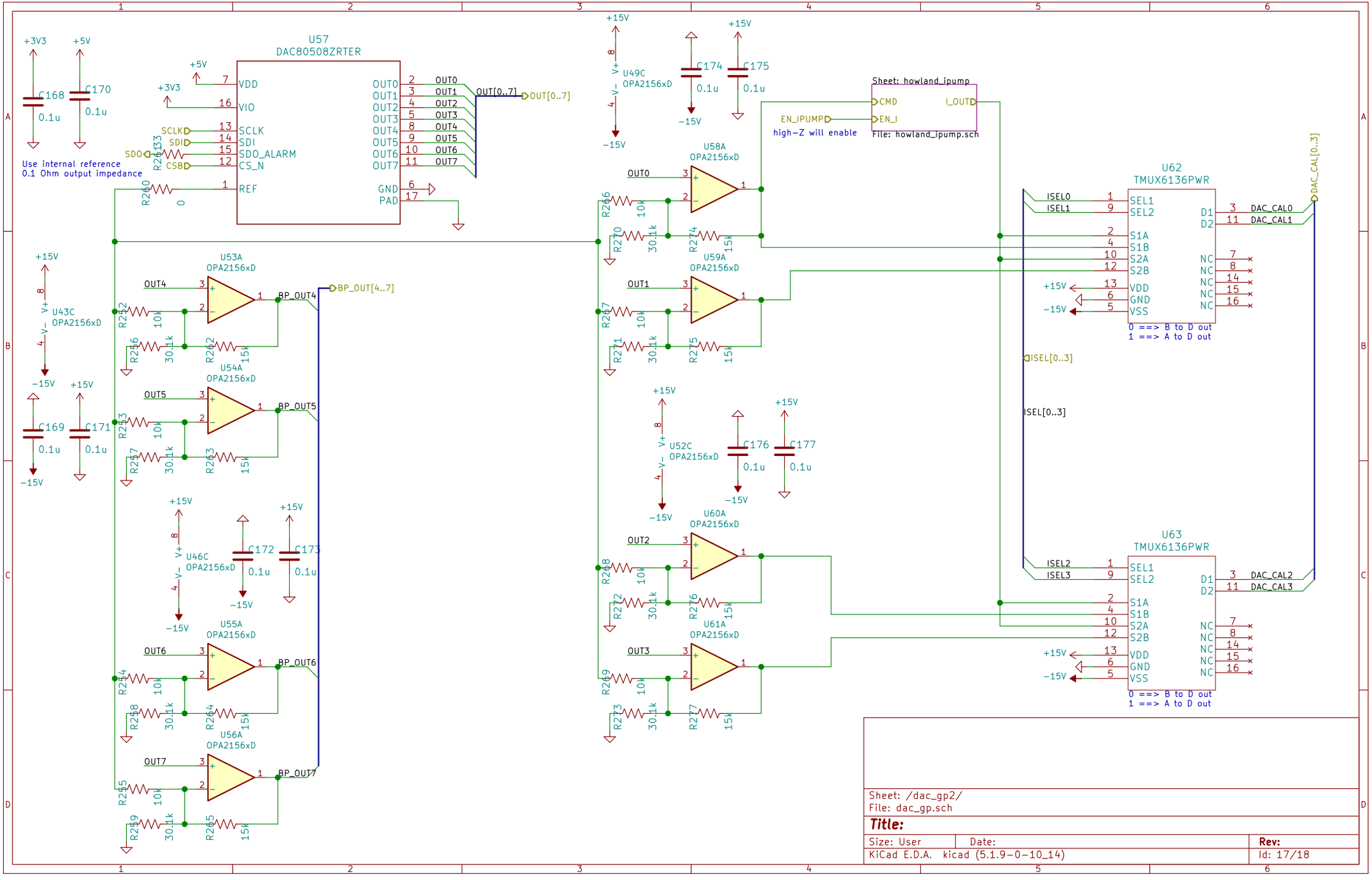

VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
IC4C
IC4A
OPA1662
+15V
-15V
2V048_REF
R184
49.9k
C133
0.1u
C134
0.1u
47M
R185
DNI
C132
33
R186
VREF_BUF
C135
DNI
+3V3
C136
0.1u
U42
AD5453
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
CSB_T
SCLK_T
SDI_T
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
2p
C137
0
R194
IC4B
OPA1662
20k
R195
20k
R197
10k
R196
U43A
OPA2156xD
x1.5 for +/-15V output
U27B
OPA2156xD
33
R200
OUT
C140
DNP
R199
1k
2k
R198
C138
0.1u
C139
0.1u
U4C
OPA2156xD
CSB
SCLK
SDI
33
R191
R192
R193
U41
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
NC
GND
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
R187
243k
R188
80.6k
R189
32.4k
R190
8.06k
Sheet: /dac2/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 13/18

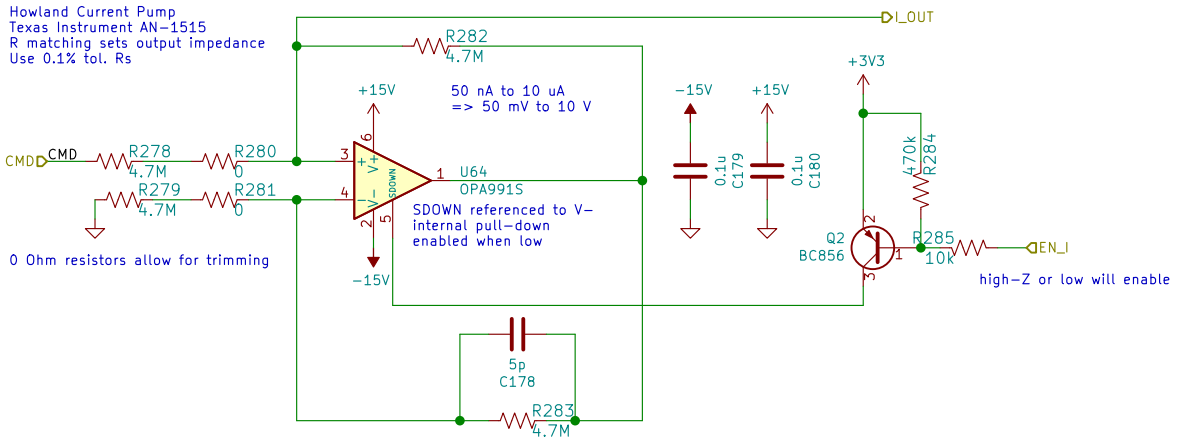


Sheet: /dac3/		
File: dac.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 14/18


VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
IC6C
IC6A
OPA1662
2V048_REF
R218
49.9k
+15V
-15V
C151
0.1u
C152
0.1u
47M
R219
DNI
C150
33
R220
C153
DNI
+3V3
C154
0.1u
U48
AD5453
VREF_BUF
CSB_T
SCLK_T
SDI_T
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
IOUT
2p
C155
0
R228
20k
R229
20k
R231
IC6B
OPA1662
10k
R230
U49A
OPA2156xD
x1.5 for +/-15V output
U2B
OPA2156xD
33
R234
OUT
OUT
C158
DNP
R233
1k
2k
R232
C156
0.1u
C157
0.1u
U37C
OPA2156xD
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
CSB
SCLK
SDI
33
R225
33
R226
33
R227
CSB_T
SCLK_T
SDI_T
U47
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
GND
NC
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
R221
243k
R222
80.6k
R223
32.4k
R224
8.06k
Sheet: /dac4/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 15/18


VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
inverting so gain can be less than 1
IC7C
IC7A
OPA1662
+15V
-15V
2V048_REF
R235
49.9k
C160
0.1u
C161
0.1u
47M
R236
DNI
C159
33
R237
C162
DNI
VREF_BUF
CSB_T
SCLK_T
SDI_T
U51
AD5453
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
+3V3
C163
0.1u
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
CSB
SCLK
SDI
33
R242
R243
R244
CSB_T
SCLK_T
SDI_T
2p
C164
0
R245
IC7B
OPA1662
20k
R246
R248
20k
10k
R247
C165
0.1u
U40C
OPA2156xD
C166
0.1u
2k
R249
U52A
OPA2156xD
x1.5 for +/-15V output
U3B
OPA2156xD
R250
1k
33
R251
OUT
C167
DNP
U50
TMUX6111PWR
160 Ohm Ron
VDD
VSS
GND
NC
S1
S2
S3
S4
D1
D2
D3
D4
SEL1
SEL2
SEL3
SEL4
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
R238
243k
R239
80.6k
R240
32.4k
R241
8.06k
Sheet: /dac5/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 16/18


U57
DAC80508ZRTER
VDD
VIO
SCLK
SDI
SDO_ALARM
CS_N
REF
GND
PAD
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT[0..7]
Use internal reference
0.1 Ohm output impedance
U49C
OPA2156xD
U58A
OPA2156xD
U59A
OPA2156xD
U52C
OPA2156xD
U60A
OPA2156xD
U61A
OPA2156xD
U53A
OPA2156xD
U54A
OPA2156xD
U46C
OPA2156xD
U55A
OPA2156xD
U56A
OPA2156xD
U43C
OPA2156xD
Sheet: howland_ipump
CMD
I_OUT
EN_I
EN_IPUMP
high-Z will enable
File: howland_ipump.sch
U62
TMUX6136PWR
U63
TMUX6136PWR
ISEL0
ISEL1
ISEL2
ISEL3
ISEL[0..3]
DAC_CAL0
DAC_CAL1
DAC_CAL2
DAC_CAL3
DAC_CAL[0..3]
0 ==> B to D out
1 ==> A to D out
BP_OUT[4..7]
BP_OUT4
BP_OUT5
BP_OUT6
BP_OUT7
Sheet: /dac_gp2/
File: dac_gp.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 17/18



Sheet: /dac_gp2/howland_ipump/		
File: howland_ipump.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 18/18