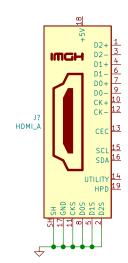
Sheet: gp\_adc File: gp\_adc.sch

Sheet: ok\_fpga File: ok\_fpga.sch Sheet: level\_shifters File: level\_shifters.sch Sheet: adc1 File: adc1.sch

Sheet: dac1 File: dac1.sch

Sheet: dac\_gp File: dac\_gp.sch Sheet: power File: power.sch

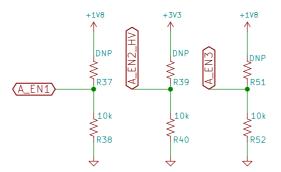






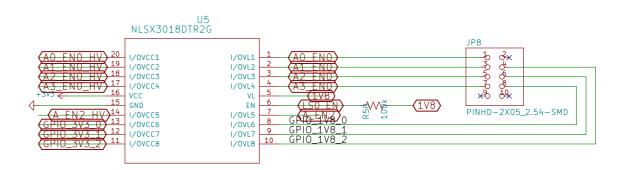


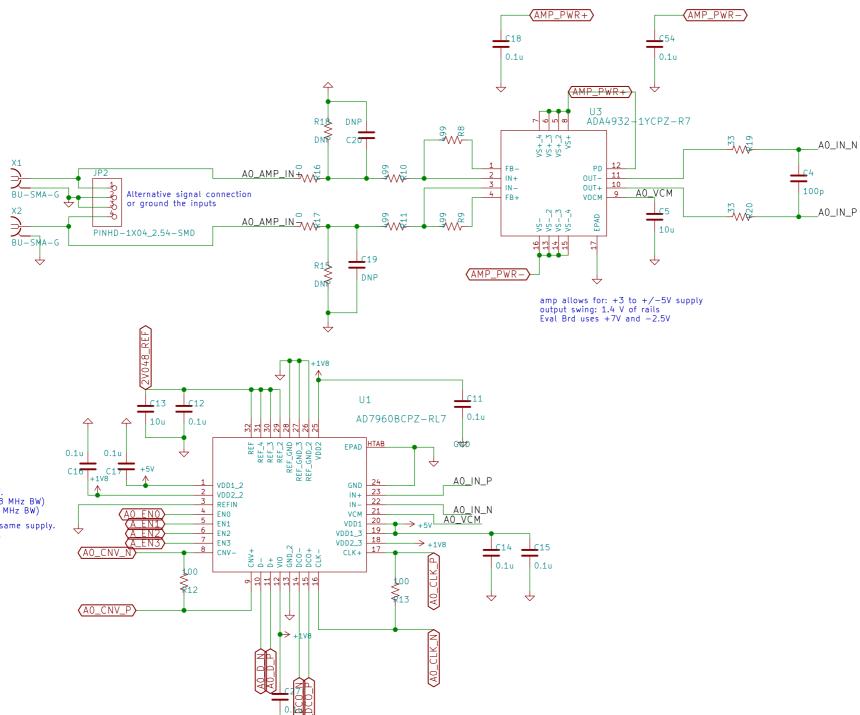
H2 MOUNT-HOLE3.0



High speed ADC enable signals Connect A\_EN2\_HV to FPGA

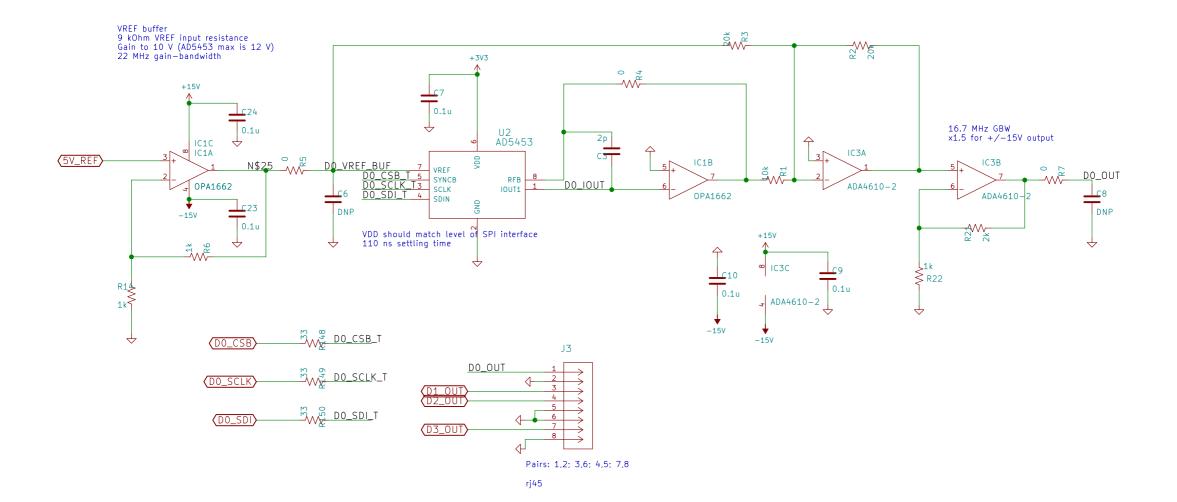
These are global (for all ADC channels) ENO is the only signal that needs FPGA control per ADC channel.

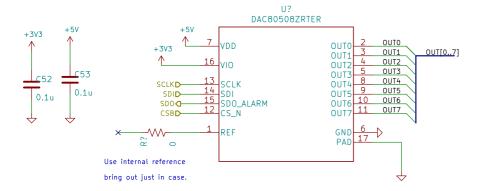




Use internal buffer with 2.048V ref. EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW) EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW)

VDD2 and VIO can come from the same supply. But route and decouple separately.





Howland Current Source (needs to MUX to any DAC HDMI signal)

Optional gain and unipolar to bipolar

Add connector here?

