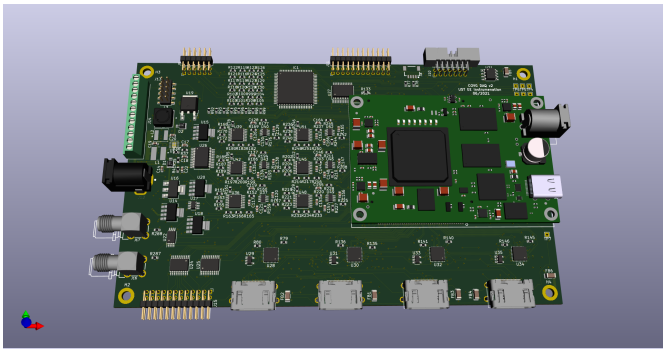
Project Description

This repository houses the KiCad schematic, layout, and BOM for a general-purpose data acquisition board (DAQ) that enables real-time feedback with latencies of < 2 us by direct interfaces of ADCs and DACs to the XEM7310 OpalKelly FPGA module. This DAQ board is designed for a digital feedback implementation of a clamp amplifier for the cut-open vaseline gap (COVG) electrophysiology method and may also find a use for other scientific studies requiring low latency control.

The **schematic is here** and a 3d rendering of the board is shown below:



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Board Description

Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs)

- **High-speed ADCs AD7961 ADC @ 5 MSPS (x4)**: 16-bit differential input ADC with LVDS data interface to the FPGA, one cycle latency. Input must be differential with a common-mode voltage that matches the common-mode output of the part (~2.5 V).
- **General purpose ADC ADS8686 (x1)**: 16 channels, maximum of 1 MSPS, SPI interface. The analog input range is programmable to +/-2.5 V, +/-5V, +/-10V. 8 channels are available on the pin-header J9; the other 8 channels are routed to the HDMI daughtercard connectors.
- **High-speed DACs AD5453 DAC (x6):** 14-bit, multiplying R-2R ladder with 100 ns settling time. These fast DAC outputs connect to the HDMI daughtercard connecters and have programmable gain with full-scale bipoloar ranges of +/- 15V, +/- 5V, +/- 2 V, +/- 500 mV, +/- 200 mV.
- **General purpose DAC DAC80508 (x2):** 8-channel, 16-bit, voltage output with 5 us settling time. The unipolar DAC outputs are converted to +/-7.5 V bipolar outputs before connecting to the HDMI daughtercard connectors. Pin header J11 has x8 bipolar outputs, x10 0-5V unipolar direct DAC output signals, and x2 "calibration" outputs which can be programmed to be the output of a current source (Howland) driven by the DAC.

Digital Interfaces

At connector J15:

- Digital I/O level-shifted to 1.8 V levels (x6). (signals DNO[0-5])
- Digital I/O level-shifted to 5.0 V levels (x6). (signals UPO[0-5])
- Digital I/O at 3.3 V levels (x4). (signals GPIO[0-3])
- I2C interface at 1.8 V (1V8_SCL, 1V8_SDA)

At connector J10:

- General LVDS I/O 4 differential pairs at 2.5 V. Can also be used as 8 LVCMOS I/O. Note the routing of these LVDS pairs is only very roughly impedance controlled. Performance at the highest frequencies will need evaluation.

At SMA connectors J16 and J17:

- J16 and J17, 3.3V LVCMOS routed to multi-region clock capable pins. Potential use is to synchronize with other systems.

At QWIIC connector, J18:

- The Sparkfun QWIIC connector has 4 pins. 3.3 V power, I2C (SDA and SCL), and Gnd. This is a standardized interface to I2C-based sensor boards.

Power

An input voltage of 6 to 7V is supplied at barrel connector J12 (PJ-002BH) with a maximum rating of 5 A.

The power system is as follows:

- Dual DC-DC converter to +/-16.5 V - The +/-16.5 V is regulated down to +/-15 V (linear)
- Regulator to 5 V (linear)

- Regulator to 3.3 V (linear)
- Regulator to 2.5 V for LVDS bank on FPGA (linear)
- Regulator to 1.8 V (linear)
- Voltage reference for 2.048 V.

All power nets are connected to a screw terminal block connector to allow for monitoring or override of the on-board regulated voltages.

FPGA capabilities

The XEM7310 OpalKelly FPGA module has a Artix7 FPGA (XC7A5T-1) with a USB 3.0 interface to a host computer (transfer rates up to 30 MiB/s). The module has 1-GiByte of DDR3 to enable burst data captures or burst data transfers.

Daughtercard Channels (x4)

The DAQ board has four connections to support analog daughtercards. The daughtercard connections are standardized and use an HDMI connector. For the COVG electrophysiology amplifier, these channels are the bath clamp, guard clamp, V1/I top clamp, and (optionally) the V2 monitor. Future experiments could use one or up to all of these daughtercard connections.

Channel connection definition

The generic HDMI-A cable pinout is defined as follows with 15 (non-shield) pins used:

- **Power**: (3 pins) +5V, +15V, -15V
- **GND**: (1 pins)
- **Analog inputs** to ADCs: (4 pins)
  - OUT_P, OUT_N differential pair (x1) to 5 MSPS ADC
  - single-ended out AMP_OUT, CAL_ADC each connect to an individual channel of 1 MSPS ADC (ADS8686)
- **Analog reference output**: (1 pin) buffered ADC common-mode voltage (nominal 2.5 V) from the AD796x.
- **Digital outputs** from DACs: (3 pins)
  - Fast DAC1 (CMD)
  - Fast DAC2 (CC) on channels 0 and 1. From general-purpose DAC on channels 2 and 3.
  - From general purpose 5 us settling time DAC (DAC8050). Either voltage source or current source (Howland current pump), programmable (CAL_DAC).
- **I2C Digital control**: (2 pins) SDA, SCL (@ 3.3 V levels). Pull-up resistors (3.3 kOhm) are placed on the DAQ board. A common approach is for the daughtercards to use an I/O expander (such as the TCA9555) to generate many control signals from the 2-wire I2C interface.
- **Utility**: (1 pin) Resistor jumper sets analog in, analog out, or digital I/O (@ 3.3 V levels). The default stuffing option is to connect this pin to the general-purpose ADC (ADS8686).

Pin	HDMI name	Generic Daughtercard	Notes
1	Data2+	fastDAC1	~ 1 us settling time. Programmable full-scale range.
2	Data2	gnd	

15	SCL	SCL	I2C clock. Pull-up resistor on DAQ board, 3.3 V levels.
16	SDA	SDA	I2C data. Pull-up resistor on DAQ board, 3.3 V levels.
17	Gnd	Gnd	
18	5V	5V	Power from linear regulator (target 200 mA max per channel with all 4 channels connected)
19	HPD	Analog/GPIO3	Analog output to ADS8686 1 MSPS. Chip inputs includes a programmable PGA for full-scale range up to +/-10V

Example Daughtercard Pinout

The pin names shown in the image below are an example daughtercard interface (COVG bath-clamp).