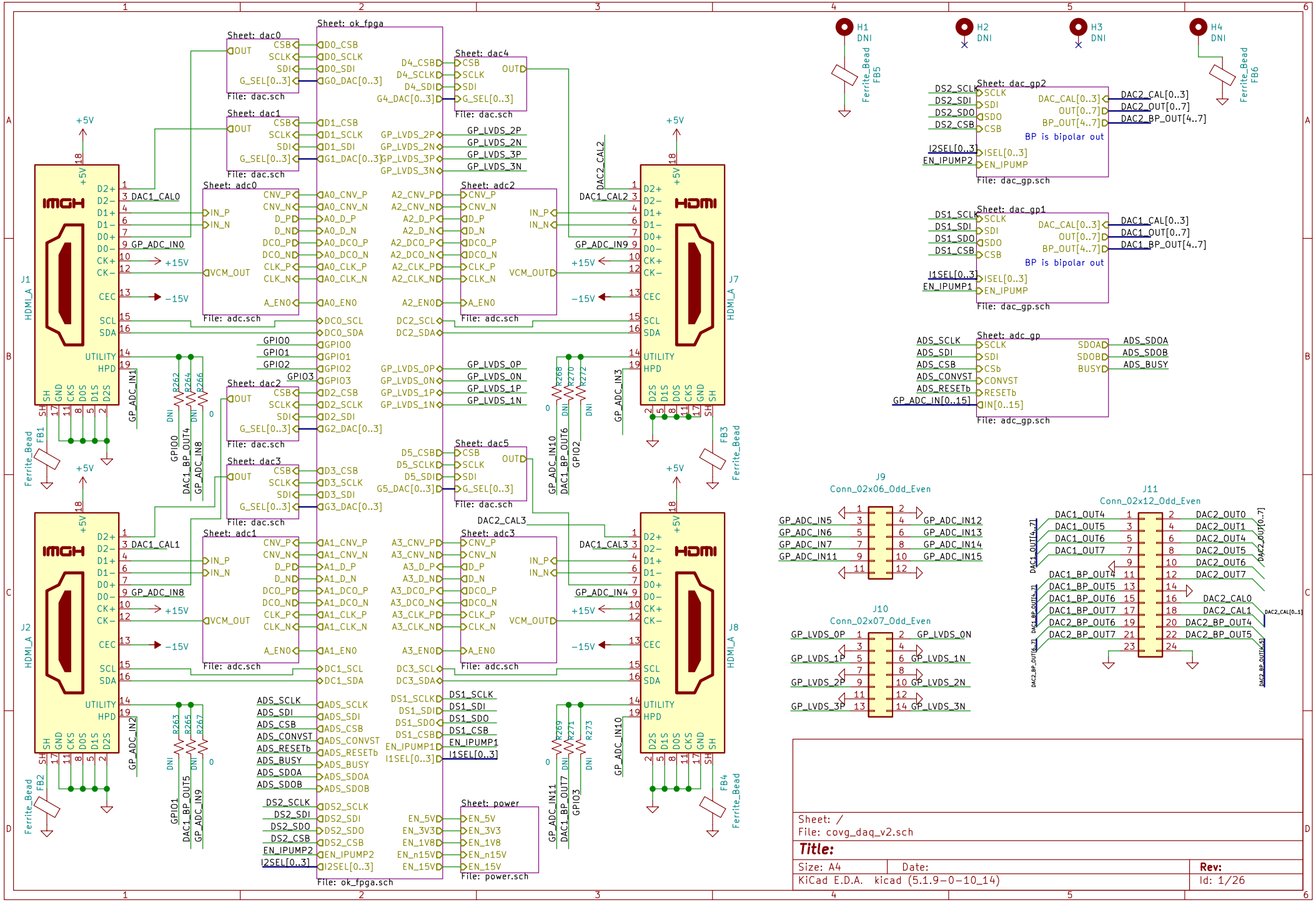
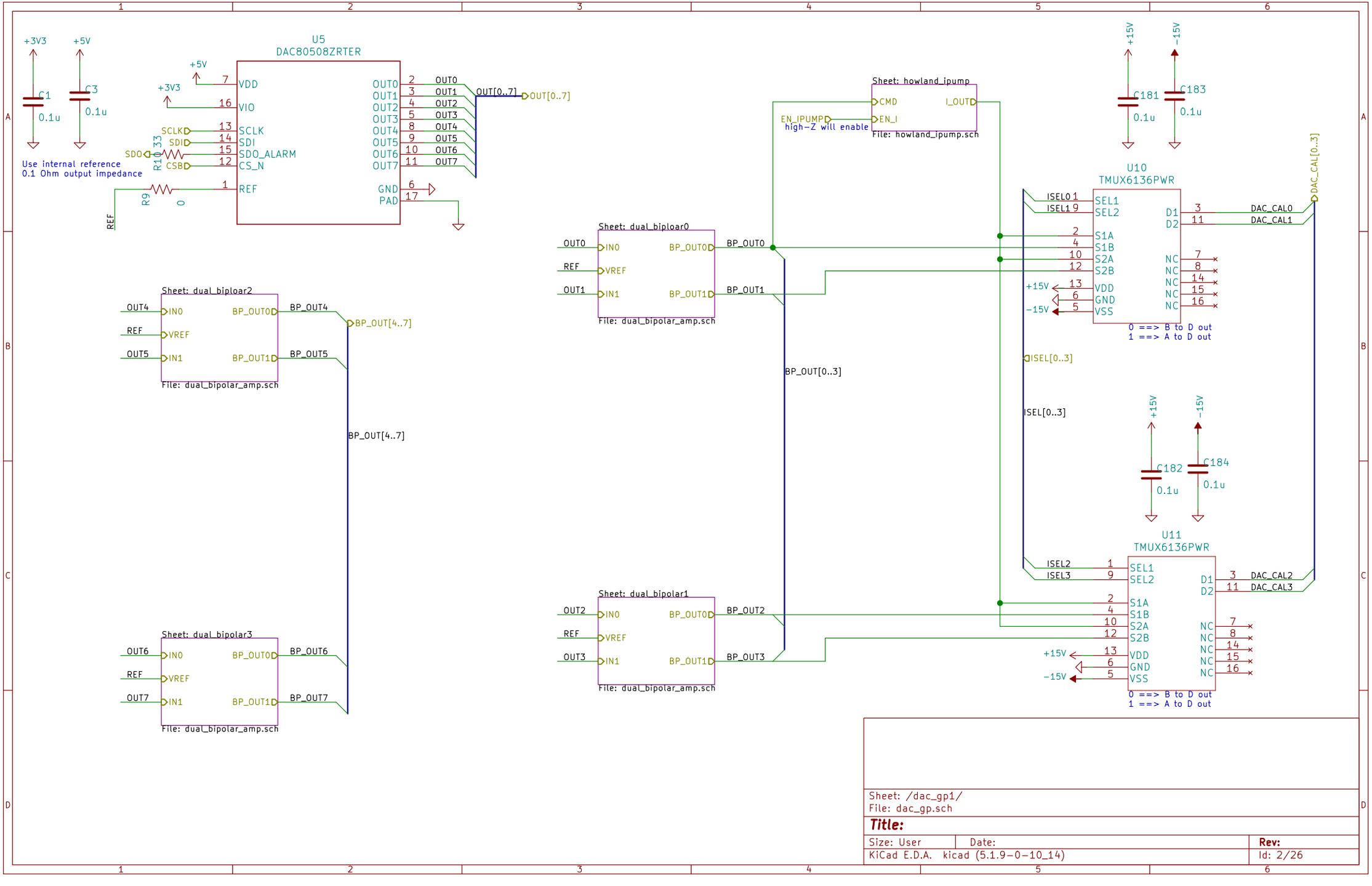
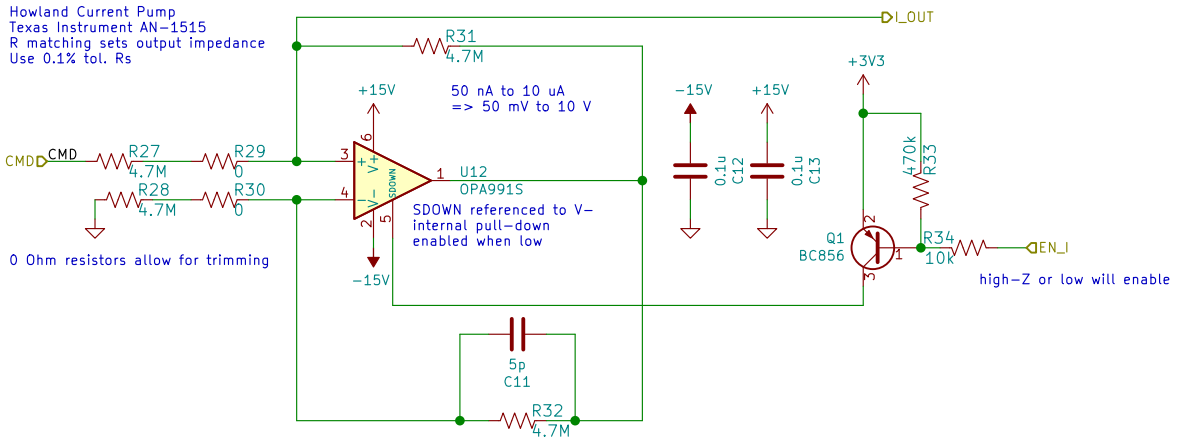
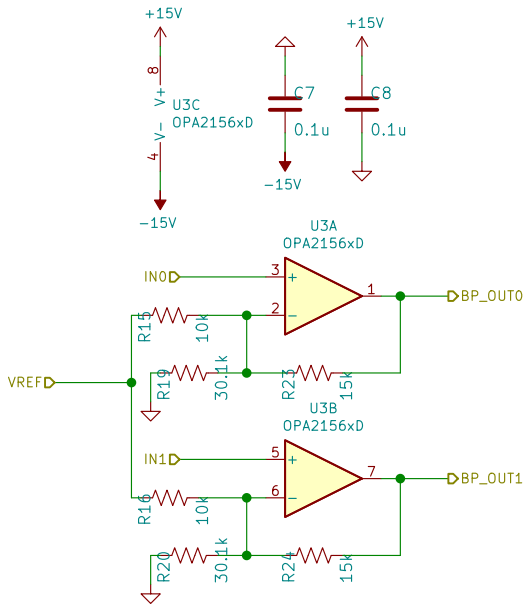

Sheet: ok_fpga
Sheet: dac0
Sheet: dac1
Sheet: dac2
Sheet: dac3
Sheet: dac4
Sheet: dac5
Sheet: adc0
Sheet: adc1
Sheet: adc2
Sheet: adc3
Sheet: power
Sheet: dac_gp2
Sheet: dac_gp1
Sheet: adc_gp
File: dac.sch
File: adc.sch
File: ok_fpga.sch
File: power.sch
File: dac_gp.sch
File: adc_gp.sch
H1 DNI
H2 DNI
H3 DNI
H4 DNI
Ferrite_Bead FB5
Ferrite_Bead FB6
Ferrite_Bead FB1
Ferrite_Bead FB2
Ferrite_Bead FB3
Ferrite_Bead FB4
J1 HDMI_A
J2 HDMI_A
J7 HDMI_A
J8 HDMI_A
J9 Conn_02x06_Odd_Even
J10 Conn_02x07_Odd_Even
J11 Conn_02x12_Odd_Even
BP is bipolar out
Sheet: /
File: covg_daq_v2.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 1/26

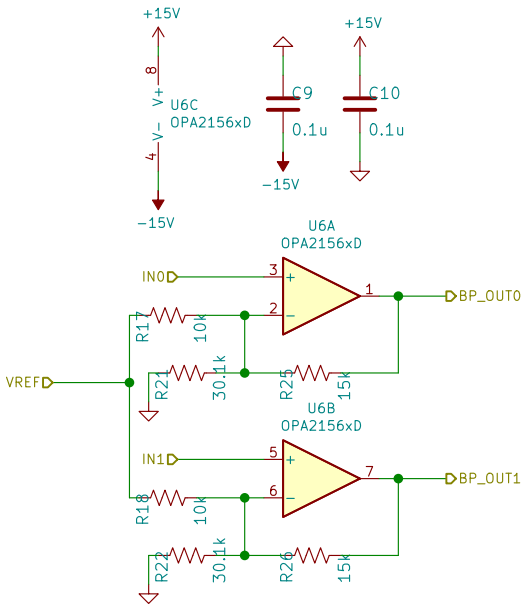

U5
DAC80508ZRTER
+3V3
+5V
C1
0.1u
C3
0.1u
Use internal reference
0.1 Ohm output impedance
VDD
VIO
SCLK
SDI
SDO_ALARM
CS_N
REF
R10
33
R9
0
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
GND
PAD
OUT[0..7]
Sheet: howland_ipump
CMD
I_OUT
EN_I
EN_IPUMP
high-Z will enable
File: howland_ipump.sch
+15V
-15V
C181
0.1u
C183
0.1u
U10
TMUX6136PWR
ISEL0
ISEL1
SEL1
SEL2
S1A
S1B
S2A
S2B
VDD
GND
VSS
D1
D2
NC
DAC_CAL0
DAC_CAL1
DAC_CAL[0..3]
0 ==> B to D out
1 ==> A to D out
ISEL[0..3]
Sheet: dual_biploar0
IN0
VREF
IN1
BP_OUT0
BP_OUT1
File: dual_bipolar_amp.sch
BP_OUT[0..3]
Sheet: dual_biploar2
BP_OUT4
BP_OUT5
BP_OUT[4..7]
Sheet: dual_bipolar1
BP_OUT2
BP_OUT3
Sheet: dual_bipolar3
BP_OUT6
BP_OUT7
C182
0.1u
C184
0.1u
U11
TMUX6136PWR
ISEL2
ISEL3
DAC_CAL2
DAC_CAL3
Sheet: /dac_gp1/
File: dac_gp.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 2/26



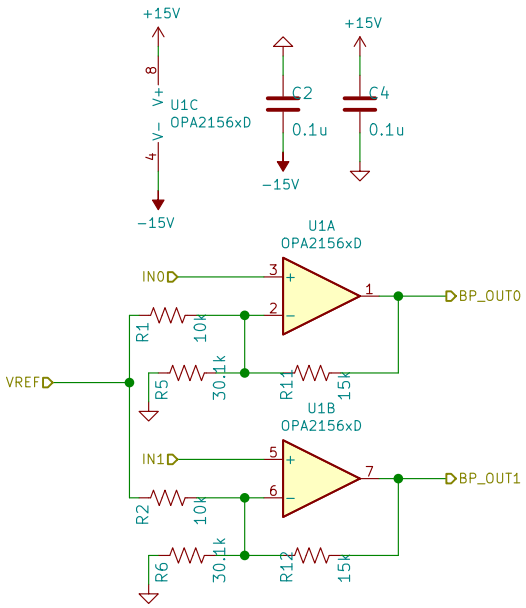
Sheet: /dac_gp1/howland_ipump/		
File: howland_ipump.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 3/26



Sheet: /dac_gp1/dual_biploar0/		
File: dual_bipolar_amp.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 4/26



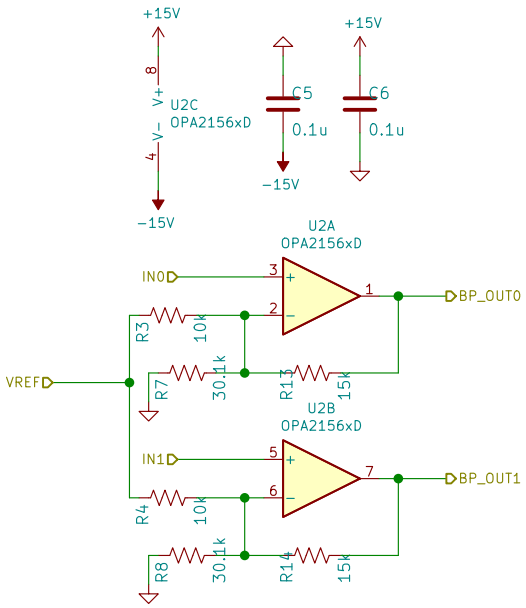
Sheet: /dac_gp1/dual_bipolar1/		
File: dual_bipolar_amp.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 5/26



Sheet: /dac_gp1/dual_biploar2/
File: dual_bipolar_amp.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 6/26



Sheet: /dac_gp1/dual_bipolar3/		
File: dual_bipolar_amp.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 7/26

PWR_FLAG PWR_FLAG PWR_FLAG PWR_FLAG

6V_IN −16V5 16V5

J12 Barrel_Jack_Switch

FB7 Ferrite_Bead

6V_IN

2.50mm ID x 5.50mm OD
5 A max

Could increase input to 7 V,
possible issues with Enables beyond that.

Vin up to 10 V
EN min is 3V with 6 V Vin

U14 LP38692MP−5.0 1 A output

6V_IN EN_5Vx IN EN OUT GND +5V

C15 1u R39 100k C21 1u

Vin up to 10 V
EN min is 3V with 6 V Vin

U15 LP38693MP−3.3

6V_IN EN_3V3x IN EN OUT GND +3V3

C24 1u R44 100k C28 1u

Vin up to 10 V
EN min is 3V with 6 V Vin

U18 LP38693MP−1.8

6V_IN EN_1V8x IN EN OUT GND +1V8

C30 1u R45 100k C33 1u

Don't use EN since this is an FPGA
bank voltage!

U20 LP38693MP−2.5

6V_IN IN EN OUT GND +2V5

500 mA output
needed for FPGA LVDS bank

C36 1u C37 1u

6V_IN

C19 4.7u

cathode is pin1

D1 D_Schottky

L1 4.7u L2 10uH 1u L3 15uH

16V5 C14 4.7u R35 232k C16 33p C20 D2 D_Schottky R42 249k C23 75p −16V5 C25 4.7u

U13 LT3471

SW1 VIN SW2 FB1P FB1N SHDN/SS1 VREF FB2P FB2N SHDN/SS2 GND

VREF_SW

R36 15k C17 0.1u R38 100k R43 15k VREF_SW

R40 100k R41 4.7k EN_n15Vx C22 0.33u

EN_15Vx R37 4.7k C18 0.33u

For noninverting regulator topologies:
VOUT = VFBP (1 + R1/R2)
VREF = 1.00 V

For inverting regulator topologies:
VOUT = VFBP (R1/R2)
VREF = 1.00 V

0.4 A output max
1.0 V dropout

U16 LM2937xMP

16V5 VI GND VO +15V

C26 0.1u C31 0.1u

−16V5 GND VI VO −15V

0.5 A output max
1.1 V dropout

C32 0.33u U19 MC79M15_TO252 C35 1u

U17
MAX6070BAUT21+T

FILTER IN EN OUTF OUTS GND 2V048_REF

+5V C27 0.1u C29 0.1u C34 0.1u

+/−10 mA output current

EN_PWR −16V5 6V_IN 16V5 −15V +3V3 +5V +15V +1V8 2V048_REF +2V5

J14 Screw_Terminal_01x12

Allows for observation
or override of supplies

J13 Conn_02x05_Odd_Even

EN_5V EN_3V3 EN_1V8 EN_15V EN_n15V

R46 0 R47 0 R48 0 R49 0 R50 0

EN_5Vx EN_3V3x EN_1V8x EN_15Vx EN_n15Vx EN_PWR

EN_PWR − supply external voltage (3.3V)
that can be jumpered to EN pins.

Default is to control by FPGA,
have 0 Ohm Rs installed,
and no jumpers on the header.

Alternative option is to add jumpers
(and if EN_PWR is > 3.3 V)remove 0 Ohm.

Sheet: /power/
File: power.sch

Title:

Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9−0−10_14)		Id: 8/26

VCCBATT is the battery backup supply for the FPGA's internal volatile memory that stores the key for the AES decryptor (not needed)

FPGA power: standard "canon-style" 2.1mm / 5.5mm jack. The outer ring is connected to DGND. The center pin is connected to +VDC.

Bank 13: 3.3V always
MC1 64 and 66-76 MC2 64 and 66-76
(24 total)

Bank 34: default 3.3V,
change by ferrite bead (FB8)
on MC1
(total of 48)

Bank 35: default 3.3V,
change by ferrite bead (FB9)
MC2 2
(total of 50)

J15
Conn_02x12_Counter_Clockwise

OK1A

OK1B

OK1C

OK1D

ADS8686
16-chan ADC

DAC80508
8-chan

DAC80508
8-chan

IO voltage for bank 35
3.3 V (leave open)

IO voltage for bank 35
3.3 V (leave open)

IO voltage for bank 34

MRCC = multi-region clock capable

U21
24AA025UID

U22
PCA9306

U23
NLSX3018DTR2

U24
TXS0108EPW

U25
TXS0108EPW

U26
TCA9555

U27
TCA9555

DAC gain control

DAC gain control

Bidirectional translator
Level shifter is not for I2C

These are global (for all ADC channels)
EN0 is the only signal that needs
FPGA control per ADC channel.
Default settings:
EN3,EN2,EN1,EN0
0,0,0,FPGA (A_EN2_HV is high-Z)

driving EN2 high outputs test
patterns on the LVDS interface

Vcc = 1.3 - 4.5 V

VL = 0.9 to VCC-0.4

VREF: needed for single-ended IO standards that use a diff. input buffer.
We do not need VREF. The FPGA also has an internal VREF which can be used if running at or below 400 MHz.
Most relevant to memory interfaces.

SparkFun qwiic connector
SM04B-SRSS-TB
3.3 V VCC

J18
QWIIC_CONNECTOR-1MM
CONN-13694

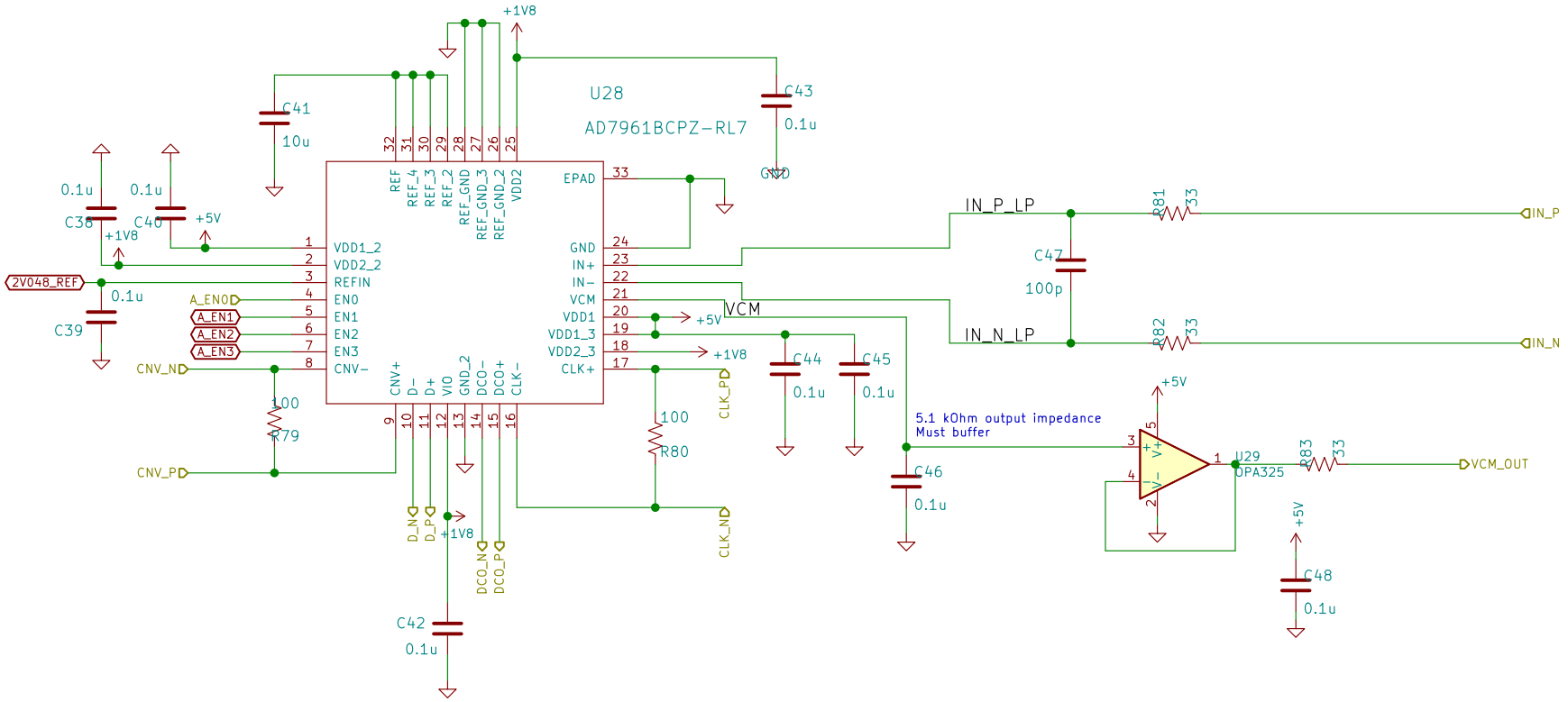
Sheet: /ok_fpga/
File: ok_fpga.sch

Title:

Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 9/26

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

VDD2 and VIO can come from the same supply.
But route and decouple separately.



Sheet: /adc1/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 10/26

AVDD bypass (1x 10uF, 1x 0.1uF per pin)

AGND_IN must be within +/−0.3 V of GND

REFIO: most guidance is 0.1uF bypass (including EVM schematics), but datasheet layout section suggests 10 uF.

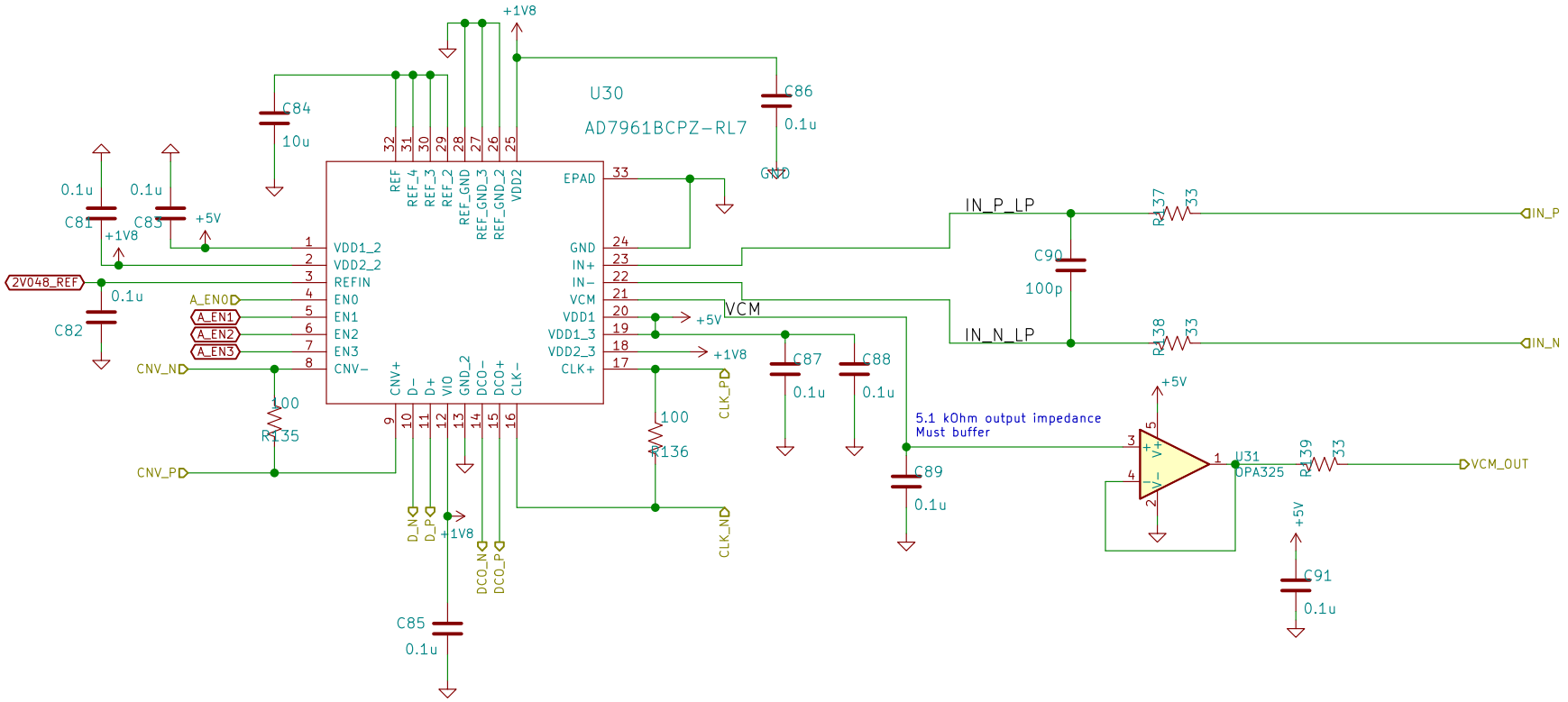
Must by pulled up by FPGA to enable. 3.3 V level.

The dual SPI interface has sufficient BW to clock the data out at the 1 MSPS (just need 16 MHz clock rate)

Sheet: /adc_gp/	
File: adc_gp.sch	
Title:	
Size: User	Date:
KiCad E.D.A. kicad (5.1.9−0−10_14)	**Rev:** Id: 11/26

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

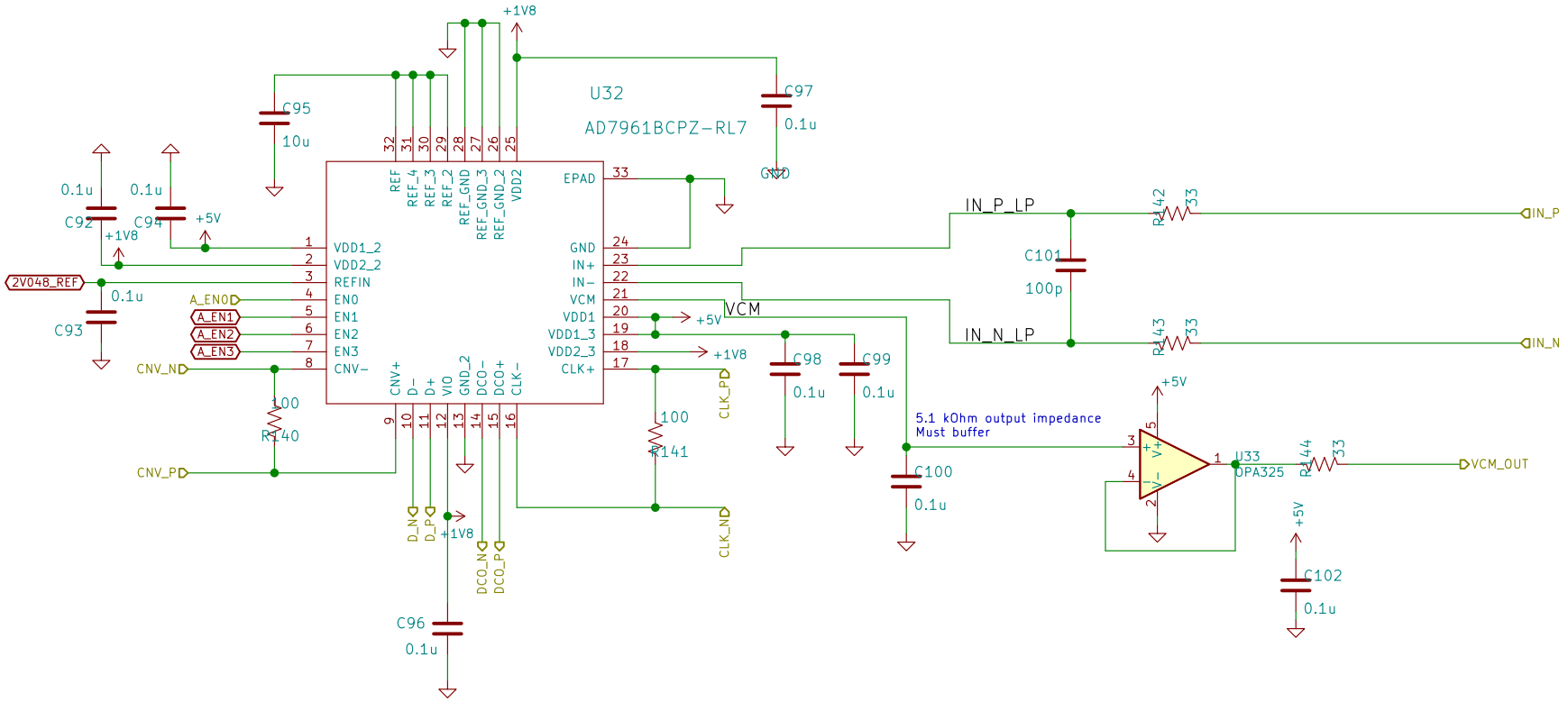
VDD2 and VIO can come from the same supply.
But route and decouple separately.



Sheet: /adc0/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 12/26

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

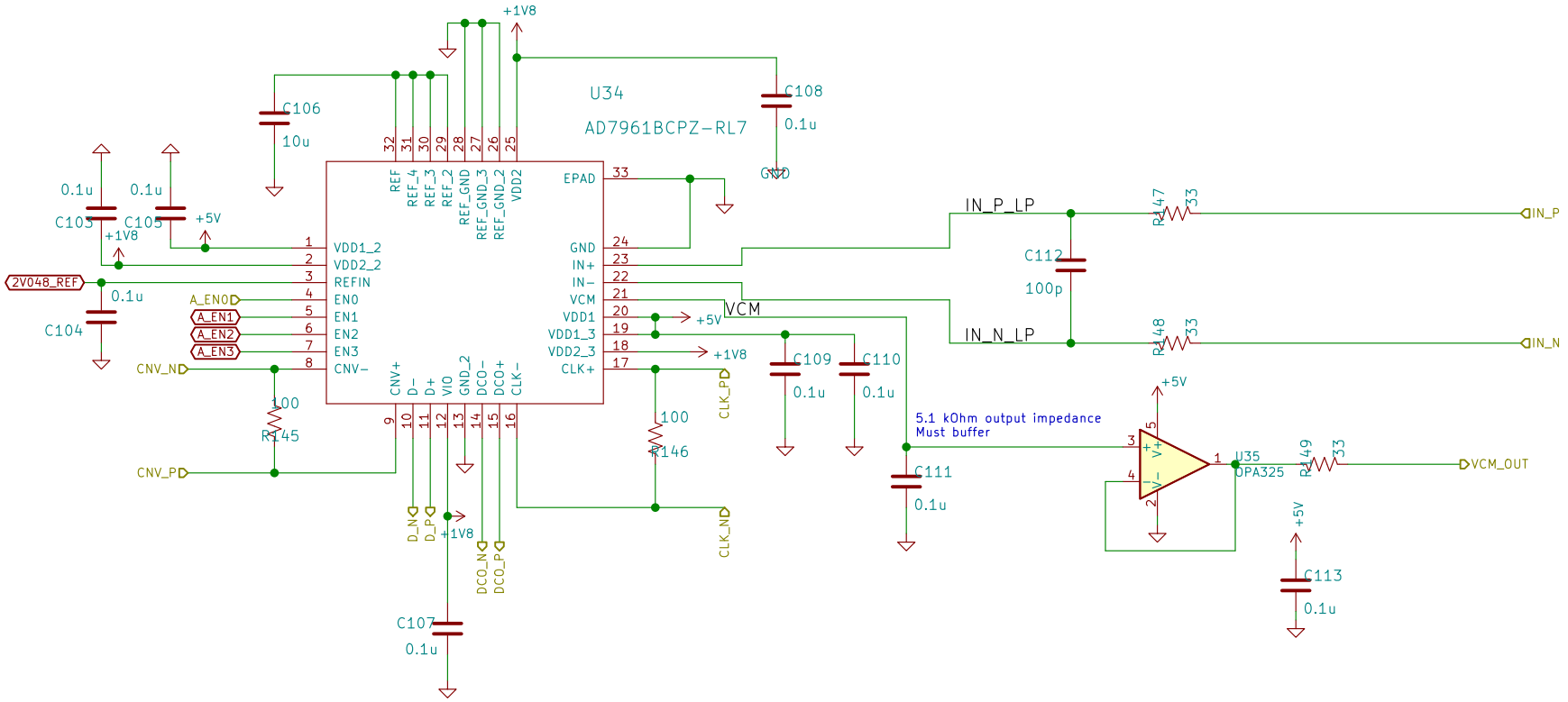
VDD2 and VIO can come from the same supply.
But route and decouple separately.



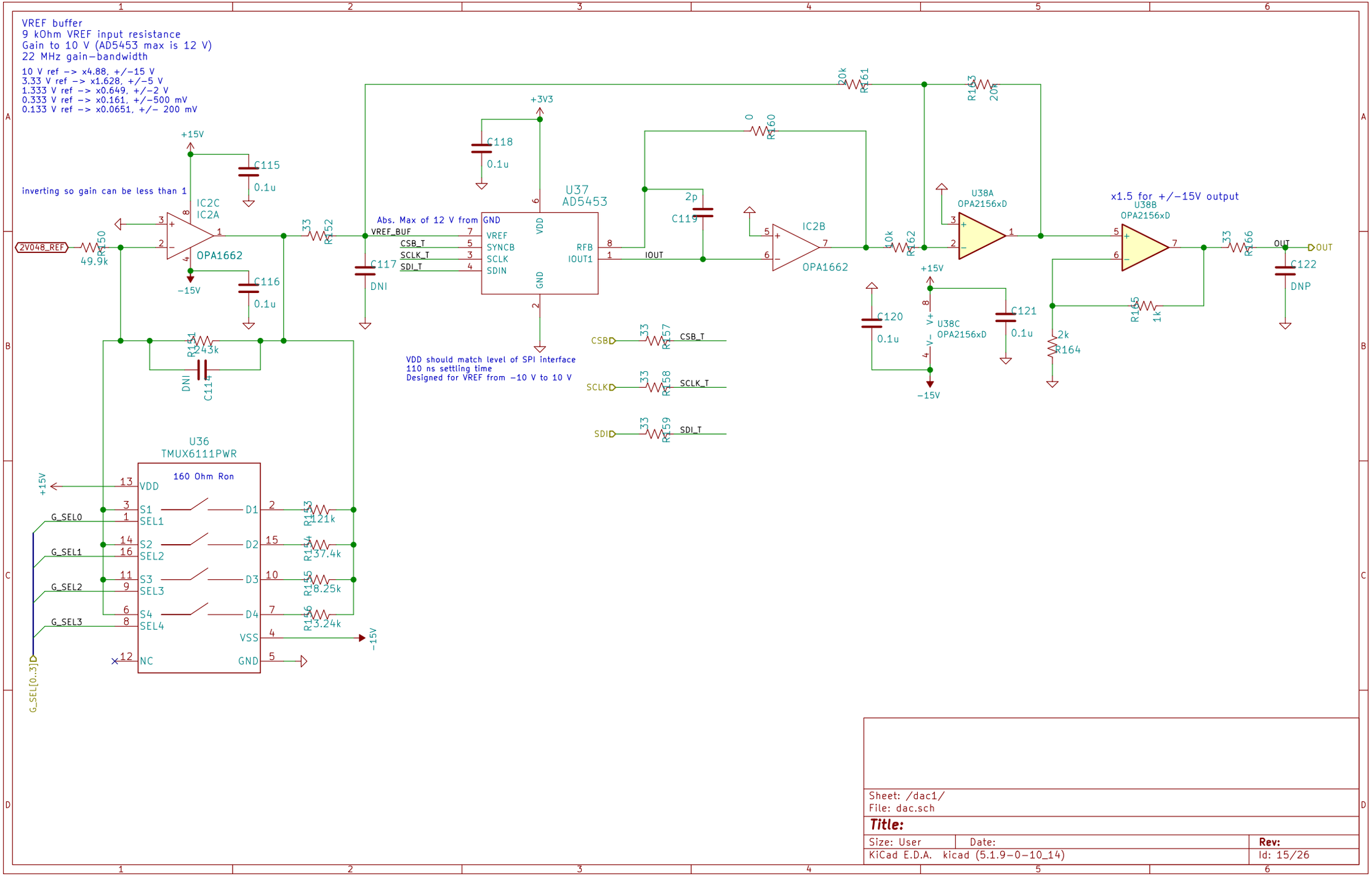
Sheet: /adc2/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 13/26

Use internal buffer (x2) with 2.048V ref.
"External reference of 2.048 V applied to the REFIN pin
(high impedance input). The on-chip buffer gains this by 2
and drives the REF pin with 4.096 V"
EN3=X, EN2=0, EN1=0, EN0=1 (28 MHz BW)
EN3=X, EN2=1, EN1=0, EN0=1 (9 MHz BW, use this BW only when the throughput is 2 MSPS or lower)

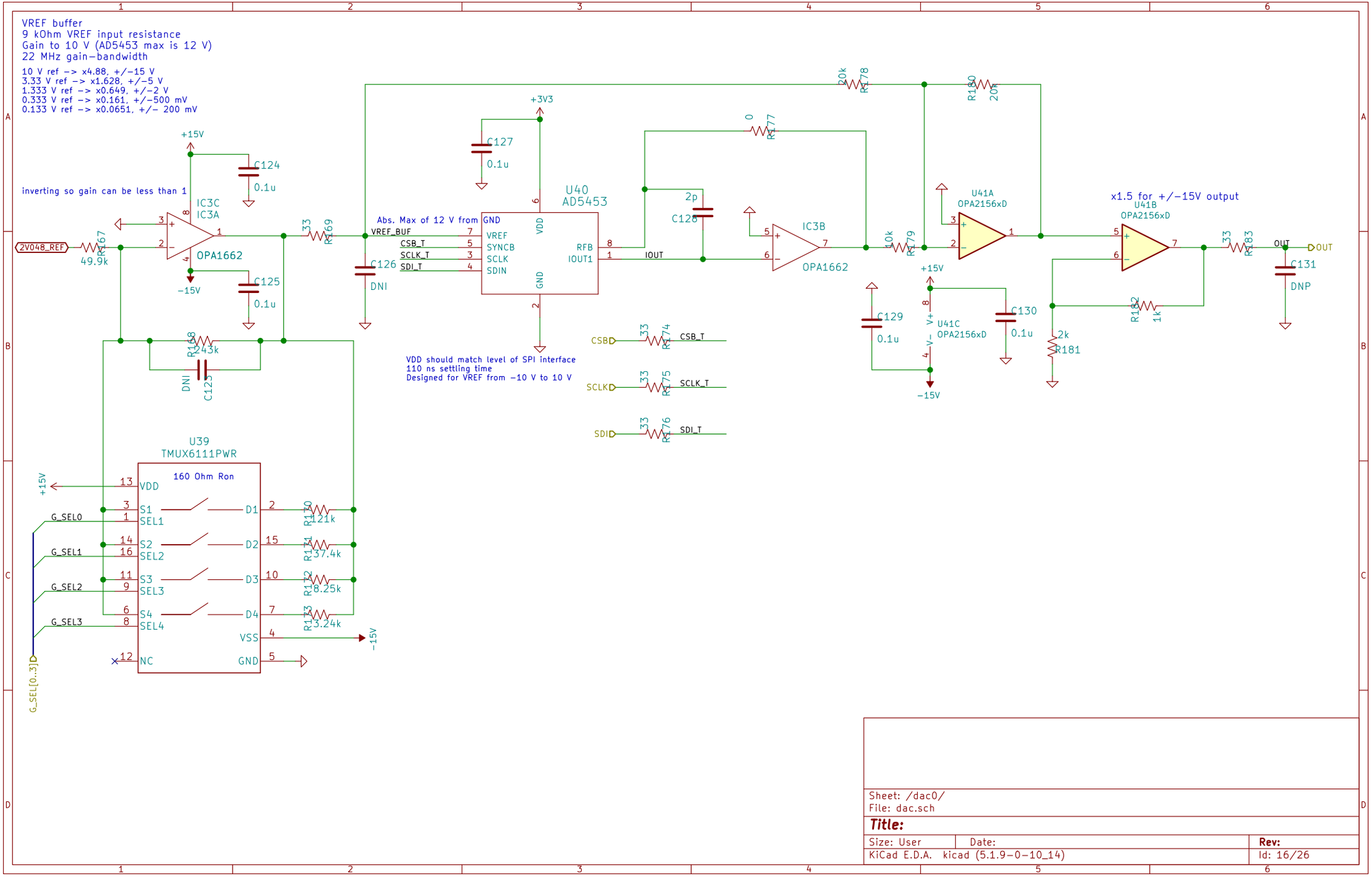
VDD2 and VIO can come from the same supply.
But route and decouple separately.

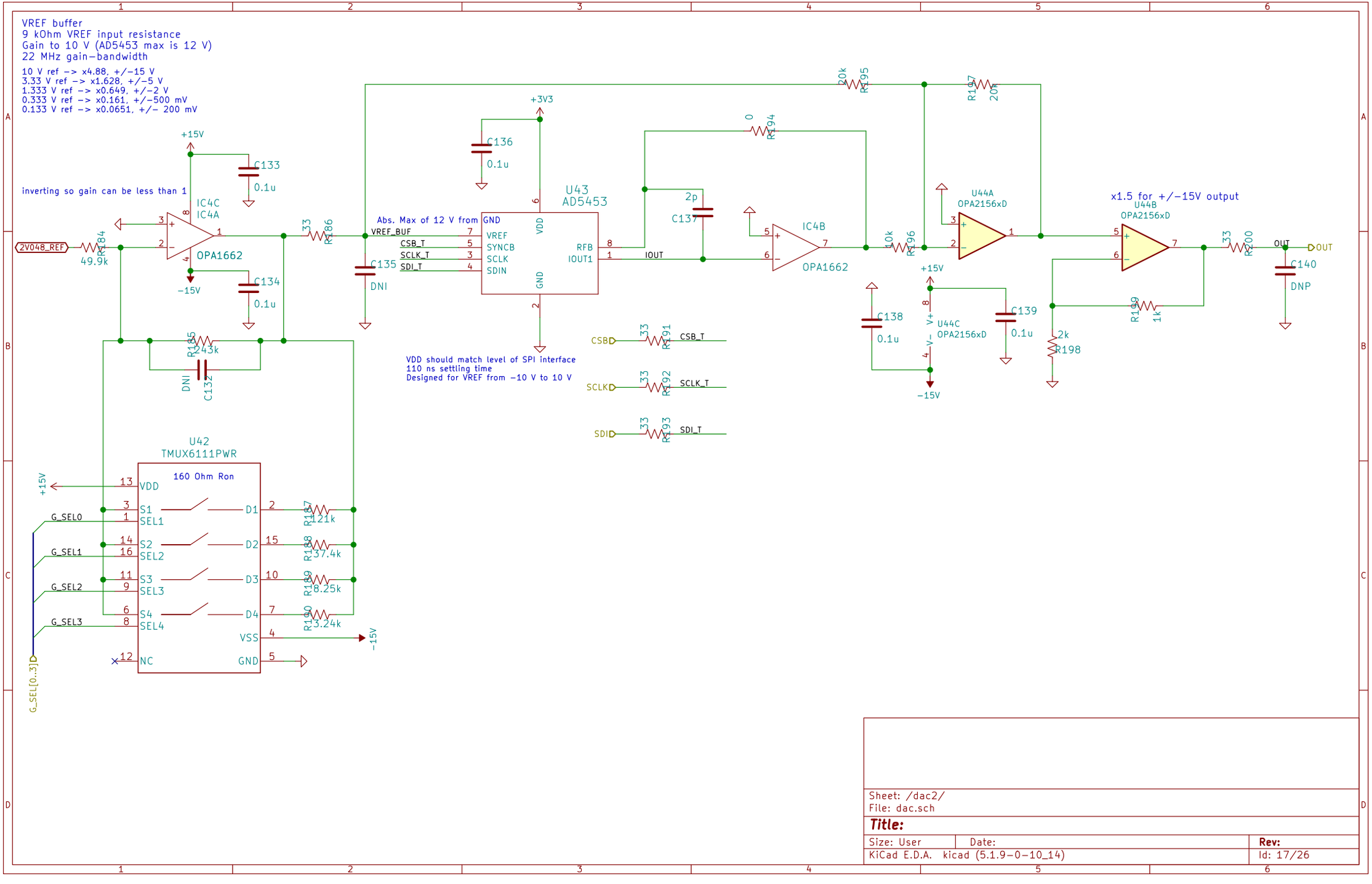


Sheet: /adc3/		
File: adc.sch		
Title:		
Size: A	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 14/26



Sheet: /dac1/		
File: dac.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 15/26


VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
0.133 V ref -> x0.0651, +/- 200 mV
inverting so gain can be less than 1
IC3C
IC3A
OPA1662
+15V
-15V
2V048_REF
R167
49.9k
C124
0.1u
C125
0.1u
R168
243k
DNI
C123
33
R169
+3V3
C127
0.1u
U40
AD5453
Abs. Max of 12 V from GND
VREF_BUF
CSB_T
SCLK_T
SDI_T
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
C126
DNI
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
2p
C128
IOUT
0
R177
20k
R178
20k
R180
IC3B
OPA1662
10k
R179
U41A
OPA2156xD
U41B
OPA2156xD
x1.5 for +/-15V output
U41C
OPA2156xD
C129
0.1u
C130
0.1u
2k
R181
1k
R182
33
R183
OUT
C131
DNP
CSB
SCLK
SDI
33
R174
R175
R176
U39
TMUX6111PWR
160 Ohm Ron
VDD
VSS
GND
NC
S1
S2
S3
S4
D1
D2
D3
D4
SEL1
SEL2
SEL3
SEL4
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
R170
121k
R171
37.4k
R172
8.25k
R173
3.24k
Sheet: /dac0/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 16/26


VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
0.133 V ref -> x0.0651, +/- 200 mV
inverting so gain can be less than 1
IC4C
IC4A
OPA1662
+15V
-15V
2V048_REF
R184
49.9k
C133
0.1u
C134
0.1u
R185
243k
DNI
C132
R186
33
C135
DNI
+3V3
C136
0.1u
U43
AD5453
Abs. Max of 12 V from GND
VREF_BUF
CSB_T
SCLK_T
SDI_T
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
IOUT
2p
C137
R194
0
20k
R195
20k
R197
IC4B
OPA1662
10k
R196
U44A
OPA2156xD
U44B
OPA2156xD
x1.5 for +/-15V output
R199
1k
2k
R198
C138
0.1u
C139
0.1u
U44C
OPA2156xD
V+
V-
33
R200
OUT
C140
DNP
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
CSB
SCLK
SDI
33
R191
R192
R193
CSB_T
SCLK_T
SDI_T
U42
TMUX6111PWR
160 Ohm Ron
VDD
S1
S2
S3
S4
SEL1
SEL2
SEL3
SEL4
D1
D2
D3
D4
VSS
GND
NC
R187
121k
R188
37.4k
R189
8.25k
R190
3.24k
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
Sheet: /dac2/
File: dac.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 17/26

VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth

10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
0.133 V ref -> x0.0651, +/- 200 mV

inverting so gain can be less than 1

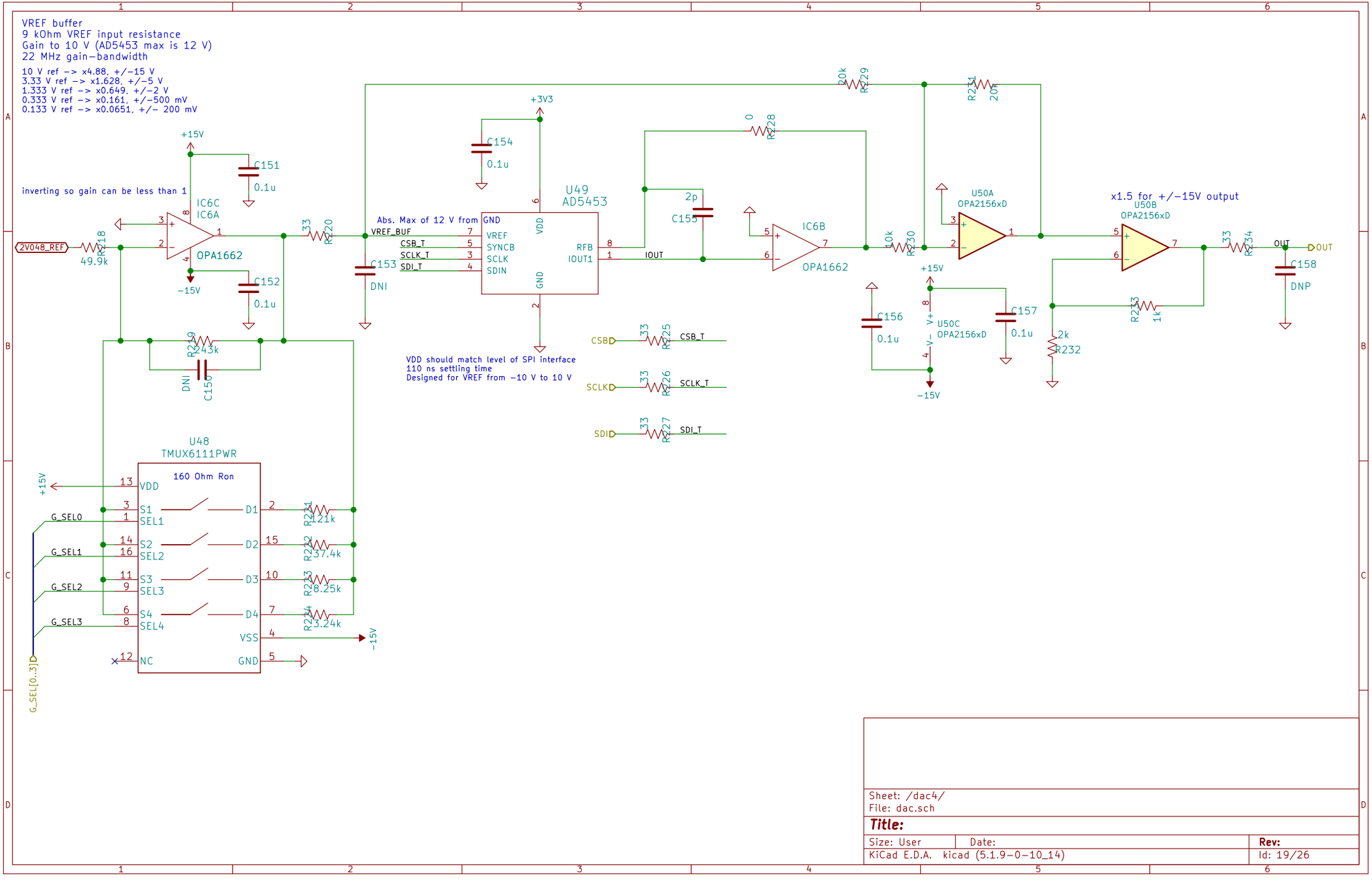
Abs. Max of 12 V from GND

VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V

x1.5 for +/-15V output

160 Ohm Ron

Sheet: /dac3/		
File: dac.sch		
Title:		
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 18/26



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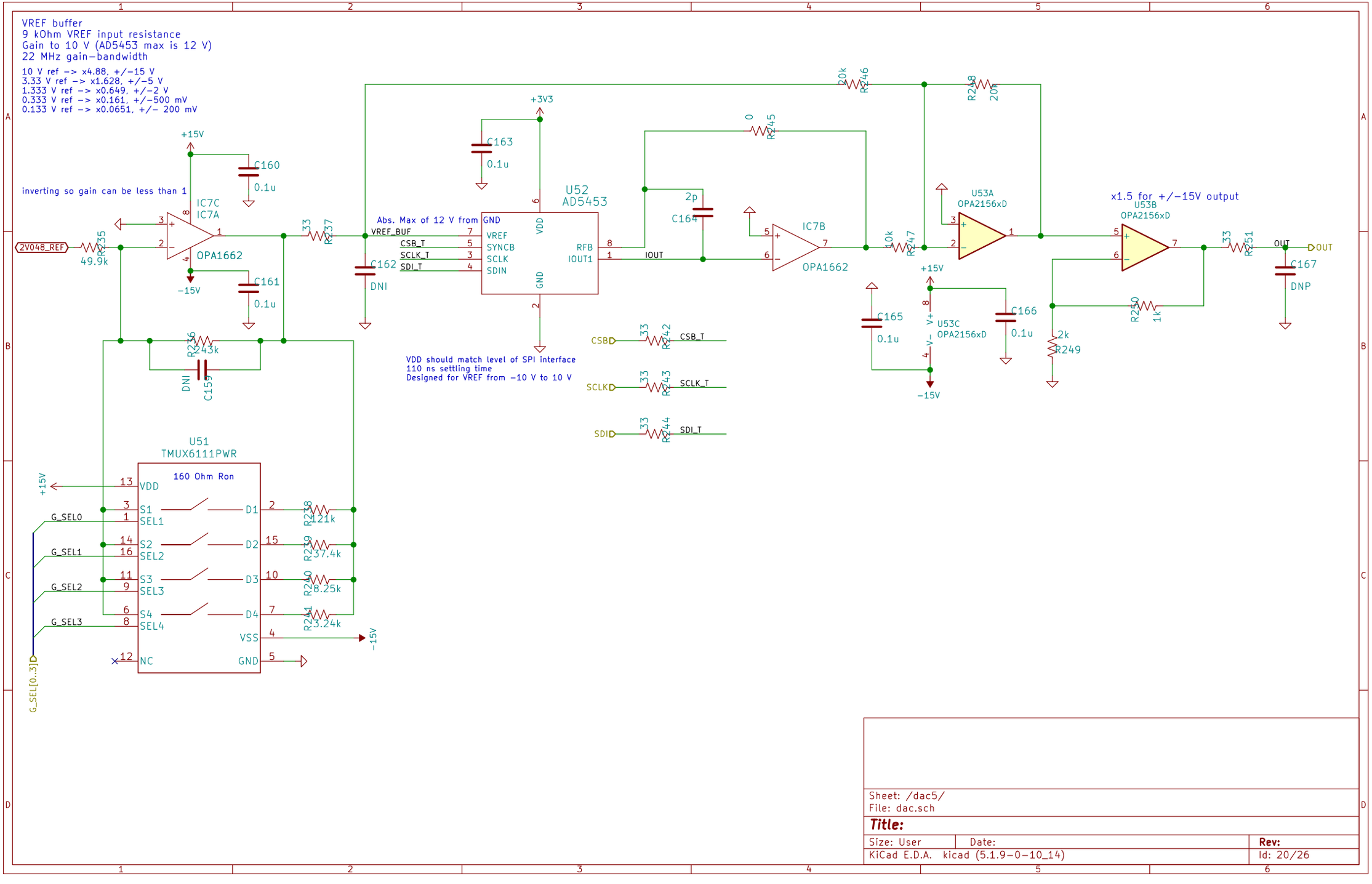
Size: User	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 19/26


VREF buffer
9 kOhm VREF input resistance
Gain to 10 V (AD5453 max is 12 V)
22 MHz gain-bandwidth
10 V ref -> x4.88, +/-15 V
3.33 V ref -> x1.628, +/-5 V
1.333 V ref -> x0.649, +/-2 V
0.333 V ref -> x0.161, +/-500 mV
0.133 V ref -> x0.0651, +/- 200 mV
inverting so gain can be less than 1
IC7C
IC7A
OPA1662
+15V
-15V
2V048_REF
R235
49.9k
C160
0.1u
C161
0.1u
R236
243k
DNI
C159
33
R237
C162
DNI
+3V3
C163
0.1u
U52
AD5453
Abs. Max of 12 V from GND
VREF_BUF
CSB_T
SCLK_T
SDI_T
VREF
SYNCB
SCLK
SDIN
VDD
GND
RFB
IOUT1
IOUT
2p
C164
VDD should match level of SPI interface
110 ns settling time
Designed for VREF from -10 V to 10 V
0
R245
20k
R246
20k
R248
IC7B
OPA1662
10k
R247
U53A
OPA2156xD
U53B
OPA2156xD
U53C
OPA2156xD
x1.5 for +/-15V output
C165
0.1u
C166
0.1u
2k
R249
1k
R250
33
R251
OUT
C167
DNP
CSB
SCLK
SDI
33
R242
R243
R244
U51
TMUX6111PWR
160 Ohm Ron
VDD
VSS
GND
NC
S1
S2
S3
S4
D1
D2
D3
D4
SEL1
SEL2
SEL3
SEL4
G_SEL0
G_SEL1
G_SEL2
G_SEL3
G_SEL[0..3]
R238
121k
R239
37.4k
R240
8.25k
R241
3.24k
Sheet: /dac5/
File: dac.sch
Title:
Size: User
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KiCad E.D.A. kicad (5.1.9-0-10_14)
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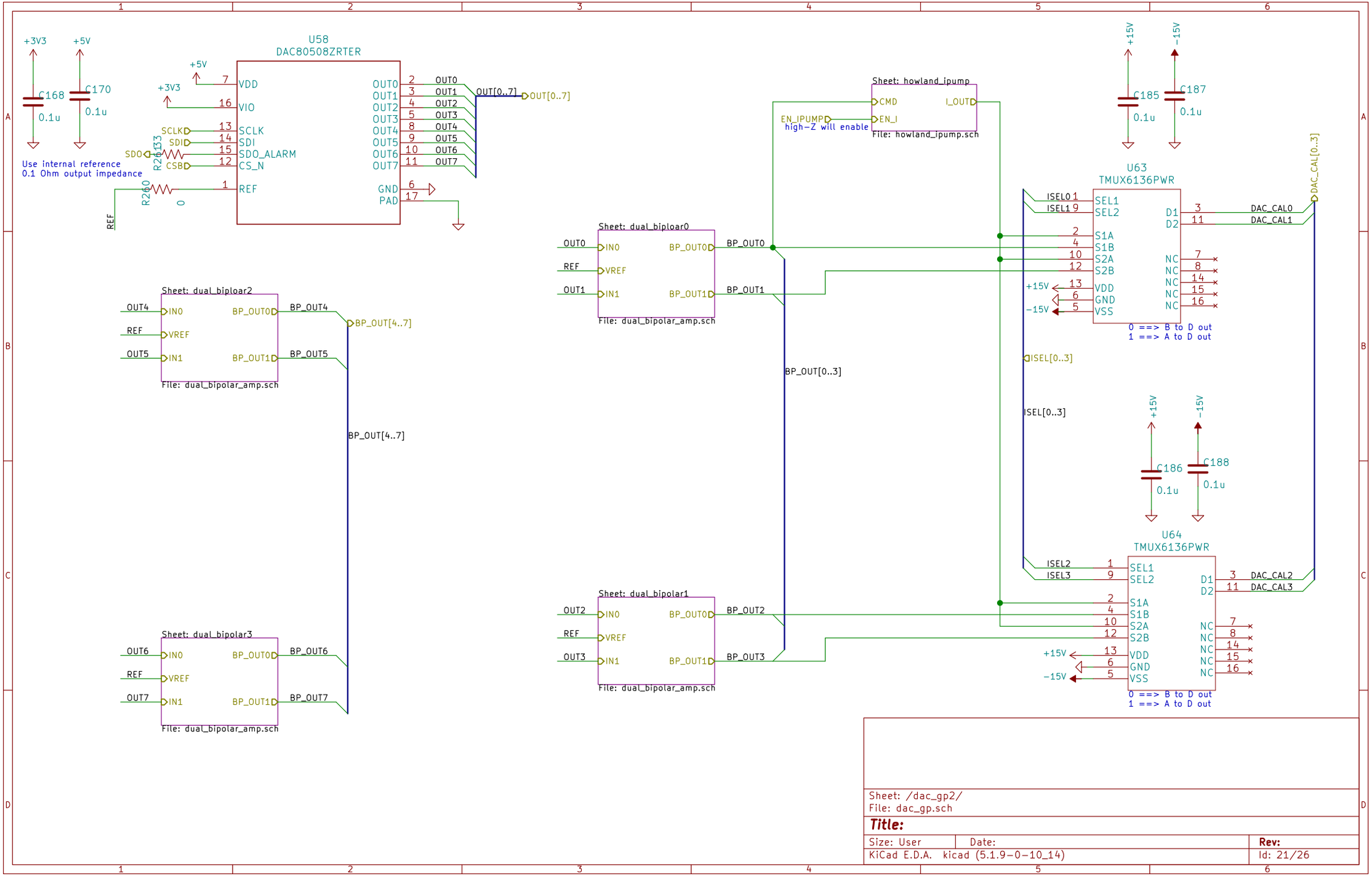
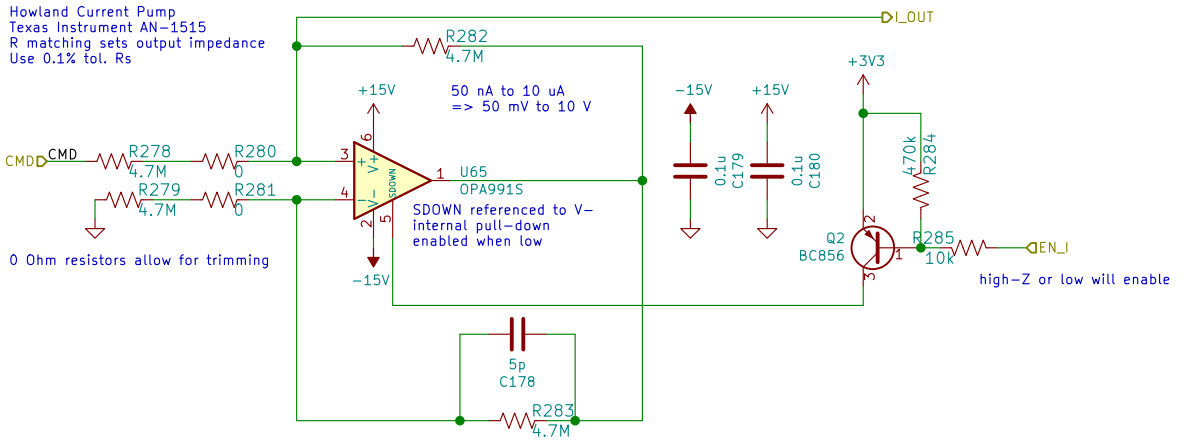

U58
DAC80508ZRTER
+3V3
+5V
C168
0.1u
C170
0.1u
Use internal reference
0.1 Ohm output impedance
R263
R260
0
REF
VDD
VIO
SCLK
SDI
SDO_ALARM
CS_N
REF
GND
PAD
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT[0..7]
Sheet: howland_ipump
CMD
I_OUT
EN_I
EN_IPUMP
high-Z will enable
File: howland_ipump.sch
+15V
-15V
C185
0.1u
C187
0.1u
U63
TMUX6136PWR
ISEL0
ISEL1
SEL1
SEL2
S1A
S1B
S2A
S2B
VDD
GND
VSS
D1
D2
NC
DAC_CAL0
DAC_CAL1
DAC_CAL[0..3]
0 ==> B to D out
1 ==> A to D out
ISEL[0..3]
Sheet: dual_biploar0
IN0
VREF
IN1
BP_OUT0
BP_OUT1
File: dual_bipolar_amp.sch
BP_OUT0
BP_OUT1
BP_OUT[0..3]
Sheet: dual_biploar2
BP_OUT4
BP_OUT5
BP_OUT[4..7]
Sheet: dual_bipolar1
BP_OUT2
BP_OUT3
Sheet: dual_bipolar3
BP_OUT6
BP_OUT7
C186
0.1u
C188
0.1u
U64
TMUX6136PWR
ISEL2
ISEL3
DAC_CAL2
DAC_CAL3
Sheet: /dac_gp2/
File: dac_gp.sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 21/26



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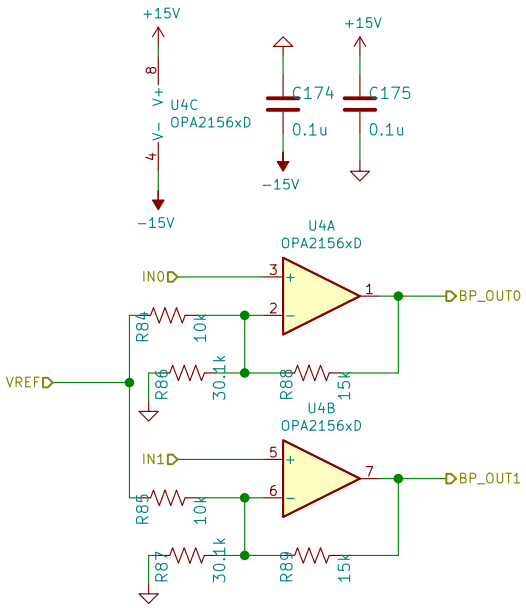
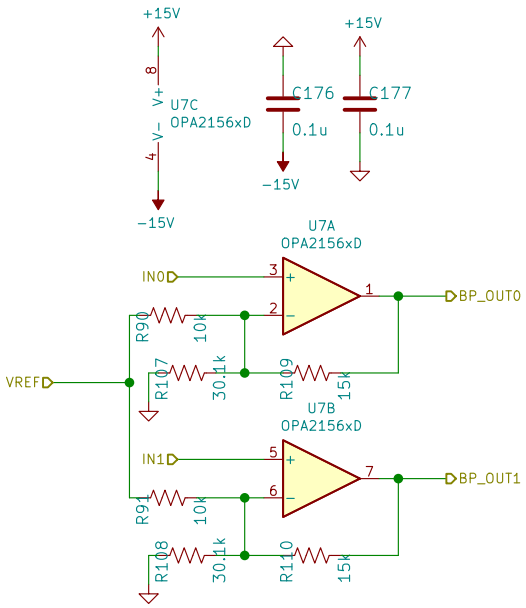
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 22/26



Sheet: /dac_gp2/dual_biploar0/		
File: dual_bipolar_amp.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 23/26



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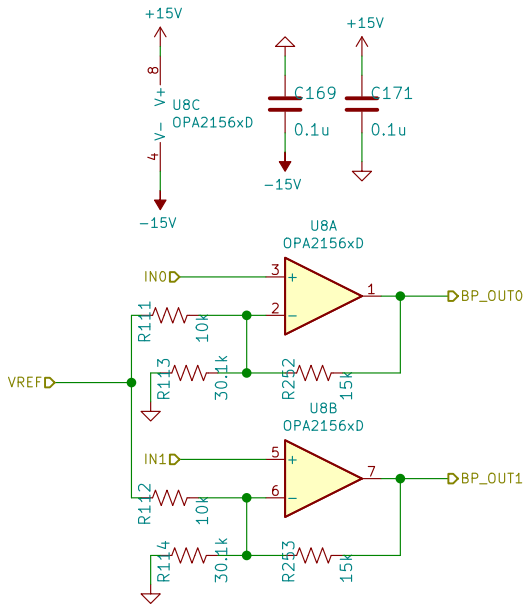
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 24/26



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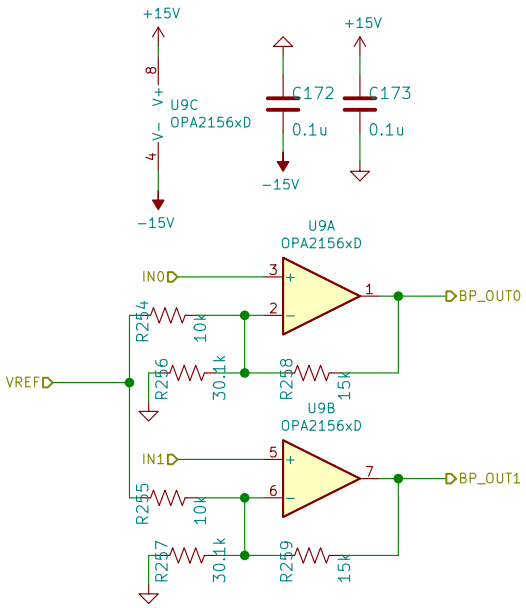
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 25/26



Sheet: /dac_gp2/dual_bipolar3/		
File: dual_bipolar_amp.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.9-0-10_14)		Id: 26/26