
STM32
CubeMX

# 1. Description

## 1.1. Project

| | |
|---|---|
| Project Name | Prototype V2 |
| Board Name | STM32U5G9J-DK2 |
| Generated with: | STM32CubeMX 6.12.1 |
| Date | 10/31/2024 |

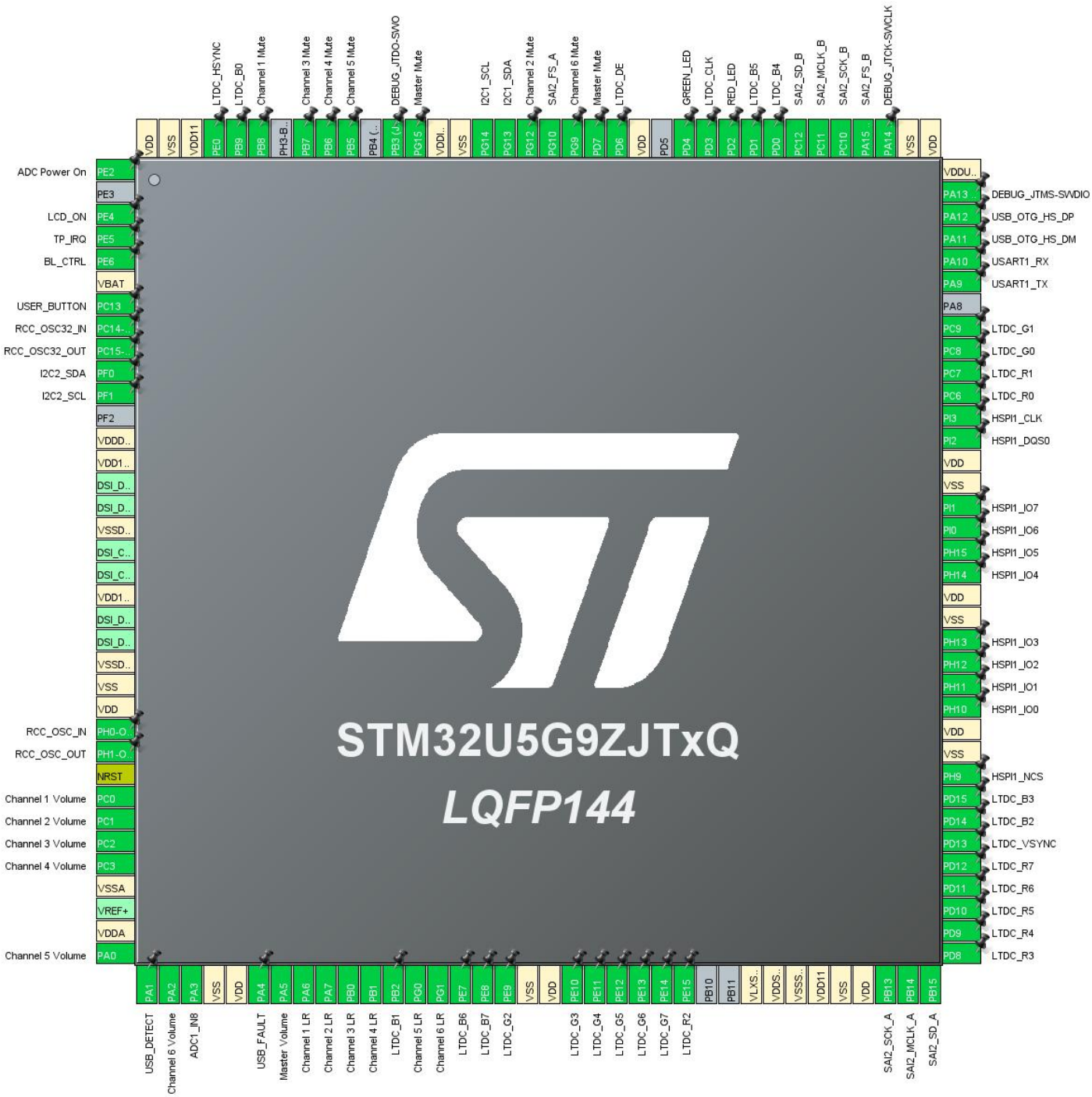
## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32U5 |
| MCU Line | STM32U5F9/5G9 |
| MCU name | STM32U5G9ZJTxQ |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

## 1.3. Core(s) information

| | |
|---|---|
| Core(s) | ARM Cortex-M33 |

## 2. Pinout Configuration



# 3. Pins Configuration

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | PE2 * | I/O | GPIO_Output | ADC Power On |
| 3 | PE4 * | I/O | GPIO_Output | LCD_ON |
| 4 | PE5 | I/O | GPIO_EXTI5 | TP_IRQ |
| 5 | PE6 | I/O | TIM3_CH4 | BL_CTRL |
| 6 | VBAT | Power | | |
| 7 | PC13 | I/O | PWR_WKUP2 | USER_BUTTON |
| 8 | PC14-OSC32_IN (PC14) | I/O | RCC_OSC32_IN | |
| 9 | PC15-OSC32_OUT (PC15) | I/O | RCC_OSC32_OUT | |
| 10 | PF0 | I/O | I2C2_SDA | |
| 11 | PF1 | I/O | I2C2_SCL | |
| 13 | VDDDSI | Power | | |
| 14 | VDD11DSI | Power | | |
| 17 | VSSDSI | Power | | |
| 20 | VDD11DSI | Power | | |
| 23 | VSSDSI | Power | | |
| 24 | VSS | Power | | |
| 25 | VDD | Power | | |
| 26 | PH0-OSC_IN (PH0) | I/O | RCC_OSC_IN | |
| 27 | PH1-OSC_OUT (PH1) | I/O | RCC_OSC_OUT | |
| 28 | NRST | Reset | | |
| 29 | PC0 | I/O | ADC1_IN1 | Channel 1 Volume |
| 30 | PC1 | I/O | ADC1_IN2 | Channel 2 Volume |
| 31 | PC2 | I/O | ADC1_IN3 | Channel 3 Volume |
| 32 | PC3 | I/O | ADC1_IN4 | Channel 4 Volume |
| 33 | VSSA | Power | | |
| 35 | VDDA | Power | | |
| 36 | PA0 | I/O | ADC1_IN5 | Channel 5 Volume |
| 37 | PA1 | I/O | GPIO_EXTI1 | USB_DETECT |
| 38 | PA2 | I/O | ADC1_IN7 | Channel 6 Volume |
| 39 | PA3 | I/O | ADC1_IN8 | |
| 40 | VSS | Power | | |
| 41 | VDD | Power | | |
| 42 | PA4 | I/O | GPIO_EXTI4 | USB_FAULT |
| 43 | PA5 | I/O | ADC1_IN10 | Master Volume |
| 44 | PA6 | I/O | ADC1_IN11 | Channel 1 LR |
| 45 | PA7 | I/O | ADC1_IN12 | Channel 2 LR |

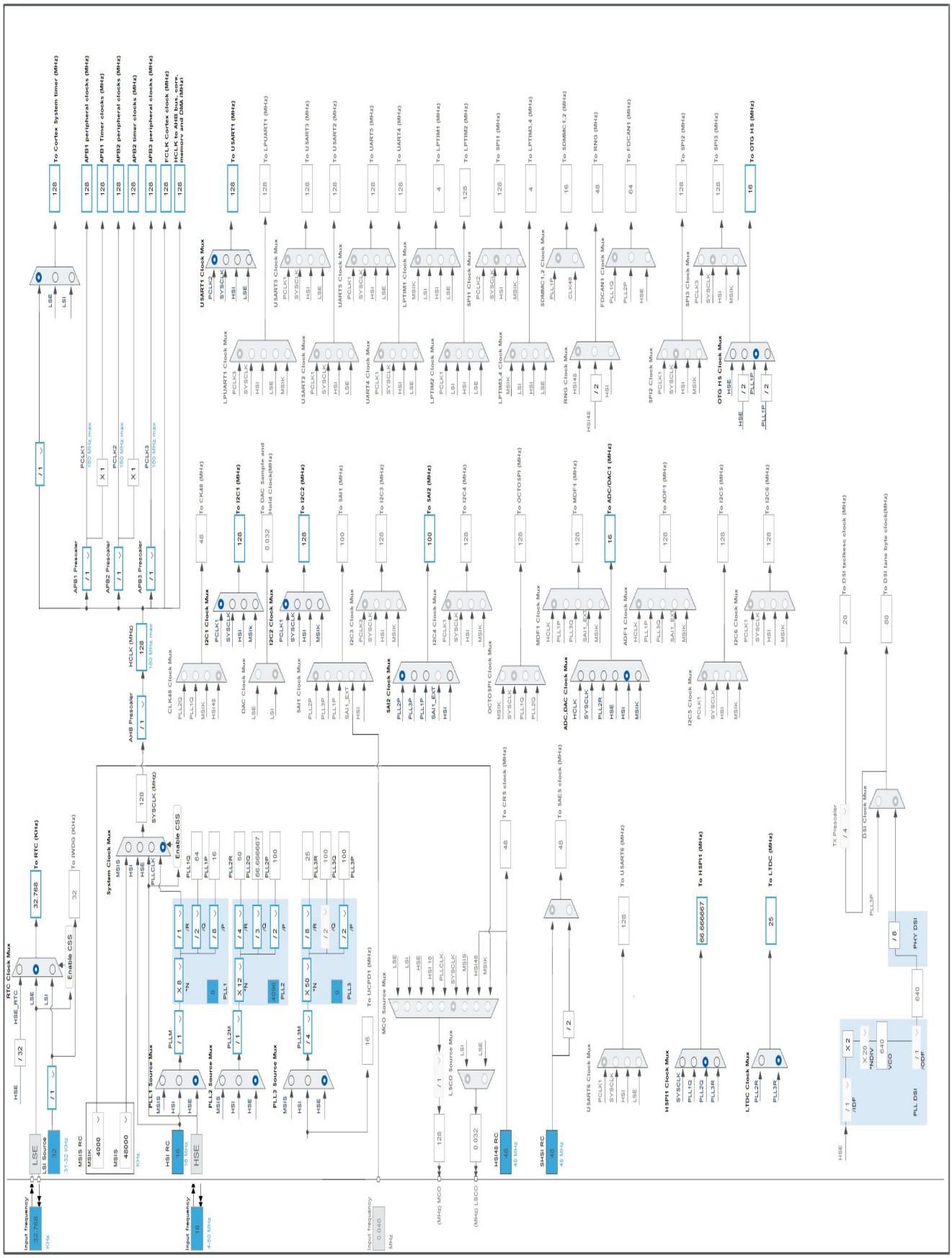
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 46 | PB0 | I/O | ADC1_IN15 | Channel 3 LR |
| 47 | PB1 | I/O | ADC1_IN16 | Channel 4 LR |
| 48 | PB2 | I/O | LTDC_B1 | |
| 49 | PG0 | I/O | ADC4_IN7 | Channel 5 LR |
| 50 | PG1 | I/O | ADC4_IN8 | Channel 6 LR |
| 51 | PE7 | I/O | LTDC_B6 | |
| 52 | PE8 | I/O | LTDC_B7 | |
| 53 | PE9 | I/O | LTDC_G2 | |
| 54 | VSS | Power | | |
| 55 | VDD | Power | | |
| 56 | PE10 | I/O | LTDC_G3 | |
| 57 | PE11 | I/O | LTDC_G4 | |
| 58 | PE12 | I/O | LTDC_G5 | |
| 59 | PE13 | I/O | LTDC_G6 | |
| 60 | PE14 | I/O | LTDC_G7 | |
| 61 | PE15 | I/O | LTDC_R2 | |
| 64 | VLXSMPS | Power | | |
| 65 | VDDSMPS | Power | | |
| 66 | VSSSMPS | Power | | |
| 67 | VDD11 | Power | | |
| 68 | VSS | Power | | |
| 69 | VDD | Power | | |
| 70 | PB13 | I/O | SAI2_SCK_A | |
| 71 | PB14 | I/O | SAI2_MCLK_A | |
| 72 | PB15 | I/O | SAI2_SD_A | |
| 73 | PD8 | I/O | LTDC_R3 | |
| 74 | PD9 | I/O | LTDC_R4 | |
| 75 | PD10 | I/O | LTDC_R5 | |
| 76 | PD11 | I/O | LTDC_R6 | |
| 77 | PD12 | I/O | LTDC_R7 | |
| 78 | PD13 | I/O | LTDC_VSYNC | |
| 79 | PD14 | I/O | LTDC_B2 | |
| 80 | PD15 | I/O | LTDC_B3 | |
| 81 | PH9 | I/O | HSPI1_NCS | |
| 82 | VSS | Power | | |
| 83 | VDD | Power | | |
| 84 | PH10 | I/O | HSPI1_IO0 | |
| 85 | PH11 | I/O | HSPI1_IO1 | |
| 86 | PH12 | I/O | HSPI1_IO2 | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 87 | PH13 | I/O | HSPI1_IO3 | |
| 88 | VSS | Power | | |
| 89 | VDD | Power | | |
| 90 | PH14 | I/O | HSPI1_IO4 | |
| 91 | PH15 | I/O | HSPI1_IO5 | |
| 92 | PI0 | I/O | HSPI1_IO6 | |
| 93 | PI1 | I/O | HSPI1_IO7 | |
| 94 | VSS | Power | | |
| 95 | VDD | Power | | |
| 96 | PI2 | I/O | HSPI1_DQS0 | |
| 97 | PI3 | I/O | HSPI1_CLK | |
| 98 | PC6 | I/O | LTDC_R0 | |
| 99 | PC7 | I/O | LTDC_R1 | |
| 100 | PC8 | I/O | LTDC_G0 | |
| 101 | PC9 | I/O | LTDC_G1 | |
| 103 | PA9 | I/O | USART1_TX | |
| 104 | PA10 | I/O | USART1_RX | |
| 105 | PA11 | I/O | USB_OTG_HS_DM | |
| 106 | PA12 | I/O | USB_OTG_HS_DP | |
| 107 | PA13 (JTMS/SWDIO) | I/O | DEBUG_JTMS-SWDIO | |
| 108 | VDDUSB | Power | | |
| 109 | VDD | Power | | |
| 110 | VSS | Power | | |
| 111 | PA14 (JTCK/SWCLK) | I/O | DEBUG_JTCK-SWCLK | |
| 112 | PA15 (JTDI) | I/O | SAI2_FS_B | |
| 113 | PC10 | I/O | SAI2_SCK_B | |
| 114 | PC11 | I/O | SAI2_MCLK_B | |
| 115 | PC12 | I/O | SAI2_SD_B | |
| 116 | PD0 | I/O | LTDC_B4 | |
| 117 | PD1 | I/O | LTDC_B5 | |
| 118 | PD2 * | I/O | GPIO_Output | RED_LED |
| 119 | PD3 | I/O | LTDC_CLK | |
| 120 | PD4 * | I/O | GPIO_Output | GREEN_LED |
| 122 | VDD | Power | | |
| 123 | PD6 | I/O | LTDC_DE | |
| 124 | PD7 * | I/O | GPIO_Input | Master Mute |
| 125 | PG9 * | I/O | GPIO_Input | Channel 6 Mute |
| 126 | PG10 | I/O | SAI2_FS_A | |
| 127 | PG12 * | I/O | GPIO_Input | Channel 2 Mute |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 128 | PG13 | I/O | I2C1_SDA | |
| 129 | PG14 | I/O | I2C1_SCL | |
| 130 | VSS | Power | | |
| 131 | VDDIO2 | Power | | |
| 132 | PG15 * | I/O | GPIO_Input | Master Mute |
| 133 | PB3 (JTDO/TRACESWO) | I/O | DEBUG_JTDO-SWO | |
| 135 | PB5 * | I/O | GPIO_Input | Channel 5 Mute |
| 136 | PB6 * | I/O | GPIO_Input | Channel 4 Mute |
| 137 | PB7 * | I/O | GPIO_Input | Channel 3 Mute |
| 139 | PB8 * | I/O | GPIO_Input | Channel 1 Mute |
| 140 | PB9 | I/O | LTDC_B0 | |
| 141 | PE0 | I/O | LTDC_HSYNC | |
| 142 | VDD11 | Power | | |
| 143 | VSS | Power | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 1. Power Consumption Calculator report

## 1.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32U5 |
| Line | STM32U5F9/5G9 |
| MCU | STM32U5G9ZJTxQ |
| Datasheet | not yet available |

## 1.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.0 |

## 1.3. Battery Selection

| | |
|---|---|
| Battery | Li-SOCL2(A3400) |
| Capacity | 3400.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 100.0 mA |
| Max Pulse Current | 200.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

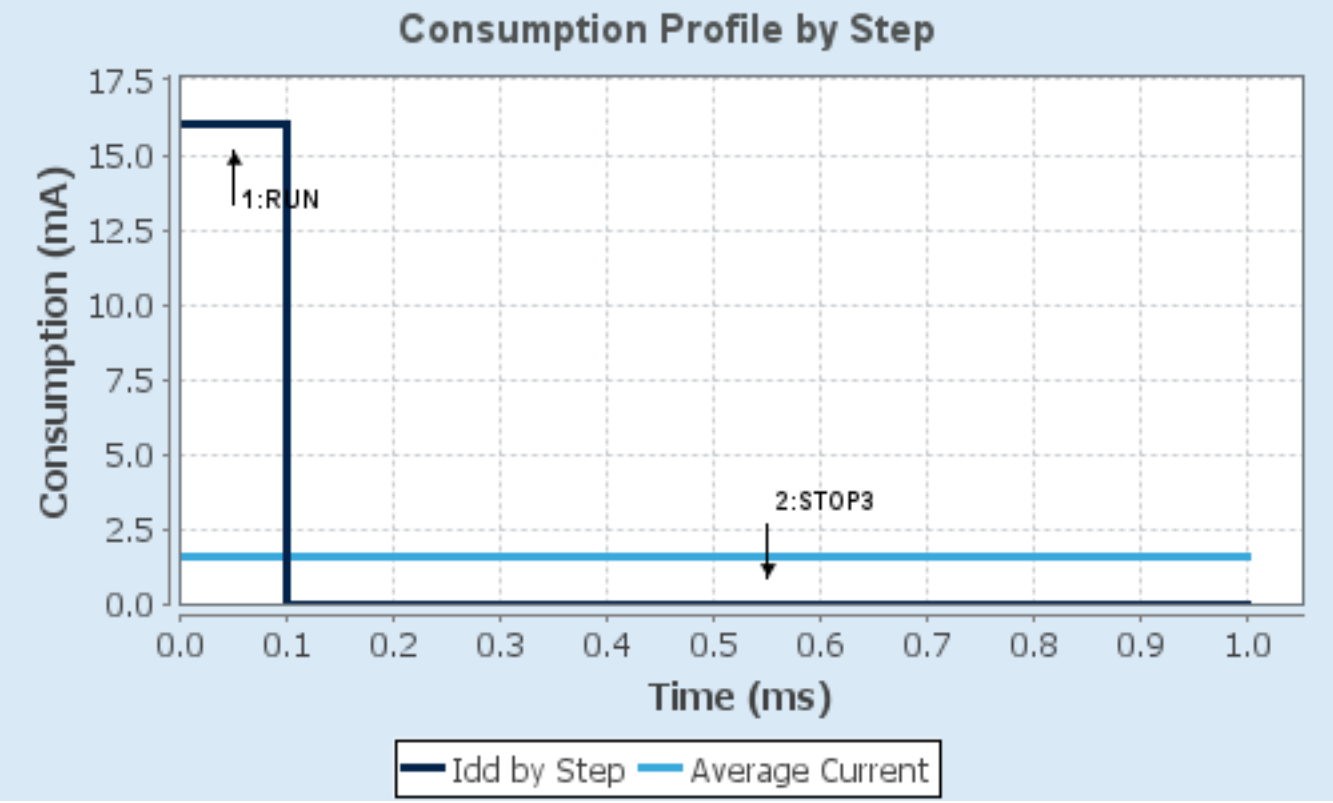
## 1.4. Sequence

| ***Step*** | Step1 | Step2 |
|---|---|---|
| ***Mode*** | RUN | STOP3 |
| ***Vdd*** | 3.0 | 3.0 |
| ***Voltage Source*** | Battery | Battery |
| ***Range*** | Range1-Medium | NoScale/SMPS |
| ***Fetch Type*** | FLASH_PwrDwnBank2/ART/Cache2Ways/ALL_RAM_RETENTION | FLASH |
| ***CPU Frequency*** | 160 MHz | 0 Hz |
| ***Clock Configuration*** | HSE BYP PLL | ALL_CLOCKS_OFF |
| ***Clock Source Frequency*** | 16 MHz | 0 Hz |
| ***Peripherals*** | | |
| ***Additional Cons.*** | 0 mA | 0 mA |
| ***Average Current*** | 16 mA | 1.9 µA |
| ***Duration*** | 0.1 ms | 0.9 ms |
| ***DMIPS*** | 240.0 | 0.0 |
| ***Ta Max*** | 138.42 | 140 |
| ***Category*** | In DS Table | In DS Table |

## 1.5. Results

| Sequence Time | 1 ms | Average Current | 1.6 mA |
|---|---|---|---|
| Battery Life | 2 months, 27 days, 9 hours | Average DMIPS | 24.0 DMIPS |

## 1.6. Chart


Consumption Profile by Step
Consumption (mA)
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP3
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

# 2. Software Project

## 2.1. Project Settings

| Name | Value |
|---|---|
| Project Name | Prototype V2 |
| Project Folder | C:\Users\C0484110\Documents\GitHub\Capstone-RLC\PrototypeV2 |
| Toolchain / IDE | STM32CubeIDE |
| Firmware Package Name and Version | STM32Cube FW_U5 V1.6.0 |
| Application Structure | Advanced |
| Generate Under Root | Yes |
| Do not generate the main() | No |
| Minimum Heap Size | 0x400 |
| Minimum Stack Size | 0x800 |

## 2.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Keep User Code when re-generating | Yes |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |
| Enable Full Assert | No |

## 2.3. Advanced Settings - Generated Function Calls

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 1 | SystemClock_Config | RCC |
| 2 | MX_GPIO_Init | GPIO |
| 3 | MX_GPDMA1_Init | GPDMA1 |
| 4 | MX_DMA2D_Init | DMA2D |
| 5 | MX_HSPI1_Init | HSPI1 |
| 6 | MX_I2C2_Init | I2C2 |
| 7 | MX_ICACHE_Init | ICACHE |
| 8 | MX_LTDC_Init | LTDC |
| 9 | MX_RTC_Init | RTC |
| 10 | MX_TIM3_Init | TIM3 |
| 11 | MX_ADC1_Init | ADC1 |

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 12 | MX_USART1_UART_Init | USART1 |
| 13 | MX_SAI2_Init | SAI2 |
| 14 | MX_ADC4_Init | ADC4 |
| 15 | MX_I2C1_Init | I2C1 |
| 16 | MX_USB_OTG_HS_PCD_Init | USB_OTG_HS |

# 3. Peripherals and Middlewares Configuration

## 3.1. ADC1

**IN1: IN1 Single-ended**
**IN2: IN2 Single-ended**
**IN3: IN3 Single-ended**
**IN4: IN4 Single-ended**
**IN5: IN5 Single-ended**
**IN7: IN7 Single-ended**
**IN8: IN8 Single-ended**
**IN10: IN10 Single-ended**
**IN11: IN11 Single-ended**
**mode: IN12**
**IN15: IN15 Single-ended**
**IN16: IN16 Single-ended**
**mode: Temperature Sensor Channel**

### 3.1.1. Parameter Settings:

| | |
|---|---|
| **ADCs_Common_Settings:** | |
| Mode | Independent mode |
| **ADC_Settings:** | |
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | ADC 14-bit resolution |
| Data Alignment | Right alignment |
| Gain Compensation | 0 |
| Scan Conversion Mode | Enabled |
| End Of Conversion Selection | End of single conversion |
| Low Power Auto Wait | **Enabled *** |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| Overrun behaviour | Overrun data preserved |
| Trigger Frequency | High frequency |
| Conversion Data Management Mode | **DMA Circular Mode *** |
| **ADC_Regular_ConversionMode:** | |
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Disable |
| Oversampling Ratio | 1 |
| Number Of Conversion | |

| | |
|---|---|
| | **13 *** |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Left Bit Shift | No bit shift |
| Rank | 1 |
| Channel | Channel 1 |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **2 *** |
| Channel | **Channel 2 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **3 *** |
| Channel | **Channel 3 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **4 *** |
| Channel | **Channel 4 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **5 *** |
| Channel | **Channel 5 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **6 *** |
| Channel | **Channel 7 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **7 *** |
| Channel | **Channel 8 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **8 *** |

| | |
|---|---|
| Channel | **Channel 10 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **9 *** |
| Channel | **Channel 11 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **10 *** |
| Channel | **Channel 12 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **11 *** |
| Channel | **Channel 15 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **12 *** |
| Channel | **Channel 16 *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |
| Rank | **13 *** |
| Channel | **Channel Temperature Sensor *** |
| Sampling Time | 5 Cycles |
| Offset Number | No offset |
| Monitored by | None |

### ADC_Injected_ConversionMode:

| | |
|---|---|
| Enable Injected Conversions | Disable |

### Analog Watchdog 1:

| | |
|---|---|
| Enable Analog WatchDog1 Mode | false |

### Analog Watchdog 2:

| | |
|---|---|
| Enable Analog WatchDog2 Mode | false |

### Analog Watchdog 3:

| | |
|---|---|
| Enable Analog WatchDog3 Mode | false |

## 3.2. ADC4
## mode: IN7
## mode: IN8

### 3.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Sequencer | Sequencer set to fully configurable |
| Scan Conversion Mode | Enabled |
| Continuous Conversion Mode | **Enabled *** |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | End of single conversion |
| Overrun behaviour | Overrun data preserved |
| Low Power Auto Wait | Disabled |
| Low Power Auto Off | Low power disabled and auto off disabled |
| SamplingTime Common 1 | 1.5 Cycles |
| SamplingTime Common 2 | 1.5 Cycles |
| Trigger Frequency | Low frequency |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Oversampling Mode | Disabled |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Enable Regular Conversions | Enable |
| Number Of Conversion | **2 *** |
| Rank | 1 |
| Channel | Channel 7 |
| Sampling Time | Sampling time common 1 |
| Offset Number | No offset |
| Rank | **2 *** |
| Channel | **Channel 8 *** |
| Sampling Time | Sampling time common 1 |
| Offset Number | No offset |

**Analog Watchdog 1:**

| | |
|---|---|
| Enable Analog WatchDog1 Mode | false |

**Analog Watchdog 2:**

| | |
|---|---|
| Enable Analog WatchDog2 Mode | false |

**Analog Watchdog 3:**

| | |
|---|---|
| Enable Analog WatchDog3 Mode | false |

## 3.3. DEBUG

## Debug: Trace Asynchronous Sw

## 3.4. DMA2D

## mode: Activated

### 3.4.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Transfer Mode | Memory to Memory |
| Color Mode | **RGB888 *** |
| Output Offset | 0 |
| DMA2D Bytes Swap | Bytes in regular order in output FIFO |
| DMA2D Line Offset Mode | Line offsets expressed in pixels |

**Foreground layer Configuration:**

| | |
|---|---|
| DMA2D Input Color Mode | RGB888 |
| DMA2D ALPHA MODE | No modification of the alpha channel value |
| Input Alpha | 0 |
| Input Offset | 0 |
| DMA2D ALPHA Inversion | Regular Alpha |
| DMA2D Red and Blue swap | Regular mode (RGB or ARGB) |

## 3.5. HSPI1

## Mode: Octo SPI

### 3.5.1. Parameter Settings:

**Generic:**

| | |
|---|---|
| Fifo Threshold | **4 *** |
| Memory Mode | Single |
| Memory Type | **Macronix *** |
| Memory Size | **1 GBits *** |
| Device Type | Not defined |
| Chip Select High Time Cycle | **2 *** |

| | |
|---|---|
| Free Running Clock | Disable |
| Clock Mode | Low |
| Wrap Size | Not Supported |
| Clock Prescaler | 0 |
| Sample Shifting | None |
| Delay Hold Quarter Cycle | Disable |
| Chip Select Boundary | Disable |
| Maximum Transfer | 0 |
| Refresh Rate | 0 |

## 3.6. I2C1

## I2C: I2C

### 3.6.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20A0C4DF *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

**Autonomous Mode:**

| | |
|---|---|
| Autonomous Mode | Disable |

## 3.7. I2C2

## I2C: I2C

### 3.7.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Speed Frequency (KHz) | 100 |

| | |
|---|---|
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x20A0C4DF *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

**Autonomous Mode:**

| | |
|---|---|
| Autonomous Mode | Disable |

## 3.8. ICACHE

**Mode: 1-way (direct mapped cache)**

## 3.9. LPBAM

**mode: LPBAM Scenario uses resources from Smart Run Domain only**

**mode: LPBAM Scenario is hosted by LPDMA1**

## 3.10. LPBAMQUEUE

**mode: QUEUE MODE**

### 3.10.1. Parameter Settings:

**DMA Channel Configuration:**

| | |
|---|---|
| Priority | Low |

**DMA Channel Interrupt Configuration:**

| | |
|---|---|
| Data Transfer Error Interrupt | Disable |
| Update Link Error Interrupt | Disable |
| User Setting Error Interrupt | Disable |
| Transfer Complete Interrupt | Disable |
| Trigger Overrun Interrupt | Disable |

## 3.11. LTDC

## Display Type: RGB888 (24 bits)

### 3.11.1. Parameter Settings:

**Synchronization for Width:**

| | |
|---|---|
| Horizontal Synchronization Width | **4 *** |
| Horizontal Back Porch | **8 *** |
| Active Width | **800 *** |
| Horizontal Front Porch | **8 *** |
| HSync Width | 3 |
| Accumulated Horizontal Back Porch Width | 11 |
| Accumulated Active Width | 811 |
| Total Width | 819 |

**Synchronization for Height:**

| | |
|---|---|
| Vertical Synchronization Height | 4 |
| Vertical Back Porch | **8 *** |
| Active Height | 480 |
| Vertical Front Porch | **8 *** |
| VSync Height | 3 |
| Accumulated Vertical Back Porch Height | 11 |
| Accumulated Active Height | 491 |
| Total Height | 499 |

**Signal Polarity:**

| | |
|---|---|
| Horizontal Synchronization Polarity | Active Low |
| Vertical Synchronization Polarity | Active Low |
| Data Enable Polarity | Active Low |
| Pixel Clock Polarity | Normal Input |

**Layer Default Color:**

| | |
|---|---|
| Red | 0 |
| Green | 0 |
| Blue | 0 |

### 3.11.2. Layer Settings:

**Layer Default Color:**

| | |
|---|---|
| Layer 0 - Alpha | 0 |
| Layer 0 - Blue | 0 |
| Layer 0 - Green | 0 |
| Layer 0 - Red | 0 |

**Number of Layers:**

| | |
|---|---|
| Number of Layers | **1 layer *** |
| **Windows Position:** | |
| Layer 0 - Window Horizontal Start | 0 |
| Layer 0 - Window Horizontal Stop | **800 *** |
| Layer 0 - Window Vertical Start | 0 |
| Layer 0 - Window Vertical Stop | **480 *** |
| **Pixel Parameters:** | |
| Layer 0 - Pixel Format | **RGB888 *** |
| **Blending:** | |
| Layer 0 - Alpha constant for blending | **255 *** |
| Layer 0 - Blending Factor1 | **Alpha constant x Pixel Alpha *** |
| Layer 0 - Blending Factor2 | **Alpha constant x Pixel Alpha *** |
| **Frame Buffer:** | |
| Layer 0 - Color Frame Buffer Start Adress | 0 |
| Layer 0 - Color Frame Buffer Line Length (Image Width) | 0 |
| Layer 0 - Color Frame Buffer Number of Lines (Image Height) | 0 |

## 3.12. MEMORYMAP
## mode: Activated

## 3.13. PWR
## mode: Wake-Up 2
## mode: Power saving mode
## mode: Privilege attributes
## mode: Control Vdda isolation

### 3.13.1. Power Saving:

| | |
|---|---|
| **System power supply:** | |
| Power Regulator | **SMPS *** |
| **SRAM power down in Run mode:** | |
| SRAM1 power down in Run mode | Disable |
| SRAM2 power down in Run mode | Disable |
| SRAM3 power down in Run mode | Disable |
| SRAM4 power down in Run mode | Disable |
| SRAM5 power down in Run mode | Disable |

| | |
|---|---|
| SRAM6 power down in Run mode | Disable |

### SRAM power down in Stop mode:

| | |
|---|---|
| SRAM1 Page1 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page2 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page3 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page4 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page5 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page6 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page7 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page8 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page9 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page10 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page11 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM1 Page12 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM2 Page1 power down in Stop (0, 1, 2) mode | Disable |
| SRAM2 Page2 power down in Stop (0, 1, 2) mode | Disable |
| SRAM3 Page1 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page2 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page3 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page4 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page5 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page6 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page7 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page8 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page9 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page10 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page11 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page12 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM3 Page13 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM4 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page1 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page2 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page3 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page4 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page5 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page6 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page7 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page8 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page9 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page10 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page11 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page12 power down in Stop (0, 1, 2, 3) mode | Disable |
| SRAM5 Page13 power down in Stop (0, 1, 2, 3) mode | Disable |

| | |
|---|---|
| ICACHE power down in Stop (0, 1, 2, 3) mode | Disable |
| DCACHE1 power down in Stop (0, 1, 2, 3) mode | Disable |
| DCACHE2 power down in Stop (0, 1, 2, 3) mode | Disable |
| DMA2D RAM power down in Stop (0, 1, 2, 3) mode | Disable |
| PKA32 RAM power down in Stop (0, 1, 2, 3) mode | Disable |
| PERIPH RAM power down in Stop (0, 1, 2, 3) mode | Disable |
| GRAPHIC PRAM power down in Stop (0, 1, 2, 3) mode | Disable |
| DSI RAM power down in Stop (0, 1, 2, 3) mode | Disable |

**SRAM fast wakeup:**

| | |
|---|---|
| SRAM4 fast wakeup from Stop (0, 1, 2, 3) modes | Disable |

### 3.13.2. PWR Privilege :

**Privilege PWR:**

| | |
|---|---|
| Privilege of PWR Secure Items | Disable |
| Privilege of PWR Non-Secure Items | Disable |
| PWR Privilege | Disable |

### 3.13.3. PWR Security:

**Secure PWR:**

| | |
|---|---|
| Wake-Up 1 secure protection | Disable |
| Wake-Up 2 secure protection | Disable |
| Wake-Up 3 secure protection | Disable |
| Wake-Up 4 secure protection | Disable |
| Wake-Up 5 secure protection | Disable |
| Wake-Up 6 secure protection | Disable |
| Wake-Up 7 secure protection | Disable |
| Wake-Up 8 secure protection | Disable |
| Voltage detection and monitoring secure protection | Disable |
| Pull-up/pull-down secure protection | Disable |
| Low power modes secure protection | Disable |
| Backup domain secure protection | Disable |

## 3.14. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

### 3.14.1. RCC Privilege :

**Privilege RCC:**

| | |
|---|---|
| Privilege of RCC Non-Secure Items | Disable |

### 3.14.2. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Flash Latency(WS) | 3 WS (4 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| MSI Calibration Value | 16 |
| MSIS/MSIK Auto Calibration | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |
| LSE Drive Capability | LSE oscillator low drive capability |

**Power Parameters:**

| | |
|---|---|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |

**PLL1/2/3 Parameters:**

| | |
|---|---|
| PLL1M BOOST EPOD Clock Divider | 1 |
| PLL1 input frequency range | Between 8 and 16 MHz |
| PLL2 input frequency range | Between 8 and 16 MHz |
| PLL3 input frequency range | Between 4 and 8 MHz |

**Low Power Parameters:**

| | |
|---|---|
| MSI in Stop mode | Disabled |
| HSI in Stop mode | Disabled |

## 3.15. RTC

**mode: Activate Clock Source**

### 3.15.1. Parameter Settings:

**General:**

| | |
|---|---|
| Hour Format | Hourformat 24 |
| Asynchronous Predivider value | 127 |
| Synchronous Predivider value | 255 |
| Bin Mode | Free running BCD calender mode |

### 3.15.2. RTC Privilege:

**Privilege RTC:**

| | |
|---|---|
| RTC full privilege | Disable |

**Backup register:**

| | |
|---|---|
| Start zone 1 | RTC_BKP_DR0 |
| Start Zone 2 | RTC_BKP_DR0 |
| start zone 3 | RTC_BKP_DR0 |

**Privilege Backup register :**

| | |
|---|---|
| Backup Register PrivZone | Non-privilege |

**Privilege RTC Feature:**

| | |
|---|---|
| RTC Initialisation | Non-Privilege |
| RTC Alarm A | Non-Privilege |
| RTC Alarm B | Non-Privilege |
| RTC Calibration | Non-Privilege |
| RTC TimeStamp | Non-Privilege |
| RTC WakeUpTimer | Non-Privilege |

## 3.16. SAI2
## Mode: Master with Master Clock Out
## mode: I2S/PCM Protocol
## Mode: Master with Master Clock Out
## mode: I2S/PCM Protocol

### 3.16.1. Parameter Settings:

**SAI A:**

| | |
|---|---|
| Synchronization Inputs | Asynchronous |
| Audio Mode | Master Transmit |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | **Tri-Sate *** |
| Protocol Parameters | |
| Protocol | **I2S Msb Justified *** |
| Data Size | **24 Bits *** |
| Number of Slots (only Even Values) | 2 |
| Clock Source | SAI PLL Clock |
| Master Clock No Divider | Enabled |

| | |
|---|---|
| Audio Frequency | **8 KHz *** |
| Real Audio Frequency | **13.02 KHz *** |
| Error between Selected | **62.75 % *** |
| Fifo Threshold | Empty |
| Output Drive | Disabled |

**SAI B:**

| | |
|---|---|
| Synchronization Inputs | Asynchronous |
| Audio Mode | **Master Receive *** |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| Protocol Parameters | |
| Protocol | I2S Standard |
| Data Size | **24 Bits *** |
| Number of Slots (only Even Values) | **8 *** |
| Clock Source | SAI PLL Clock |
| Master Clock No Divider | Enabled |
| Audio Frequency | **96 KHz *** |
| Real Audio Frequency | **97.656 KHz *** |
| Error between Selected | **1.72 % *** |
| Fifo Threshold | **Half Full *** |
| Output Drive | Disabled |

## 3.17. SYS

## Timebase Source: SysTick

## 3.18. TIM3

## Channel4: PWM Generation CH4

### 3.18.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **160 *** |
| Counter Mode | Up |
| Dithering | Disable |
| Counter Period (AutoReload Register - 32 bits value ) | **100 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | **75 *** |
| Output compare preload | **Disable *** |
| Fast Mode | Disable |
| CH Polarity | High |

## 3.19. USART1

## Mode: Asynchronous

### 3.19.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |
| ClockPrescaler | 1 |
| Fifo Mode | Disable |
| Txfifo Threshold | 1 eighth full configuration |
| Rxfifo Threshold | 1 eighth full configuration |
| Autonomous Mode | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## 3.20. USB_OTG_HS

## Internal HS Phy: Device_Only

### 3.20.1. Parameter Settings:

| | |
|---|---|
| Speed | Device High Speed 480MBit/s |
| Enable internal IP DMA | Disabled |
| Physical interface | Internal HS Phy |
| Low power | Disabled |
| Link Power Management | Disabled |
| Use dedicated end point 1 interrupt | Disabled |
| VBUS sensing | Disabled |
| Signal start of frame | Disabled |

**OTG PHY reference clock selection:**

| | |
|---|---|
| Ref Clock Selection | 16 Mhz |

*** User modified value**

# 4. System Configuration

## 4.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PC0 | ADC1_IN1 | Analog mode | No pull-up and no pull-down | n/a | Channel 1 Volume |
| | PC1 | ADC1_IN2 | Analog mode | No pull-up and no pull-down | n/a | Channel 2 Volume |
| | PC2 | ADC1_IN3 | Analog mode | No pull-up and no pull-down | n/a | Channel 3 Volume |
| | PC3 | ADC1_IN4 | Analog mode | No pull-up and no pull-down | n/a | Channel 4 Volume |
| | PA0 | ADC1_IN5 | Analog mode | No pull-up and no pull-down | n/a | Channel 5 Volume |
| | PA2 | ADC1_IN7 | Analog mode | No pull-up and no pull-down | n/a | Channel 6 Volume |
| | PA3 | ADC1_IN8 | Analog mode | No pull-up and no pull-down | n/a | |
| | PA5 | ADC1_IN10 | Analog mode | No pull-up and no pull-down | n/a | Master Volume |
| | PA6 | ADC1_IN11 | Analog mode | No pull-up and no pull-down | n/a | Channel 1 LR |
| | PA7 | ADC1_IN12 | Analog mode | No pull-up and no pull-down | n/a | Channel 2 LR |
| | PB0 | ADC1_IN15 | Analog mode | No pull-up and no pull-down | n/a | Channel 3 LR |
| | PB1 | ADC1_IN16 | Analog mode | No pull-up and no pull-down | n/a | Channel 4 LR |
| ADC4 | PG0 | ADC4_IN7 | Analog mode | No pull-up and no pull-down | n/a | Channel 5 LR |
| | PG1 | ADC4_IN8 | Analog mode | No pull-up and no pull-down | n/a | Channel 6 LR |
| DEBUG | PA13 (JTMS/SWDIO) | DEBUG_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 (JTCK/SWCLK) | DEBUG_JTCK-SWCLK | n/a | n/a | n/a | |
| | PB3 (JTDO/TRACESWO) | DEBUG_JTDO-SWO | n/a | n/a | n/a | |
| HSPI1 | PH9 | HSPI1_NCS | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PH10 | HSPI1_IO0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PH11 | HSPI1_IO1 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PH12 | HSPI1_IO2 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PH13 | HSPI1_IO3 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PH14 | HSPI1_IO4 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PH15 | HSPI1_IO5 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PI0 | HSPI1_IO6 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PI1 | HSPI1_IO7 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PI2 | HSPI1_DQS0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PI3 | HSPI1_CLK | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| I2C1 | PG13 | I2C1_SDA | Alternate Function Open Drain | No pull-up and no pull-down | Low | |
| | PG14 | I2C1_SCL | Alternate Function Open Drain | No pull-up and no pull-down | Low | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| I2C2 | PF0 | I2C2_SDA | Alternate Function Open Drain | No pull-up and no pull-down | Low | |
| | PF1 | I2C2_SCL | Alternate Function Open Drain | No pull-up and no pull-down | Low | |
| LTDC | PB2 | LTDC_B1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE7 | LTDC_B6 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE8 | LTDC_B7 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE9 | LTDC_G2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE10 | LTDC_G3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE11 | LTDC_G4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE12 | LTDC_G5 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE13 | LTDC_G6 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE14 | LTDC_G7 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE15 | LTDC_R2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD8 | LTDC_R3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD9 | LTDC_R4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD10 | LTDC_R5 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD11 | LTDC_R6 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD12 | LTDC_R7 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD13 | LTDC_VSYNC | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD14 | LTDC_B2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD15 | LTDC_B3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC6 | LTDC_R0 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC7 | LTDC_R1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC8 | LTDC_G0 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC9 | LTDC_G1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD0 | LTDC_B4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD1 | LTDC_B5 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD3 | LTDC_CLK | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD6 | LTDC_DE | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB9 | LTDC_B0 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE0 | LTDC_HSYNC | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| PWR | PC13 | PWR_WKUP2 | n/a | n/a | n/a | USER_BUTTON |
| RCC | PC14-OSC32_IN (PC14) | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15-OSC32_OUT (PC15) | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PH0-OSC_IN (PH0) | RCC_OSC_IN | n/a | n/a | n/a | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PH1-OSC_OUT (PH1) | RCC_OSC_OUT | n/a | n/a | n/a | |
| SAI2 | PB13 | SAI2_SCK_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB14 | SAI2_MCLK_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB15 | SAI2_SD_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA15 (JTDI) | SAI2_FS_B | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC10 | SAI2_SCK_B | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC11 | SAI2_MCLK_B | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC12 | SAI2_SD_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PG10 | SAI2_FS_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM3 | PE6 | TIM3_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | BL_CTRL |
| USART1 | PA9 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA10 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| USB_OTG_HS | PA11 | USB_OTG_HS_DM | n/a | n/a | n/a | |
| | PA12 | USB_OTG_HS_DP | n/a | n/a | n/a | |
| GPIO | PE2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | ADC Power On |
| | PE4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LCD_ON |
| | PE5 | GPIO_EXTI5 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | TP_IRQ |
| | PA1 | GPIO_EXTI1 | **External Interrupt Mode with Rising/Falling edge** | No pull-up and no pull-down | n/a | USB_DETECT |
| | PA4 | GPIO_EXTI4 | **External Interrupt Mode with Falling edge trigger detection** | **Pull-up *** | n/a | USB_FAULT |
| | PD2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | RED_LED |
| | PD4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | GREEN_LED |
| | PD7 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Master Mute |
| | PG9 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Channel 6 Mute |
| | PG12 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Channel 2 Mute |
| | PG15 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Master Mute |
| | PB5 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Channel 5 Mute |
| | PB6 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Channel 4 Mute |
| | PB7 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Channel 3 Mute |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PB8 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | Channel 1 Mute |

### 4.2. GPDMA1

**Channel 3 - 2 Words Internal FIFO : Standard Request Mode**
**Channel 2 - 2 Words Internal FIFO : Standard Request Mode**
**Channel 1 - 2 Words Internal FIFO : Standard Request Mode**
**Channel 0 - 2 Words Internal FIFO : Standard Request Mode**

#### 4.2.1. All Channels:

**Channel 0:**

Request GPDMA1_REQUEST_ADC1

**Channel 1:**

Request GPDMA1_REQUEST_SAI2_B

**Channel 2:**

Request GPDMA1_REQUEST_ADC4

**Channel 3:**

Request GPDMA1_REQUEST_SAI2_A

#### 4.2.2. SECURITY:

**CH3:**

Enable Channel as Privileged NON PRIVILEDGED

**CH2:**

Enable Channel as Privileged NON PRIVILEDGED

**CH1:**

Enable Channel as Privileged NON PRIVILEDGED

**CH0:**

Enable Channel as Privileged NON PRIVILEDGED

#### 4.2.3. CH3:

**Circular configuration:**

Circular Mode Disable

**Request Configuration:**

Request **SAI2_A ***

| | |
|---|---|
| DMA Handle in IP Structure | hdmarx |
| Block HW request protocol | Single/Burst Level |

**Channel configuration:**

| | |
|---|---|
| Priority | **Medium *** |
| Transaction Mode | Normal |
| Direction | **Memory To Peripheral *** |

**Source Data Setting:**

| | |
|---|---|
| Source Address Increment After Transfer | **Enabled *** |
| Data Width | **Word *** |
| Burst Length | 1 |
| Allocated Port for Transfer | Port 0 |

**Destination Data Setting:**

| | |
|---|---|
| Destination Address Increment After Transfer | Disabled |
| Data Width | Byte |
| Burst Length | 1 |
| Allocated Port for Transfer | Port 0 |

**Data Handling:**

| | |
|---|---|
| Data Handling Configuration | Disable |

**Trigger:**

| | |
|---|---|
| Trigger Configuration | Disable |

**Transfer Event Configuration:**

| | |
|---|---|
| Transfer Event Generation | The TC (and the HT) event is generated at the (respectively half) end of each block |

### 4.2.4. CH2:

**Circular configuration:**

| | |
|---|---|
| Circular Mode | Disable |

**Request Configuration:**

| | |
|---|---|
| Request | **ADC4 *** |
| DMA Handle in IP Structure | DMA_Handle |
| Block HW request protocol | Single/Burst Level |

**Channel configuration:**

| | |
|---|---|
| Priority | Low |
| Transaction Mode | Normal |
| Direction | Peripheral To Memory |

**Source Data Setting:**

| | |
|---|---|
| Source Address Increment After Transfer | Disabled |
| Data Width | **Half Word *** |
| Burst Length | 1 |

| | |
|---|---|
| Allocated Port for Transfer | Port 0 |

**Destination Data Setting:**

| | |
|---|---|
| Destination Address Increment After Transfer | **Enabled *** |
| Data Width | **Half Word *** |
| Burst Length | 1 |
| Allocated Port for Transfer | Port 0 |

**Data Handling:**

| | |
|---|---|
| Data Handling Configuration | Disable |

**Trigger:**

| | |
|---|---|
| Trigger Configuration | Disable |

**Transfer Event Configuration:**

| | |
|---|---|
| Transfer Event Generation | The TC (and the HT) event is generated at the (respectively half) end of each block |

### 4.2.5. CH1:

**Circular configuration:**

| | |
|---|---|
| Circular Mode | **Enable *** |
| Circular Port | Port 0 |

**Request Configuration:**

| | |
|---|---|
| Request | **SAI2_B *** |
| DMA Handle in IP Structure | hdmarx |
| Block HW request protocol | Single/Burst Level |

**Channel configuration:**

| | |
|---|---|
| Priority | **Medium *** |
| Transaction Mode | Normal |
| Direction | Peripheral To Memory |
| Node Type | GPDMA Linear Addressing |

**Source Data Setting:**

| | |
|---|---|
| Source Address Increment After Transfer | Disabled |
| Data Width | **Word *** |
| Burst Length | 1 |
| Allocated Port for Transfer | Port 0 |

**Destination Data Setting:**

| | |
|---|---|
| Destination Address Increment After Transfer | **Enabled *** |
| Data Width | **Word *** |
| Burst Length | 1 |
| Allocated Port for Transfer | Port 0 |

**Data Handling:**

| | |
|---|---|
| Data Handling Configuration | Disable |

**Trigger:**

| | |
|---|---|
| Trigger Configuration | Disable |

**Transfer Event Configuration:**

| | |
|---|---|
| Transfer Event Generation | The TC (and the HT) event is generated at the (respectively half) end of each block |

**Channel Configuration for Linked List:**

| | |
|---|---|
| Execution Mode (circular/linear) of the Linked List | Circular |
| Linked List Execution Mode | The List is fully executed |

### 4.2.6. CH0:

**Circular configuration:**

| | |
|---|---|
| Circular Mode | **Enable *** |
| Circular Port | Port 0 |

**Request Configuration:**

| | |
|---|---|
| Request | **ADC1 *** |
| DMA Handle in IP Structure | DMA_Handle |
| Block HW request protocol | Single/Burst Level |

**Channel configuration:**

| | |
|---|---|
| Priority | Low |
| Transaction Mode | Normal |
| Direction | Peripheral To Memory |
| Node Type | GPDMA Linear Addressing |

**Source Data Setting:**

| | |
|---|---|
| Source Address Increment After Transfer | Disabled |
| Data Width | **Half Word *** |
| Burst Length | 1 |
| Allocated Port for Transfer | Port 0 |

**Destination Data Setting:**

| | |
|---|---|
| Destination Address Increment After Transfer | **Enabled *** |
| Data Width | **Half Word *** |
| Burst Length | 1 |
| Allocated Port for Transfer | **Port 1 *** |

**Data Handling:**

| | |
|---|---|
| Data Handling Configuration | Disable |

**Trigger:**

| | |
|---|---|
| Trigger Configuration | Disable |

**Transfer Event Configuration:**

| | |
|---|---|
| Transfer Event Generation | The TC (and the HT) event is generated at the (respectively half) end of each block |

**Channel Configuration for Linked List:**

| | |
|---|---|
| Execution Mode (circular/linear) of the Linked List | Circular |
| Linked List Execution Mode | The List is fully executed |

## 4.3. LINKEDLIST

## 4.4. LPDMA1

## 4.5. NVIC configuration

### 4.5.1. NVIC

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Prefetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 15 | 0 |
| EXTI Line1 interrupt | true | 0 | 0 |
| EXTI Line4 interrupt | true | 0 | 0 |
| EXTI Line5 interrupt | true | 0 | 0 |
| GPDMA1 Channel 0 global interrupt | true | 0 | 0 |
| GPDMA1 Channel 1 global interrupt | true | 0 | 0 |
| GPDMA1 Channel 2 global interrupt | true | 0 | 0 |
| GPDMA1 Channel 3 global interrupt | true | 0 | 0 |
| ADC1 and ADC2 global interrupt | true | 0 | 0 |
| I2C2 Event interrupt | true | 0 | 0 |
| I2C2 Error interrupt | true | 0 | 0 |
| USART1 global interrupt | true | 0 | 0 |
| LCD-TFT global interrupt | true | 0 | 0 |
| Flash non-secure global interrupt | unused | | |
| RCC non-secure global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| I2C1 Event interrupt | unused | | |
| I2C1 Error interrupt | unused | | |
| USB OTG HS global interrupt | unused | | |
| PWR wake up from Stop3 interrupt | unused | | |
| Serial Audio Interface 2 global interrupt | unused | | |
| FPU global interrupt | unused | | |
| Instruction cache global interrupt | unused | | |
| ADC4 (12bits) global interrupt | unused | | |
| DMA2D global interrupt | unused | | |
| HSPI1 global interrupt | unused | | |
| LCD-TFT Error interrupt | unused | | |

### 4.5.2. NVIC Code generation

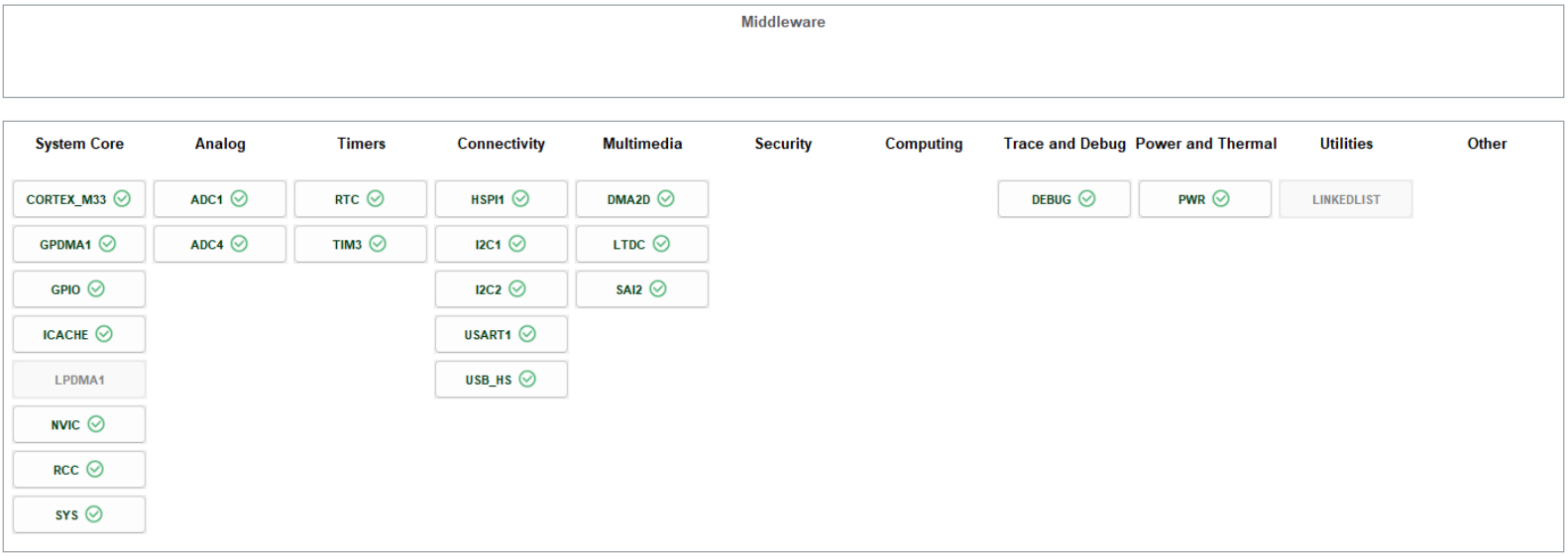
| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|---|---|---|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| Prefetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | true | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | true | false |
| System tick timer | false | true | true |
| EXTI Line1 interrupt | false | true | true |
| EXTI Line4 interrupt | false | true | true |
| EXTI Line5 interrupt | false | true | true |
| GPDMA1 Channel 0 global interrupt | false | true | true |
| GPDMA1 Channel 1 global interrupt | false | true | true |
| GPDMA1 Channel 2 global interrupt | false | true | true |
| GPDMA1 Channel 3 global interrupt | false | true | true |
| ADC1 and ADC2 global interrupt | false | true | true |
| I2C2 Event interrupt | false | true | true |
| I2C2 Error interrupt | false | true | true |
| USART1 global interrupt | false | true | true |
| LCD-TFT global interrupt | false | true | true |

*** User modified value**

# 5. System Views

## 5.1. Category view

### *5.1.1. Current*



# 6. Docs & Resources

| Type | Link |
|---|---|
| BSDL files | https://www.st.com/resource/en/bsdl_model/stm32u5_bsdl.zip |
| IBIS models | https://www.st.com/resource/en/ibis_model/stm32u5-ibis.zip |
| System View Description | https://www.st.com/resource/en/svd/stm32u5_svd.zip |
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