

DATE 11-07-18

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170-30168

IMXRT1050 EVKB

REV B

NXP SEMICONDUCTOR

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FILM ARTWORK LAYERO3

6501 WILLIAM CANNON DRIVE WEST AUSTIN. TEXAS 78735 USA THIS DOCUMENT CONTAINS INFORMATION

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6 OF 10

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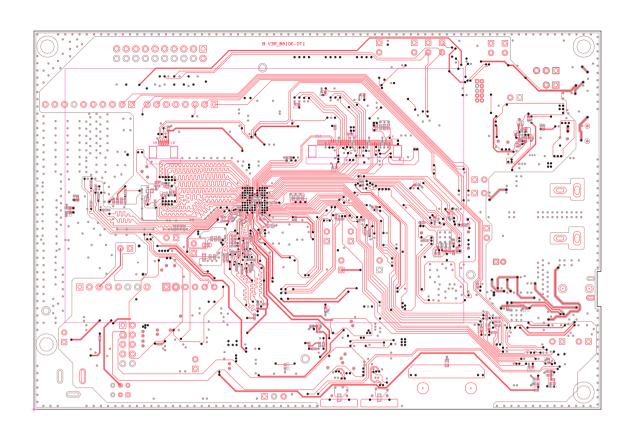
FILM ARTWORK LAYER02

6501 WILLIAM CANNON DRIVE WEST AUSTIN. TEXAS 78735 USA

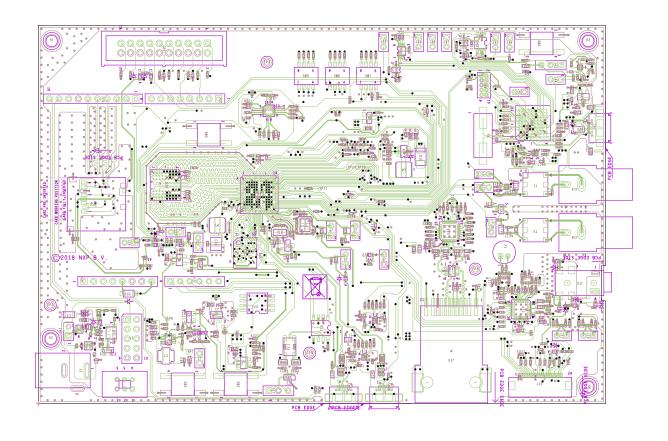
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5 OF 10

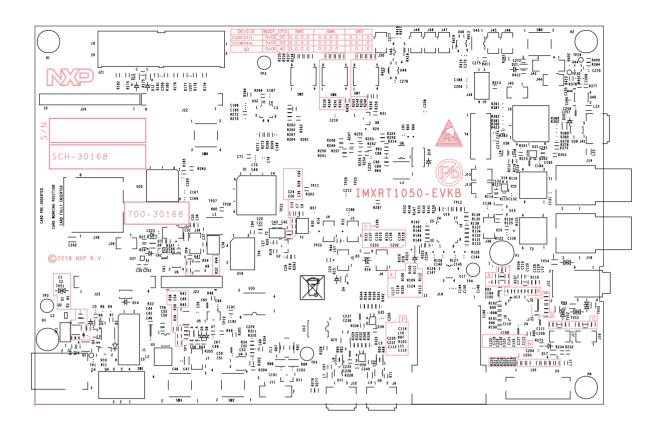
ZONE REV DATE APPROVED DESCRIPTION NOTES (UNLESS OTHERWISE SPECIFIED): A ORIGINAL RELEASE 12-21-17 SHAWN 11-07-18 SHAWN 1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE LAYER STACKUP WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION). SCALE: NONE 2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS. .062" THK +/- 10% 3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98 IMPEDANCE TOLERANCE IS 10% Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS. 1/2oz+plating Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS. Layers Trace Width (Mils) Trace Width (Ohms) (Mils) Trace Spacing (Ohms) (Mils) Trace Spacing (Ohms) (Mils) Trace Width (Mils) (Mils) 4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A' 5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B' LAYER 4 SOLDER SIDE 1/2oz+plating 6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .00X"/.00X" 7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD): .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER DRILL CHART: TOP to BOTTOM 2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL ALL UNITS ARE IN MILS 8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT. PLATED QTY PLATED 1674 + 3 . 0 / - 3 . 0 9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES. + 2 . 0 / - 2 . PLATED MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE. PLATED + 3 . 0 / - 3 . (10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS. PLATED + 3 . 0 / - 3 . (PLATED + 3 . 0 / - 3 . (11. ELECTRICAL TEST - 100% IPCD356. PLATED + 3 . 0 / - 3 . 12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED. + 3 . 0 / - 3 . (PLATED PLATED + 3 . 0 / - 3 . (13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, PLATED + 3 . 0 / - 3 . 0 UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE. PLATED + 3 . 0 / - 3 . (14. ADD TEARDROPS TO ALL SIGNAL LAYERS. PLATED + 3 . 0 / - 3 . 0 15. SOLDER SAMPLES TO BE PROVIDED. + 2 . 0 / - 2 . 0 /16 BASIC GRID INCREMENT AT 1:1 IS .0001. 59.0x20. PLATED 79.0x40.0 /17.\ SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN. 86.61x47.24 PLATED - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0 +2.0/-2.0 PLATED 18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (PG) 118.0x31.0 +2.0/-2.0 PLATED 19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C) 137.8x31.5 + 2 . 0 / - 2 . 0 20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM. 21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURING REQUIREMENT. ADDITION OF .25" RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION PANELIZATION MUST BE APPROVED BY FREESCALE. 6666666666 **- 5905.50 [150] -**THIS DOCUMENT CONTAINS INFORMATION __ PUBI (PUBLIC INFORMATION) NXP SEMICONDUCTOR PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN X FIUO (NXP INTERNAL USE ONLY) PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF FCP (NXP CONFIDENTIAL PROPRIETARY) 6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA APPROVALS DATE TITLE: UNLESS OTHERWISE SPECIFIED PRINTED WIRING BOARD DIMENSIONS ARE IN INCHES TOLERANCES ARE: Albert Li | 11-07-18 | IMXRT1050-EVKB DECIMALS ANGLES .XX .01 .XXX .005 Shawn Shi 11-07-18 SIZE CAD FILE NAME DWG. NO. ✓ RMS ALL MACHINED SURFACES BREAK ALL SHARP EDGES AND CORNERS, FAB-30168 REMOVE BURRS. UNDERLINED DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1



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