CORDIC (COordinate Rotation DIgital Computer)

Trabajo Final de Circuitos Lógicos Programables

Carrera de Especialización en Sistemas Embebidos

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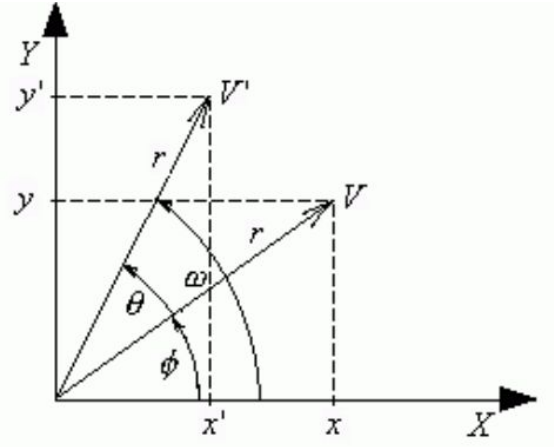
Introducción

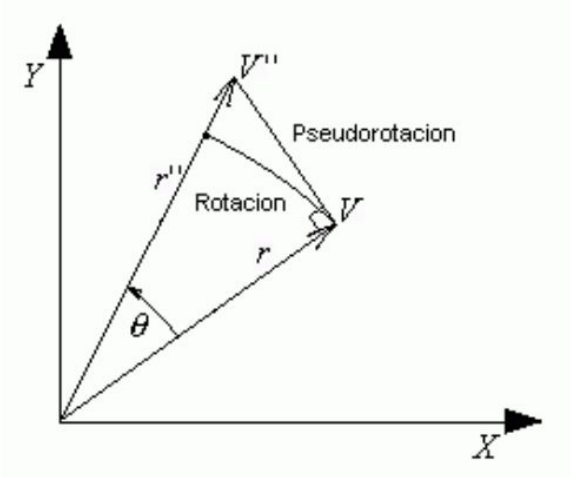
- Algoritmo descrito por Jack E. Volder en 1959
- Iterativo
- Calcular funciones por medio de sumas y desplazamiento de bits
- Consiste en rotar un vector

Funcionamiento



$$x' = x\cos\theta - y\,\mathrm{sen}\,\theta$$
$$y' = y\cos\theta + x\,\mathrm{sen}\,\theta$$

Rotación de un vector



$$x' = \cos\theta\left(x - y\,\mathrm{tg}\,\theta\right)$$
$$y' = \cos\theta\left(y + x\,\mathrm{tg}\,\theta\right)$$

Pseudorotación de un vector

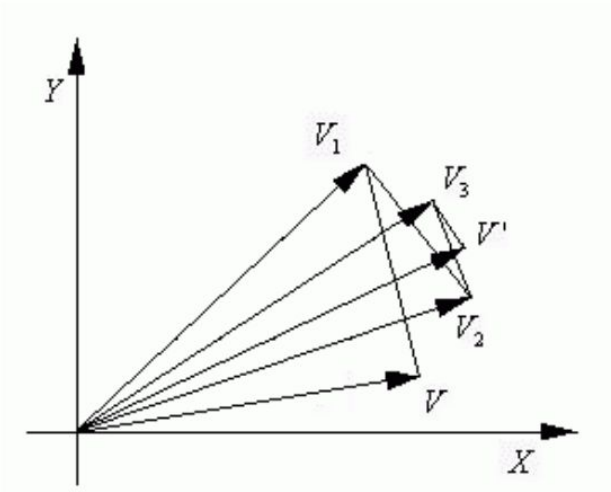
Funcionamiento

Restringiendo el valor de la tangente: $\operatorname{tg}\theta = \pm 2^{-i}, i \in \mathrm{N}$

$$x_{i+1} = K_i \left(x_i - y_i d_i 2^{-i} \right)$$
$$y_{i+1} = K_i \left(y_i + x_i d_i 2^{-i} \right)$$

$$K_i = \cos\theta_i = \cos\left(\operatorname{arctg} 2^{-i}\right) = \frac{1}{\sqrt{1+\operatorname{tg}^2\theta_i}} = \frac{1}{\sqrt{1+2^{-2i}}}$$

Ecuaciones generales



$$x_{i+1} = x_i - y_i d_i 2^{-i}$$
$$y_{i+1} = y_i + x_i d_i 2^{-i}$$
$$z_{i+1} = z_i - d_i \operatorname{arctg}\left(2^{-i}\right)$$

$$d_i = \begin{cases} -1 & , si\ z_i < 0 \\ 1 & , si\ z_i \geq 0 \end{cases}$$

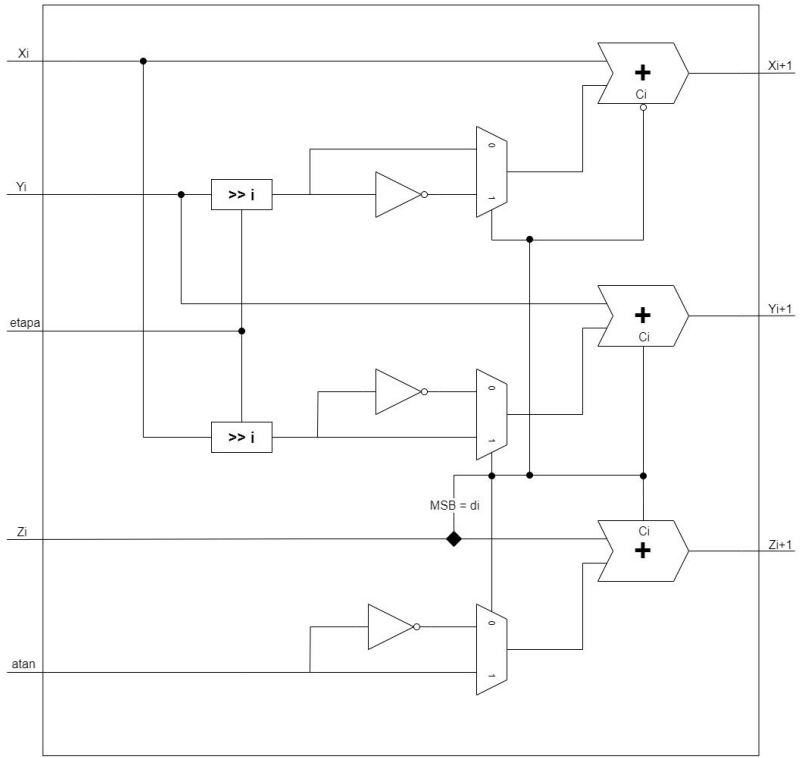
Rotación por pseudorotaciones

Tabla de rotación

Iteración = i	2^(-i)	atan(2^(-i))	Decimal	Bits
0	1	45°	32768	0010000000000000
1	0.5	26.56°	19344	0001001011100100 00
…	…	..	..	…
14	0.000061035	0.00349	3	0000000000000011
15	0.000030517	0.001749	1	0000000000000001

Diseño

Módulo principal CORDIC



Recordatorio

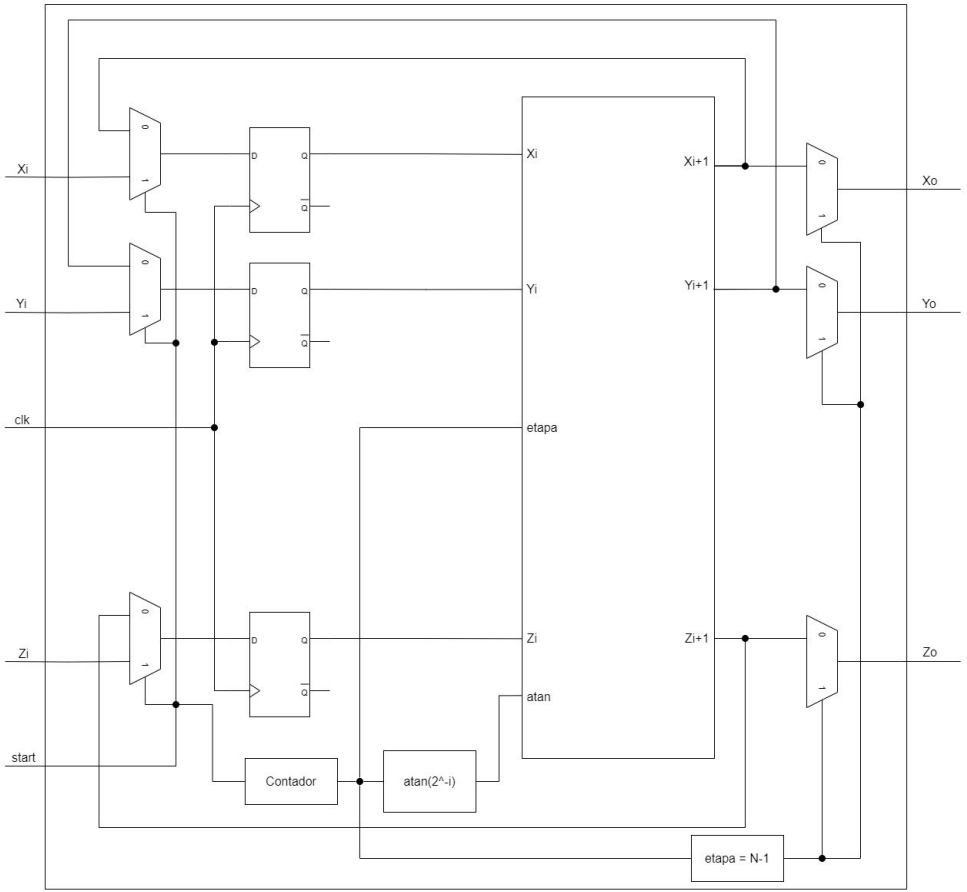
$$x_{i+1} = x_i - y_i d_i 2^{-i}$$

$$y_{i+1} = y_i + x_i d_i 2^{-i}$$

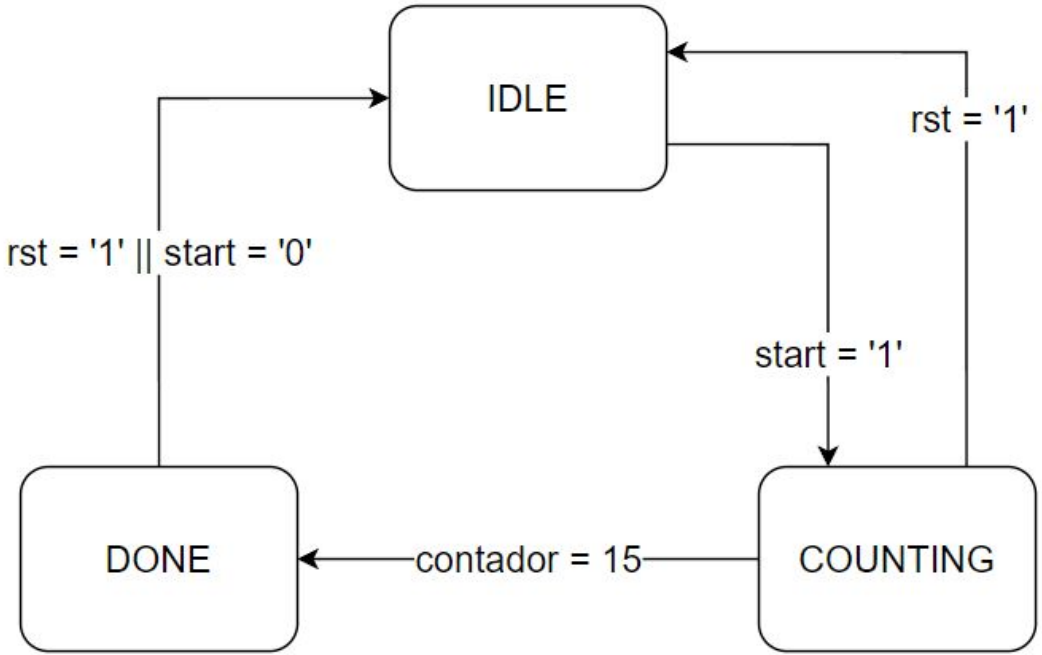
$$z_{i+1} = z_i - d_i \operatorname{arctg}\left(2^{-i}\right)$$

Diseño

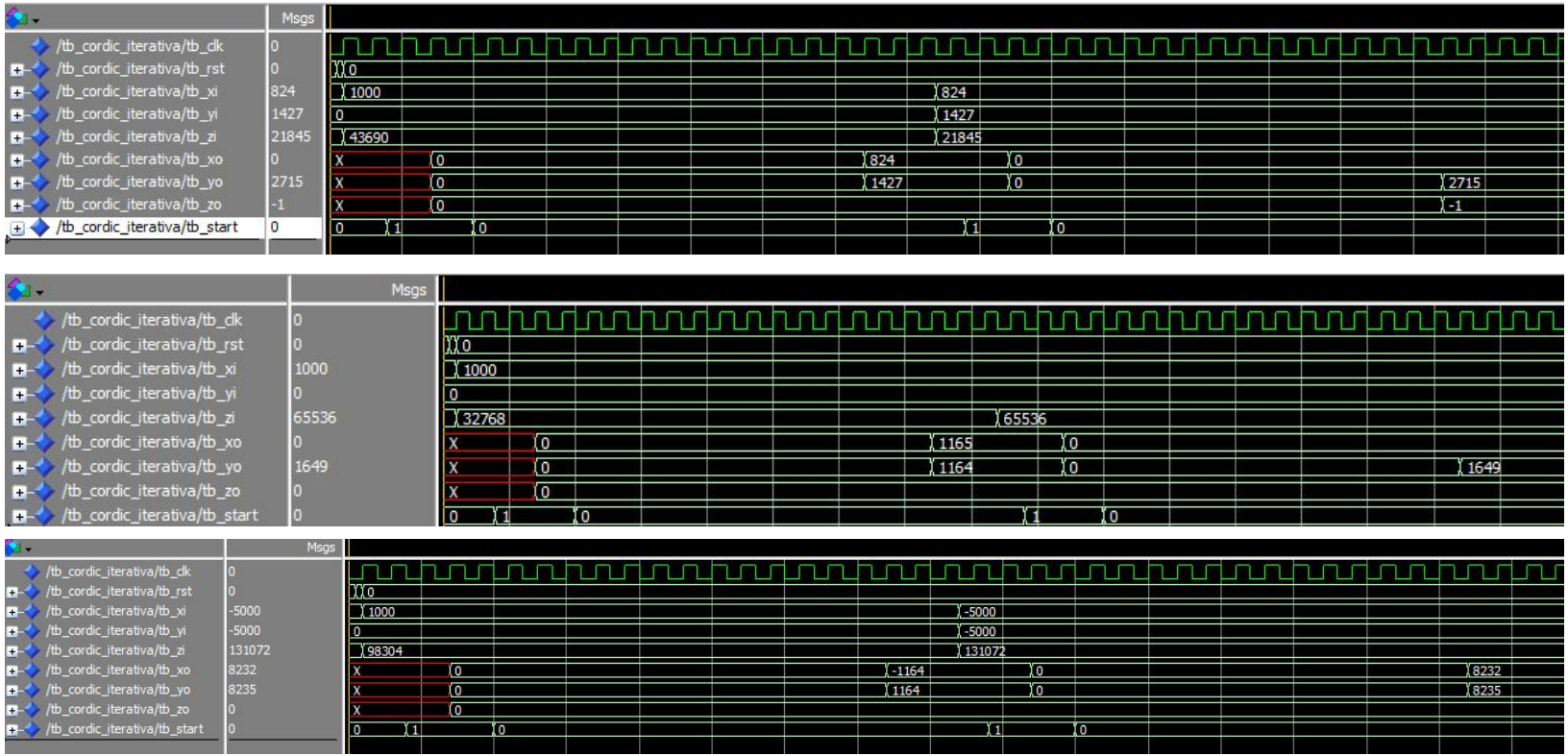
Arquitectura iterativa



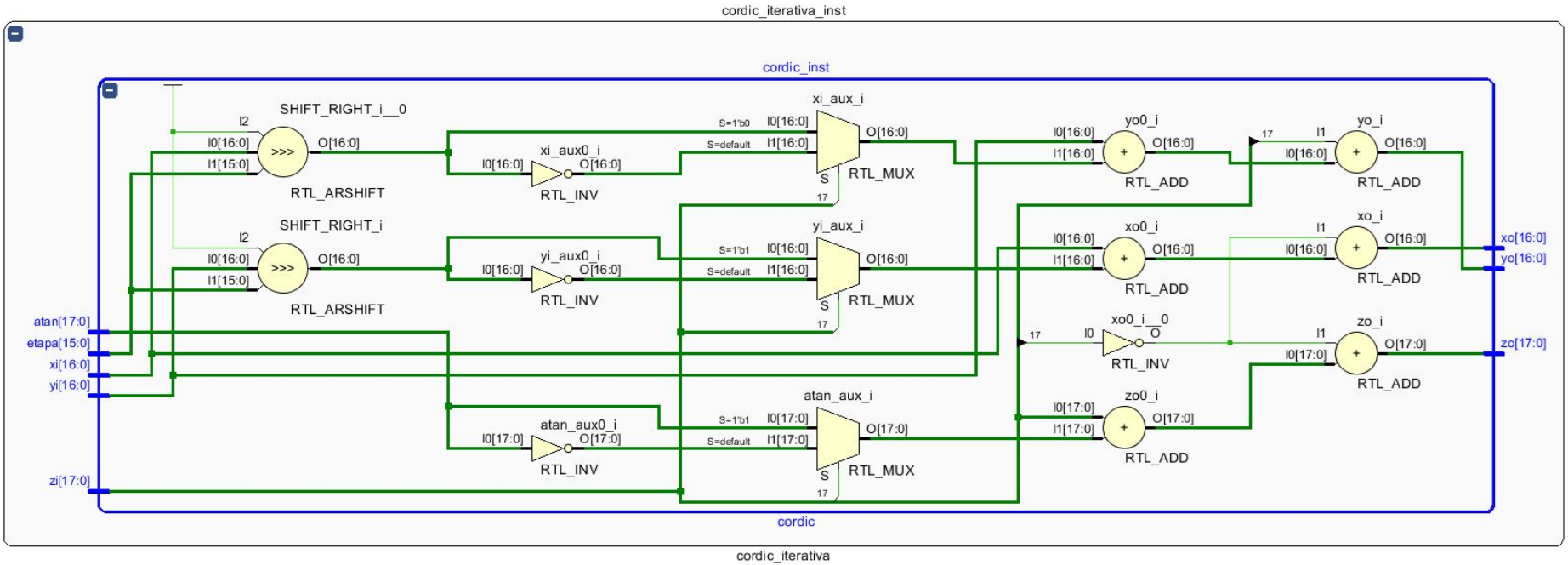
Máquina de Estados



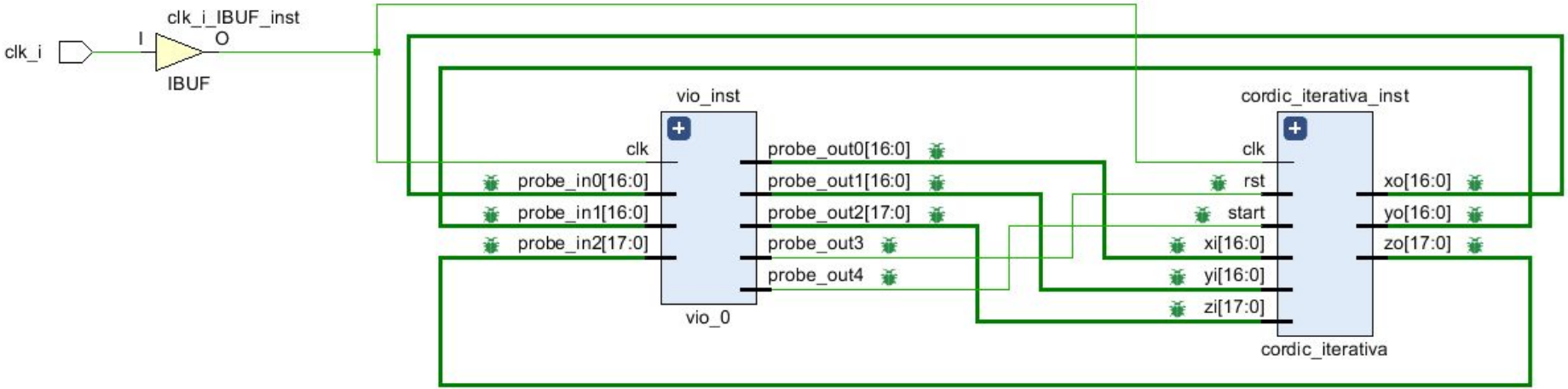
Simulaciones



Síntesis e implementación



VIO


clk_i
clk_i_IBUF_inst
I
O
IBUF
vio_inst
clk
probe_in0[16:0]
probe_in1[16:0]
probe_in2[17:0]
probe_out0[16:0]
probe_out1[16:0]
probe_out2[17:0]
probe_out3
probe_out4
vio_0
cordic_iterativa_inst
clk
rst
start
xi[16:0]
yi[16:0]
zi[17:0]
xo[16:0]
yo[16:0]
zo[17:0]
cordic_iterativa

Recursos utilizados

Name	Slice LUTs (17600)	Slice Registers (35200)	Slice (4400)	LUT as Logic (17600)	LUT as Memory (6000)	LUT Flip Flop Pairs (17600)	Bonded IOB (100)	BUFGCTRL (32)	BSCANE2 (4)
cordic_VIO	6.14%	4.52%	10.41%	6.00%	0.40%	3.78%	1.00%	6.25%	25.00%
cordic_iterativa_inst (c...	1.37%	0.35%	1.68%	1.37%	0.00%	0.45%	0.00%	0.00%	0.00%
dbg_hub (dbg_hub)	2.63%	2.05%	5.14%	2.49%	0.40%	1.69%	0.00%	3.13%	25.00%
vio_inst (vio_0)	2.14%	2.12%	4.11%	2.14%	0.00%	1.59%	0.00%	0.00%	0.00%

Prueba en FPGA

Name	Value	Activity	Direction	VIO
rst	[B] 0		Output	hw_vio_1
start	[B] 1		Output	hw_vio_1
xi[16:0]	[U] 1000		Output	hw_vio_1
yi[16:0]	[U] 0		Output	hw_vio_1
zi[17:0]	[U] 43690		Output	hw_vio_1
input_x_vio[16:0]	[S] 824		Input	hw_vio_1
input_y_vio[16:0]	[S] 1427		Input	hw_vio_1
input_z_vio[17:0]	[U] 0		Input	hw_vio_1

Rotación 60°

Name	Value	Activity	Direction	VIO
rst	[B] 0		Output	hw_vio_1
start	[B] 1		Output	hw_vio_1
xi[16:0]	[U] 824		Output	hw_vio_1
yi[16:0]	[U] 1427		Output	hw_vio_1
zi[17:0]	[U] 21845		Output	hw_vio_1
input_x_vio[16:0]	[S] 0		Input	hw_vio_1
input_y_vio[16:0]	[S] 2715		Input	hw_vio_1
input_z_vio[17:0]	[S] -1		Input	hw_vio_1

Rotación 30°

Name	Value	Activity	Direction	VIO
rst	[B] 0		Output	hw_vio_1
start	[B] 1		Output	hw_vio_1
xi[16:0]	[S] 1000		Output	hw_vio_1
yi[16:0]	[S] 0		Output	hw_vio_1
zi[17:0]	[S] 32768		Output	hw_vio_1
input_x_vio[16:0]	[S] 1165		Input	hw_vio_1
input_y_vio[16:0]	[S] 1164		Input	hw_vio_1
input_z_vio[17:0]	[S] 0		Input	hw_vio_1

Rotación 45°

Name	Value	Activity	Direction	VIO
rst	[B] 0		Output	hw_vio_1
start	[B] 1		Output	hw_vio_1
xi[16:0]	[S] 1000		Output	hw_vio_1
yi[16:0]	[S] 0		Output	hw_vio_1
zi[17:0]	[S] 65536		Output	hw_vio_1
input_x_vio[16:0]	[S] 0		Input	hw_vio_1
input_y_vio[16:0]	[S] 1649		Input	hw_vio_1
input_z_vio[17:0]	[S] 0		Input	hw_vio_1

Rotación 90°

Prueba en FPGA

Name	Value	Activity	Direction	VIO
rst	[B] 0		Output	hw_vio_1
start	[B] 1		Output	hw_vio_1
xi[16:0]	[S] 1000		Output	hw_vio_1
yi[16:0]	[S] 0		Output	hw_vio_1
zi[17:0]	[S] 98304		Output	hw_vio_1
input_x_vio[16:0]	[S] -1164	↑	Input	hw_vio_1
input_y_vio[16:0]	[S] 1164	↕	Input	hw_vio_1
input_z_vio[17:0]	[S] 0		Input	hw_vio_1

Rotación 135°

Name	Value	Activity	Direction	VIO
rst	[B] 0		Output	hw_vio_1
start	[B] 1		Output	hw_vio_1
xi[16:0]	[S] -5000		Output	hw_vio_1
yi[16:0]	[S] -5000		Output	hw_vio_1
zi[17:0]	[U] 131072		Output	hw_vio_1
input_x_vio[16:0]	[S] 8232	↕	Input	hw_vio_1
input_y_vio[16:0]	[S] 8235	↕	Input	hw_vio_1
input_z_vio[17:0]	[S] 0		Input	hw_vio_1

Rotación 180°

Código implementado en VHDL

¡Gracias!
¿Preguntas?