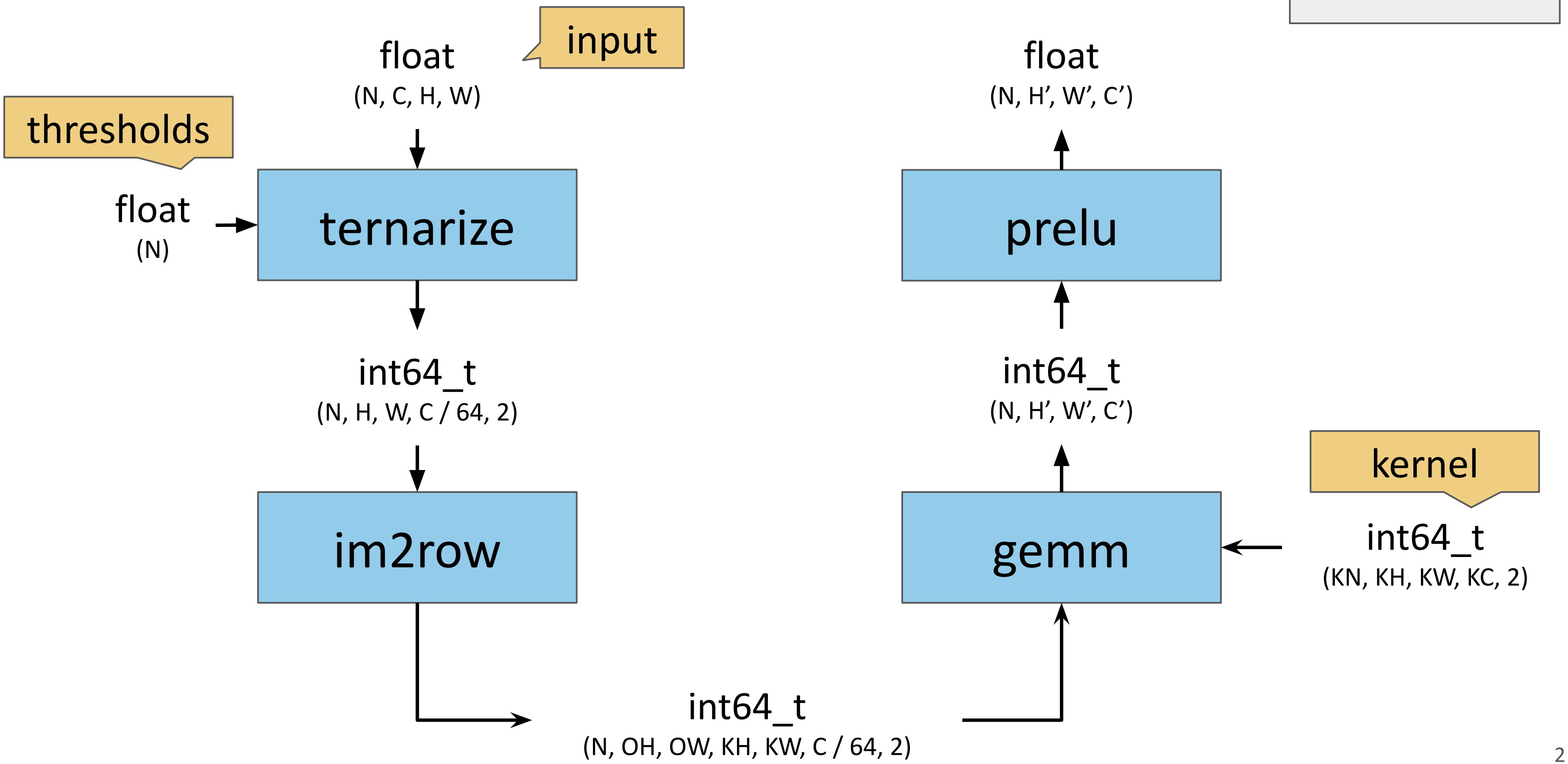
Bitwise Convolution for Ternary Neural Networks

Felix Möller, Daniel Nezamabadi, Rudy Peterson, Luca Tagliavini
Supervisor: Shien Zhu

Advanced Systems Lab - Final Presentation, ETH Zurich
June 7th, 2024

Overview: Algorithm

std::vector



input

float

(N, C, H, W)

thresholds

float

(N)

ternarize

int64_t

(N, H, W, C / 64, 2)

im2row

int64_t

(N, OH, OW, KH, KW, C / 64, 2)

gemm

kernel

int64_t

(KN, KH, KW, KC, 2)

int64_t

(N, H’, W’, C’)

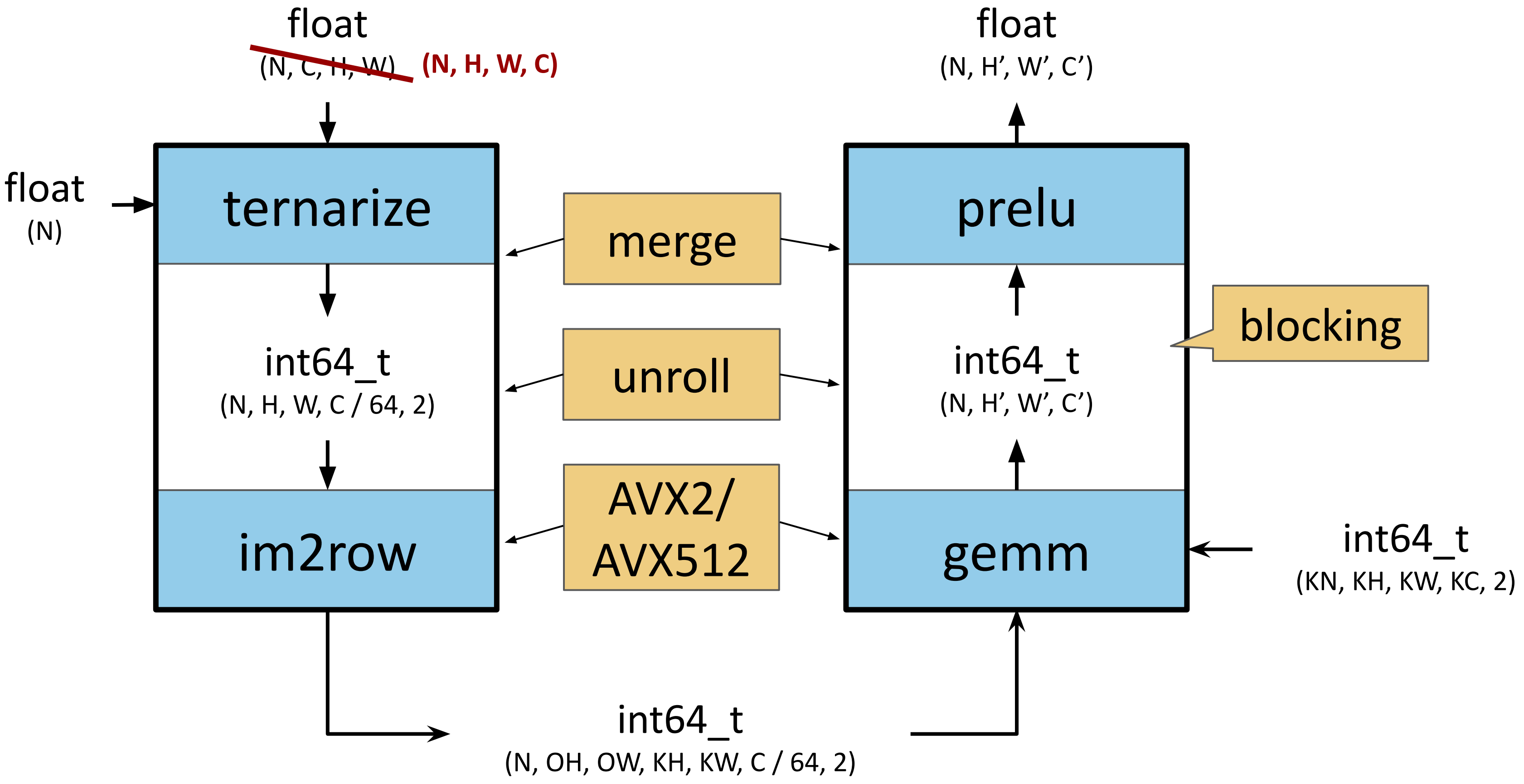
prelu

float

(N, H’, W’, C’)

Overview: Our Work

Tensor ~~std::vector~~



Using Tensors

```
class Tensor3D {
  T *data;
  const size_t dim1;
  const size_t dim2;
  const size_t dim3;
}
```

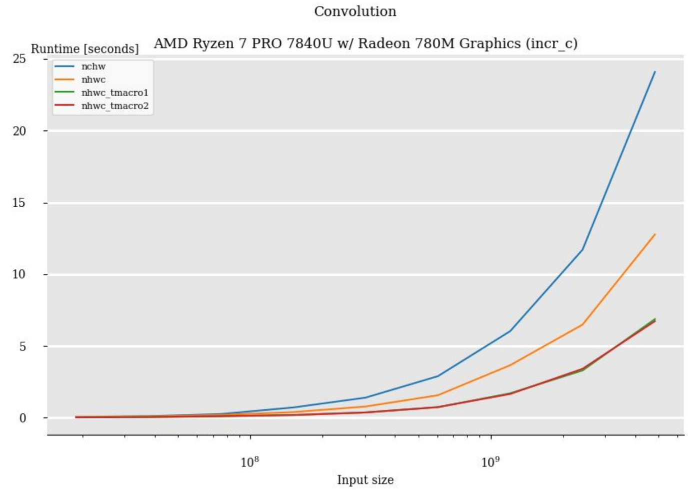
nhwc_tmacro1

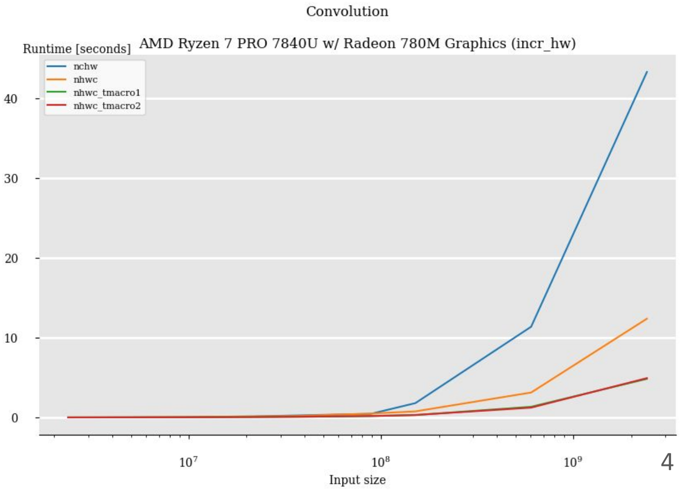
```
#define tensor3d_set(data, dim2, dim3, value, i, j, k)          \
  ((data)[((i) * ((dim2) * (dim3))) + ((j) * (dim3)) + (k)] = (value))
```

nhwc_tmacro2

```
#define tensor3d_set(data, dim2, dim3, value, i, j, k)          \
  ((data)[((i) * (dim2) + (j)) * (dim3) + (k)] = (value))
```

gcc with O3 and disabled vectorization



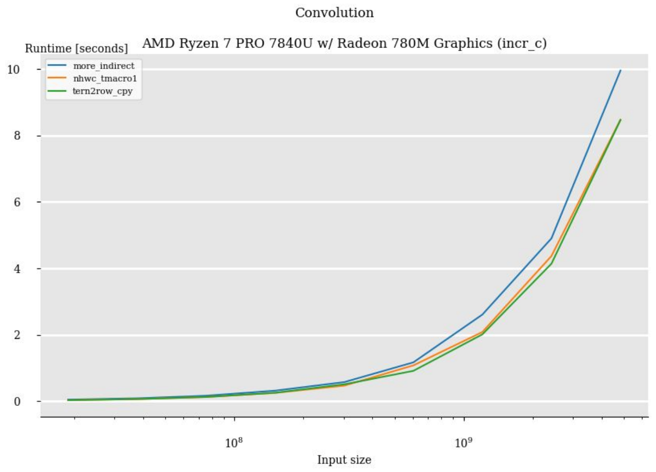


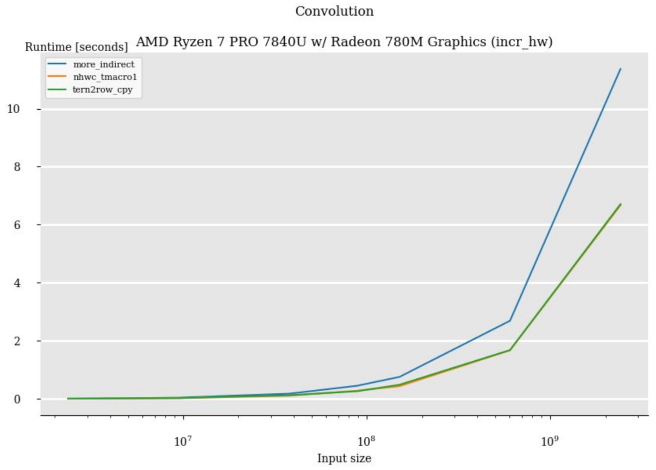
Merging im2row

Don’t merge im2row

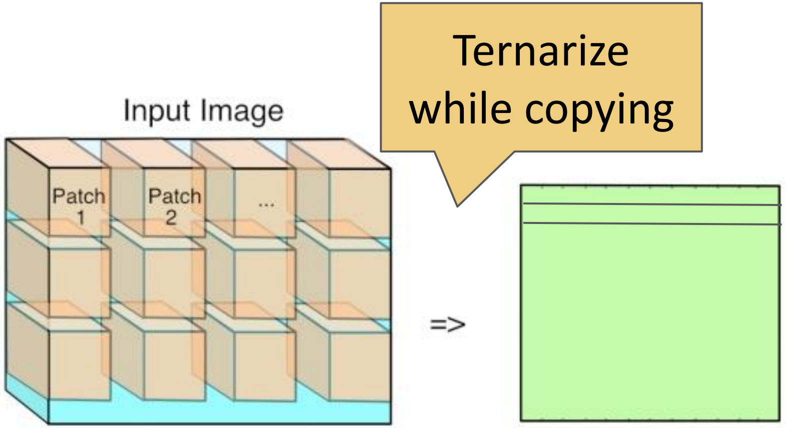
Merge ternarize and im2row

Merge im2row and gemm (indirect)

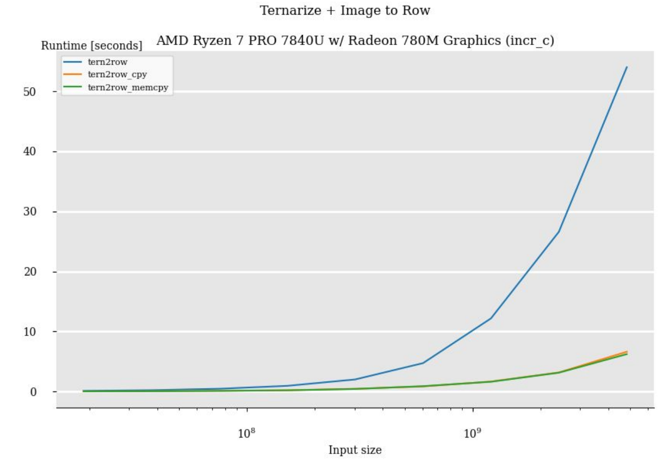




ternarize + im2row



Ternarize while copying



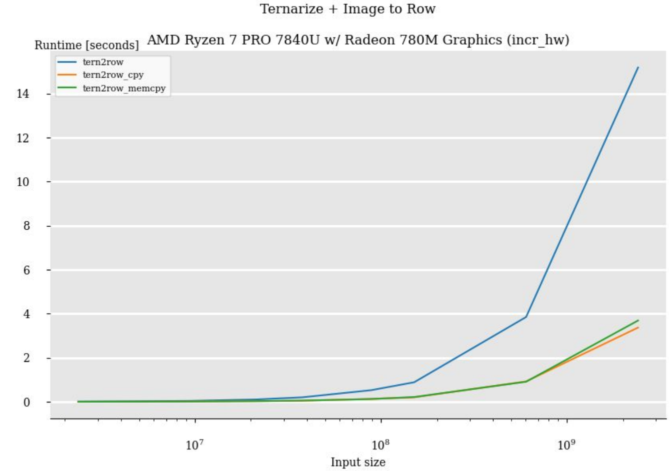
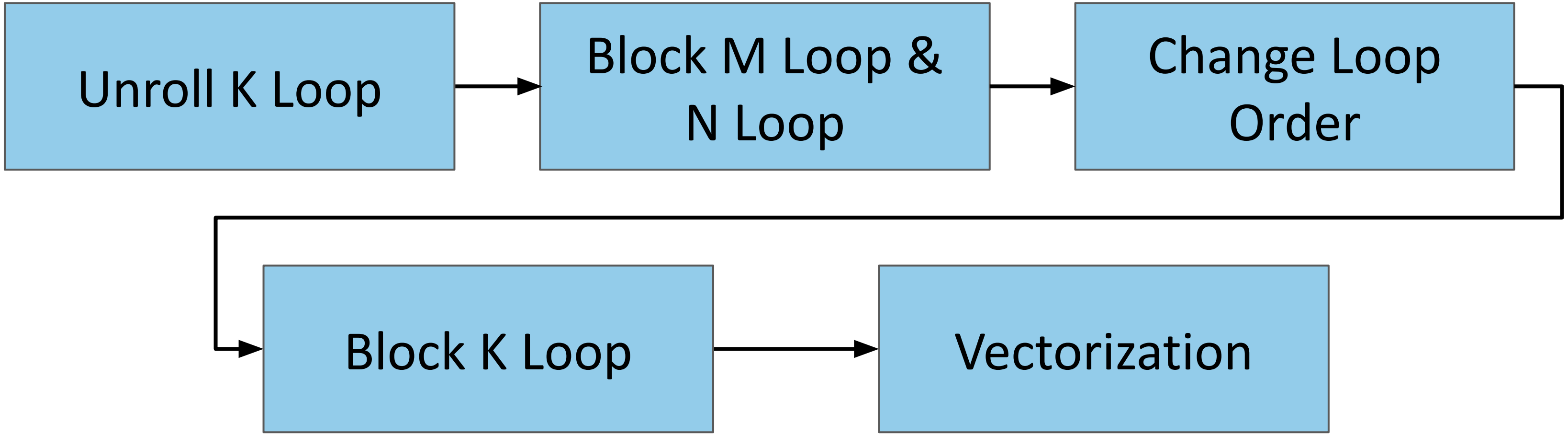
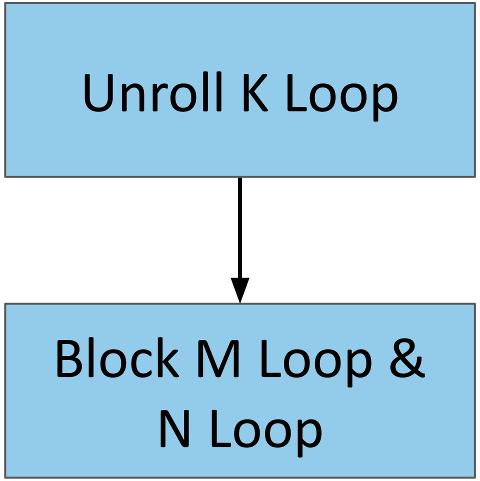


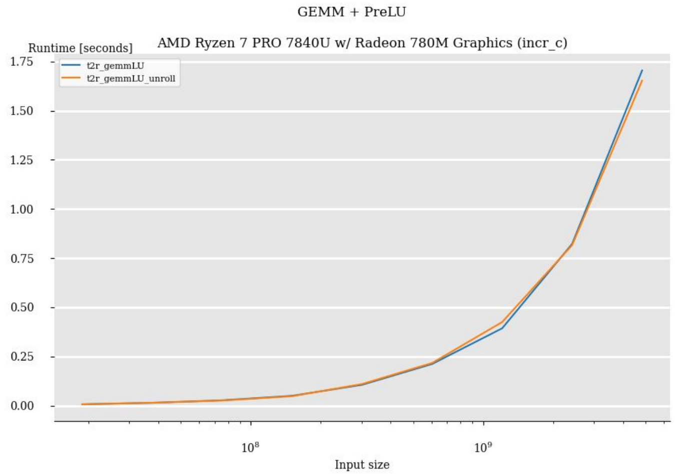
Image adapted from https://leonardoaraujosantos.gitbook.io/artificial-inteligence/machine_learning/deep_learning/convolution_layer/making_faster

GEMM + PReLU - Optimization Plan

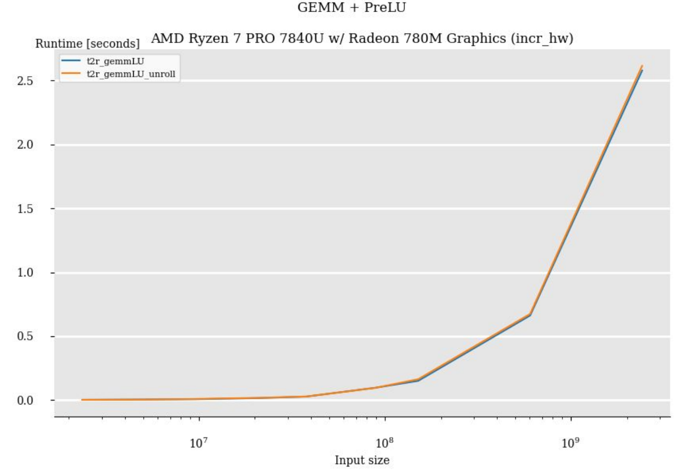


GEMM + PReLU - Unrolling over K & Blocking over M and N



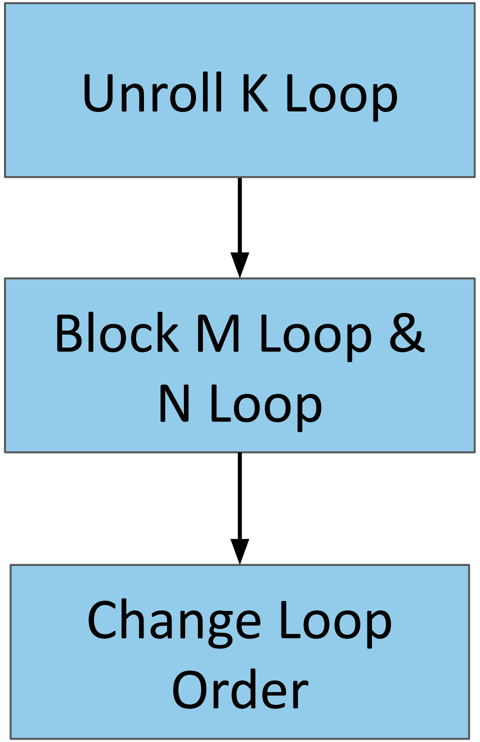

GEMM + PreLU

AMD Ryzen 7 PRO 7840U w/ Radeon 780M Graphics (incr_c)


GEMM + PreLU

AMD Ryzen 7 PRO 7840U w/ Radeon 780M Graphics (incr_hw)

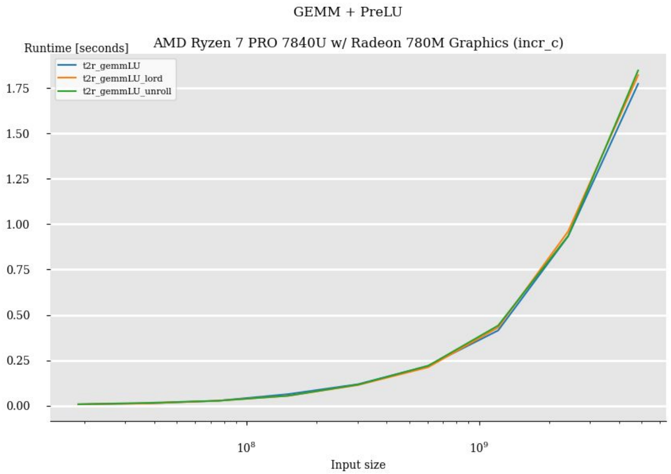
GEMM + PReLU - Changing the Loop Order

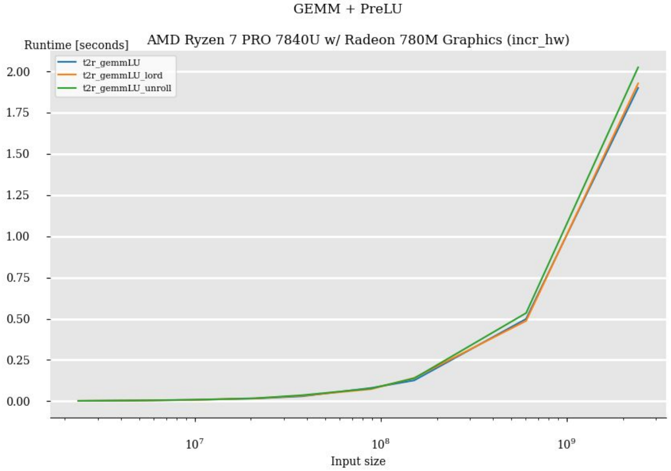


Unroll K Loop

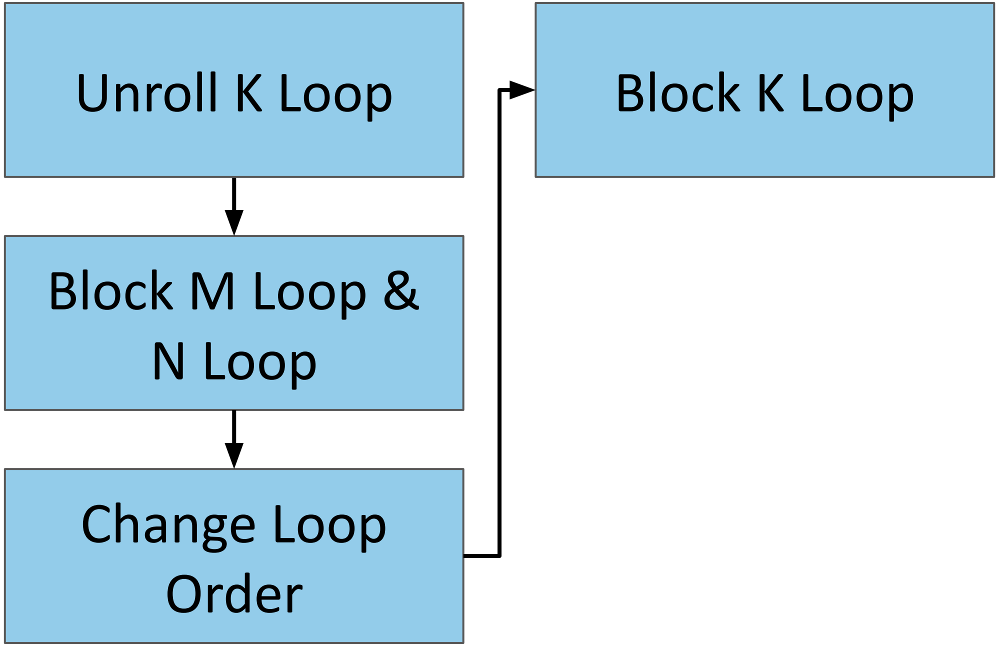
Block M Loop & N Loop

Change Loop Order





GEMM + PReLU - Blocking over K

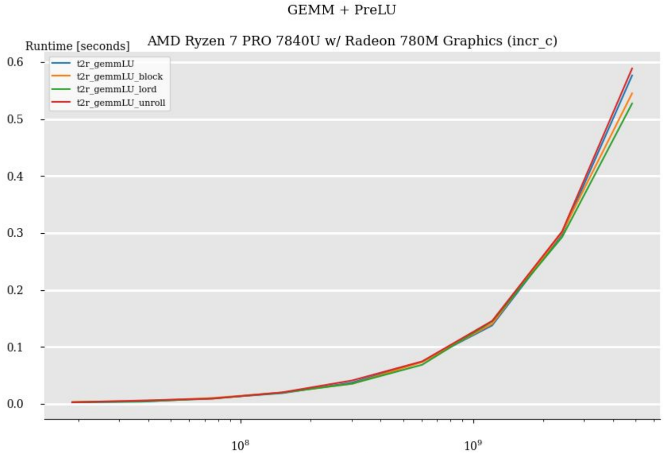


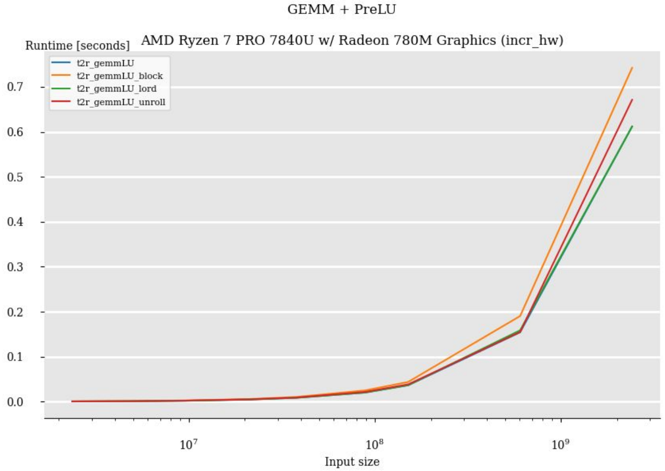
Unroll K Loop

Block M Loop & N Loop

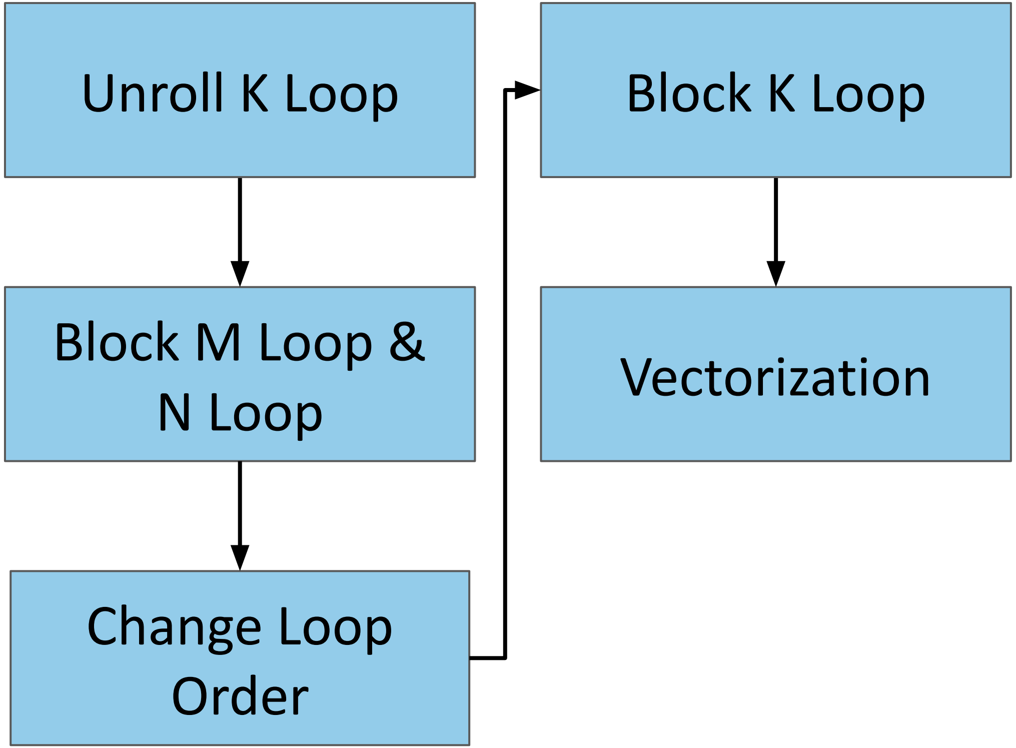
Change Loop Order

Block K Loop





GEMM + PReLU - Vectorization with AVX2 and AVX512



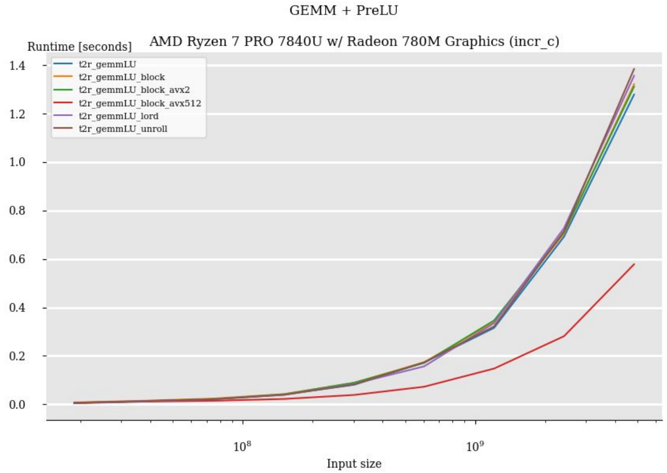
Unroll K Loop

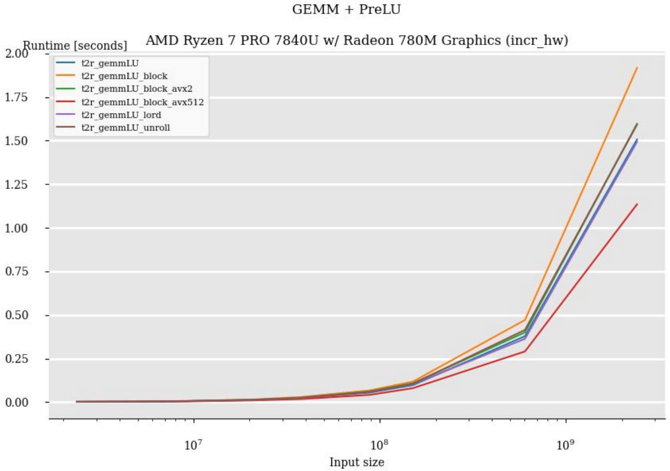
Block M Loop & N Loop

Change Loop Order

Block K Loop

Vectorization



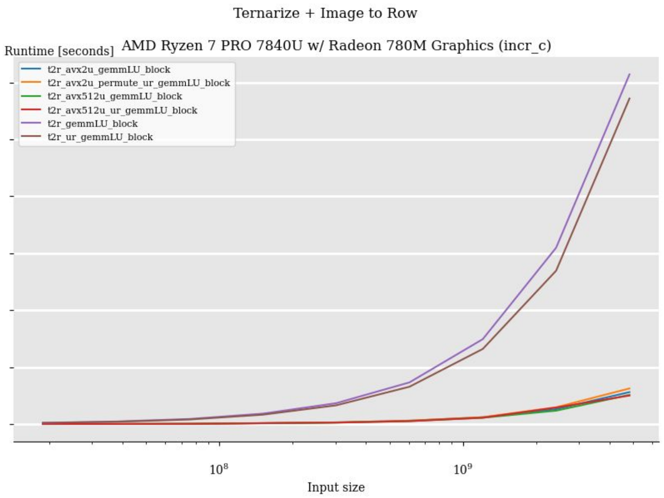


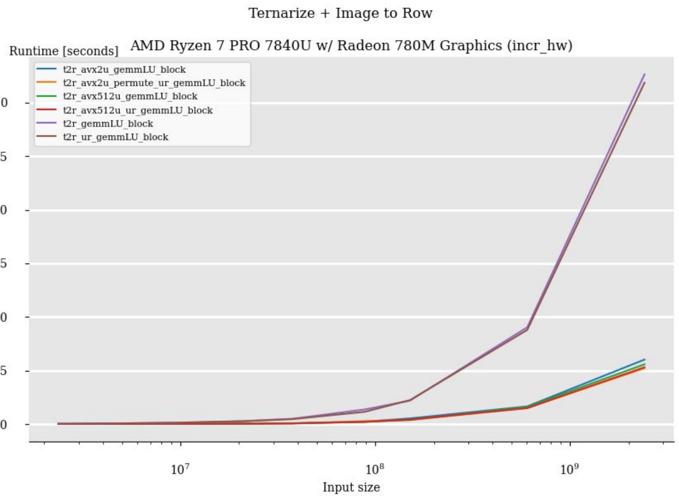
Optimizing Ternarize + im2row

Loop Unrolling

AVX2

AVX512



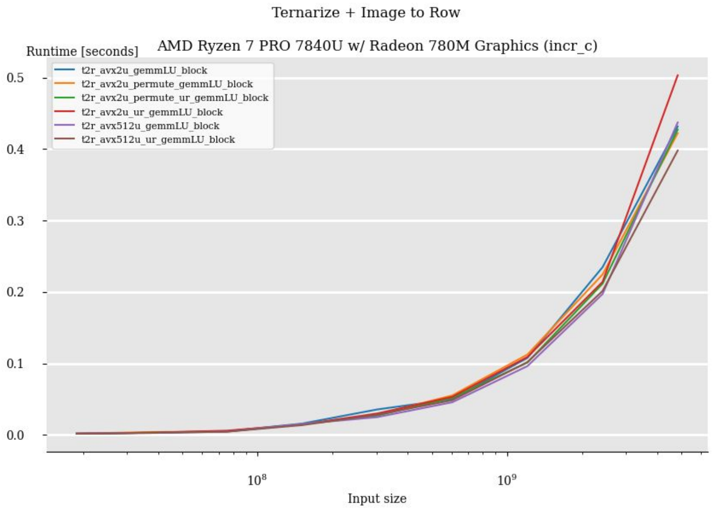


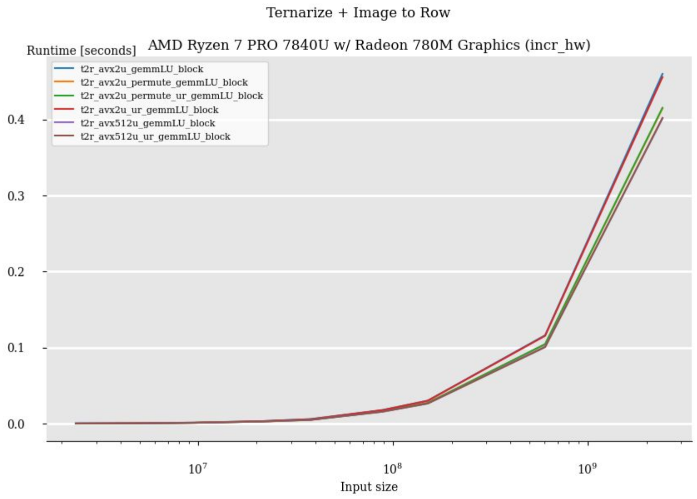
Optimizing Ternarize + im2row

Loop Unrolling

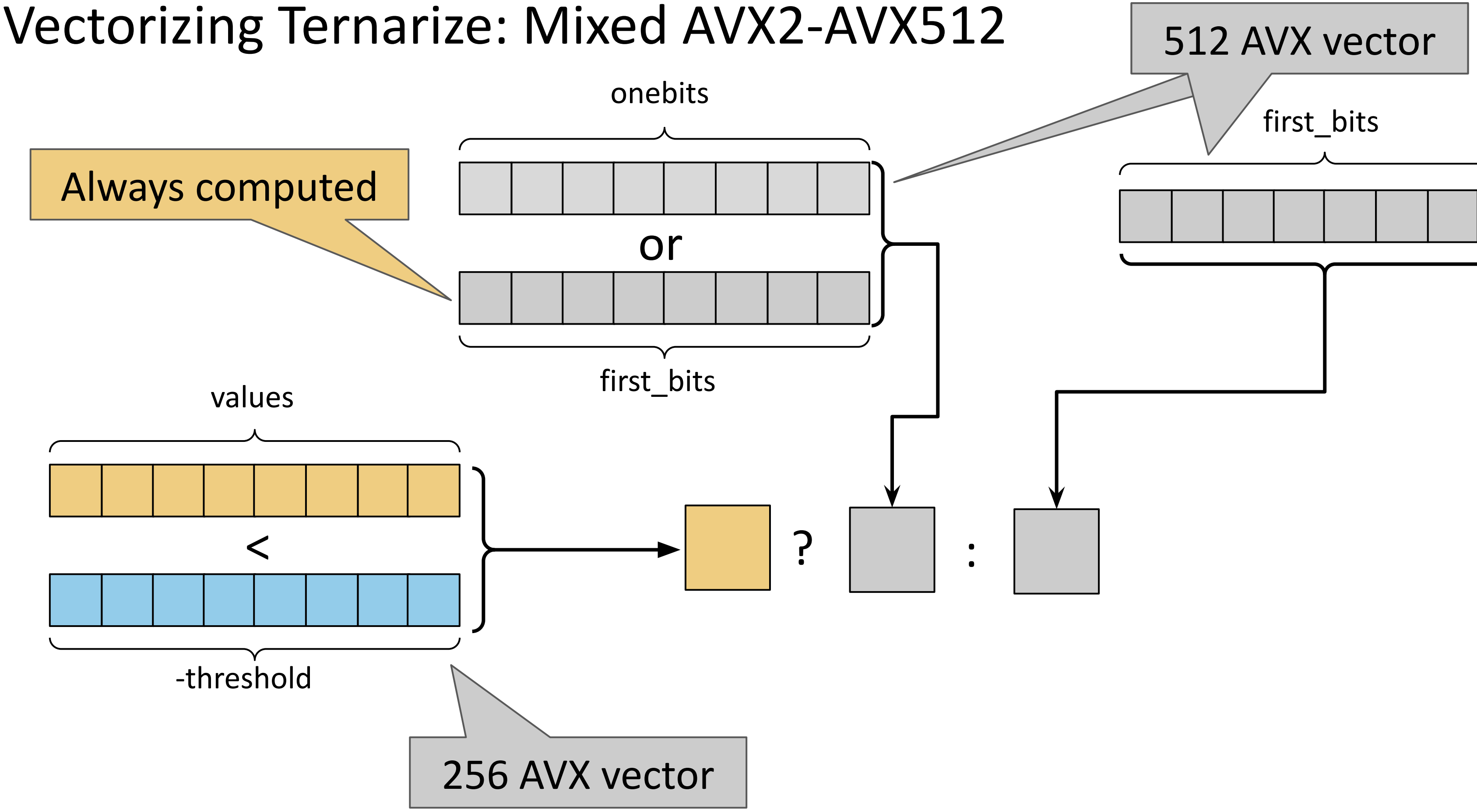
AVX2

AVX512

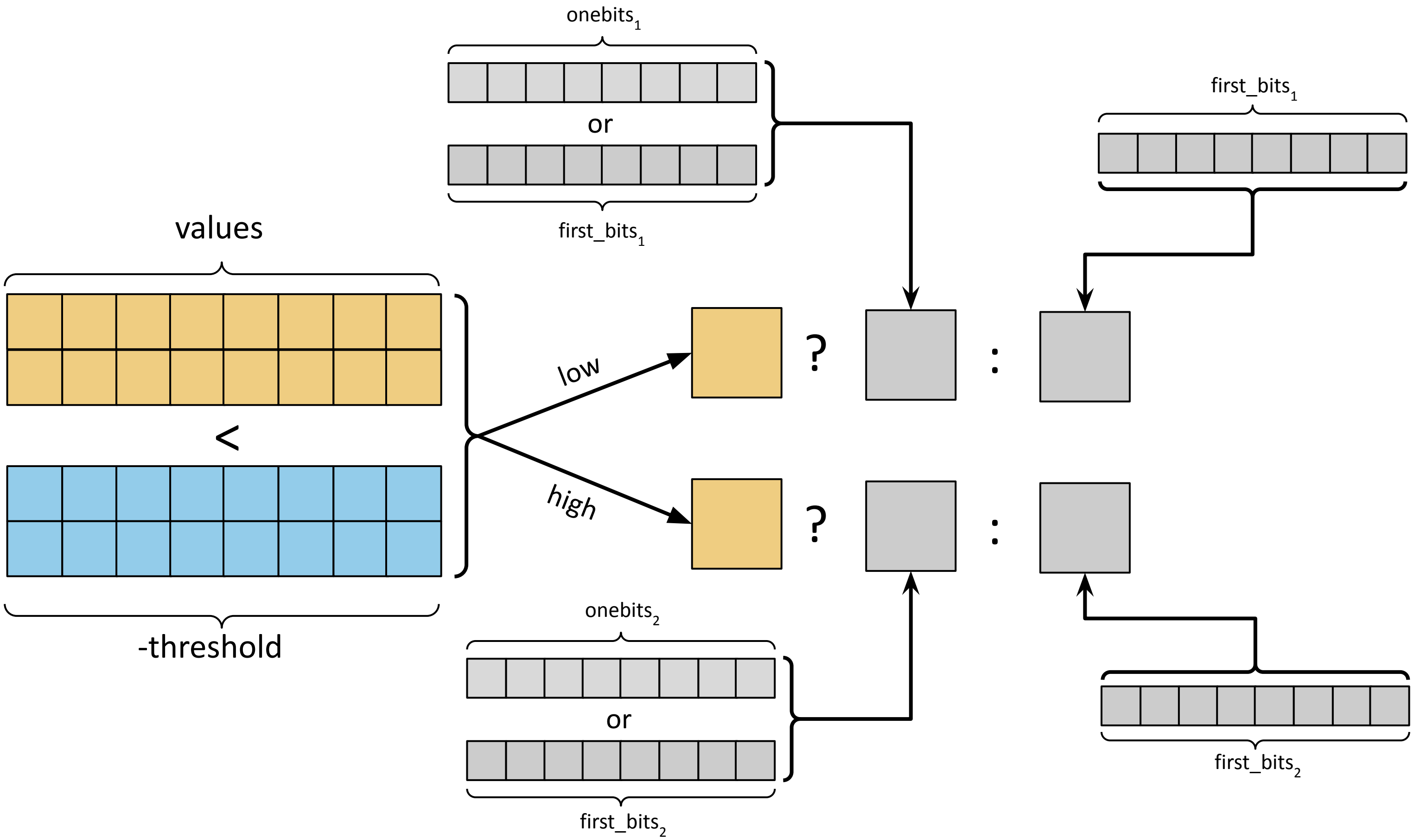




Vectorizing Ternarize: Mixed AVX2-AVX512

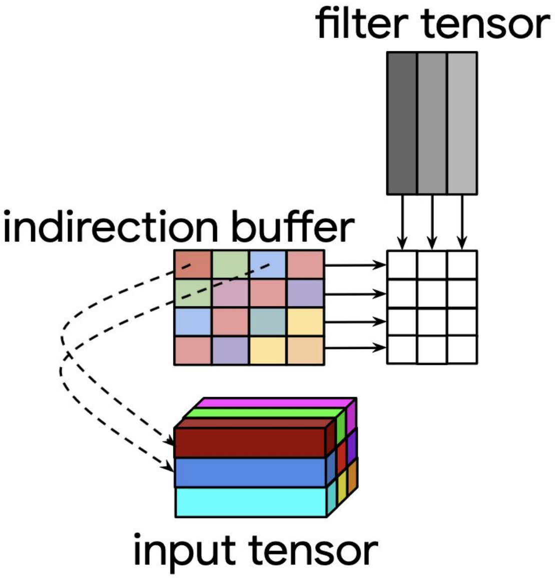


Vectorizing Ternarize: AVX512 only

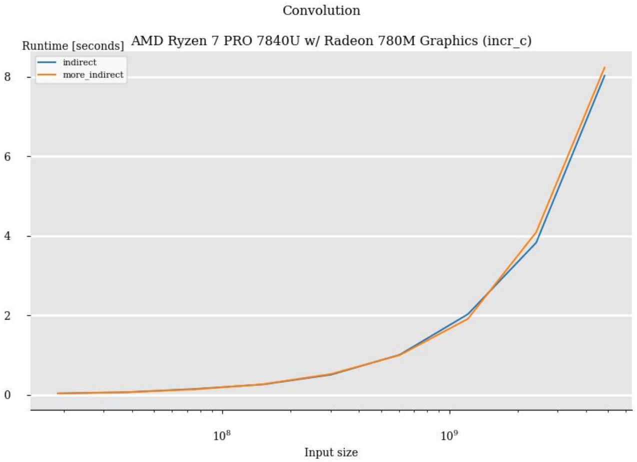


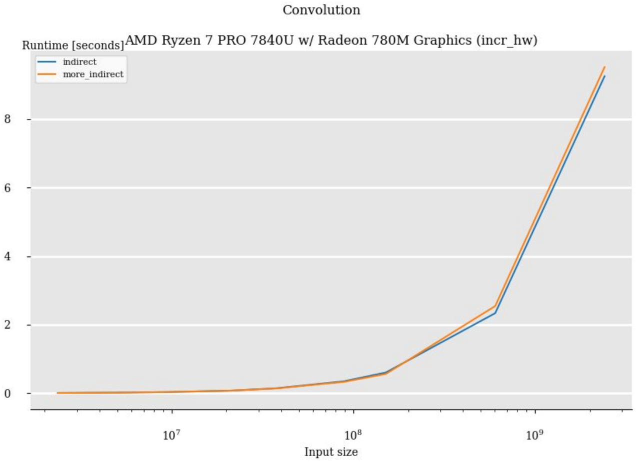
im2row + GEMM

Indirect Convolution

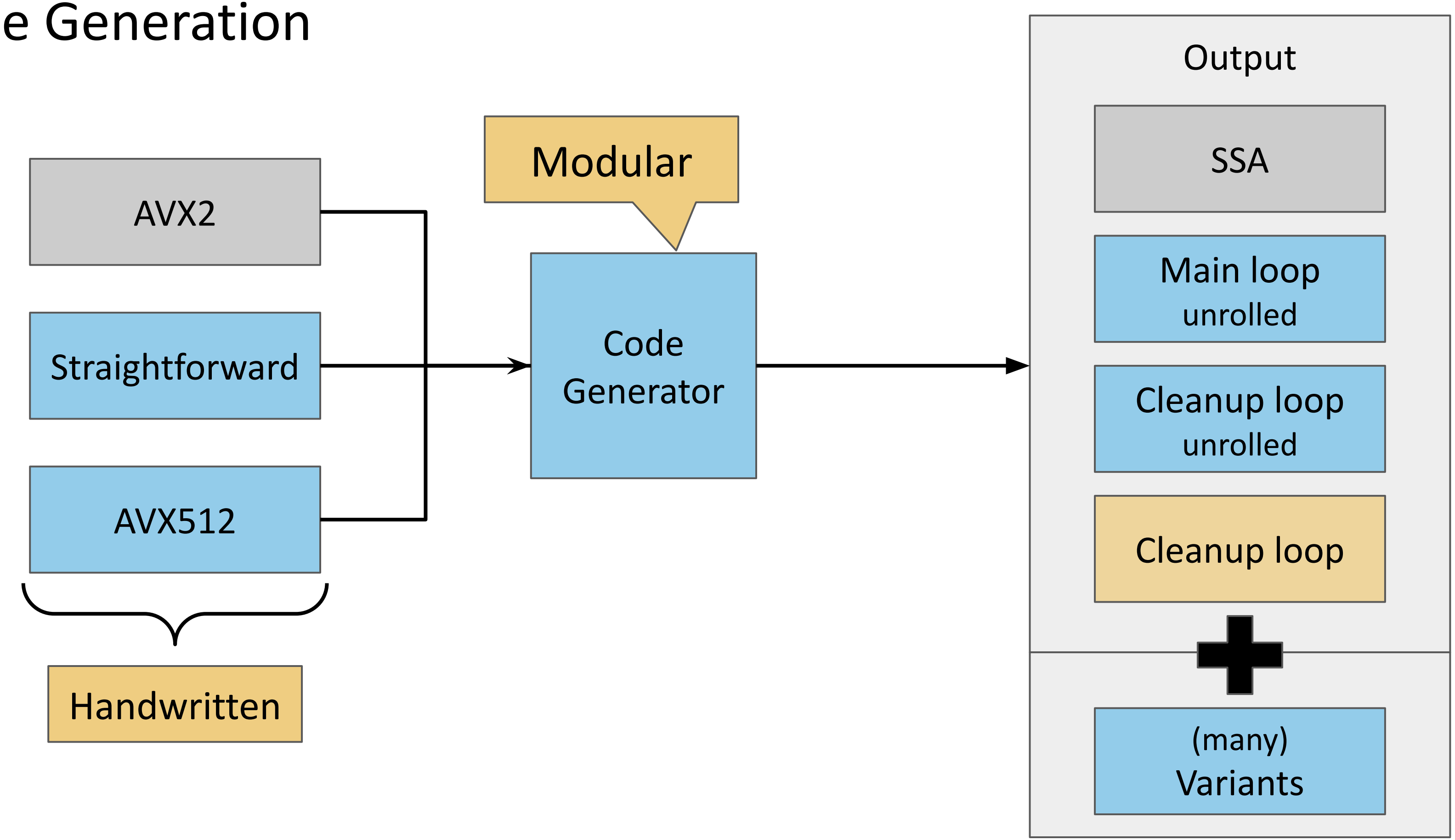


Source: M.Dukhan, The Indirect Convolution Algorithm, *arxiv 2019*





Code Generation



AVX2

Straightforward

AVX512

Handwritten

Modular

Code Generator

Output

SSA

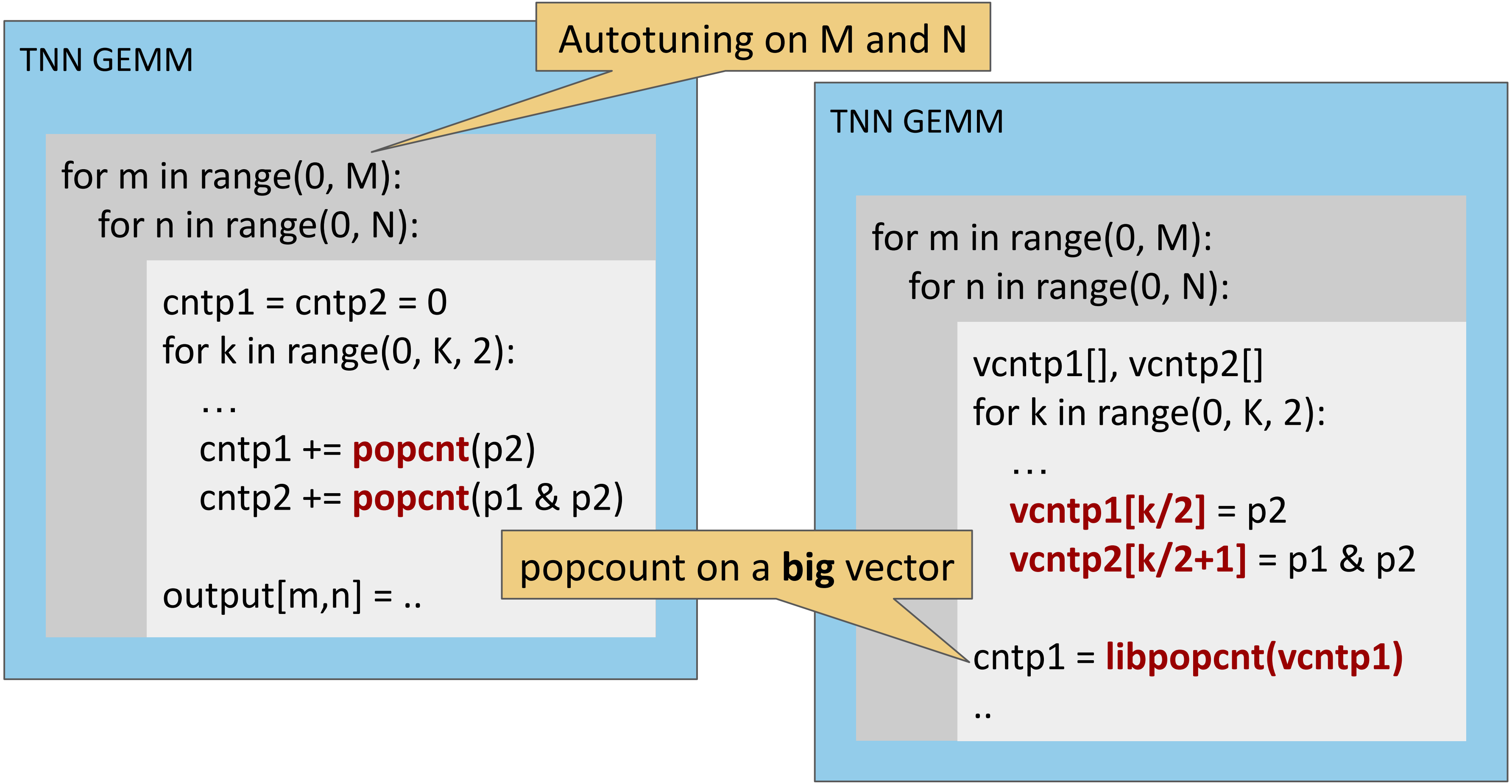
Main loop unrolled

Cleanup loop unrolled

Cleanup loop

(many) Variants

Code Generation - Variant: Autotuning + libpopcnt



TNN GEMM

```
for m in range(0, M):
    for n in range(0, N):
        cntp1 = cntp2 = 0
        for k in range(0, K, 2):
            ...
            cntp1 += popcnt(p2)
            cntp2 += popcnt(p1 & p2)

        output[m,n] = ..
```

Autotuning on M and N

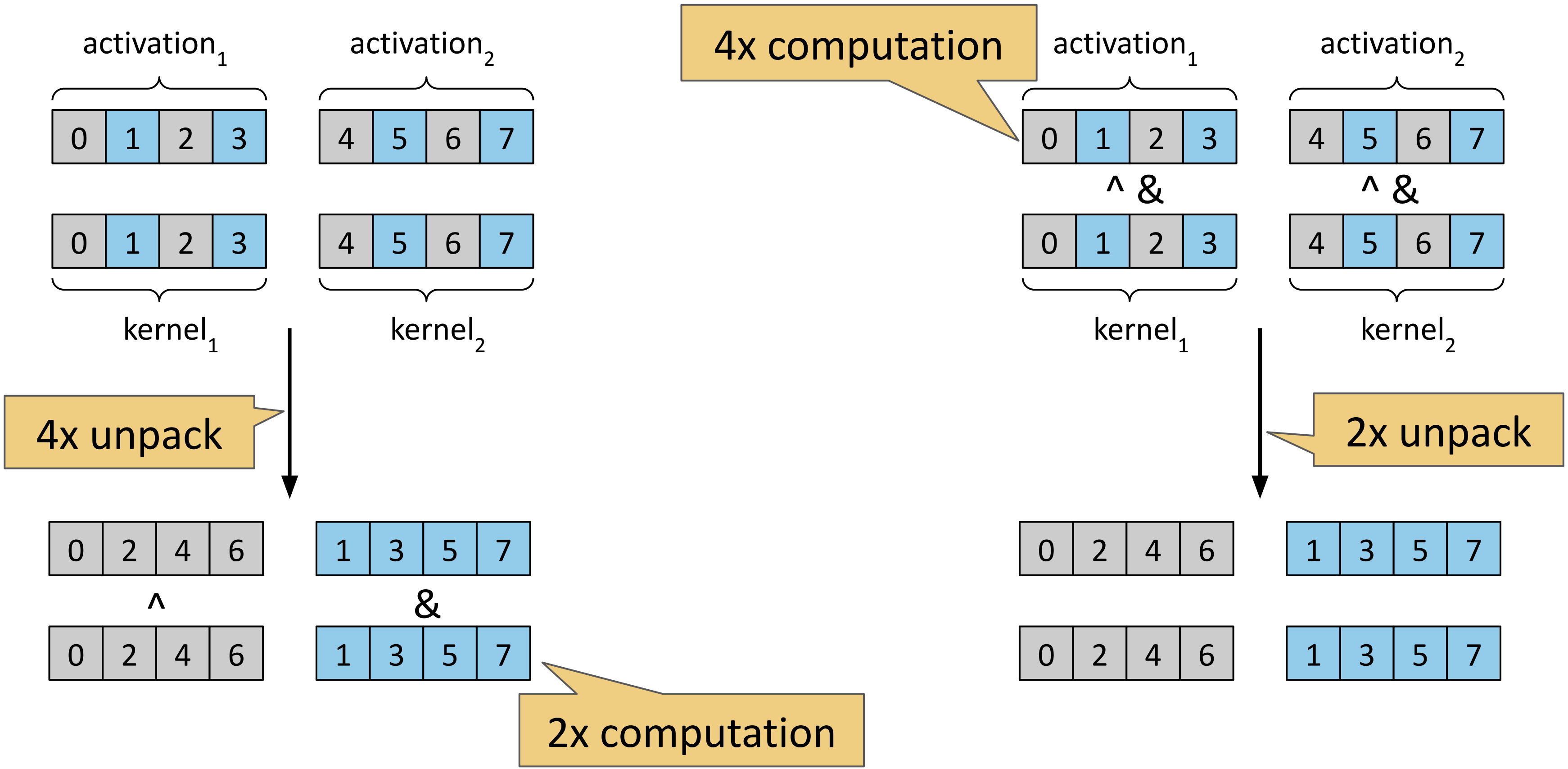
TNN GEMM

```
for m in range(0, M):
    for n in range(0, N):
        vcntp1[], vcntp2[]
        for k in range(0, K, 2):
            ...
            vcntp1[k/2] = p2
            vcntp2[k/2+1] = p1 & p2

        cntp1 = libpopcnt(vcntp1)
        ..
```

popcount on a **big** vector

Code Generation - Variant: Less Unpacking



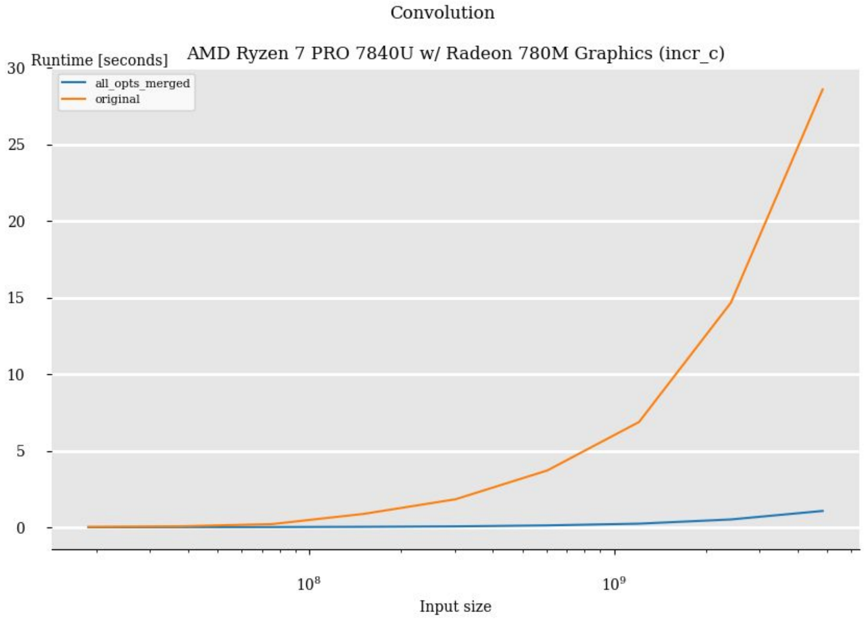
4x unpack

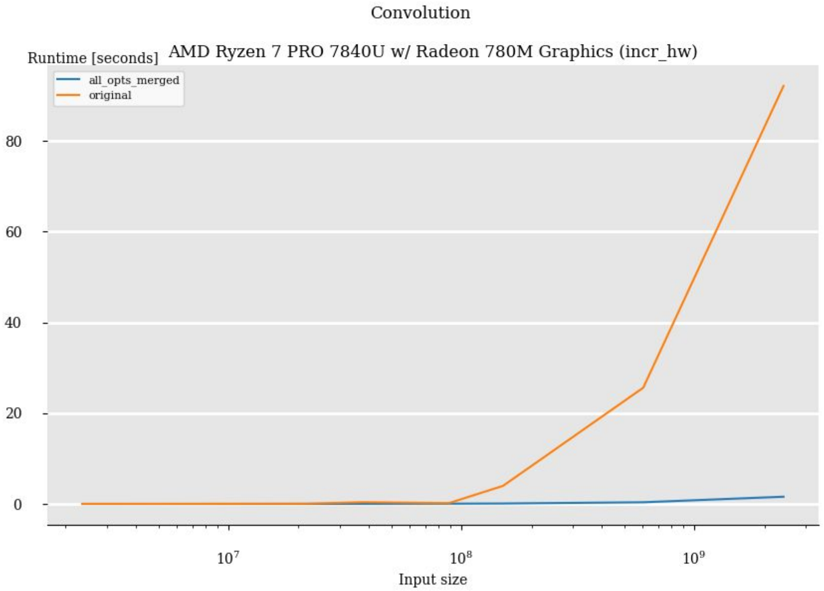
2x computation

4x computation

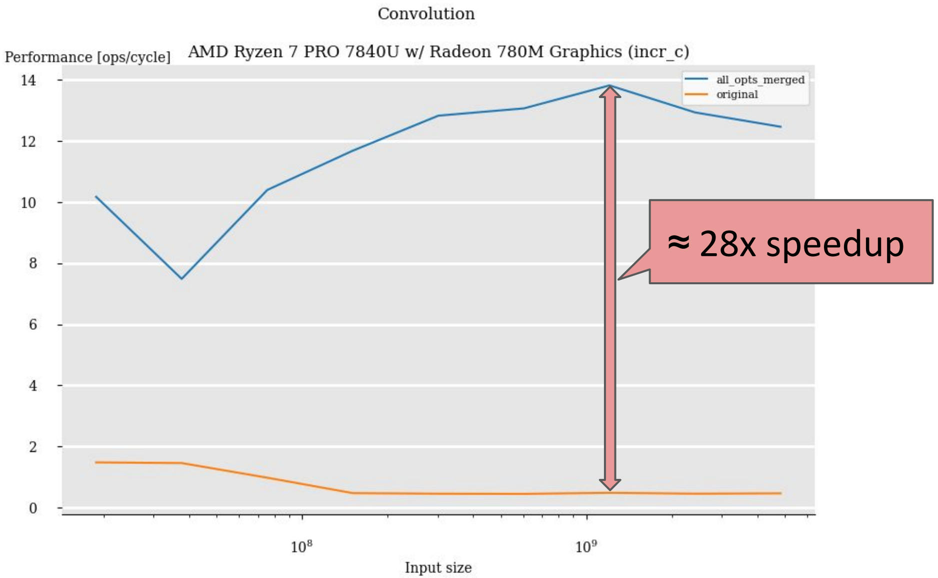
2x unpack

Conclusion

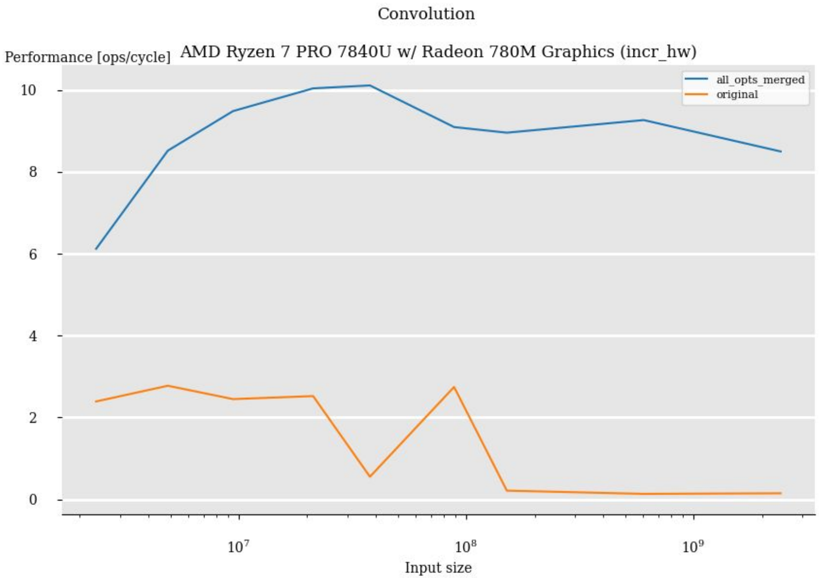

Convolution
AMD Ryzen 7 PRO 7840U w/ Radeon 780M Graphics (incr_c)
Runtime [seconds]
all_opts_merged
original
30
25
20
15
10
5
0
10^8
10^9
Input size


Convolution
AMD Ryzen 7 PRO 7840U w/ Radeon 780M Graphics (incr_hw)
Runtime [seconds]
all_opts_merged
original
80
60
40
20
0
10^7
10^8
10^9
Input size

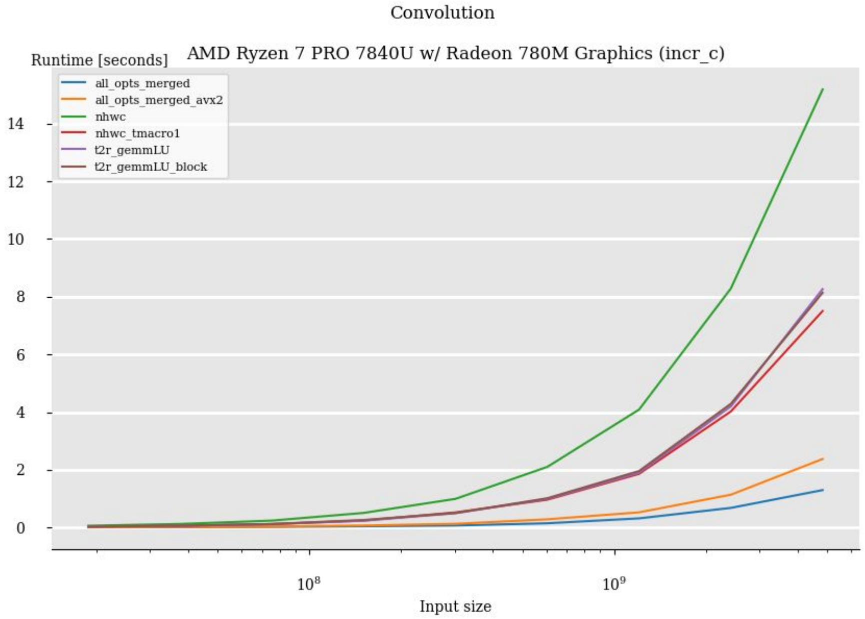
Conclusion



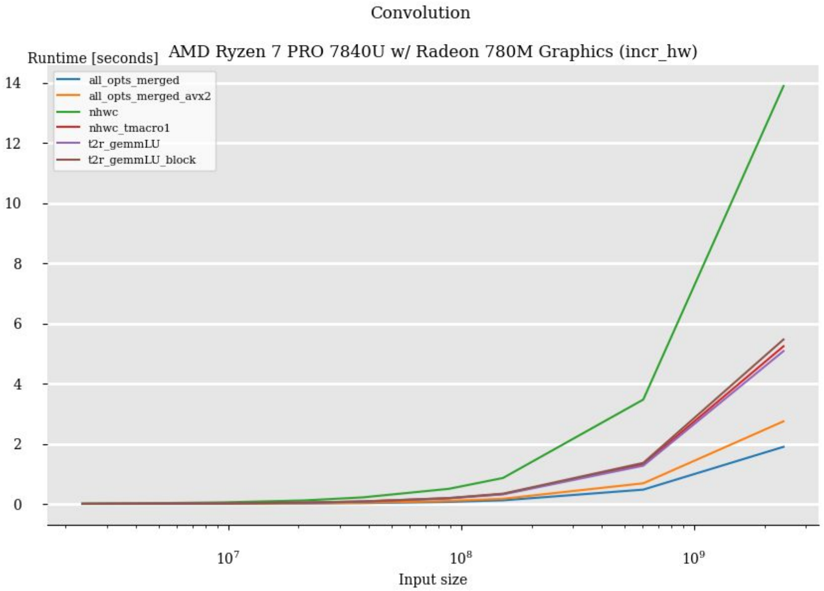
≈ 28x speedup



Conclusion



Convolution
AMD Ryzen 7 PRO 7840U w/ Radeon 780M Graphics (incr_c)
Runtime [seconds]
all_opts_merged
all_opts_merged_avx2
nhwc
nhwc_tmacro1
t2r_gemmLU
t2r_gemmLU_block
0
2
4
6
8
10
12
14
10^8
10^9
Input size



Convolution
AMD Ryzen 7 PRO 7840U w/ Radeon 780M Graphics (incr_hw)
Runtime [seconds]
all_opts_merged
all_opts_merged_avx2
nhwc
nhwc_tmacro1
t2r_gemmLU
t2r_gemmLU_block
0
2
4
6
8
10
12
14
10^7
10^8
10^9
Input size